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Entering a New Era of Innovation in Semiconductor Technologies with Increased Interdisciplinary Synergies for Advanced Compute Scaling

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The need for increased computing keeps growing at ultra high speed, required to support an ever larger and wider range of applications, with generative AI significantly accelerating this trend. Logic standard cell shrinkage remains at the core of the compute roadmap. Its momentum is expected to carry on, even as 2D scaling has become increasingly challenging, by introducing novel device architectures, new materials, scaling boosters like backside (BS) power delivery (PD) with its significant benefits for power integrity, and an overall increased use of design-technology co-optimization (DTCO)-driven design improvements.
A key support pillar of the roadmap remains continued dimensional scaling, enabled by progressive advances in holistic patterning which increasingly rely on the use of extreme ultraviolet (EUV) lithography (evolving into high numerical aperture (NA) EUV lithography) to obtain cost-effective scaling and considerably lower energy consumption. At transistor level, nanosheet (NS)-based FETs are taking the central stage, first as single-level devices consisting of several vertically stacked NS per structure, and potentially evolving into 3D stacked configurations like the so-called complementary FET (CFET) for which several options may be possible regarding the materials and crystal orientations of the stacked channels. Moreover, changes in how the devices are connected, as they become sandwiched and accessed from levels above and below them, also allow interesting new opportunities for device engineering and circuit design. Exploring further the third (vertical) dimension is, in fact, a common current trend of both logic and memory roadmaps, with new options feasible to envision thanks to the recent advances in bonding, 3D and photonic technologies which are allowing new connectivity possibilities besides the typical on-chip interconnects at system-on-chip (SoC) level. That is enabling a system (r)evolution towards smart partitioning, wherein, looking ahead, compute systems have the potential to be assembled in ways enabling much more versatile, hybridized platforms for enhanced system performance. Such scenario is becoming possible thanks largely to an increased embrace of the use of both wafer sides, 3D stacking and sequential integration, together with an overall leveraging of the unique capabilities of different technologies like logic, memory, and 3D under the umbrella of system-technology co-optimization (STCO). The latter's adoption is instrumental in driving the proposal and evaluation of new technology options tailored to the specific requirements of different applications such as mobile, GPU, server or wearables.
This presentation aims to highlight and discuss some of these key advances, including challenges and opportunities, occurring in the area of advanced compute/logic scaling, wherein exciting, sustainability-aware innovations with increased interdisciplinary synergies are shaping the roadmap ahead.

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