

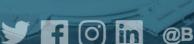
U.S. DEPARTMENT OF ENERGY



G.W.Deptuch (gdeptuch@bnl.gov)



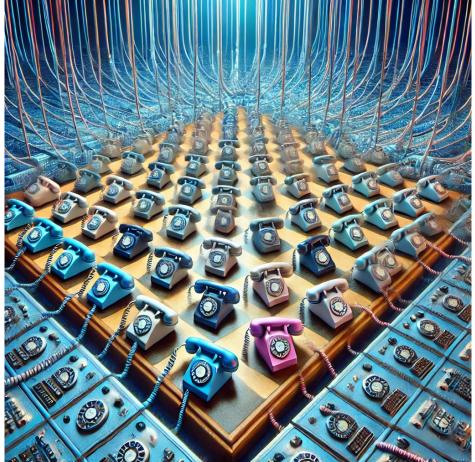
PIXEL 2024 18 - 22 NOV 2024 STRASBOURG, FRANCE



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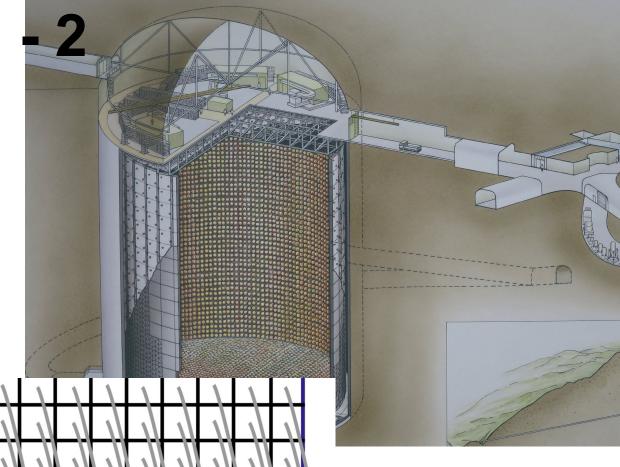


1-to-1 connections ⇒ impossibility of routing

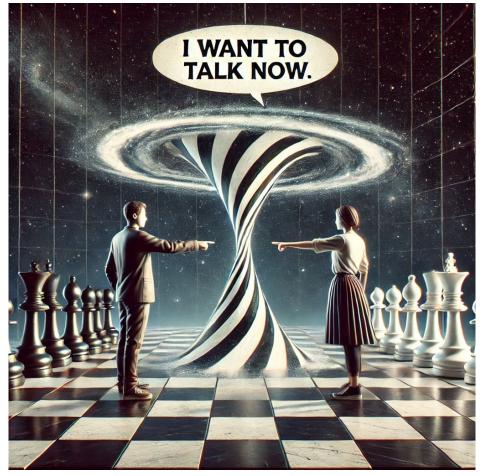


Al-generated image by ChatGPT

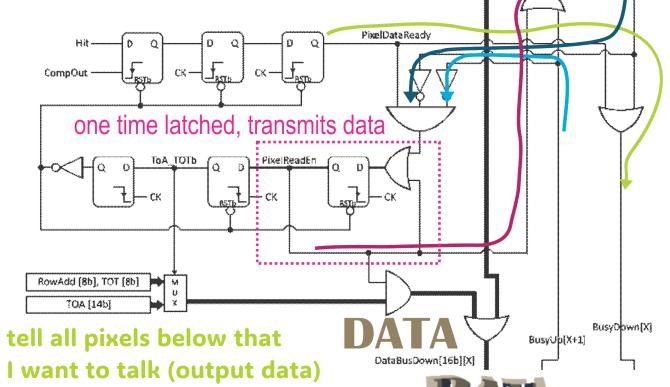
**■**interconnects**■** 



- 1-to-1 ⇒ no conflicts on links
- an only be applied (almost) in specific case



Al-generated image by ChatGPT

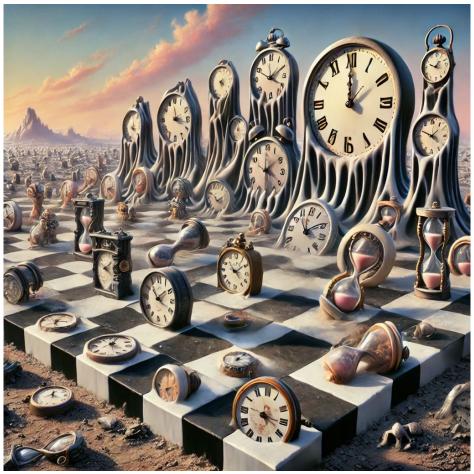


Data8usDown[16b][X-1]

BusyDown[X-1]

- no pixel above was not first to talk?
- no pixel below is already talking?
- I start talking and tell all pixels above that I'm talking!
- It should prevent talking simultaneously, but information has some latency, and CKs are not the same in all pixels



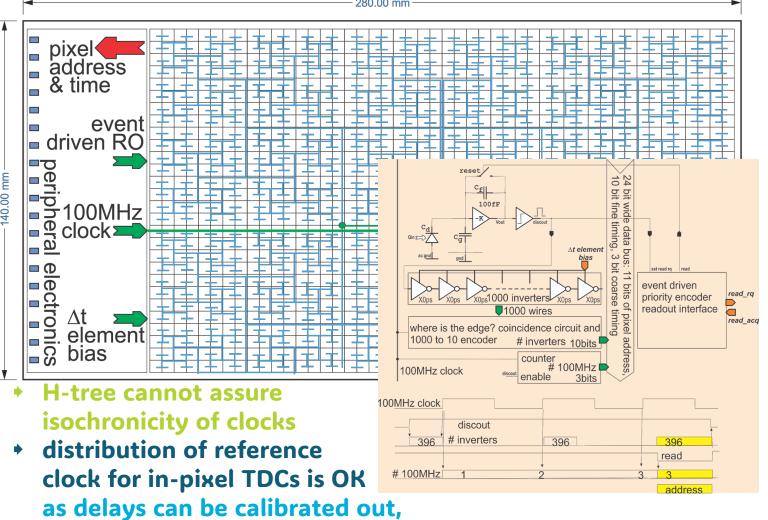


every pixel has different clock

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Al-generated image by ChatGPT



but wrongly resolved concurrency leads to corrupted data



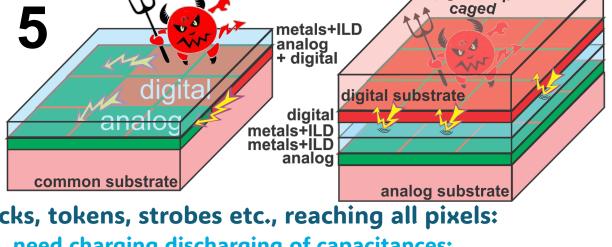


more activity

Al-generated image by ChatGPT

more dissipated heat and more interferences

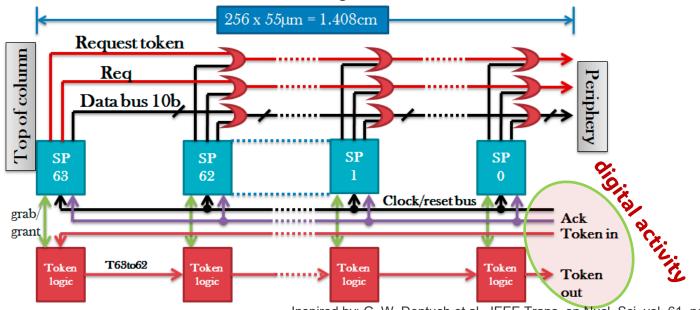




clocks, tokens, strobes etc., reaching all pixels:

digital imn

- need charging discharging of capacitances;
- causes interferences (and 3D-IC is not always available) Full column length =



power and interferences

Inspired by: G. W. Deptuch et al., IEEE Trans. on Nucl. Sci. vol. 61, no. 1, pp. 663-674, Feb. 2014, doi: 10.1109/TNS.2013.2294673 and T. Poikela "Readout Architecture for Hybrid Pixel

digital imp

Readout Chips", PhD thesis 2015

## From the Past - 1

**DELPHI PIXEL DETECTOR MODULE** 

16 electronic chips bump-bonded on

22 mm

1 large detector plaquette (9 cm ) <sup>2</sup>

electronic chip:

total =  $8 \times 19$  modules = 1300 cm<sup>2</sup>



Al-generated image by ChatGPT

24 x 24 pixels of 330x330 µm busses on the 70 mm detector chip electronic chip: 16 x 24 pixels of 330x330 um 19 modules / half layer

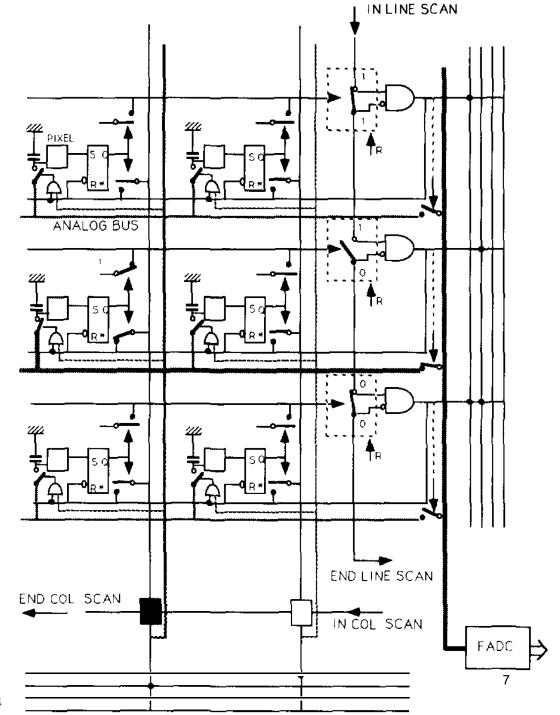
pixel detector readout,
with two-dimensional
X-Y signaling and scanning
sparse data scan
(with added feature of
analog readout)
2D ambiguity



P. Delpierre and J.J. Jaeger, Nuclear Instruments and Methods in Physics Research A305 (1991) 627

Erik H.M. Heijne, spk., CERN DRDC/93-54 RD19 Status Report 1 January 1994

17 mm



## 2 Steps in Data Flow

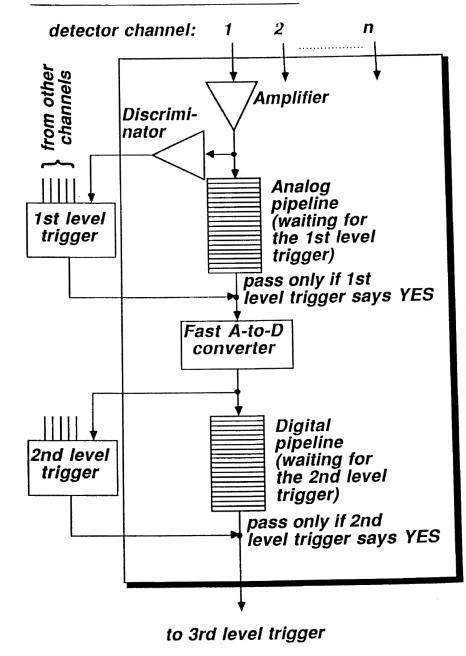


Al-generated image by ChatGPT

#### two steps:

- get data from pixels to periphery (buffers)
- organize output awating trigger arrival

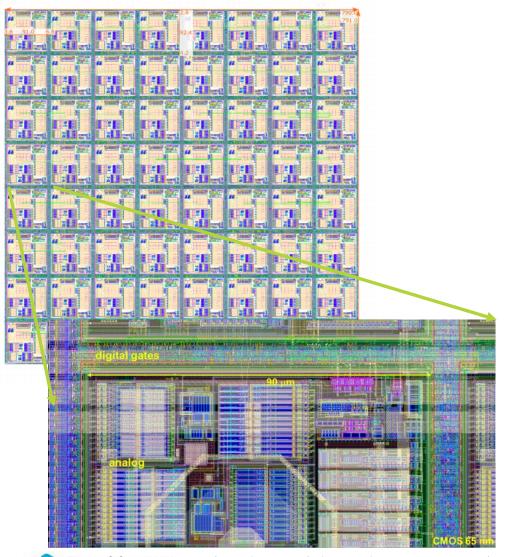
focus on extracting data from within pixel matrix to peripherals



HARP: schematic overview

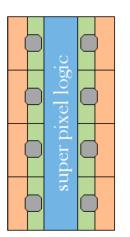


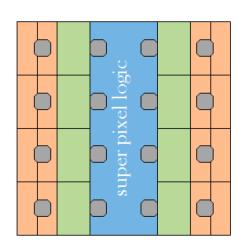
## Design with Selected Readout Platform

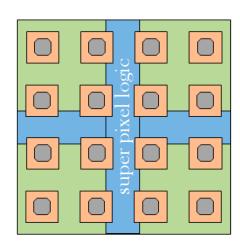


### common approach of building

- super pixel 2×4, 4×4 and 4×4
- analog islands encircled by logic.
- Digital pixel front-end
- Analog pixel front-end
- Bump pads









# **Summary of Solutions - 1**

### Frame-less POLLING (DATA-DRIVEN):

- typically circulating token(s) queries each pixel's state for data to transmit
- unnecessary transfers removed,
- varrying latency or dead time introduced (propagation of token)
- continuos activity (token and strobes need to be cont. repeated)

#### Frame-readout:

- all pixels are read out sequentially
- predefined order of data retrieval
- large amounts of dubious information
- no timing from readout

Brookhaven<sup>\*</sup>

Sparsified

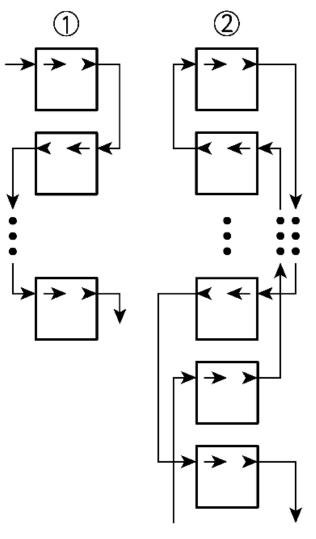
#### Frame-less EVENT-DRIVEN:

- pixels independently signal themselves for readout
- unnecessary transfers removed,
- fixed or no latency or dead time
- **ZERO** activity until anything to read
- automated CAD/EDA circuital implementation possible

### Frame-based sparsified:

- snapshot taken first
- static arbitration predefined order
- pixels fished out with:
  - priority encoder
  - token passing
- zero-supressed
- no timing from readout

## **Summary of Solution - 2**



### Frame readout

typically snaky style - shift registers:

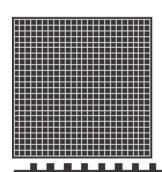
- data out (typically count values in SPC mode)
- data in (configuration)
- data accumulated during exposure window moves a long shift registers
- often shift registers are reconfigured counters for real estate efficiency
- many detectors developed for Photon Science operating in SPC mode
- very simple ⇒ will not spend time on this type



threshold for using is occupancy

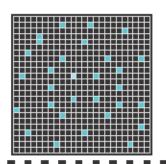
# **Summary of Solution - 3**

### Comparison



full frame readout



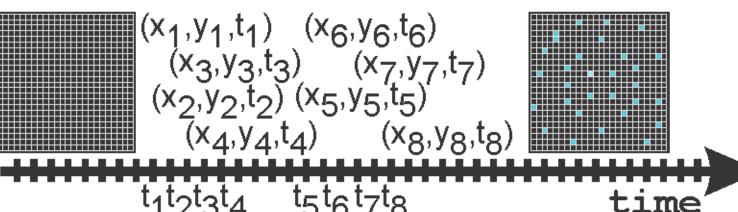


Frame- Based Sparsified

time

sparsified / address event encoding

Frame- Less Polling Event-Driven



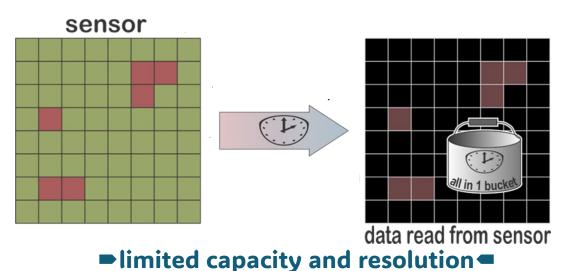


### **Arbitration methods**

#### **Static Arbitration:**

with combinational logic (priority encoder / token passing)

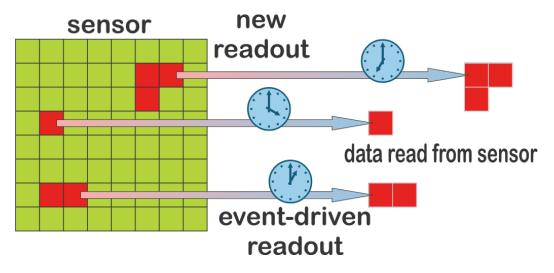
- state of matrix snapshot before readout to prevent corruption if requests with higher priority arrive
- data sent in packages (with period of snapshotting clock)



**Dynamic Arbitration:** 

true event-driven with sequential logic (queuing with memory elements)

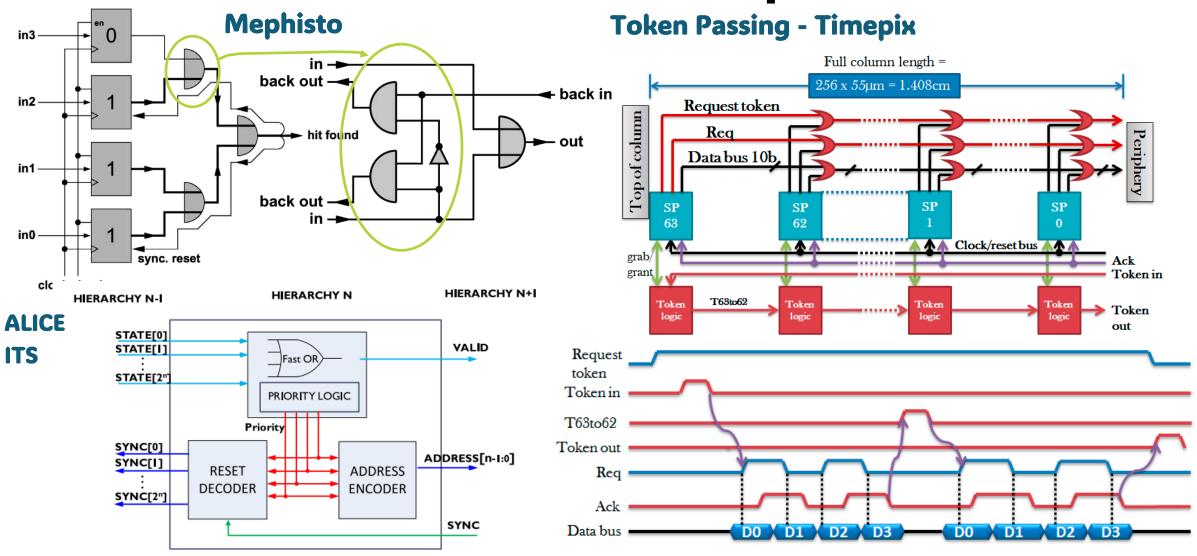
- arbiter cell stops and queues requests clearing them one by one
- data points sent one by one (time resolution depends event rate)



■ maximum capacity and resolution

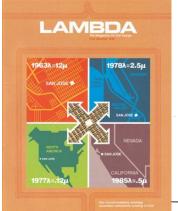


## **Arbitration methods - examples**





### Dynamic Arbitration: GALS LAGS - 1





Charles L. Seitz

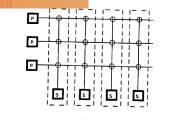


FIGURE 1 Processor (P) Storage (S) Crosspoint Structure.

FIGURE 2 Symbol for Self-Timed Arbiter.

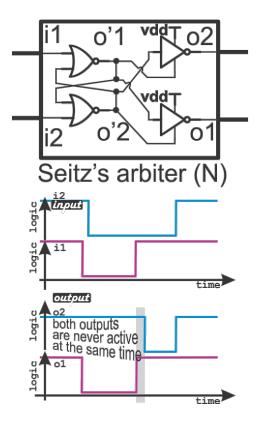
n arbiter is a mechanism that governs the sharing of a resource among a number of processes. An everyday example is a stoplight at an intersection. It is intended to allow the street crossing to be shared safely between two traffic flows. The traffic-actuated type of stoplight is considered to be superior to the clock-cycled type, because it does a better job of keeping the resource (the street crossing) active and the traffic flowing. Using a mechanism that allocates the resource dynamically in response to the demand achieves a better use of the resource.

One of the most common examples of arbitration in digital systems is the sharing of the main (randomaccess) storage of a computer system amongst a number of processors-instruction processors, peripheral processors, data channels, and so forth. Figure 1 shows a crosspoint structure that allows multiple processors to make concurrent accesses to main storage distributed across several independent boxes. The systems within the dashed lines are multiport stores, each of which

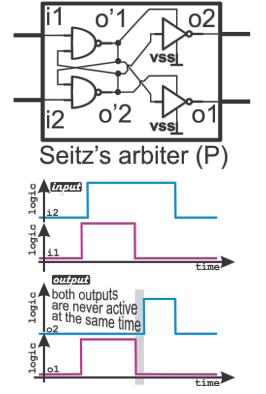
covers a different range of addresses and can operat independently of the other storage boxes.

One might think of processors as placing an addres and a request for a storage cycle on the (horizontal paths that thread through the storage boxes. Eacl storage box can detect the request and whether the address is one of its own. If more than one reques appears on a storage box's ports, how does the store determine which request to service next?

The required arbitration is sometimes accomplished by a fixed allocation of the store to different processor: on different periodically repeated time slots. This approach is not unlike the clock-cycled stoplight, and is guaranteed to leave a lot of bus and storage cycles unused unless the load is perfectly balanced. Dynamic allocation of time slots that are fixed within a synchronous communication discipline is workable scheme whose implementation is straightforward. The only disadvantages of this scheme are the usual problems inherent to synchronous systems in (1) clock distribution and (2)





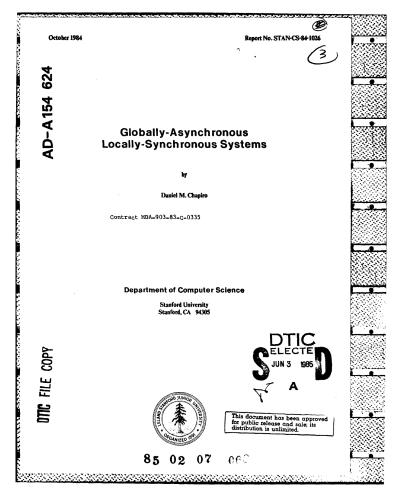


1	1	prev	ious	prev	ious
1	0	0	1	1	0
0	1	1	0	0	1
0	0	1	1	0	0
i1	i2	o'1	o'2	01	o2

"ghost paper" everyone cites it, but nobody can see it

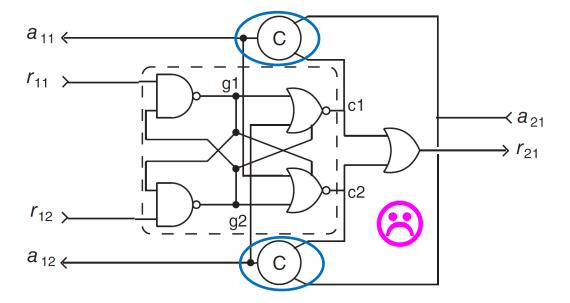
10 LAMBDA First Quarter 1980

### Dynamic Arbitration: GALS LAGS - 2



D.M. Chapiro, PhD thesis, https://apps.dtic.mil/sti/pdfs/ADA154624.pdf

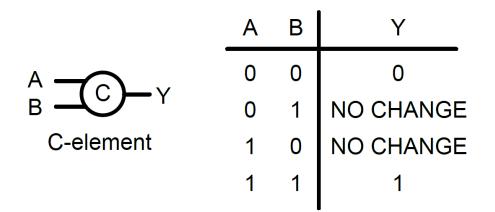
- in inter-processor networks (CALTECH), sources are synchronous and acquisition is asynchronous (Global Asynchronous – Local Synchronous)
- arbiters with Mueller-C gates, where:
  - access granted can only be canceled by source, and
  - communication with source is impossible after Mueller-C gate is set
- each source has to 🕑 its access to medium

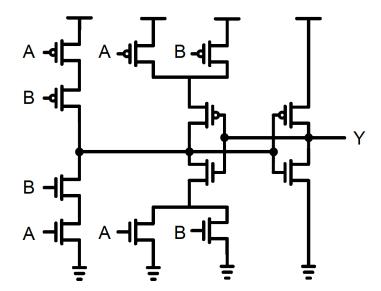


- but pixel systems are LAGS!!
- memory is needed to avoid switching

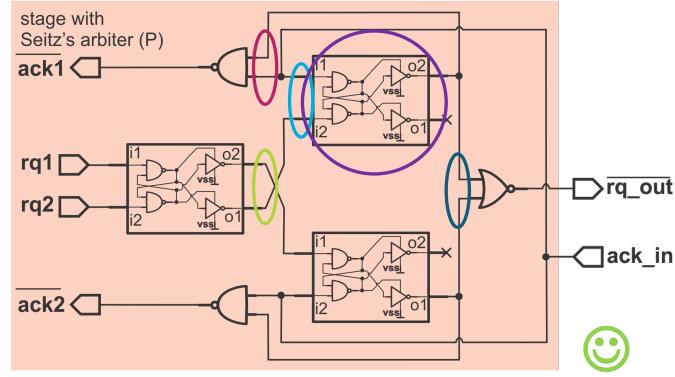
Park, Jongkil, PhD thesis, https://escholarship.org/uc/item/0sc4s9v7 Shih-Chii Liu, et al, "Event-Based Neuromorphic Systems", Wiley 2015

### Dynamic Arbitration: GALS LAGS - 3



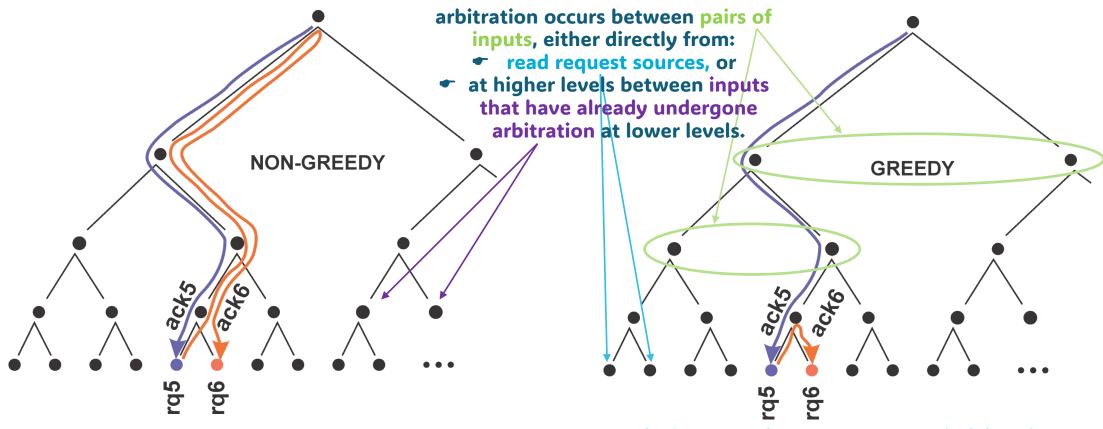


**■**once the C-gate is set, both inputs must deactivate, but interaction with other side is blocked ■



- who was first? (glitch-less)
- Who is first, req or ack? (req blocked if ack high first)
- req goes up if any req passed through (@ ack low)
- if req passed though any ack change will pass down!
- this arbiter disallows any rq1 rq2 grappling (gone + appear again, faster than deactivation of ack, etc )
- **■**interaction with other side is unblocked

# Non-Greedy and Greedy Arbitration



search for a new data source always resets randomizes/democratizes data retrieval but disrupts geometrical associations

search favors the same or neighboring source may show preference for certain part of detector where rates of requests are higher due to e.g. noise





Non-Greedy EDWARD

fastest, selective,

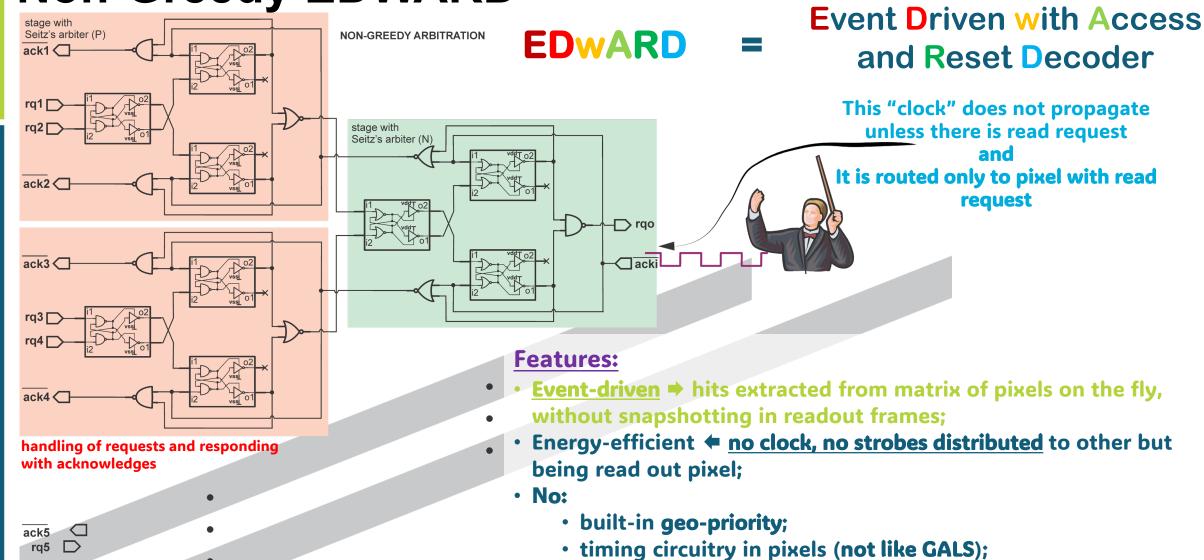
dead-timeless readout

ackn-1

ackn

...aven

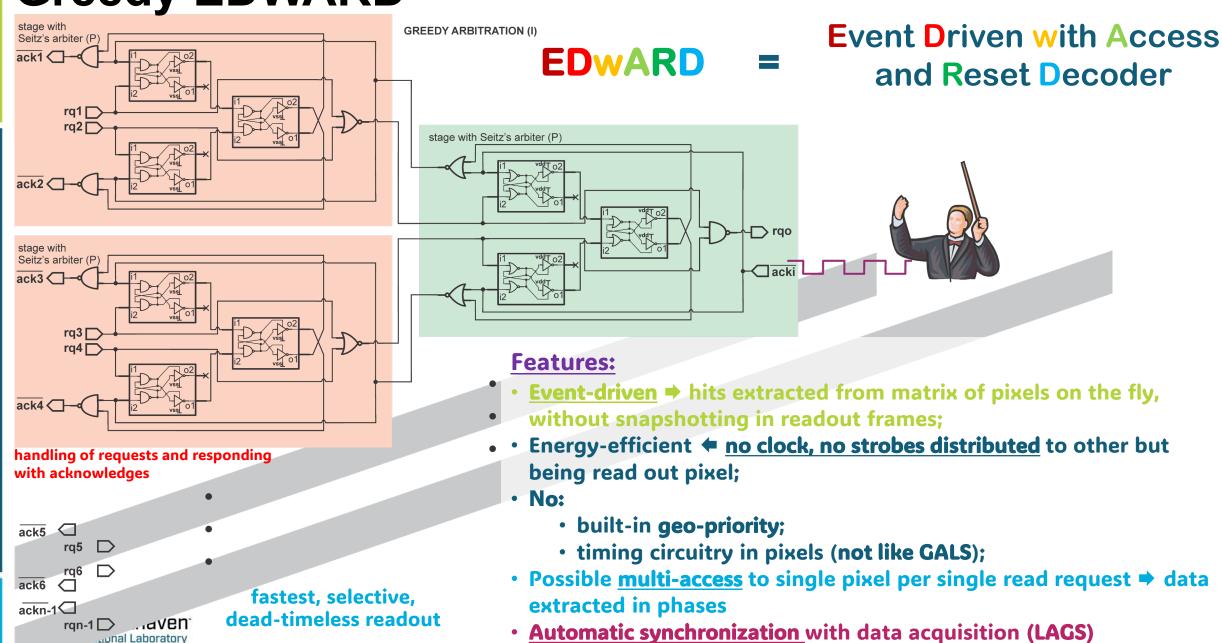
acional Laboratory



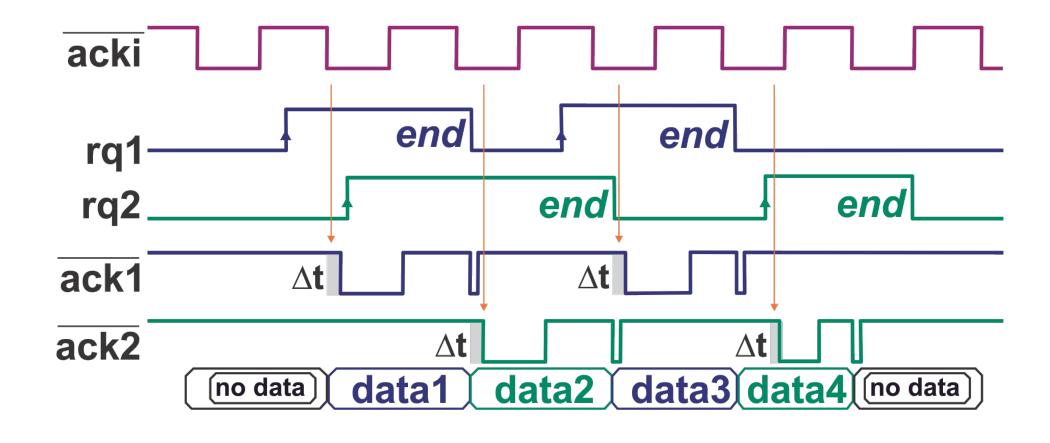
- Possible <u>multi-access</u> to single pixel per single read request ⇒ data extracted in phases
  - Automatic synchronization with data acquisition (LAGS)

**Greedy EDWARD** 

ackn

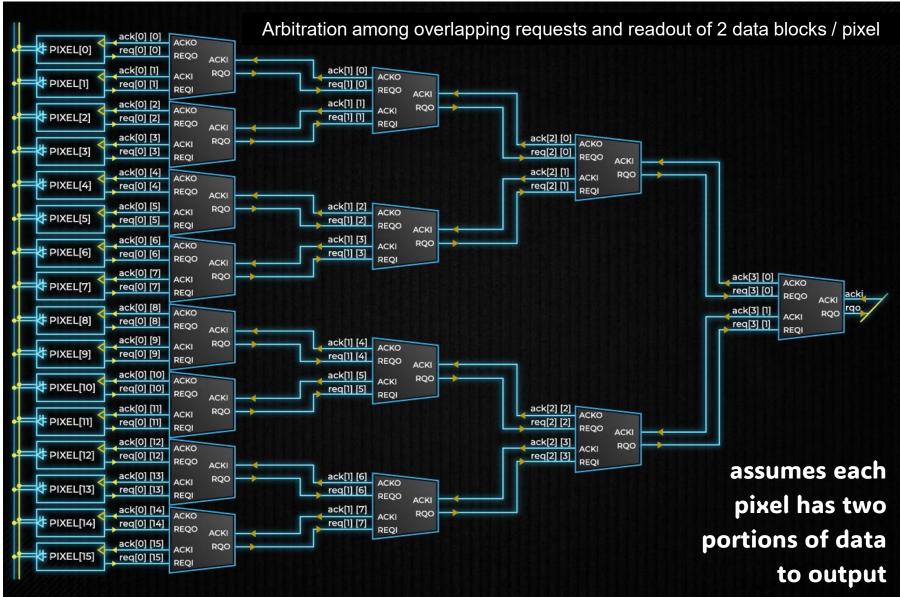


## Data Flow in Non-Greedy EDWARD



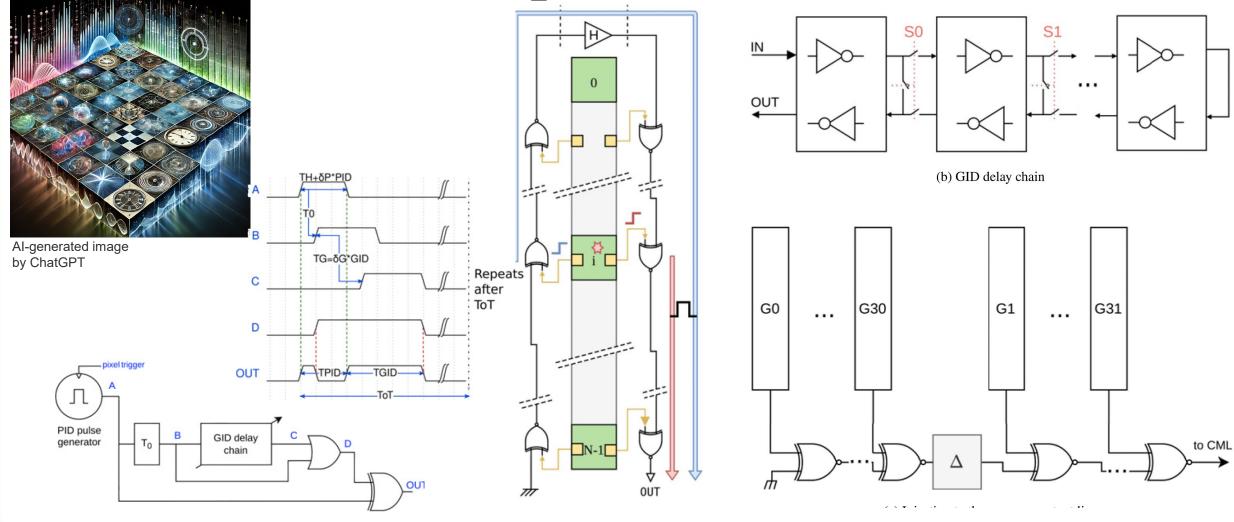


# Readout in Non-Greedy EDWARD





Time Instead Voltage/Current -1





reading using a single line, relying on the time interval between pulses and the position of the pixel being read

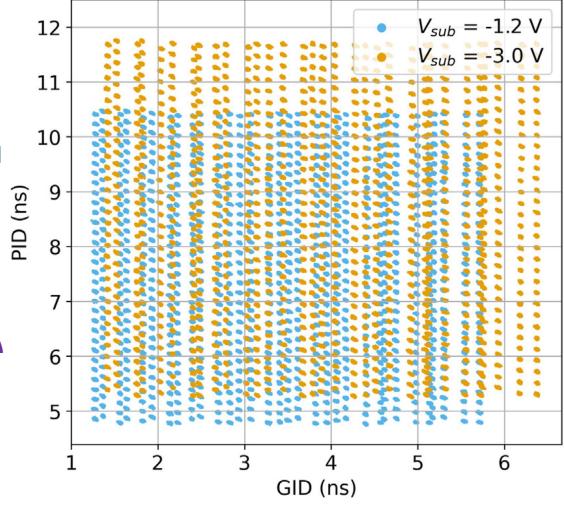
- L. Cecconi et al 2023 JINST 18 C02025
- G. Aglieri Rinella, et al., Nuclear Instruments and Methods in Physics Research A 1056 (2023) 168589

# Time Instead Voltage/Current -2

challenge of method:

- dependence of propagation speeds of pulses on power supplies and biases
- dependence on production process variations and measurement conditions
- dependence on temperature
- how to provide continuous calibration?
- time measurement needed to decode positions
- CAD/EDA tools do not provide equivalence of STA (time enclosure) for time-domain circuit design

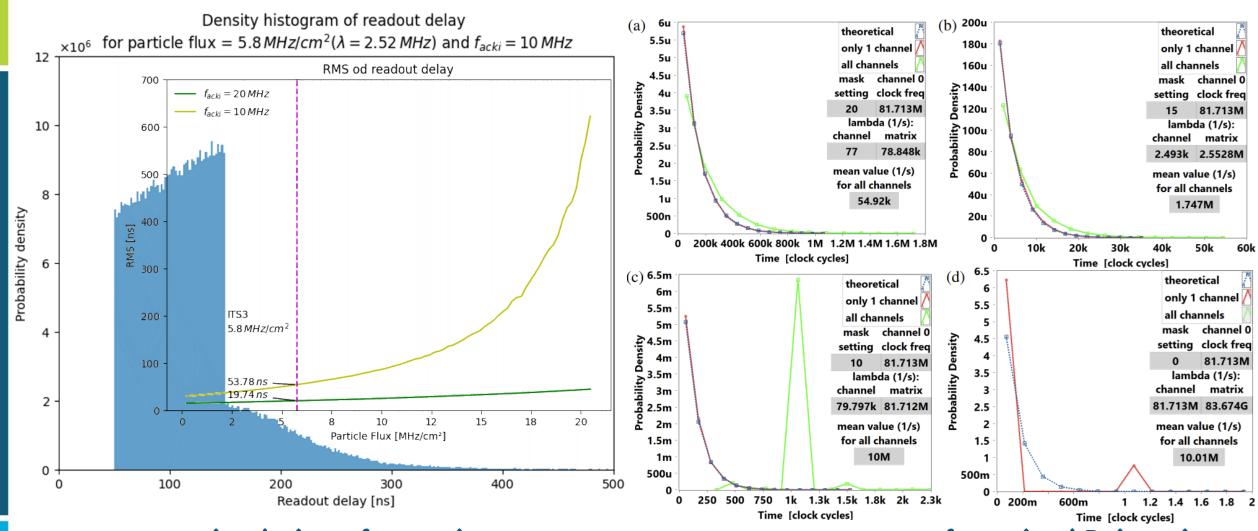
perspective and inspirational!





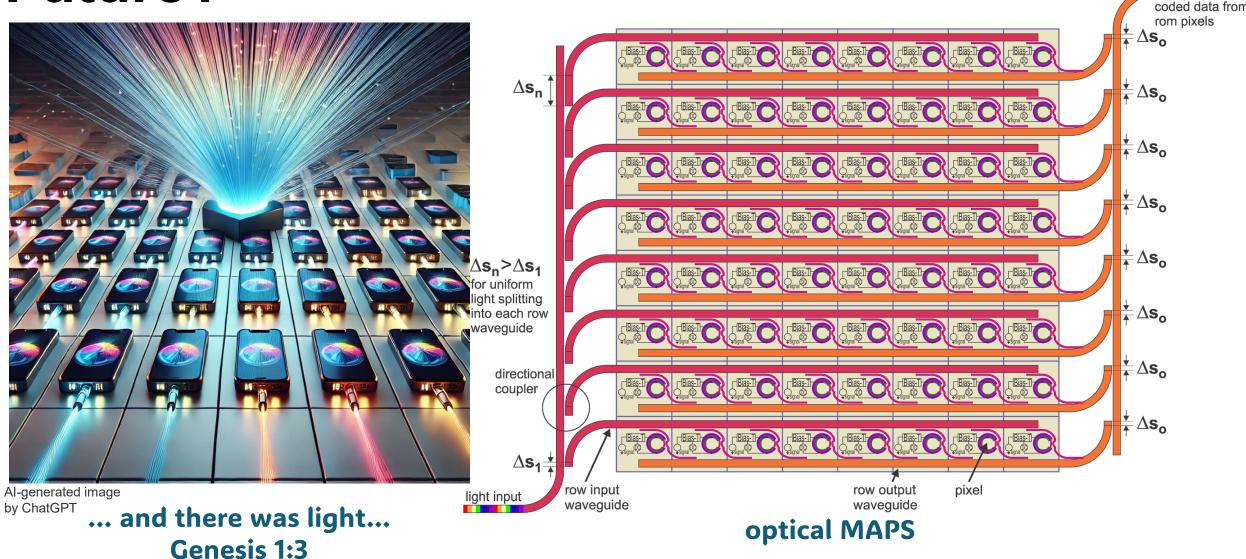
# Intrinsic Timing Resolution







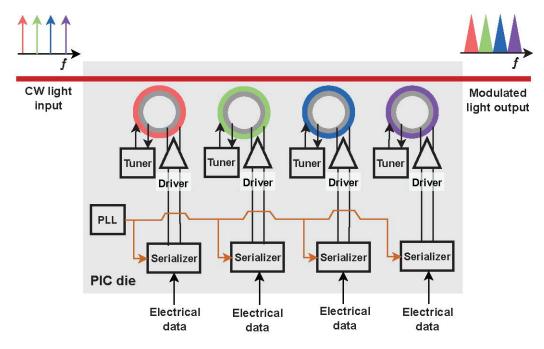
## Future?



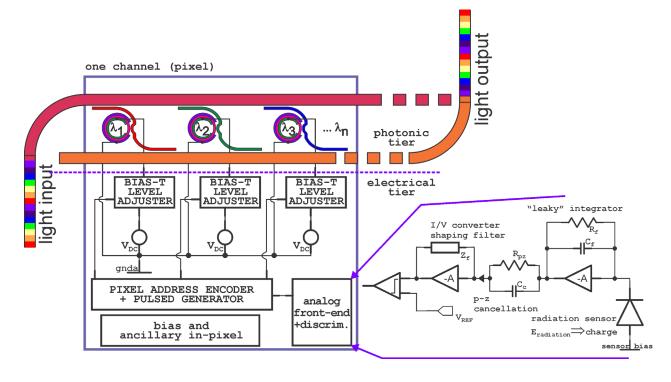


light output

### Future?



micro-ring resonant modulators are used for data transmission, allowing modulation of CW in data transmission



through 3D integration of MAPS with Siphotonics, electrical data transfer can be eliminated



### **Summary**

- Optimizing Readout of segmented radiation detectors:
  - Goal: data integrity at minimal resource overhead
  - Challenges: balancing speed and power consumption
  - Focus: efficient data acquisition for radiation detectors
- Evolutionary path for zero-suppressed readouts

#### from:

- X-Y coordinate signaling
- covering large areas token passing
- static arbitration
- data polling

to event-driven no clock/strobe distributed/broadcasted and total silence before request

- voltage domain (EDWARD)
  - \* RTL code for implementation parameterized and scalable including individual pixel configuration available upon request to accelerate design
- time domain (DPTS)
  - very compact implementation
  - challenging calibration



### Acknowledgements

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- This work has been authored by employees of Brookhaven Science Associates, LLC under Contract No. DE-SC0012704 with the U.S. Department of Energy.
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  - NASA Grant NNX16AC42G
  - LDRD-A21-020, LDRD-A24-054, B&R Code: YN0100000
  - DOE Office of Science, DE-S00012704, KA2501032/FWP# P0024
  - TM24-01 ATRO/10 FY24TMALG

