## Eleventh International Workshop on Semiconductor Pixel Detectors for Particles and Imaging



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## Rapid prototyping platform for highly segmented detectors

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We present the design and implementation of a comprehensive testing setup for validating pixelated detectors, emphasizing rapid prototyping and minimizing printed circuit board design and debugging efforts. The system features an off-the-shelf embedded controller with an Intel CPU running under LinuxRT, paired with an Artix 7 FPGA. This FPGA supports both VHDL and LabVIEW code, enhancing setup preparation and testing efficiency, particularly for pixelated structures. We will present results obtained with the presented circuits to demonstrate developments of the integrated circuits, interfaces and external readout and processing hardware.

We discuss the overall concept and the realization of three distinct systems: an asynchronous event-based readout interface (EDWARD), the hexagonal-shaped pixelated detector readout IC (HEXID), and a Full Field Fluorescence Imaging (3FI) pixelated hybrid detector readout IC. The proposed systems consist of programmable voltage reference sources, power supply stages, and high-speed, 16-channel, 14-bit ADCs sampled at 65MHz. These systems are optimized for low noise and high sampling rates, resulting in over a 10Gbps data stream processed in the FPGA for feature extraction.

All presented solutions are pixelated structures. The EDWARD IC enables the verification of an event-driven readout, controlled by an I2C interface, with data generated inside each channel streamed out using an encoded digital protocol. Similar methods are further utilized in HEXID and 3FI—pixelated CZT hybrid detector readout integrated circuits. The setup is designed to facilitate fast prototyping, significantly enhancing performance, development speed, and the efficiency of validating various pixelated detector technologies.

In addition to the technical components, the setup incorporates modular design principles, allowing for easy reconfiguration and scalability. This flexibility ensures that the system can be adapted for a wide range of testing scenarios, from initial prototyping to final validation stages. By leveraging these innovative components and design strategies, our testing setup stands out as a crucial tool for advancing the development and validation of next-generation pixelated detectors.

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