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A Column-level ADC designed to CMOS image sensors

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Due to their advantages of fast readout rate, high integration and low power consumption of CMOS image sensors, they have been widely used in medical imaging, security monitoring, and space X-ray detection. As an important part of CMOS image sensors, the performance of analog-to-digital converters (ADCs) directly affects the quality of imaging. In large-area and high-speed CMOS image sensors, ADCs are usually arranged in a column-level readout mode. The traditional structure is a single or dual slope ADC, which is not fast enough. This work is to research and design a 12-bit 5MS/s low-power Cyclic ADC using 180nm process.
The ADC adopts a SHA-less front-end sample-and-hold structure, which reduces sampling time, saves power consumption and area. Each working cycle adopts 1.5bit MDAC, where 1 bit is the effective bit and 0.5bit is the redundant correction bit.
In order to reduce the impact of the offset voltage of the comparator, the sub-ADC uses a pre-amplified large latched dynamic comparator, embeds an automatic zeroing technology.
The overall post-simulation results show that, when the sampling rate is 5MS/s, the input signal frequency is 300KHz, the input range is 0.4V~1.4V, the SNR of the Cyclic ADC is 70.4dB, the SFDR is 79.3dB, the THD is -77.8dB, and the ENOB is 11.28bit. The chip is under testing now, test results will be presented then as well.

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