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## Design and measurement of a large CMOS pixel with nanosecond collection time

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For particle counting detectors with high repetition rate, low latency and low jitter using direct detection of incident electrons, a short transit time of the secondary generated electrons and holes within the pixel structure is required. Additionally, for a pixel array that spans a large area, we wish to minimize the overall power consumption by minimizing the number of pixels, implying larger pixel areas. The conversion of electron-hole pairs generated by the incident electrons to a useful signal, requires a dedicated per-pixel circuit with a high SNR. Modeling and simulations show that this circuit requires a small input capacitance. Reducing the transit time can primarily be achieved through application of a (negative) backside voltage.

In this paper, we explore the trade-off of a short transit time in combination with a low junction capacitance and pixel area. We make a brief survey of different pixel topologies (SPADs, APDs, scintillators, resistive-feedback and capacitive-feedback transimpedance amplifiers) and compare their theoretical noise performance for high repetition rate counting applications.

We present TCAD simulations and measurements for an implementation of such a pixel in a mixed CMOS process. In TCAD, we attempt to extract a worst-case transit time. We observe a double peak in the current waveform.

We attempt to confirm these TCAD findings with measurements using a short pulsed laser using a wavelength of 640nm that exhibits a similar penetration depth as the Continuous Slowing Down Approximation (CSDA) of the incident electron.

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