



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences



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INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCES



中国科学院
上海微系统与信息技术研究所



上海科技大学
ShanghaiTech University

Performances of the first full-scale HYLITE readout chip and the prototype module of SHINE XFEL

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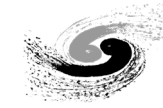
1 Institute of High Energy Physics, Chinese Academy of Science.

2 ShanghaiTech University.

3 Shanghai Institute of Microsystem and Information Technology, CAS.

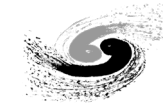
4 Institute of Microelectronics, CAS.

Outline



- Introduction: SHINE XFEL & STARLIGHT detector
- Chip Design of HYLITE
- Module Design and Production
- Test results
 - ASIC Performances
 - Module Preliminary Test
- Conclusions

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SHINE XFEL

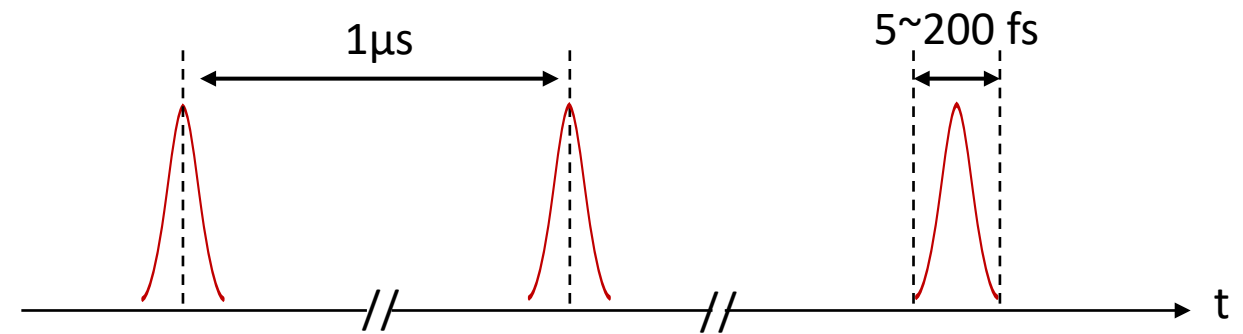


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Shanghai **H**igh repetition **N** rate
XFEL and **E**xtrême light facility

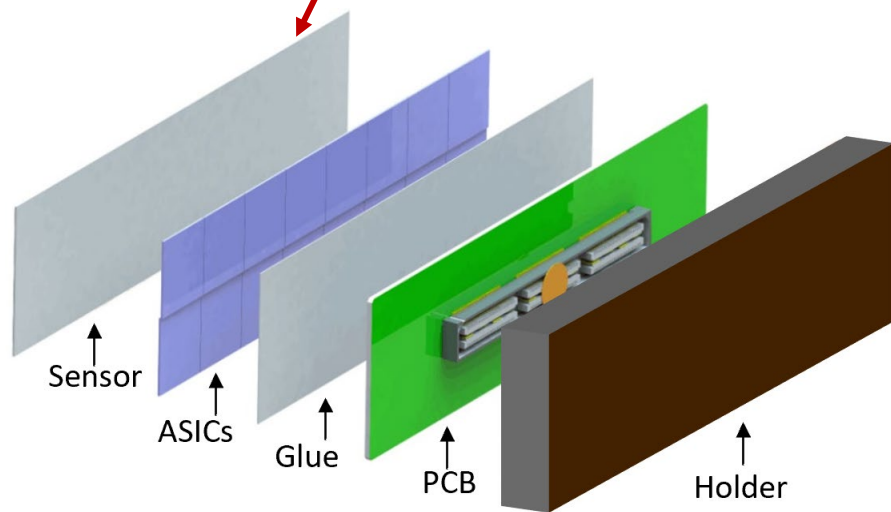
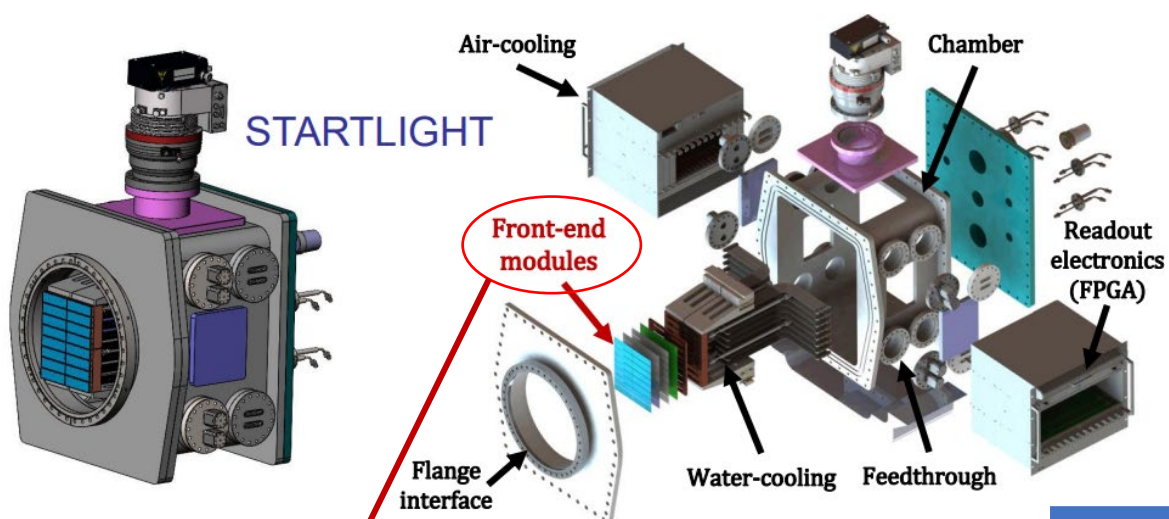
- 3 FEL beamlines: FEL-I, FEL-II, FEL-III
- Photon Energy: 0.4~25 keV
 - FEL-I: 3~15 keV
 - FEL-II: 0.4~3 keV
 - FEL-III: 10~25 keV
- Pulse Duration: 20~50 fs (5~200 fs)
- Repetition Frequency: 10kHz (1MHz)
- Peak Brightness: $10^{32} \sim 10^{33}$
photons/ $\mu\text{m}^2/\text{rad}^2/\text{s}/0.1\% \text{BW}$

Ref:doi:10.18429/JACoW-FEL2017-MOP055



Typical Time Structure of the SHINE Photon Beam

STARLIGHT Detector

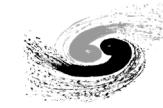


Front-end Module Structure

- Semiconductor Array detector with Large dynamic range and charge integrating readout
- The first step is to develop a single module detector with 200 μm pixel pitch and 1kHz frame rate to explore and verify the whole production process.

Specs	Ultimate Parameters	The First Step
Sensor	500 μm silicon PIN	/
Pixel Size	100 μm \times 100 μm	200 μm \times 200 μm
Array Size	128 \times 128	64 \times 64
Dynamic range	1~10000 ph./pulse/pixel @12 keV	/
Frame rate	12kHz (continuous readout)	1kHz
Detector	A 4M pixel detector in vacuum, quadrant movable	2*8 ASIC module

Outline

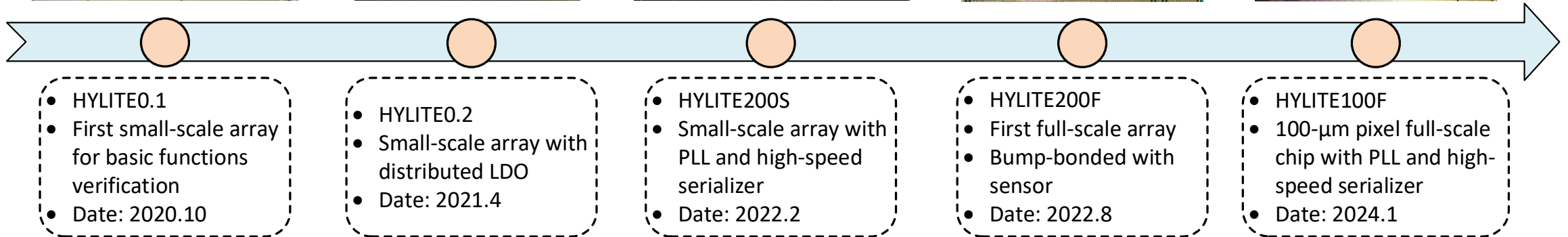
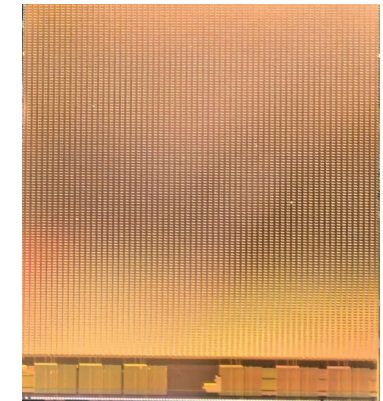
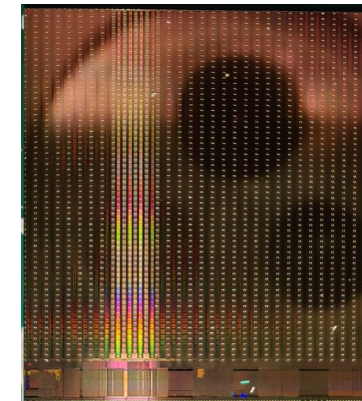
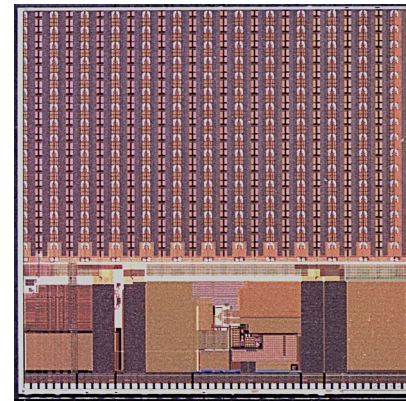
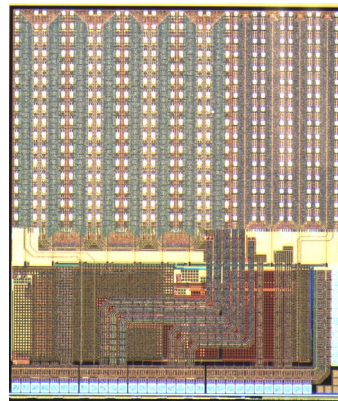
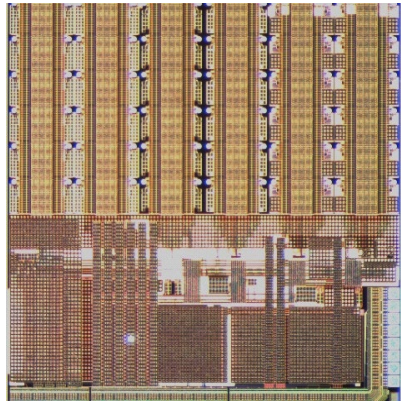


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HYLITE: the Readout Chip



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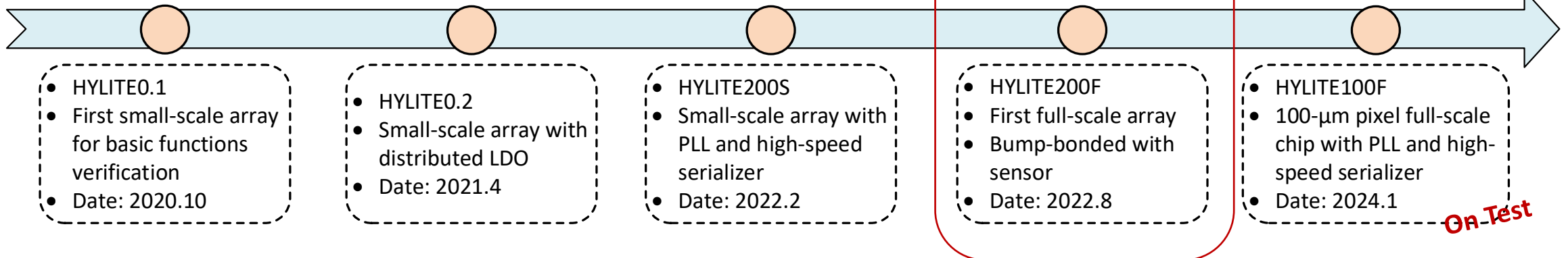
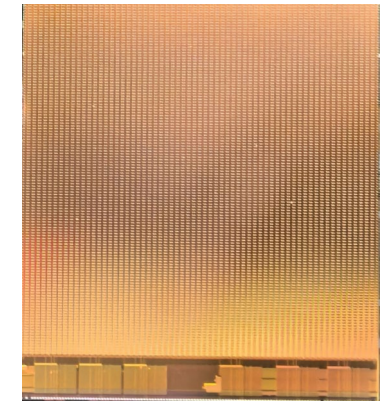
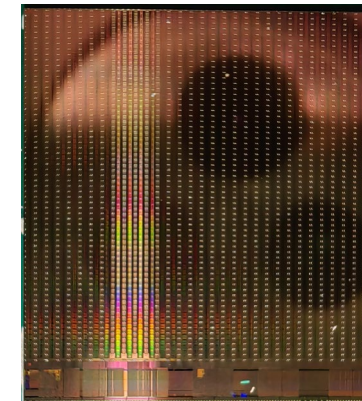
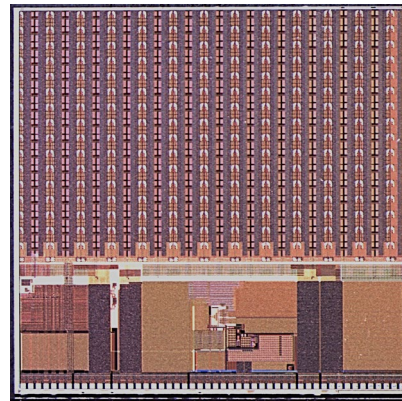
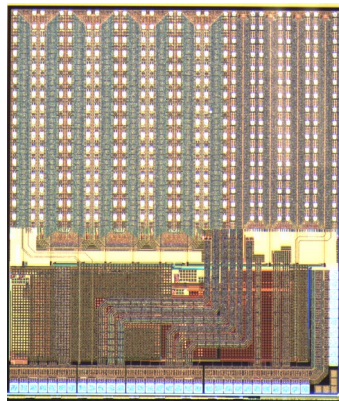
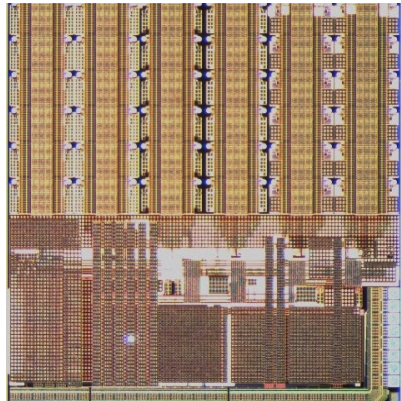


- **HYLITE** (High dYmamic range free electron Laser Imaging deTEctor) is a **charge-integration** pixel detector readout chip, which is designed for SHINE STARLIGHT Detector.

HYLITE: the Readout Chip

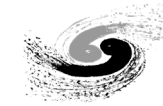


Today's Talk



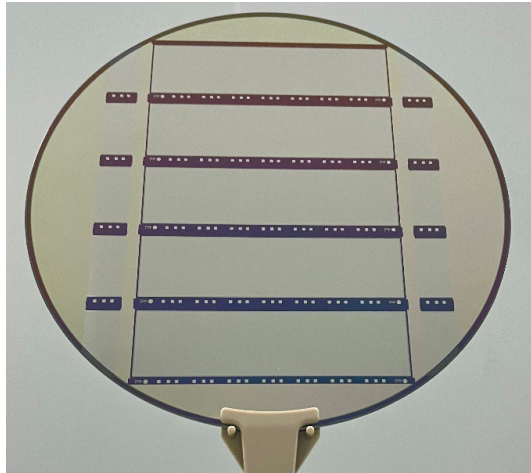
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Outline

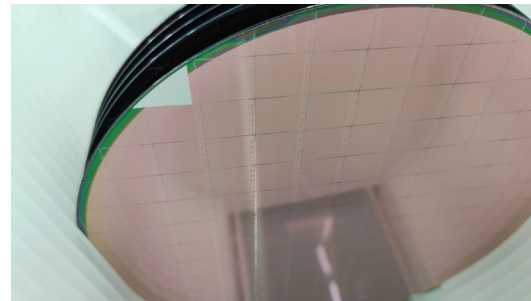


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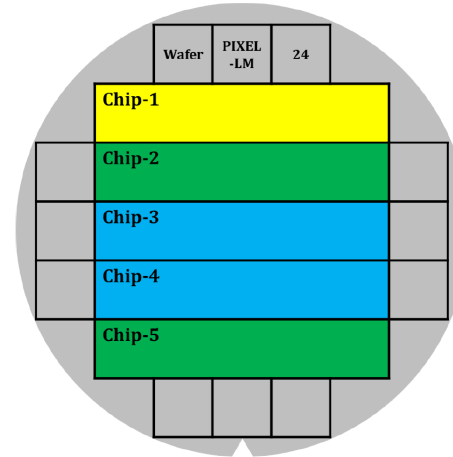
Sensor & ASIC Wafer Test



8-inch sensor wafer



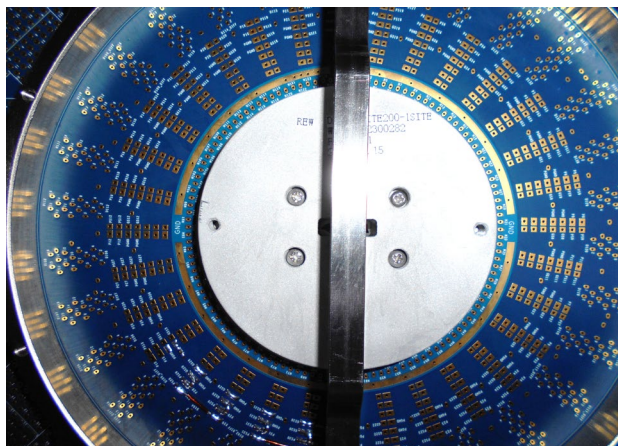
ASIC Wafers



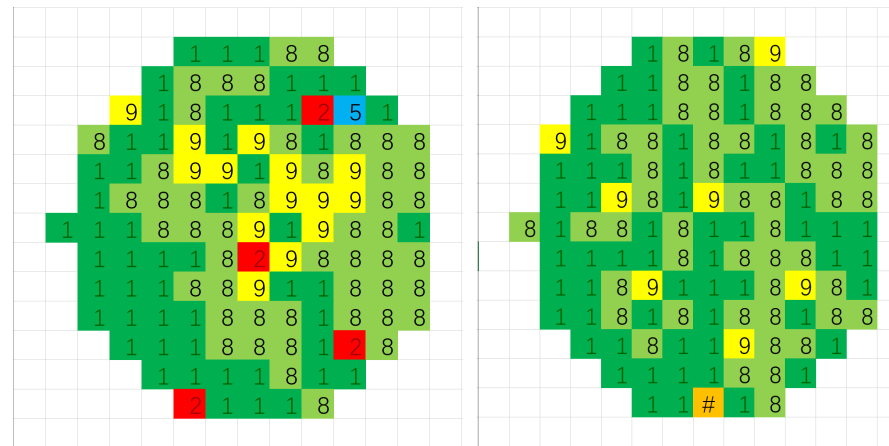
Sensor Level Map

● Sensor

- Large Area: 10.5cm*2.8cm
- Manufactured by photolithography graphic splicing
- Classified into 5 levels
- The A+ and A levels are accepted for bump bonding.



ASIC Wafer Probe Card



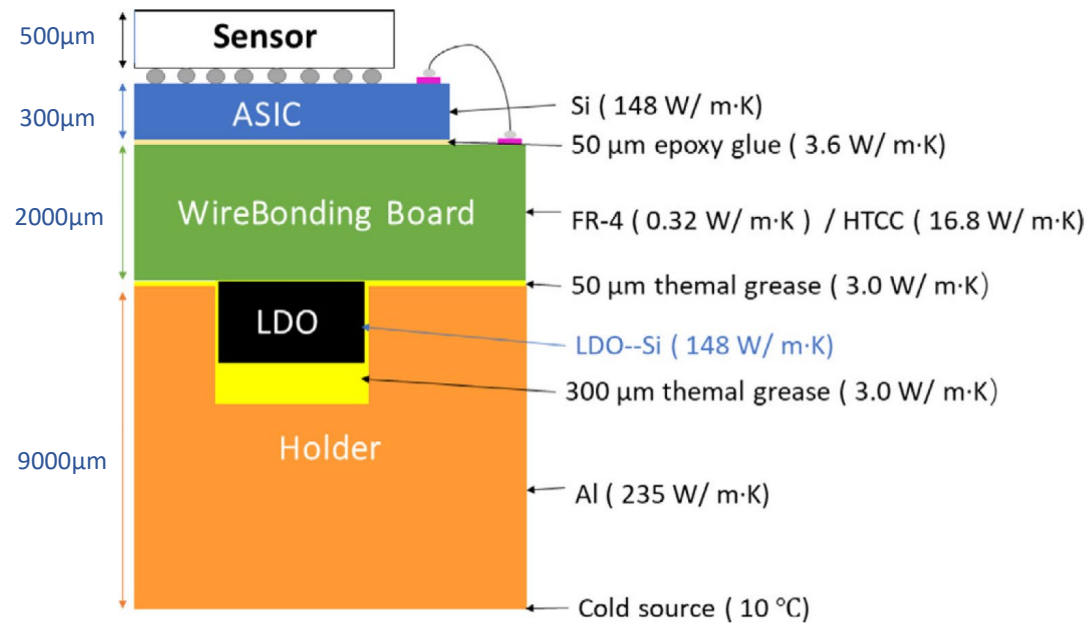
ASIC Level Map

● ASIC

- level 1, 8, and 9 are accepted.
- Average yield of 5 wafers: **83.7%**

Ref: doi:10.1016/j.nima.2023.168388

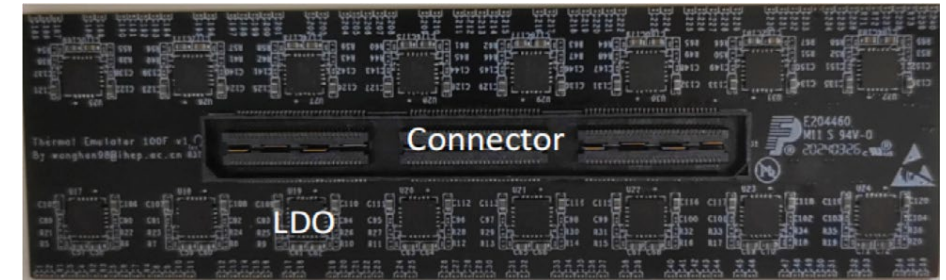
Module Mounting: preparation



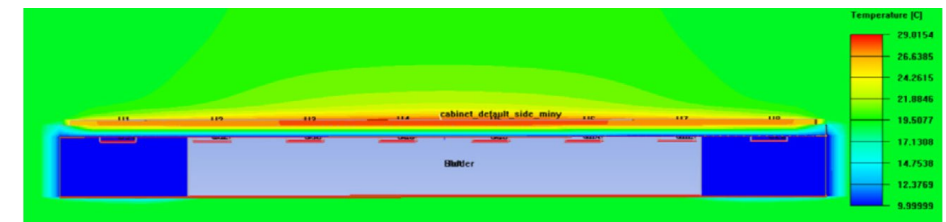
Module Structure and Corresponding Temp. Factors



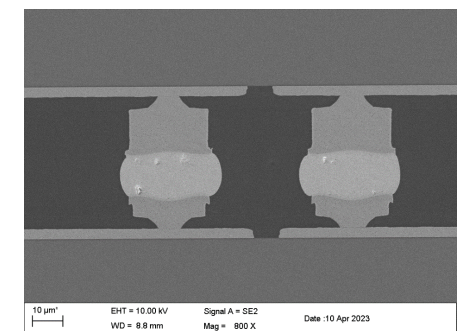
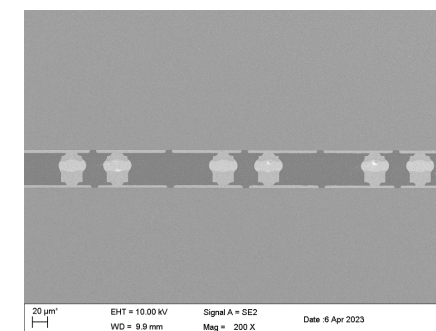
Bump Bonding Process Verification with Dummy Dies



Wire-bonding board

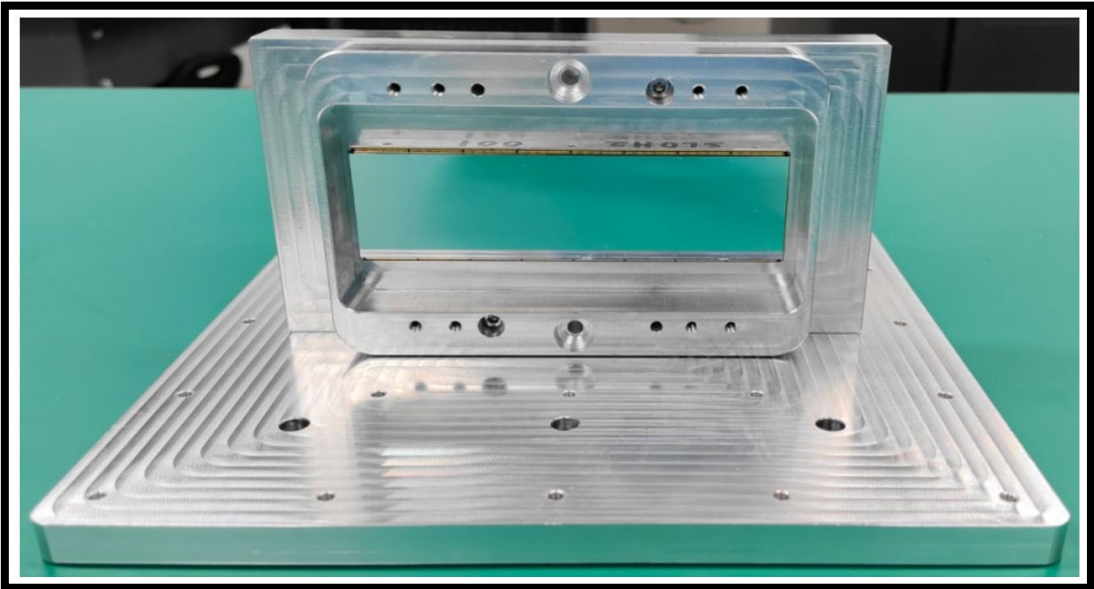


Thermal simulation of the wire-bonding board

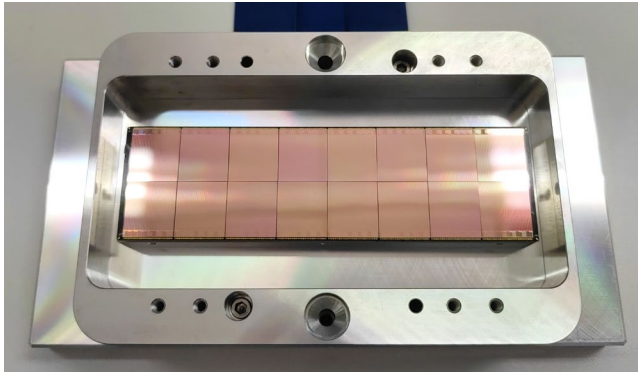
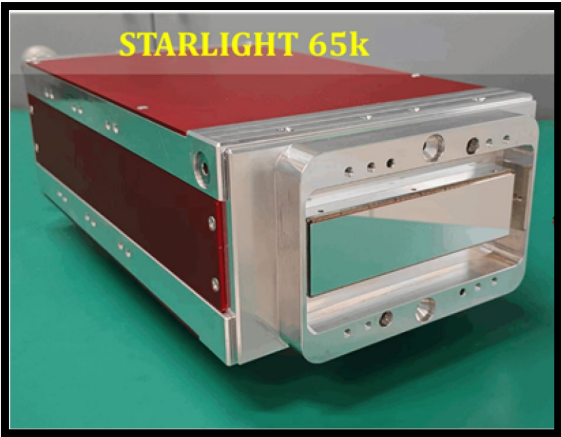


Bump Quality Verification

Modules



Different Scales of the Prototype Module

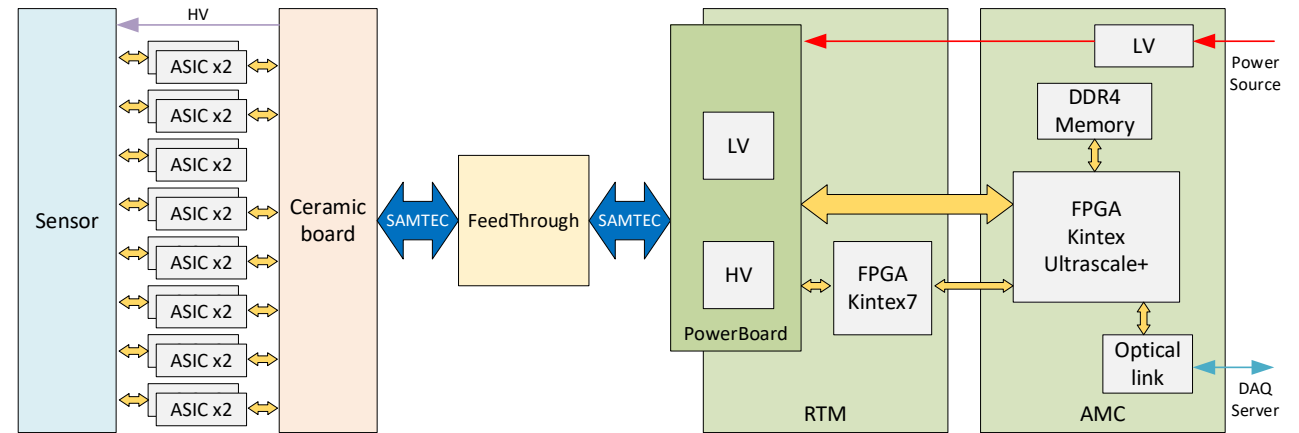


2*8 ASICs mounted on the module PCB
without sensor

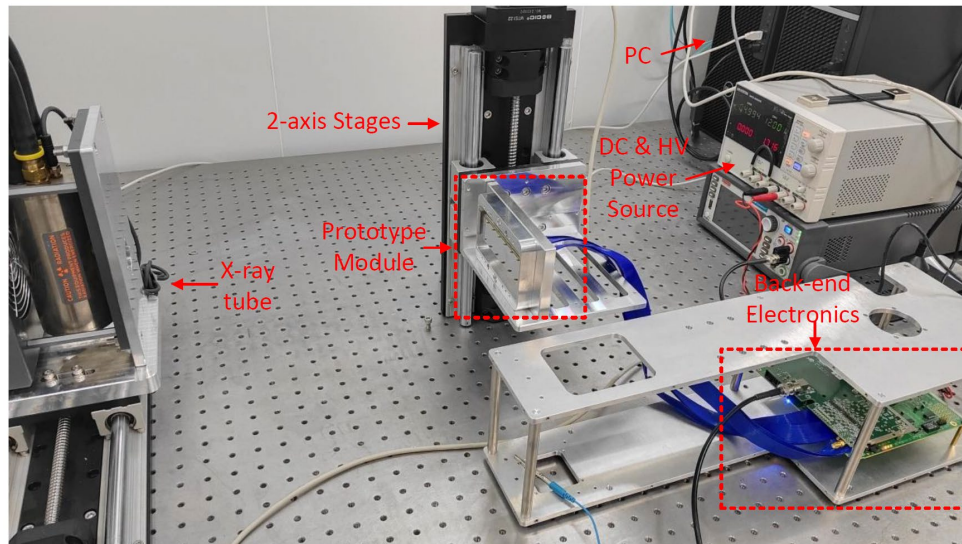
Testing Setup



Readout FPGA Board



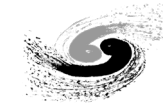
Structure of the readout System



Test Environment

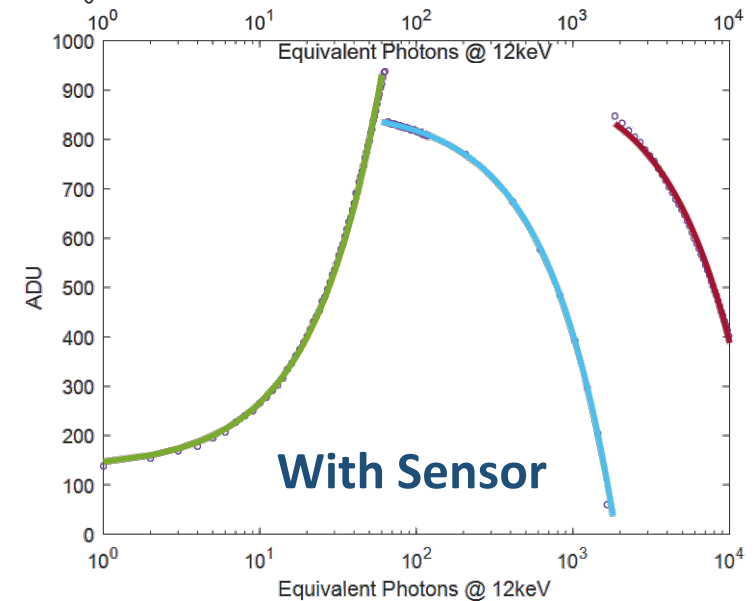
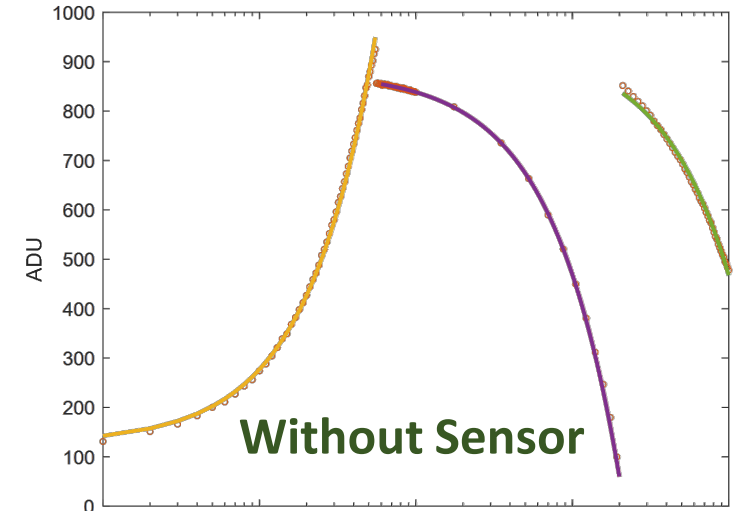
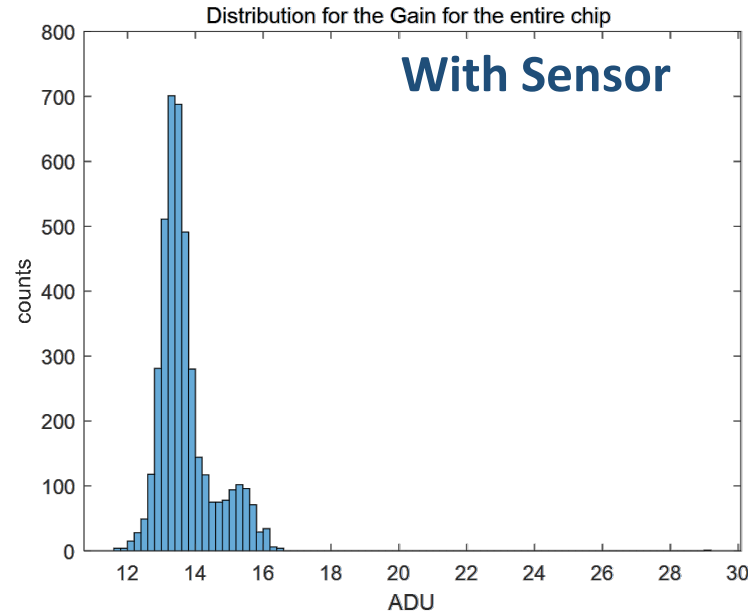
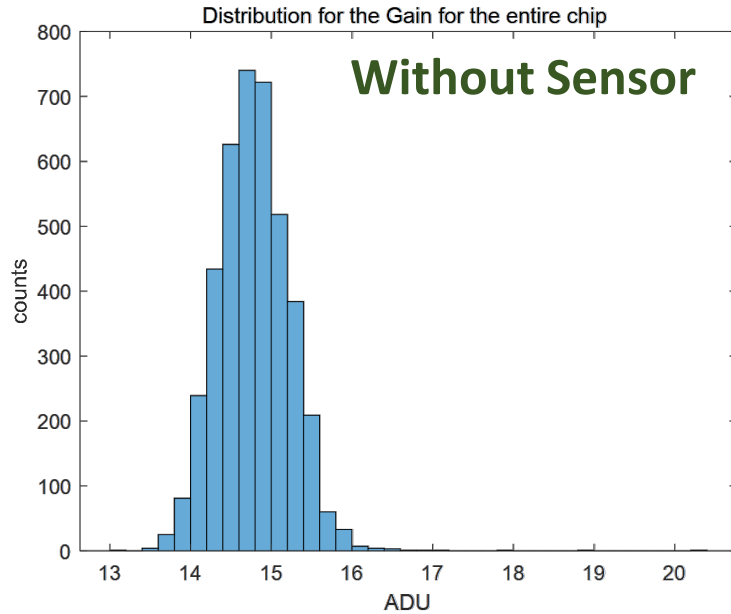
- The core of the chip and module testing setup is of the back-end FPGA board: RTM
- As the first step, chips are read out in sequence. Parallel readout is on developing.
- Internal calibration circuits and X-ray tube are adopted as the input source.

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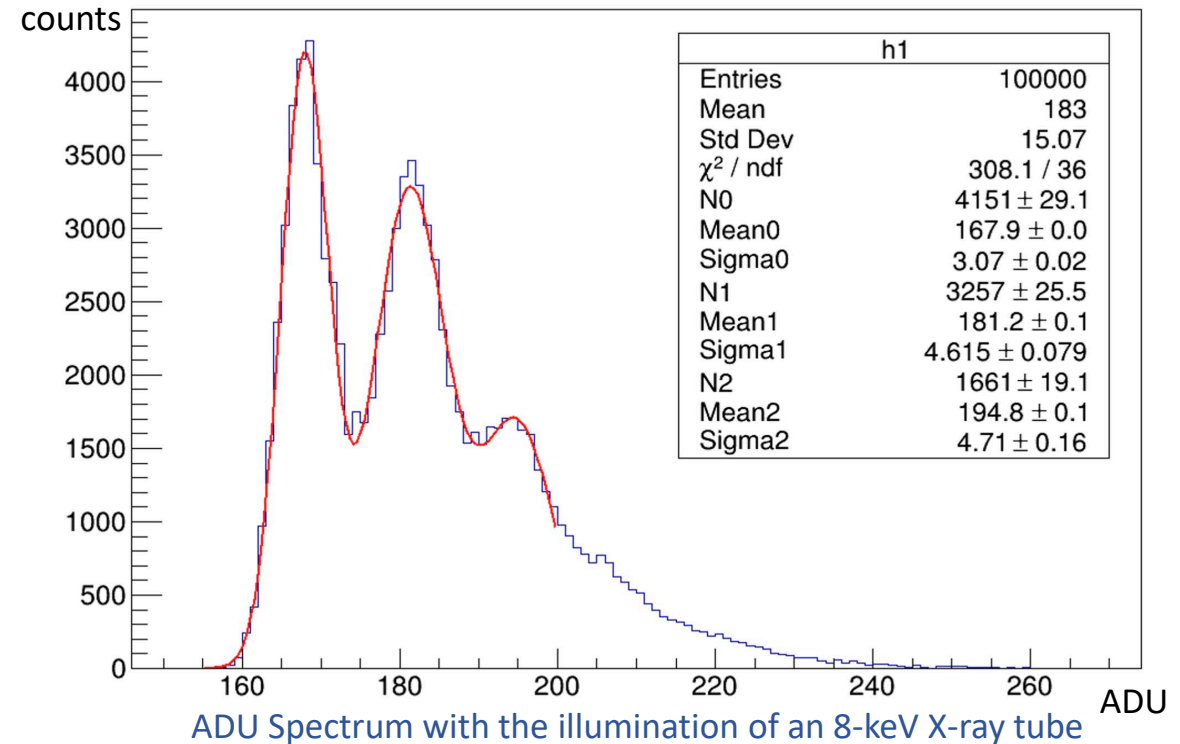
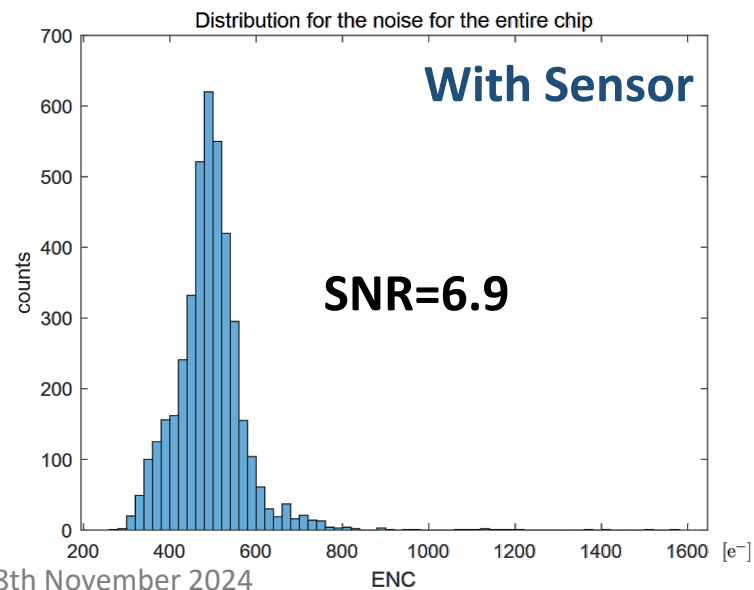
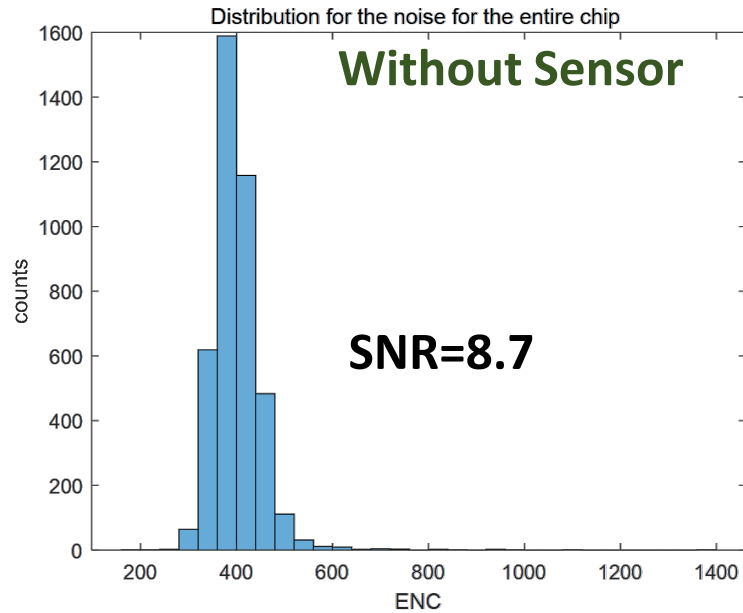
Dynamic Range & Gain by Self-Cali



	High Gain	Medium Gain	Low Gain
With Sensor	14.8 ADU/ph.	0.416 ADU/ph.	0.0413 ADU/ph.
Without Sensor	13.7 ADU/ph.	0.471 ADU/ph.	0.0440 ADU/ph.

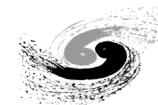
- 1 “Photon” is generated by an 8-mV step pulse and internal capacitors, which need further calibration.

Noise

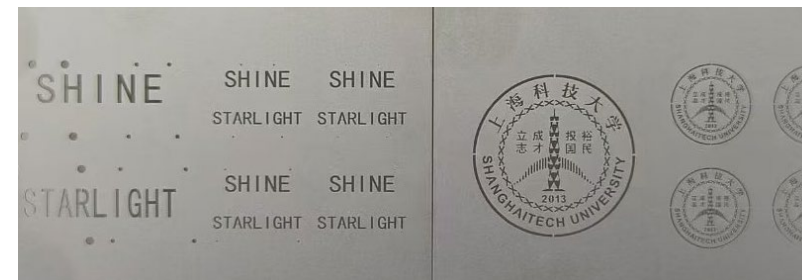
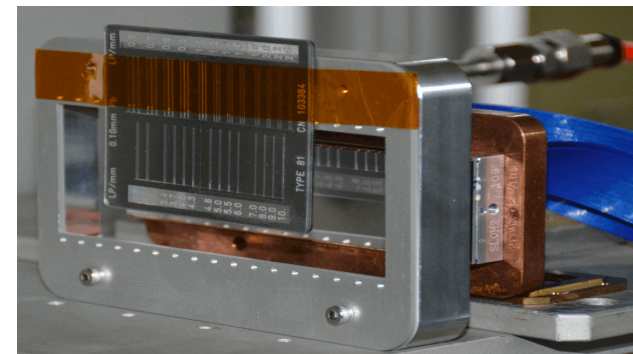
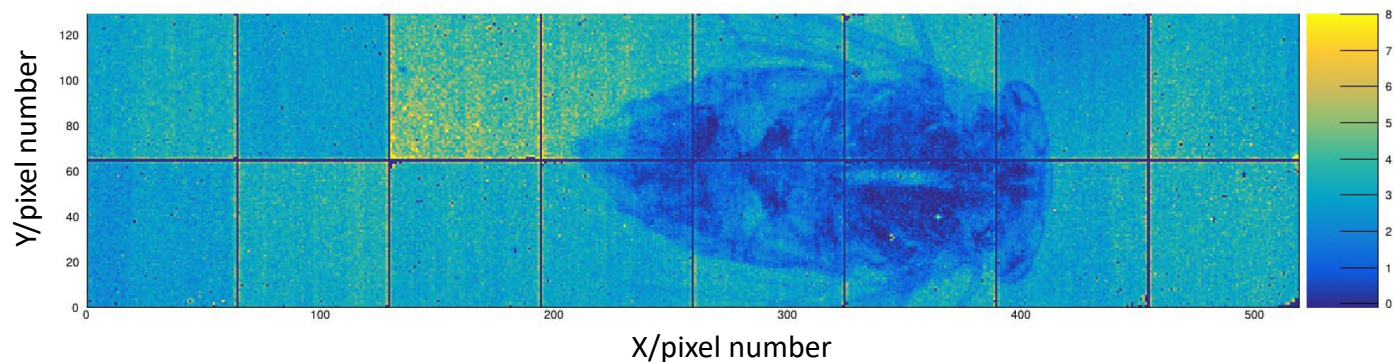
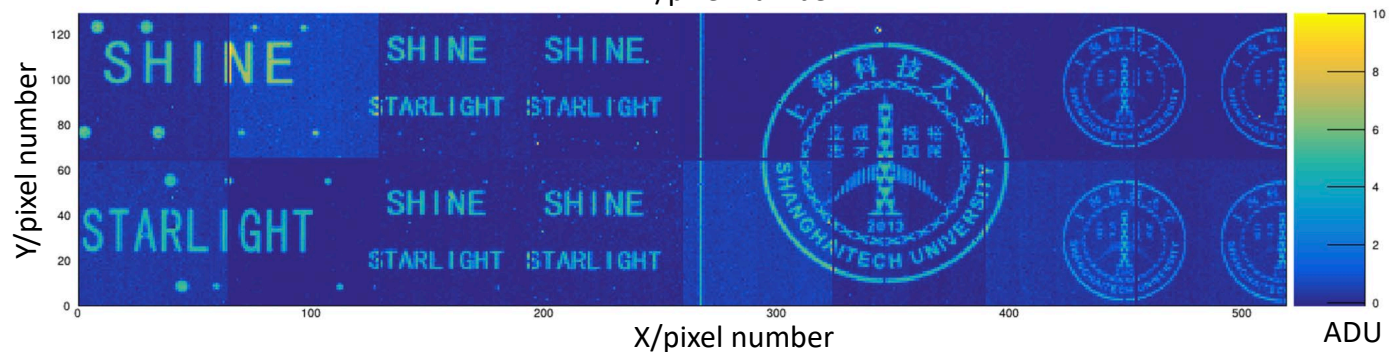
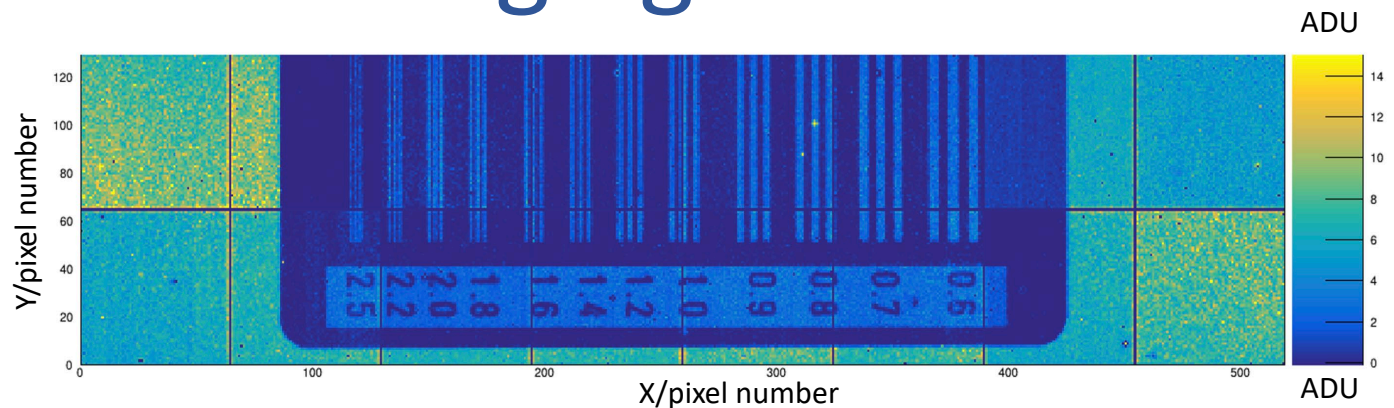


- ENC: 386 e- vs. 487e- @ single photon injection.
- X-ray tube test shows the pedestal, single-photon peak, and two-photon peak.
- The absolute calibration will be carried out on a synchrotron beamline.

Static Imaging Test

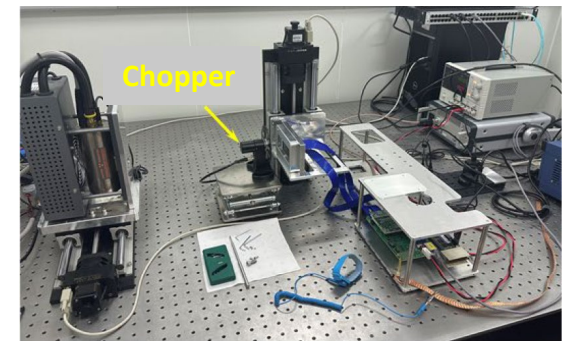
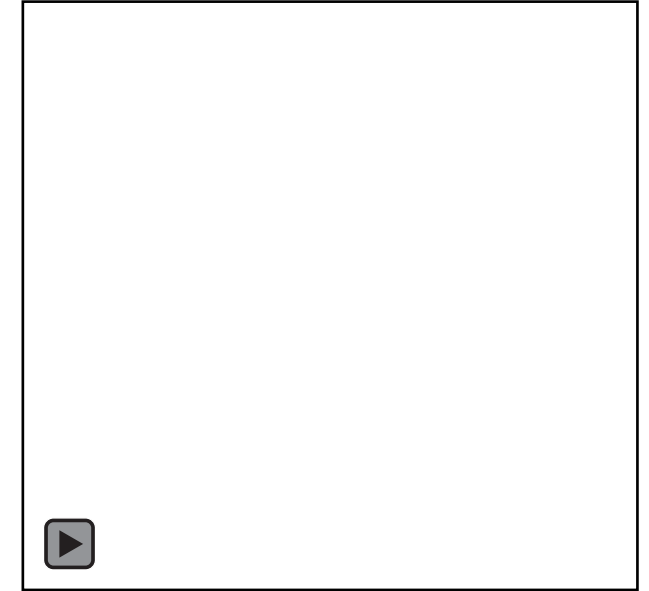
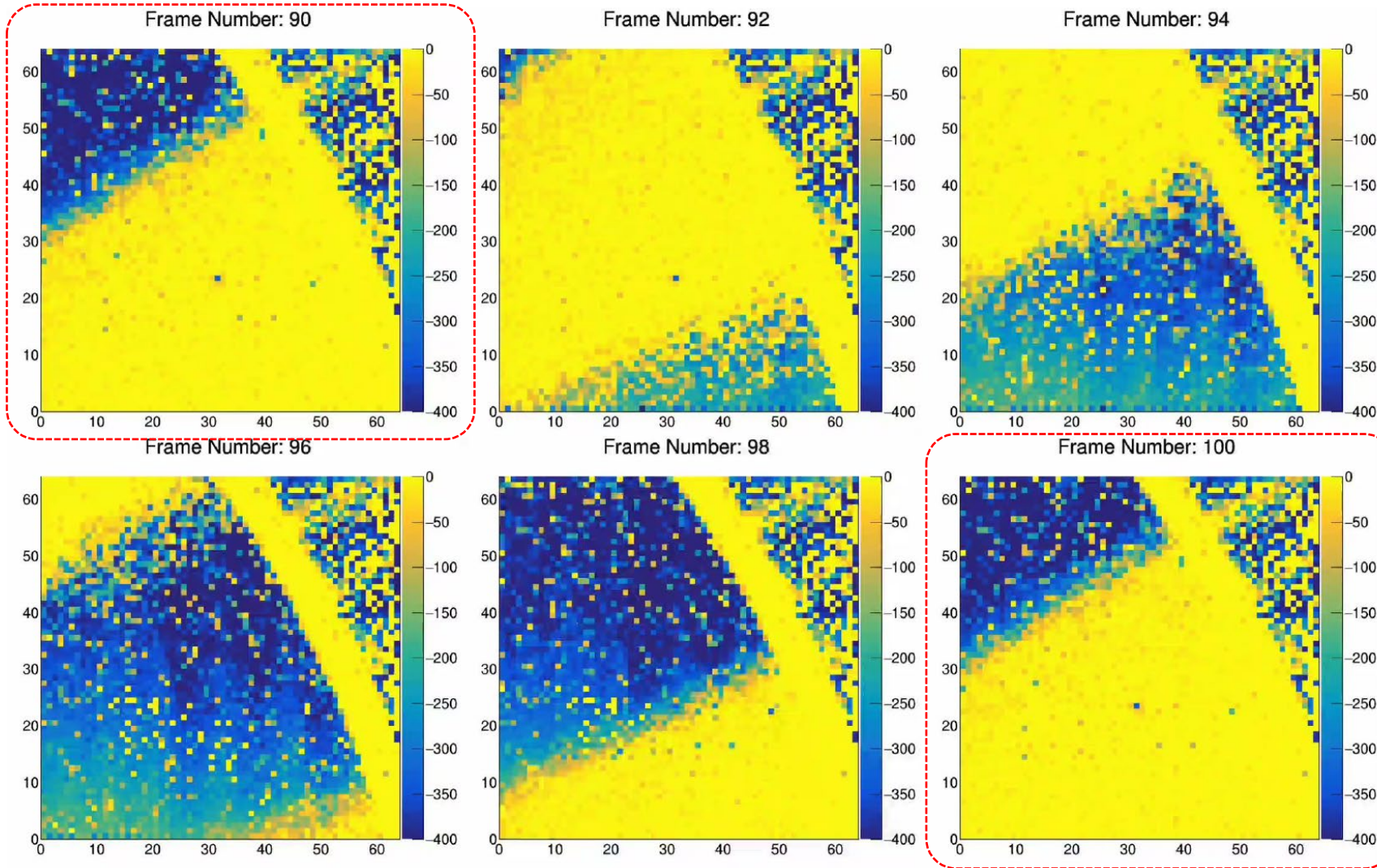


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- Preliminary Test **Without Calibration**

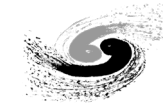
Dynamic Frame Rate Test



● Frame Rate: 1 kHz

Chopper Rotation frequency: 100Hz

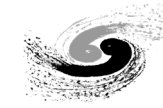
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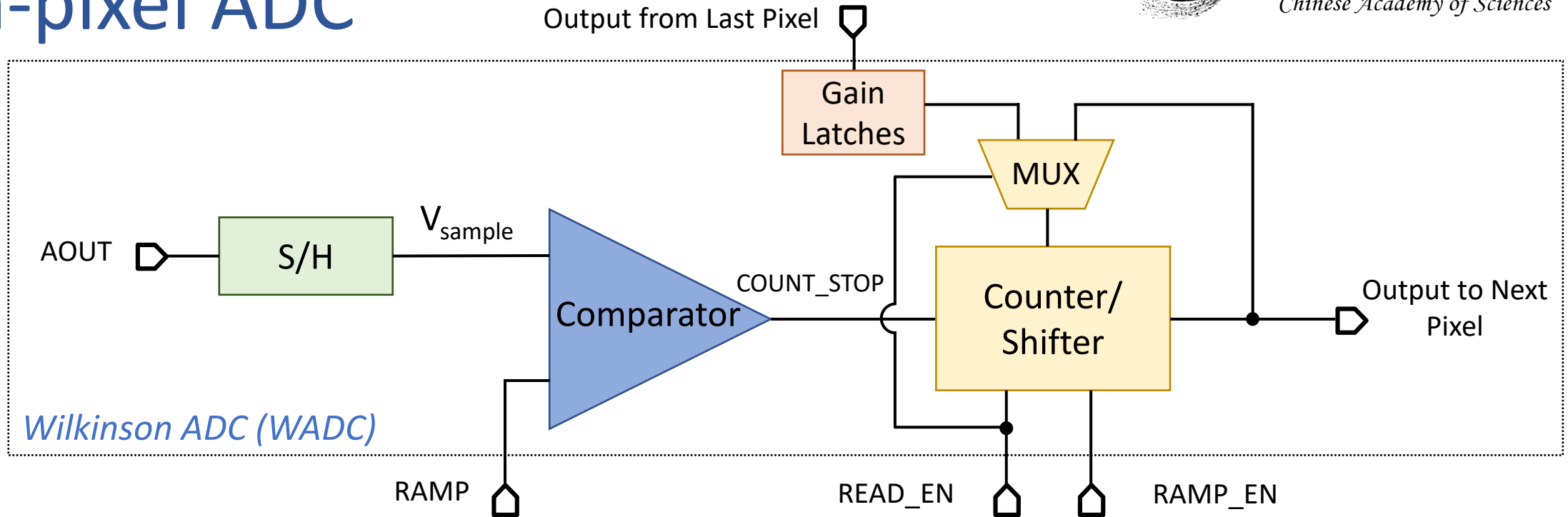
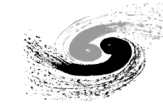
Conclusions

- HYLITE200F is the first full-scale engineering-run chip of HYLITE. The ASIC shows correct functions and good yields.
- Imaging tests indicate that the module works properly and the frame rate can reach the goal of 1 kHz.
- As the next step, the bump-bonding process will be improved further. Detailed tests and calibrations will be carried out on the full-size module.



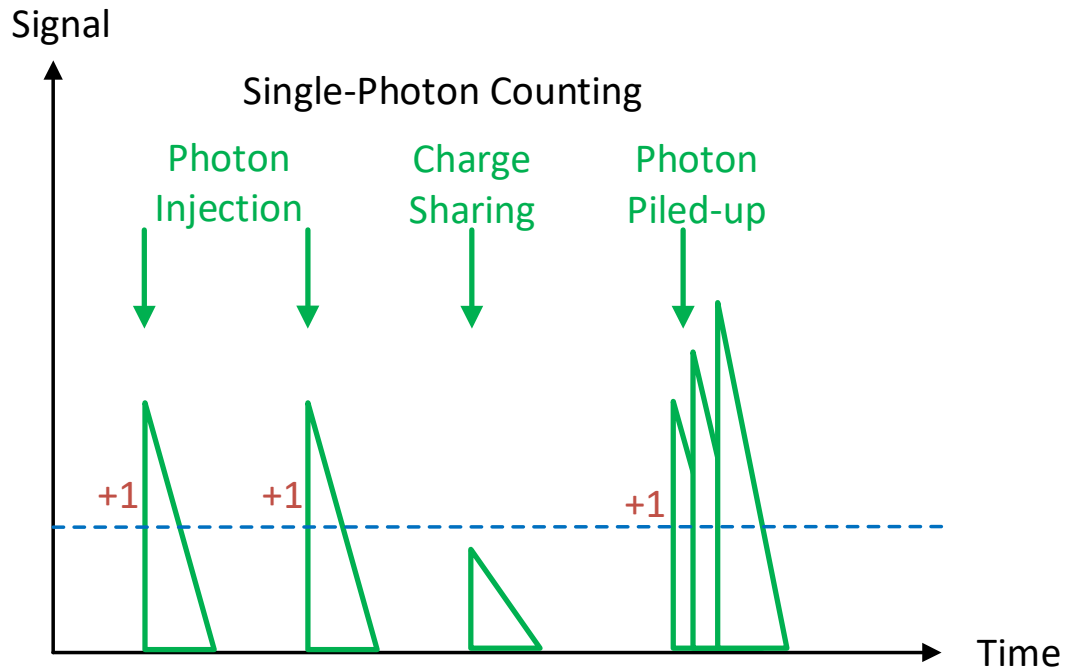
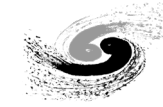
Back Up Slides

In-pixel ADC

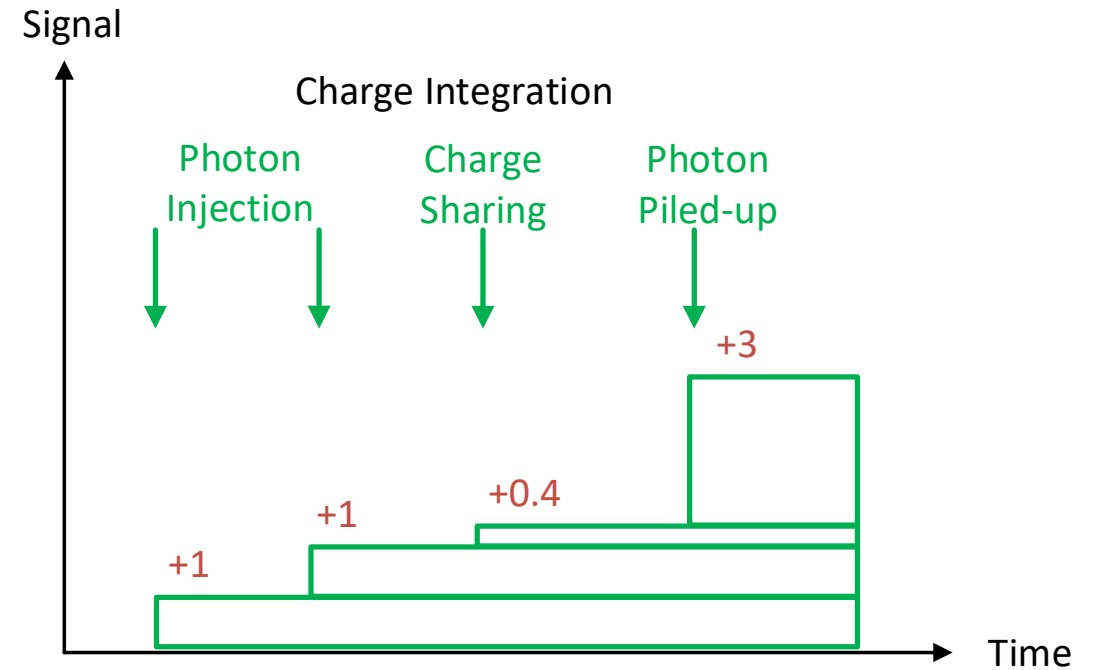


- S/H: Sample and Hold Circuit
- Comparator: Generates the stop signal of counting
- Counter/Shifter: Based on a 10-bit Linear Feedback Shift Register (LFSR), working frequency: 50 MHz
- MUX: Switches modes between counting and shifting
- Gain Latches: 2-bits registers latches gain, located in gain-switching circuits
- Power Consumption: 7.5 μ W

Counting VS Integrating

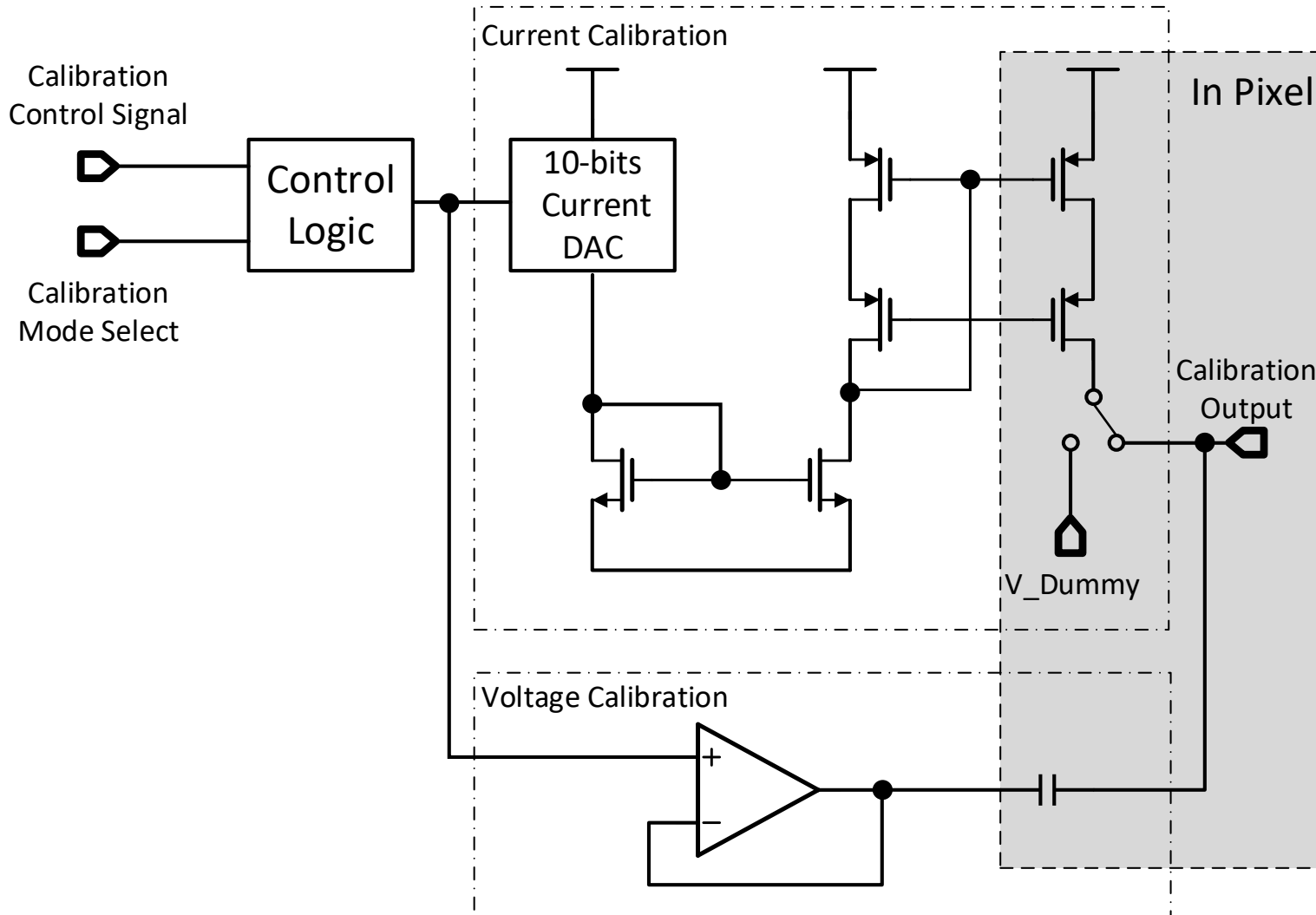
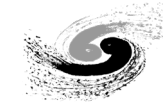


- “Zero Noise” but photons are piled up.



- All of the Charges are integrated including noise.

Calibration Block



- Covers Full Dynamic Range of 10000 photons @12 keV
- Voltage Mode
 - High Linearity
 - Small Input Range
 - 8 mV amplitude voltage pulse -> a 12 keV Photon (“equivalent photons” by calculating input charges)
- Current Mode
 - Large Input Range
 - Worse Linearity
 - DAC Code=1, 150 ns width digital pulse -> 10 12 keV Photons

Energy Linearity

