Eleventh International Workshop on Semiconductor Pixel Detectors for Particles and Imaging

ID de Contribution: **30** Type: **Oral**

Characterization of silicon Monolithic Stitched Sensors (MOSS) for the ALICE ITS3 for the LHC Run 4

jeudi 21 novembre 2024 16:40 (17 minutes)

ALICE (A Large Ion Collider Experiment) is one of the four main experiments at the CERN Large Hadron Collider (LHC), and it is mainly designed to study heavy-ion collisions at ultra-relativistic energies. In view of the LHC Run 4, foreseen to start in 2029, ALICE will replace the three innermost cylindrical layers of its current inner tracking system (ITS2) during the Long Shutdown 3 (2026-2028).

The new system, ITS3, will improve the pointing resolution by a factor of two over a large momentum range and the tracking efficiency at low transverse momenta of $p_T < 0.3$ GeV/c. It will consist of ultra-thin, i.e. ≤ 50 µm, stitched wafer-scale Monolithic Active Pixel Sensors (MAPS), built using the 65 nm CMOS imaging process. These sensors can be bent, allowing the formation of truly cylindrical barrel with a radial distance from the beam pipe as low as 19 mm for the innermost layer and a very low material budget of 0.09 X/X_0 in average per layer.

The development of the ITS3 includes a number of cutting-edge R&D efforts: the production and characterization of the MAPS in the 65 nm CMOS process, the fabrication of the stitched wafer-scale MAPS, and the development of an ultra-light detector mechanics and a new air cooling system. In particular, the 65 nm CMOS technology for particle tracking and radiation hardness was validated with a set of test structures called Multi-Layer Reticle 1 (MLR1). In mid 2023 the first stitched prototypes called MOnolithic Stitched Sensors (MOSS) have been produced with the primary goals of demonstrating the feasibility of the stitching process and of studying the yield and performance of wafer-scale sensors, in view of the production of the ITS3 final-size full-functionality prototype sensor chip.

A single MOSS chip measures 1.4×25.9 cm^2 and has a total of 6.7 million pixels. It is composed of one left endcap, 10 repeated sensor units with eight pixel matrices each, to increase power granularity and hence resilience to manufacturing faults: 256×256 pixels with 22.5 µm pitch in each top matrix and 320×320 pixels with 18 µm pitch in each bottom matrix. The different layouts are used to compare the yield depending on the densities and spacing margins.

This presentation will focus on the results from the characterisation campaign of the stitched sensors in the laboratory and in beam tests, including the verification of power domain impedances, DAC performance, pixel front-end readout response, threshold and fake-hit rate scans. Test results have proven that MOSS has an efficiency higher than 99% with a Fake Hit Rate lower than 0.1 $pixel^{-1}$ s^{-1} , which satisfies ITS3 sensor requirements for LHC Run 4.

Auteur principal: TERLIZZI, Livia (Università and INFN Torino)

Orateur: TERLIZZI, Livia (Università and INFN Torino)

Classification de Session: Monolithic sensors

Classification de thématique: Monolithic sensors