ID de Contribution: **26** Type: **12mOral**

Suitability of a 65 nm CMOS imaging process to reach the position resolution required by a vertex detector at FCCee

jeudi 21 novembre 2024 17:48 (17 minutes)

The performance of monolithic CMOS pixel sensors depends on their fabrication process and especially the feature size which directly drives the pixel size. A consortium led by the CERN EP R&D program, the ALICE experiment, and various European projects (AIDAinnova, EURIZON) is investigating the benefits of a 65~nm CMOS imaging process to design a new generation of pixel sensors. These developments have enabled the upgrade of the inner layers (ITS3) of the ALICE experiments and are fostering further studies for detectors including those for future e+e- colliders that are still currently unmatched by any technology.

Three fabrications of a variety of prototype sensors already took place, in 2020, 2022, and 2023. The present contribution reports on the characterization of the second version of the CE-65-v2 (Exploratory Circuit) sensor family. The CE-65-v2 sensor includes AC-coupled and analog output pixels either in a squared or staggered arrangement. They include analog output matrices featuring 48×24 (1152) pixels with either 15-µm, 18-µm or 22.5-µm pixels. Three versions of the sensing node were fabricated to modify the charge sharing between pixels. Sensors were irradiated to non-ionizing fluences between 10^{13} and 5x10^{14} n_{eq} as well as to few hundreds Mrad as ionizing dose. Illumination with Fe source allowed us to estimate the equivalent collection node capacitance and its pixel-to-pixel fluctuation, as well as the leakage current before and after irradiation. Non-irradiated sensors were tested in beams with 4-GeV electron or 120-GeV mixed hadrons to study in detail the charge sharing among pixels and extract the sensor detection efficiencies as well as their position resolutions. The evolution of the latter with digitization strategies, simulated from the data, was also investigated to explore the potential of pixels with binary or few bits output, designed in this 65-nm process, to match the excellent resolution expected for the inner layers of an FCCee detector. We pursue to continue developing the 65-nm process to fulfill all FCCee vertex detector requirements and improve upon them.

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Classification de Session: Monolithic sensors

Classification de thématique: Monolithic sensors