Suitability of a 65 nm CMOS imaging process to reach the position resolution required by a vertex detector at FCCee

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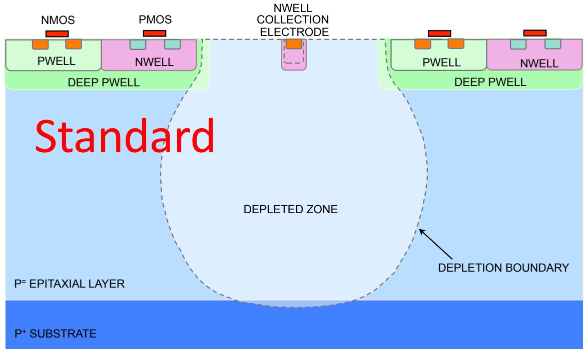
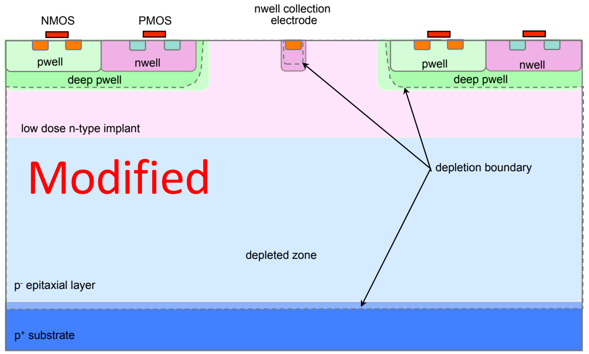
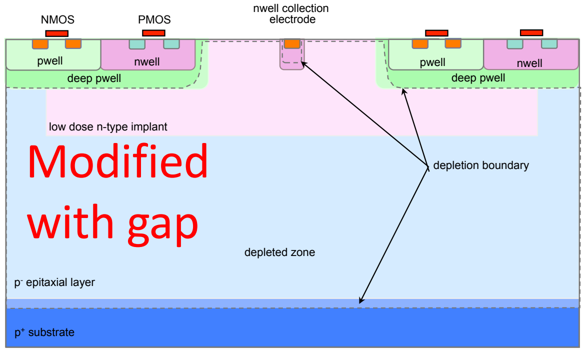
TPSco 65 nm: Benefits and Specifities

- Benefits: 65 nm vs 180 nm
  - Better spatial resolution due to smaller feature size
  - Larger wafers: 300 mm vs 200 mm => final sensor: 27x9 cm^2
  - Lower power supply: 1.2 V vs 1.8 V => Low power consumption
  - Lower material budget: thinner sensitive layer (~ 10 um)
- Provides 2D stitching
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)





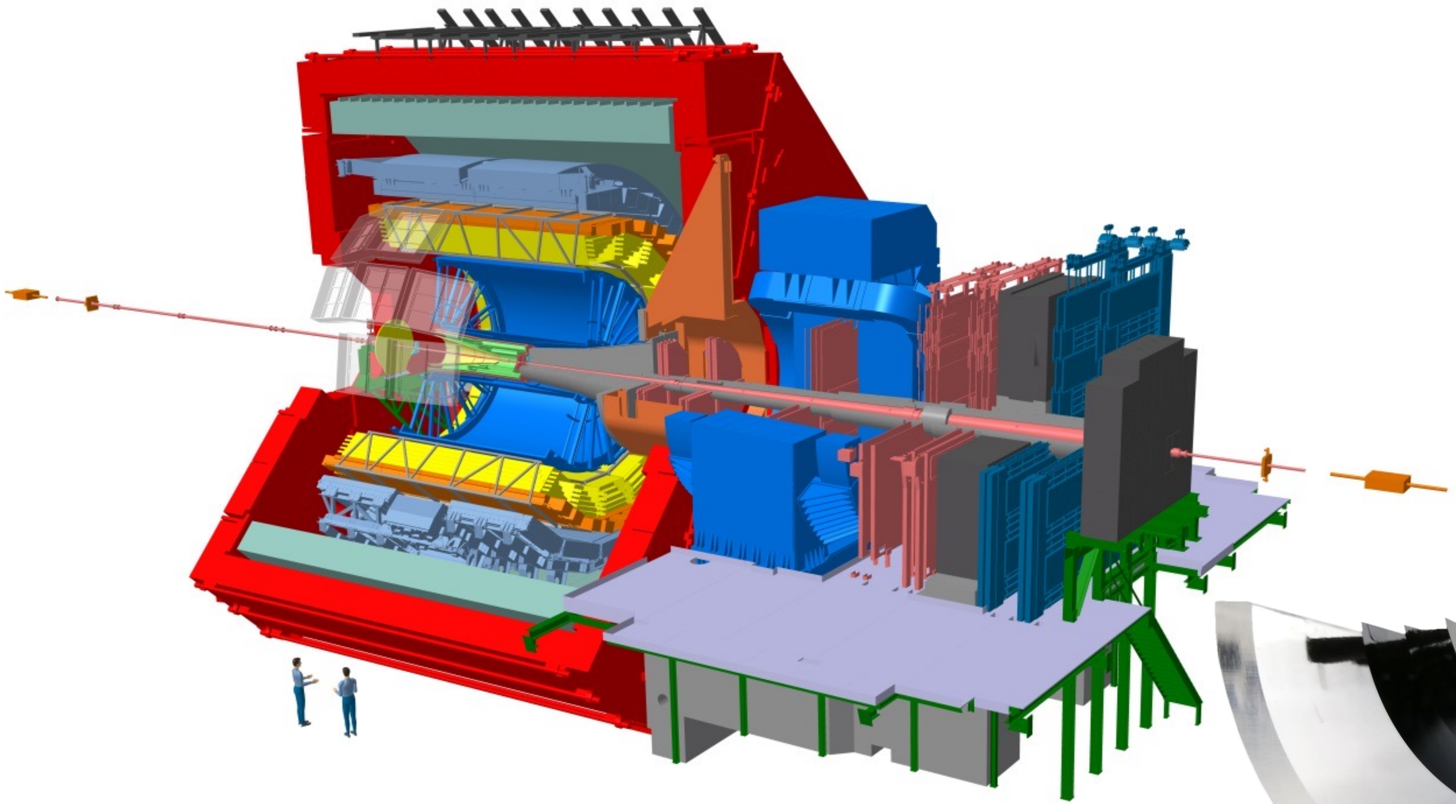
https://doi.org/10.1016/j.nima.2017.07.046



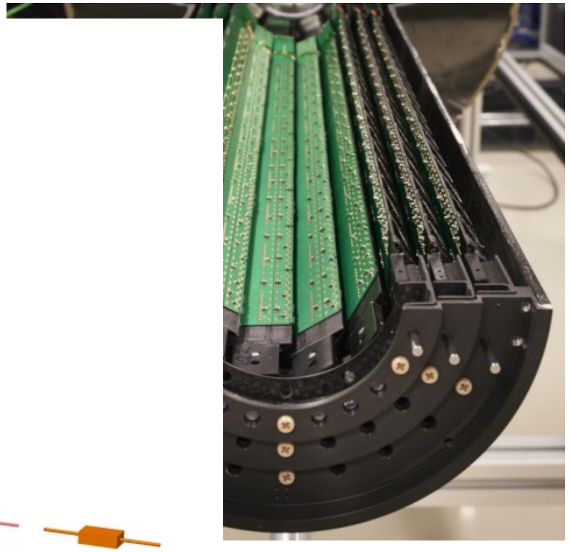
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

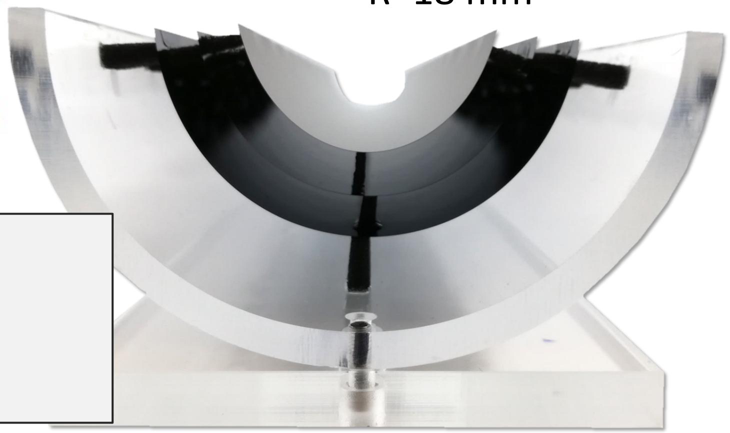
ALICE DETECTOR LS3 UPGRADE: ITS2 (180 nm) → ITS3 (65 nm)

R. Ricci, PSD 2023



ALICE – general purpose detector at LHC:
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)





ITS2:

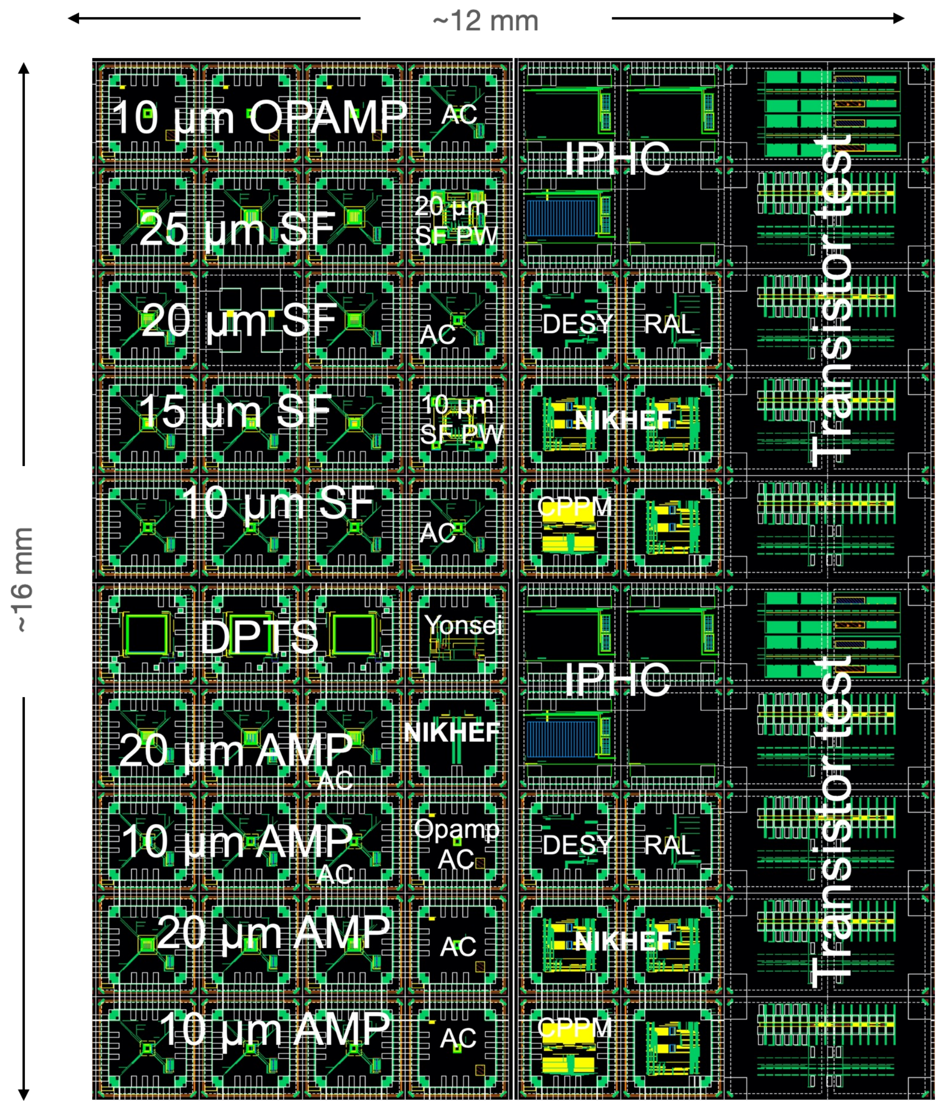
(S.Beolé, iWoRiD 2022)
- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 μm^2
- Water cooling
- **0.3 % X_0 / inner layer**

ITS3

(M. Šuljić, iWoRiD 2023)
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness <= 50 µm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

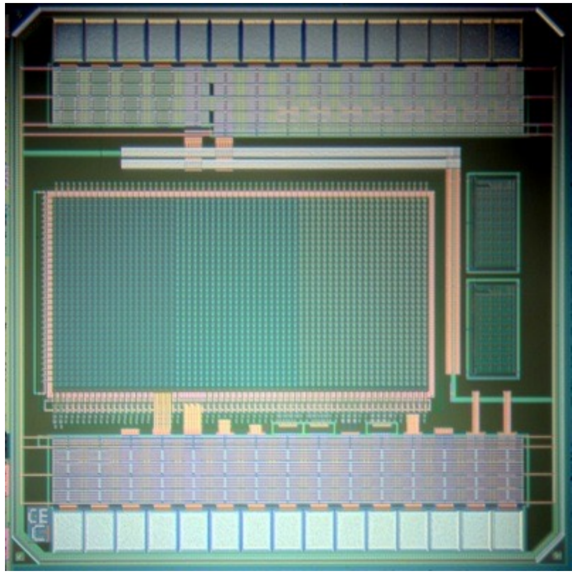
First test submission : MLR1

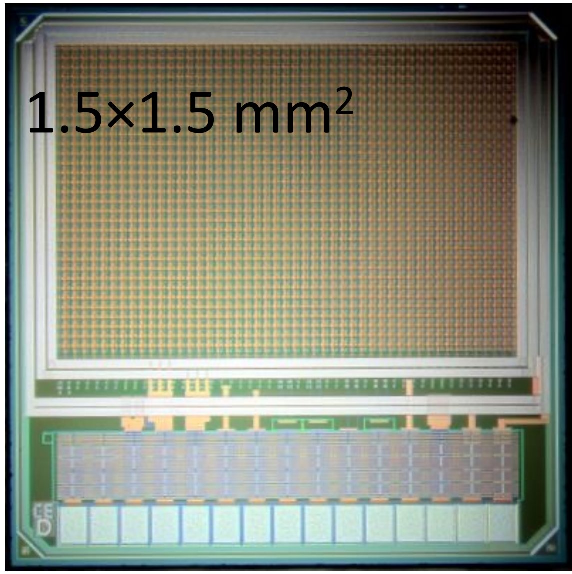
- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**



Circuit Exploratoire : CE-65 nm

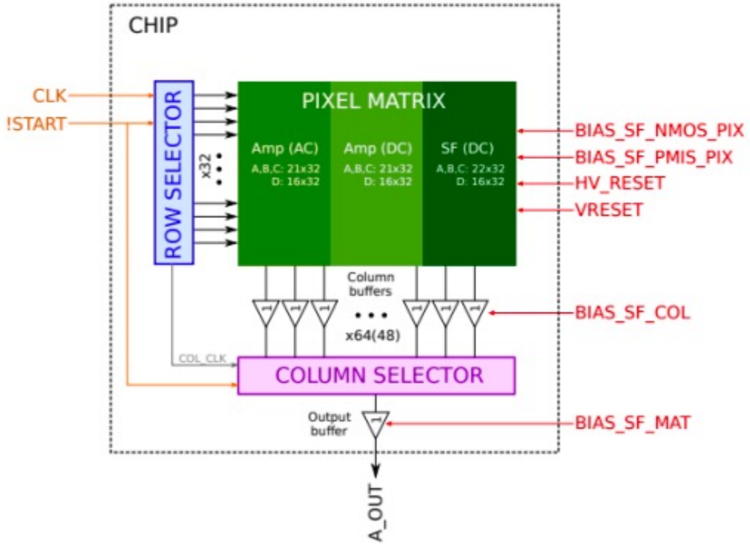
- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch
- Fabrication in September 2021
- Presented results from CERN PS beam test : May 2022





CE-65 nm variants: pixel pitch and process

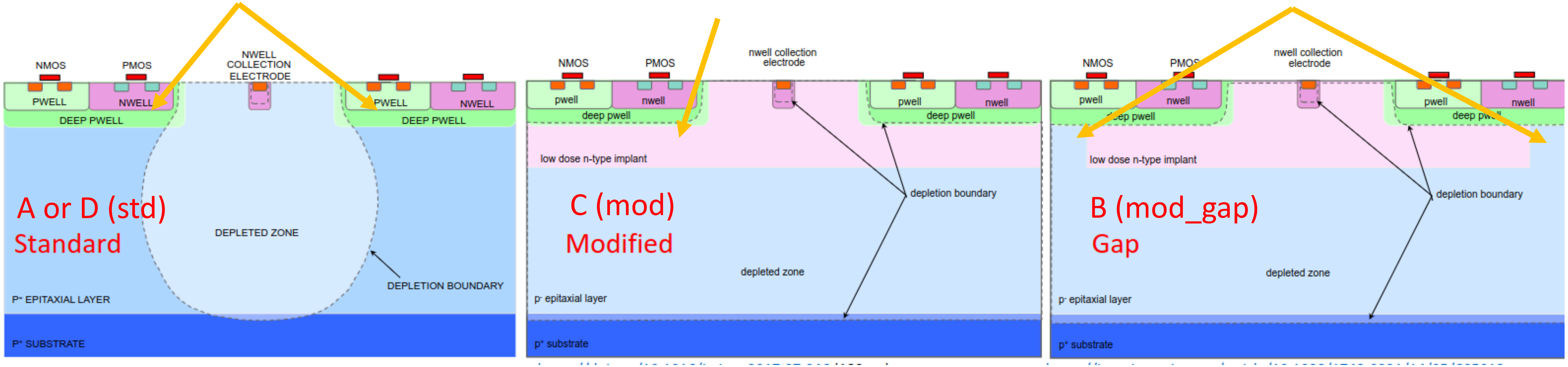
Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	$15\mu m$	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	$15\mu m$	64×32	AC/21, DC/21, SF/22
CE65-C	mod	$15\mu m$	64×32	AC/21, DC/21, SF/22
CE65-D	std	$25\mu m$	48×32	AC/16, DC/16, SF/16



Prevent circuitry's nwells from collecting charge

To obtain a full depletion

To overcome the weak electric field near the edges



Beam Test Setup

Telescope:

Reference Arms : 4 ALPIDE planes for track reconstruction
DUT : CE65
TRG : DPTS

Test beam:

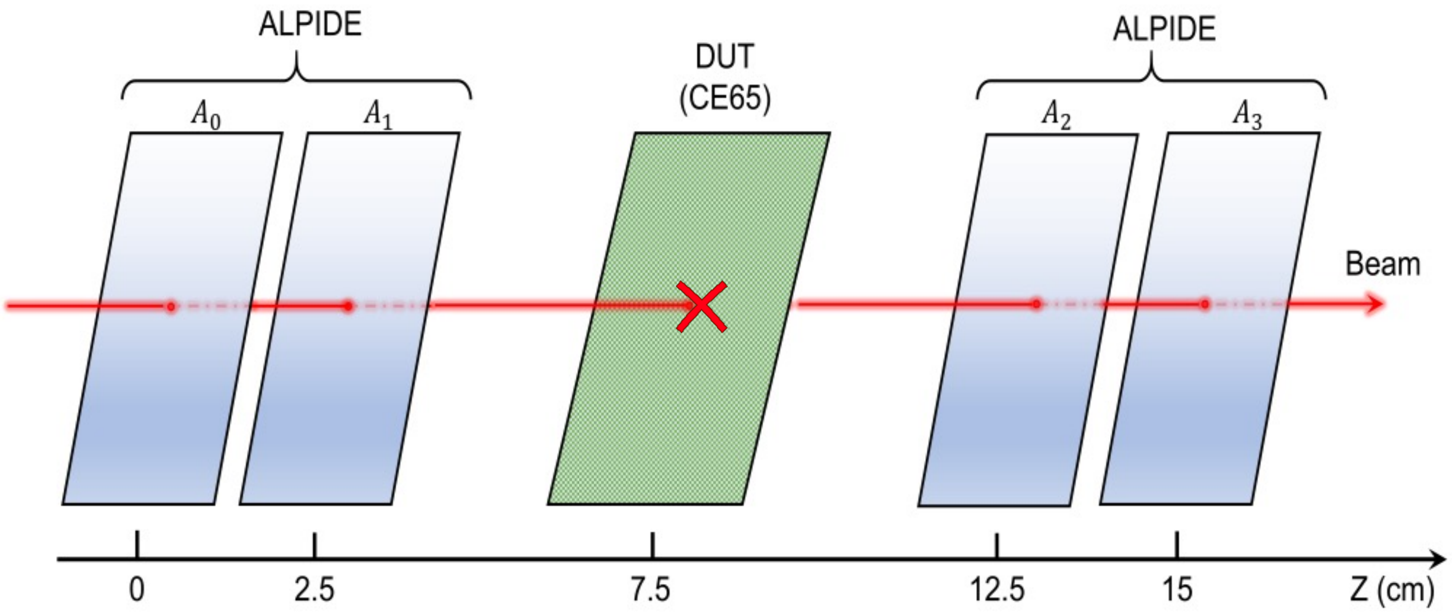
May 2022 at CERN-PS

Support provided by Alice Collaboration

4 frames for each event → **Pedestal map** **Noise map** — **Calibration file**

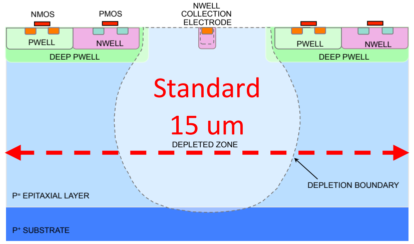
Data acquisition:
EUDAQ2
Event reconstruction algorithm and data analysis framework:
Corryvreckan

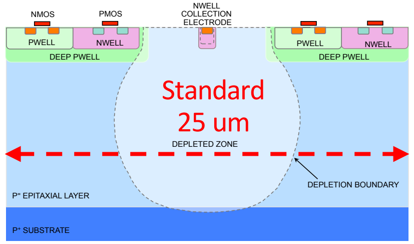
Noise run-**Beam** run:
correlated double sampling method (**CDS**)



Pixel size impact

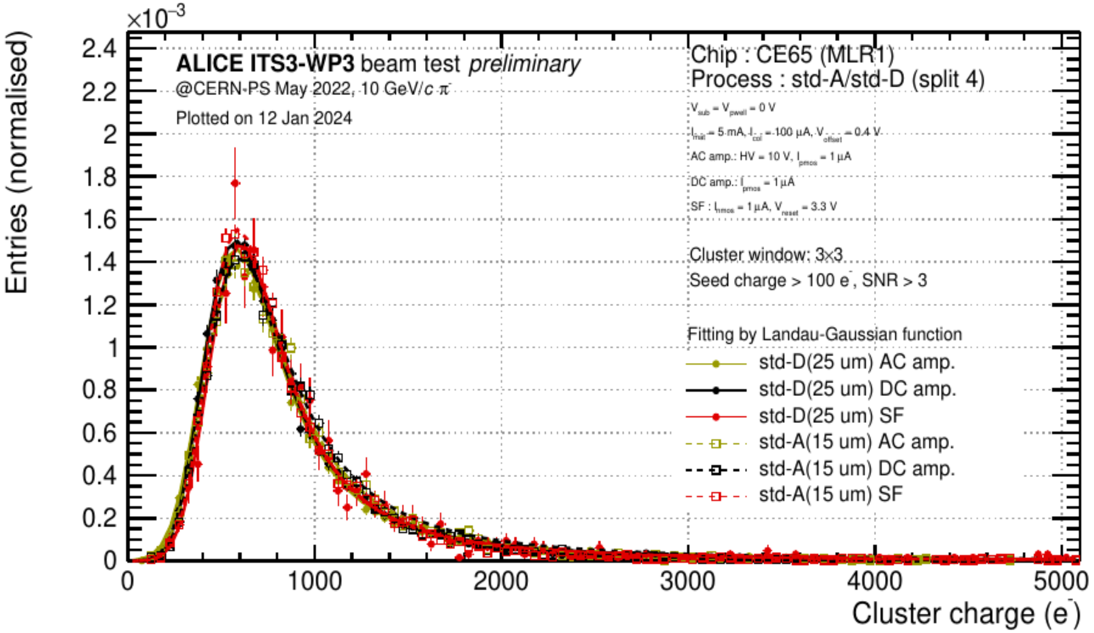
A. Kumar, AIDAinnova 2024

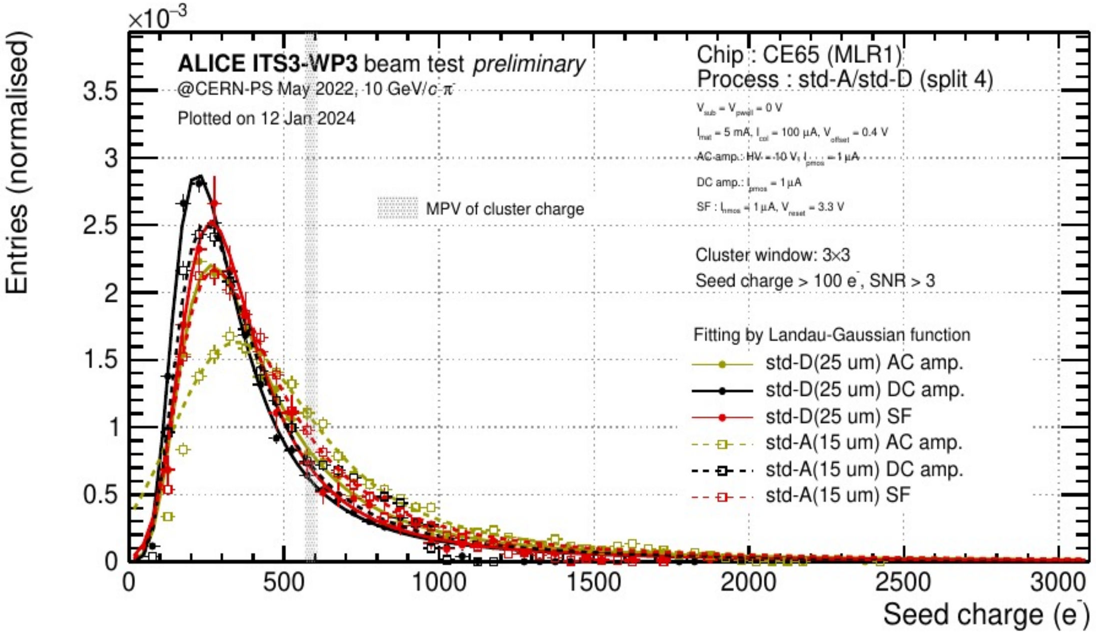




- **Cluster charge: Charge collected over the total 3x3 pixels cluster**
- **Seed Charge: Charge collected in the seed pixel**

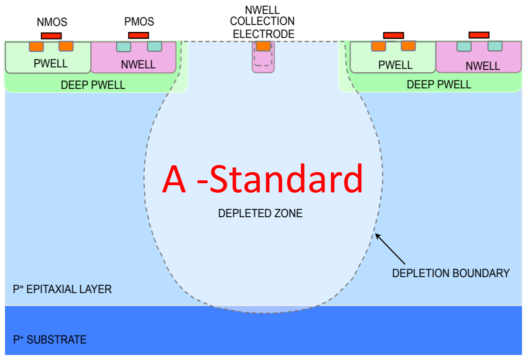
The closest is the peak to the Maximum Probability Value, the less is the charge-sharing

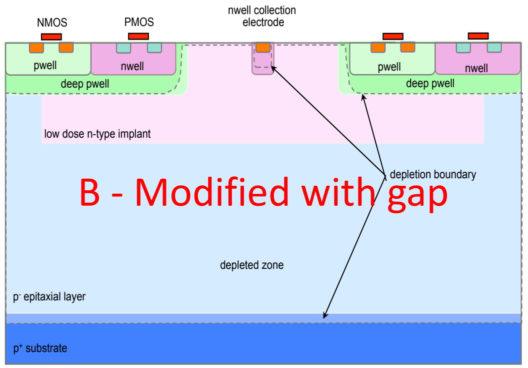


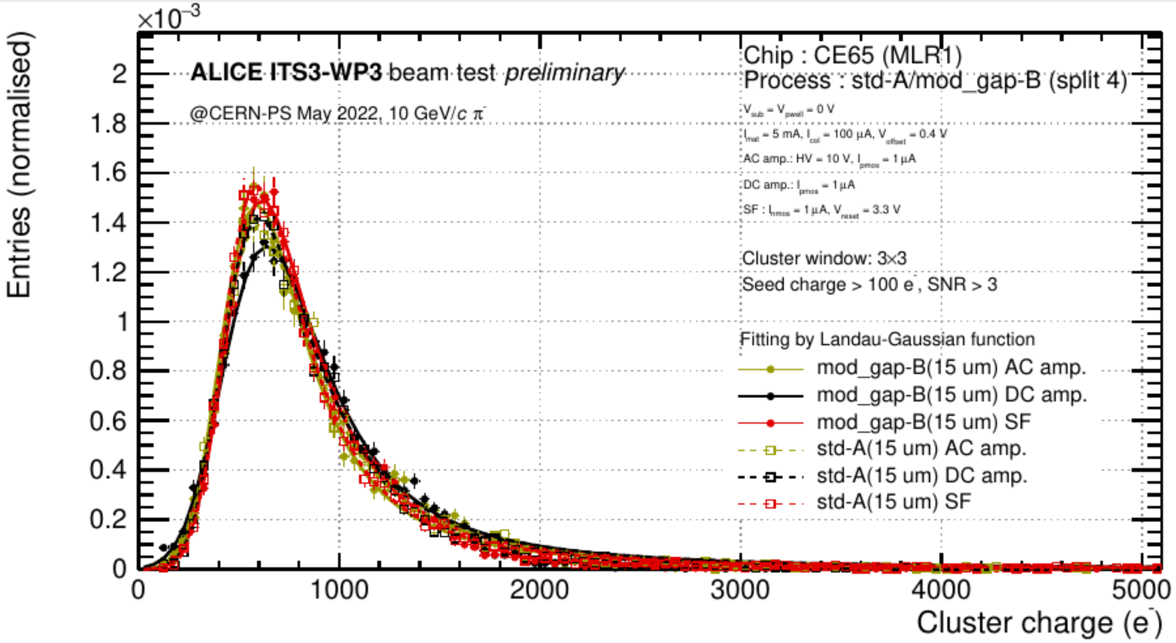


- **Charge sharing is large in pixel (25 um) compared to pixel (15 um)**
- **Diffusion dominates over depletion**

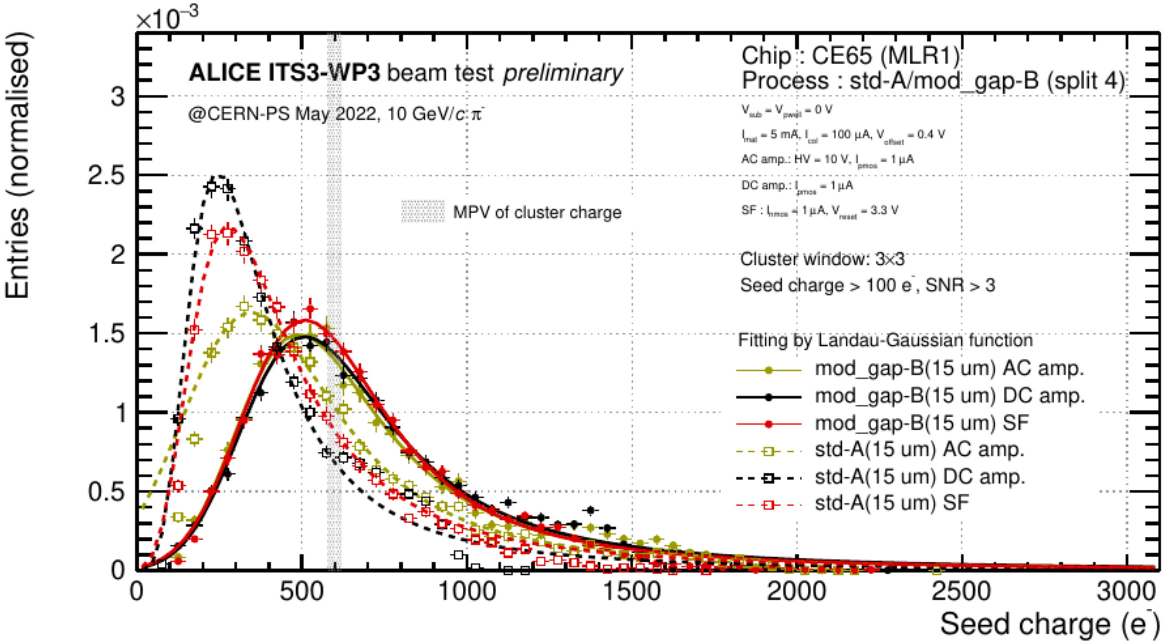
Process modification impact



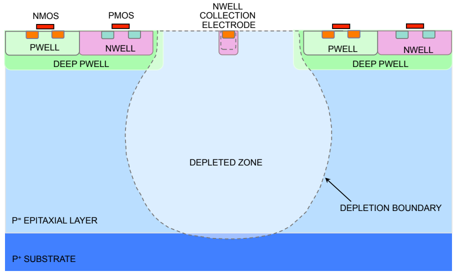


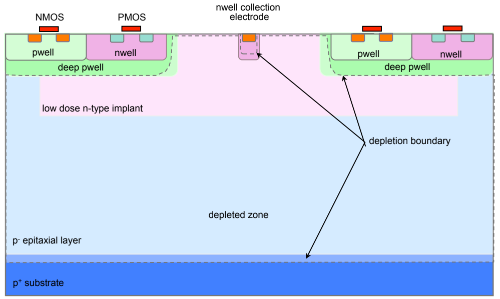


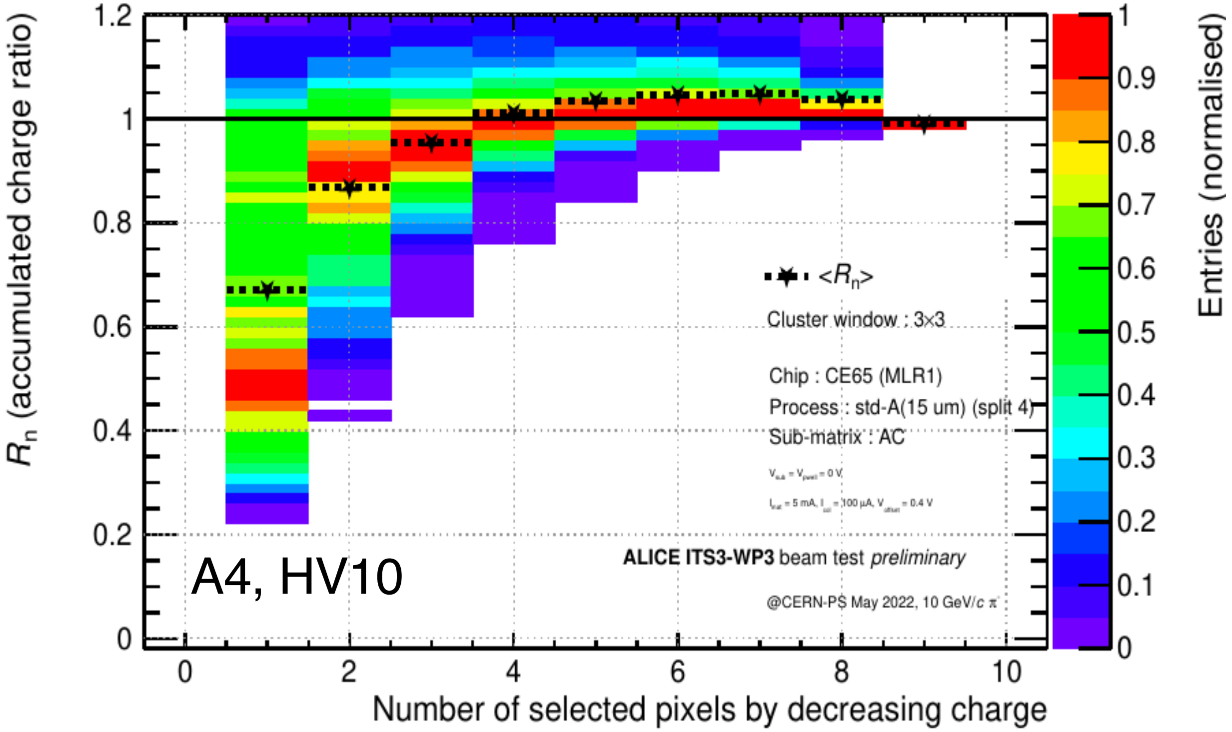
For a pitch of 15 um, the charge sharing is more important in the standard process than the mod-gap process

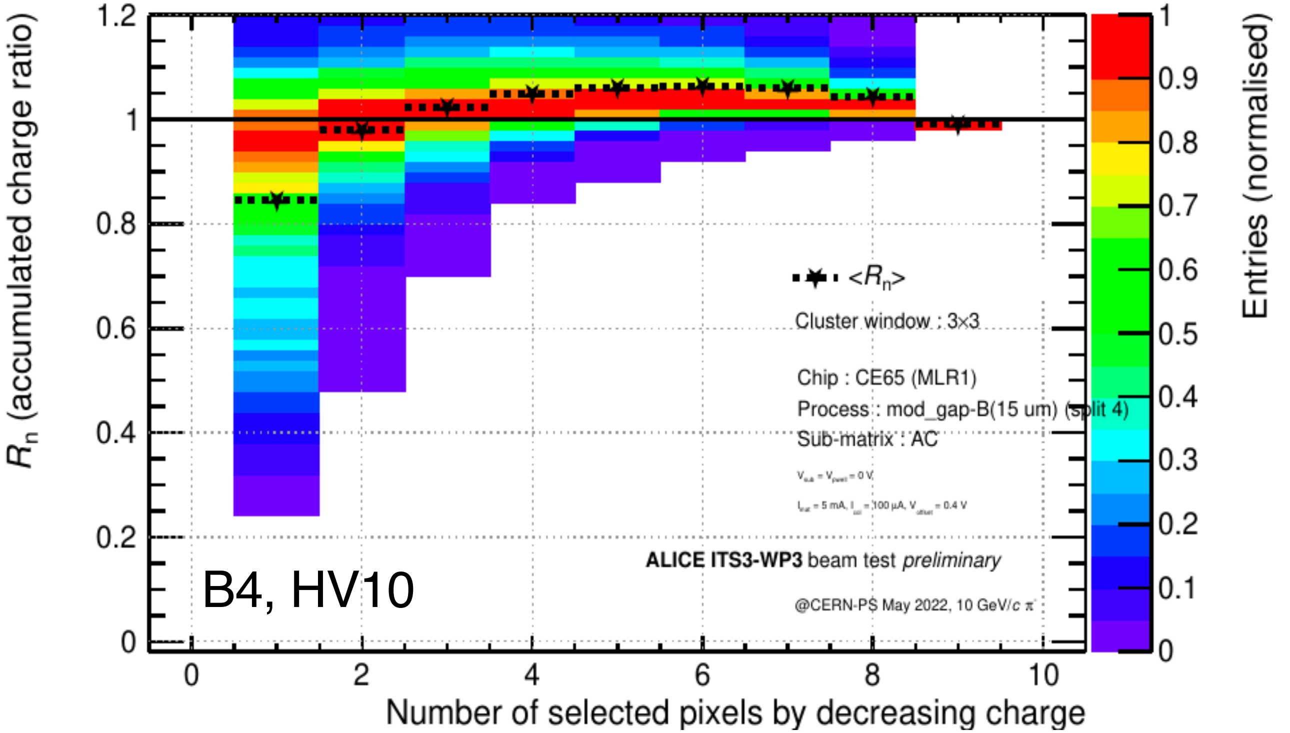


Process modification: charge sharing



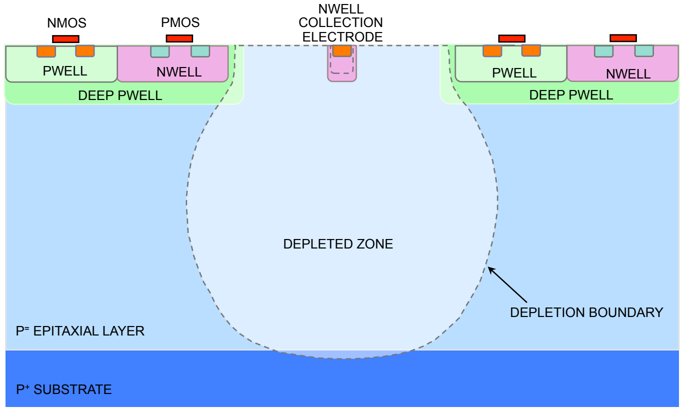


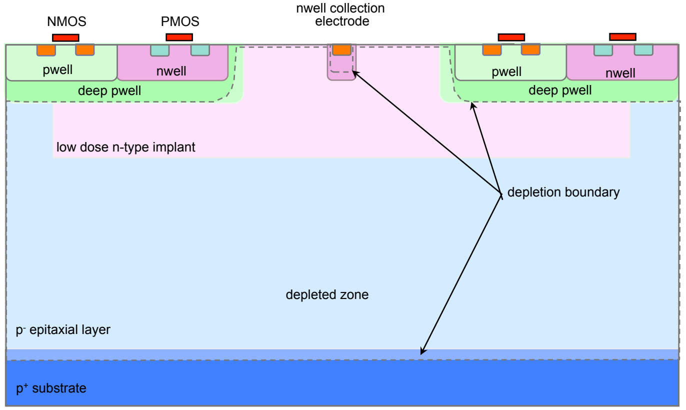


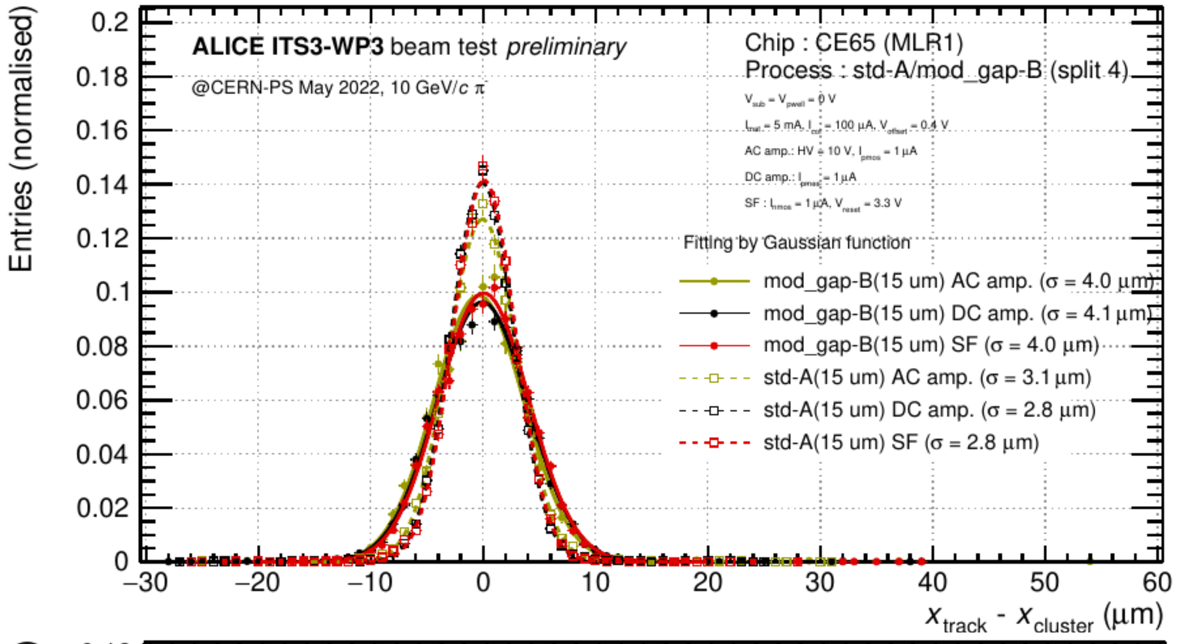


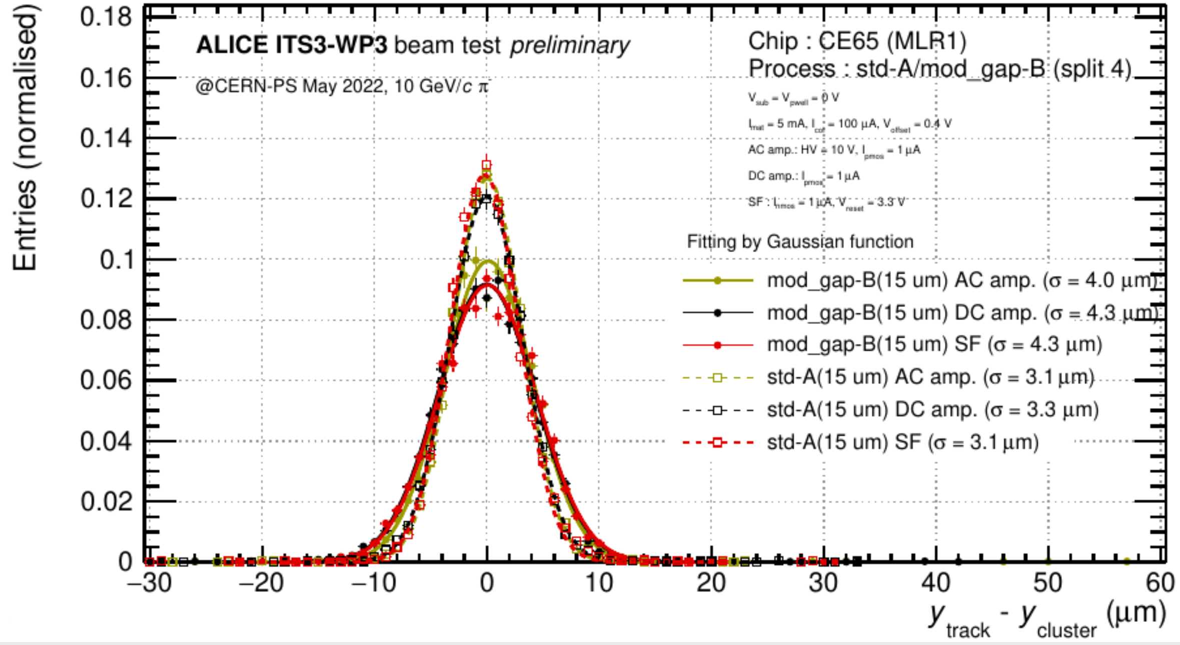
Charge sharing (std) > Charge sharing (mod)

Process modification: spatial resolution





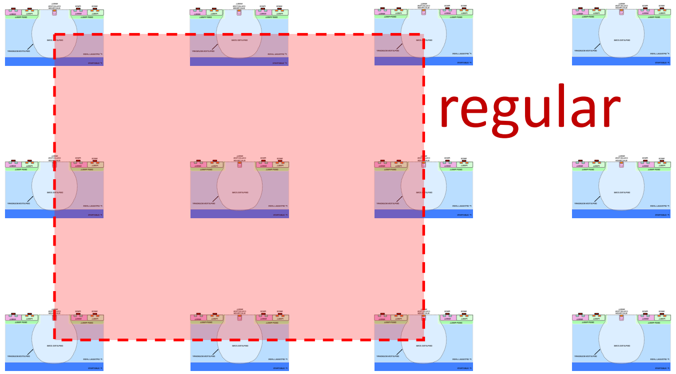


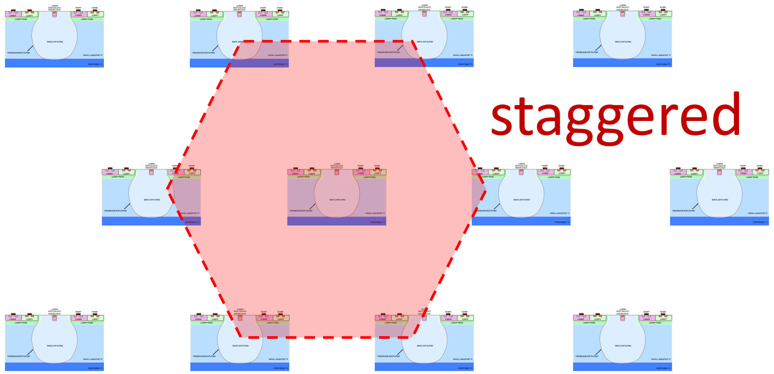


The residual in the standard process is reduced compared to mod-gap process

CE65-v2

- AC-coupled
- Three processes (STD, GAP, BLANKET)
- Three pixel pitch values (15 um, 18 um, 22.5 um)
- Pixel arrangement





Spatial resolution: summary

PCB	Geo	Process	Pitch(um)	HV(V)	Sp. Res.(um) (telescope resolution subtracted)
10	SQ	GAP	22.5	10	~5.1
02	SQ	GAP	18	10	~4.1
19	SQ	GAP	15	10	~3.2
18	SQ	STD	22.5	10	~2.4
23	SQ	STD	18	10	~1.8
06	SQ	STD	15	10	~1.3

Telescope resolution: **~2.1um** (Calculated from https://mmager.web.cern.ch/telescope/tracking.html)

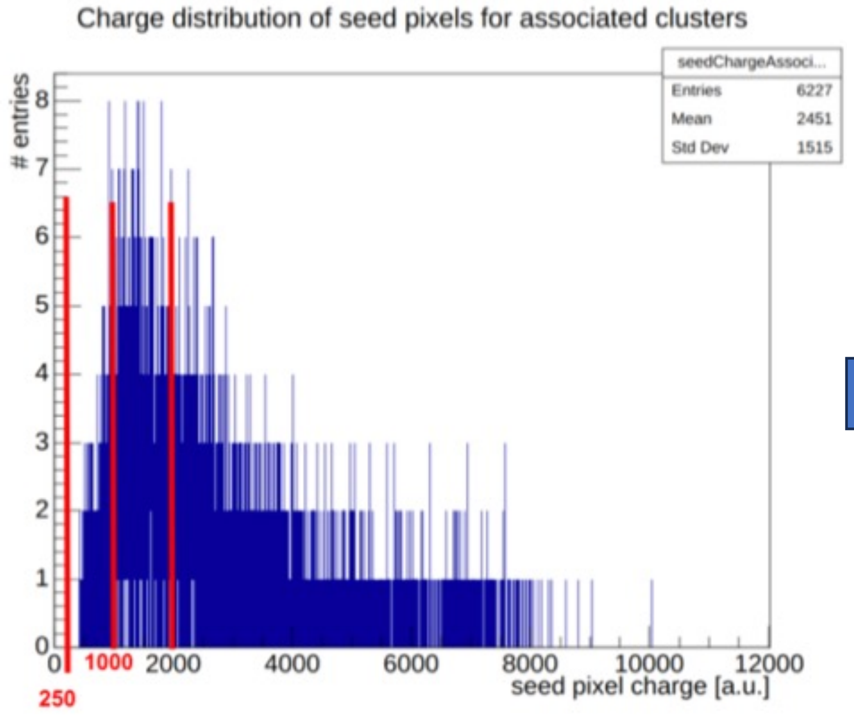
Digitization

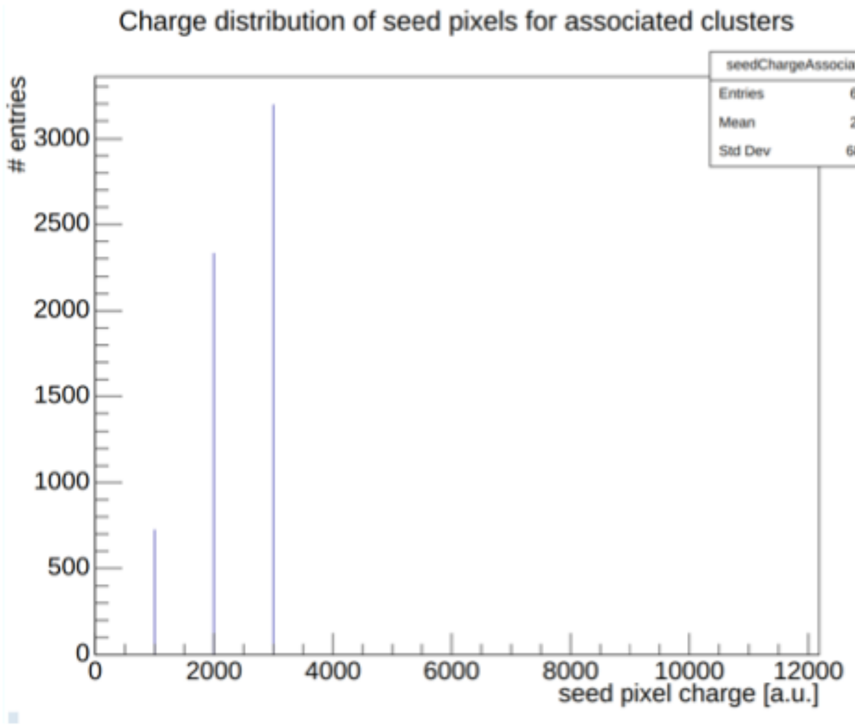
What is required from a sensor?

- Fast Readout → Digital Readout
- Low spatial resolution → Analog Output
- Radiation tolerance…
- etc ….

Is there any trade-off that preserves the spatial resolution without sacrificing the readout speed?
What if we use two bits for digitization, three or maybe four instead of 1 bit?

Digitization* : seed pixel signal – 2 bits examples

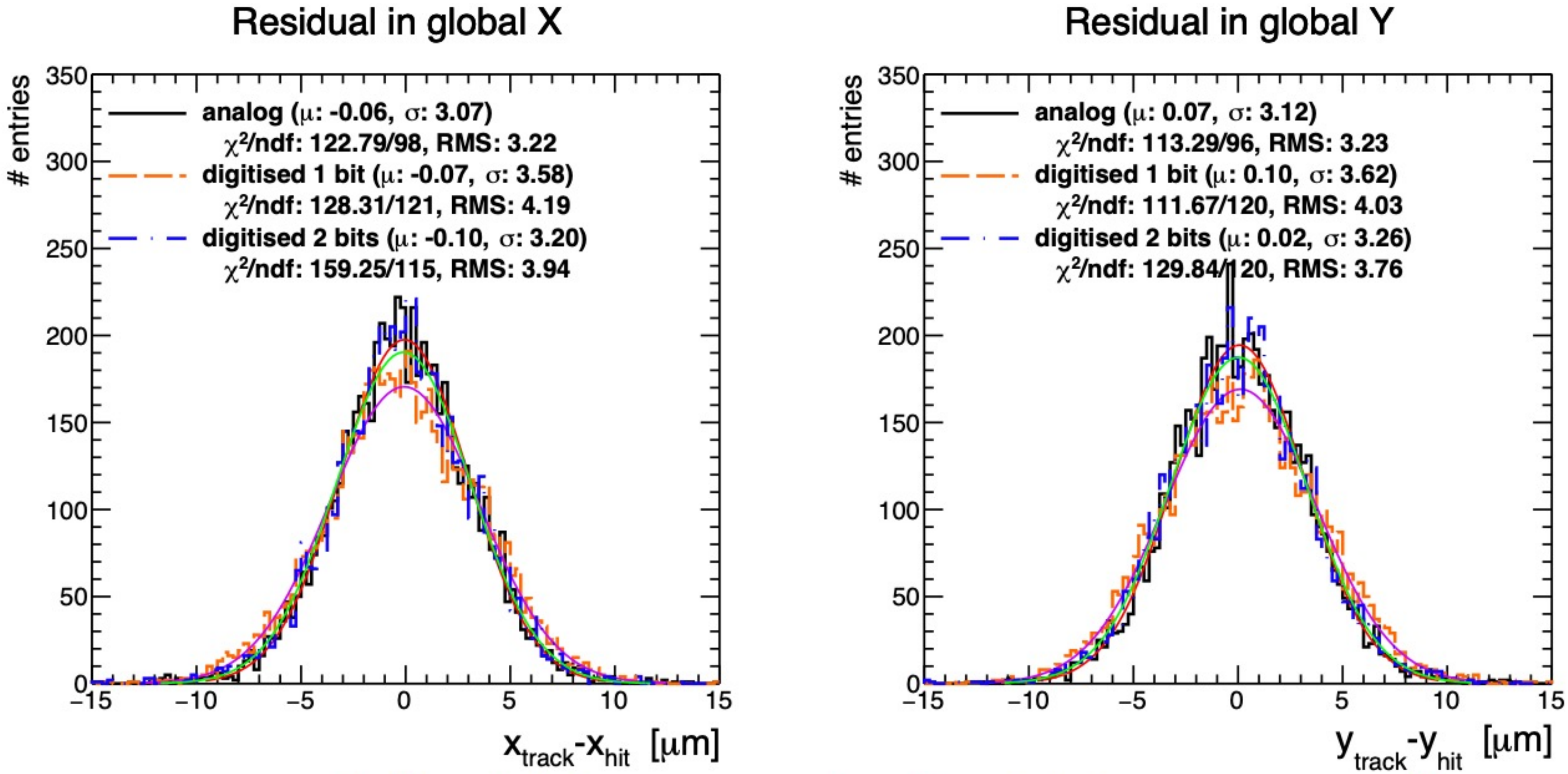




Two important parameters :
- **Threshold value**
- **Bit Size**

*PhD Gaëlle SADOWSKI

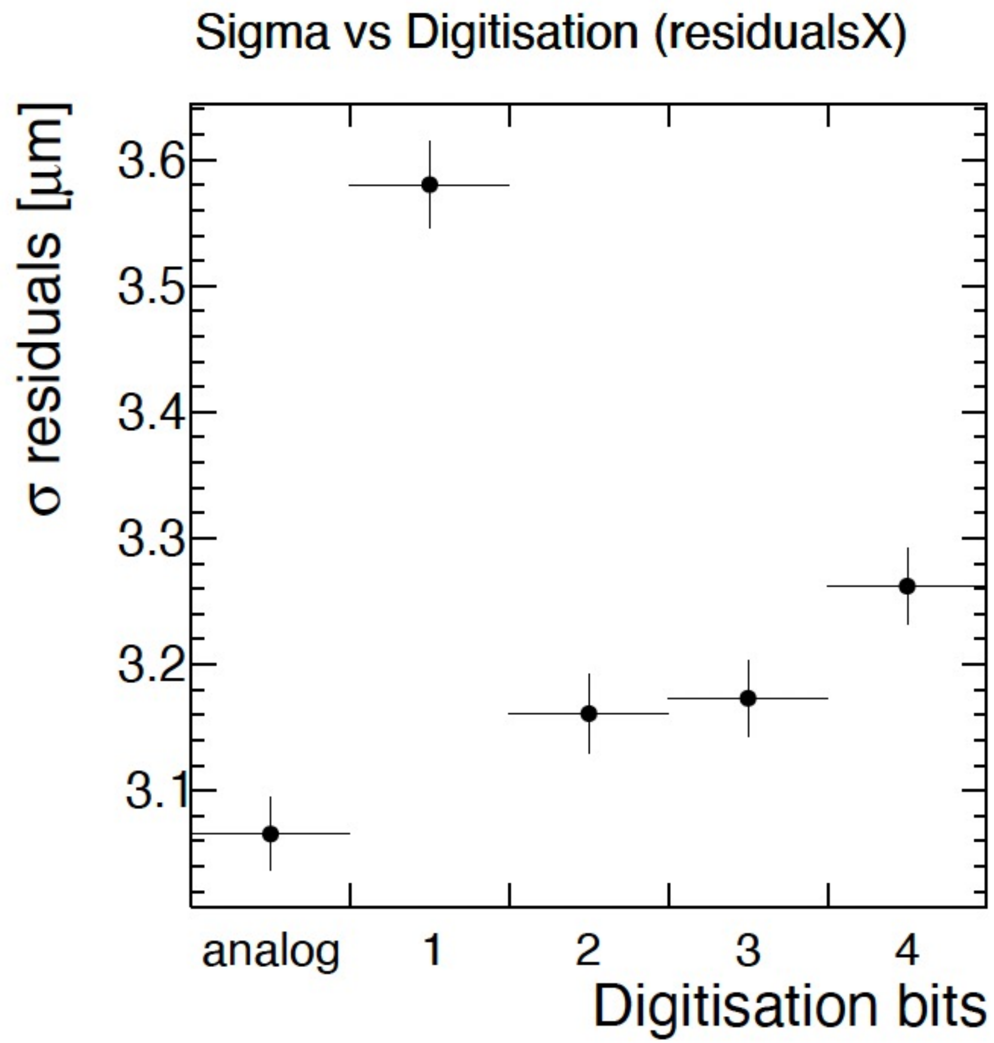
Digitization*: the impact of the number of bits on the position residuals

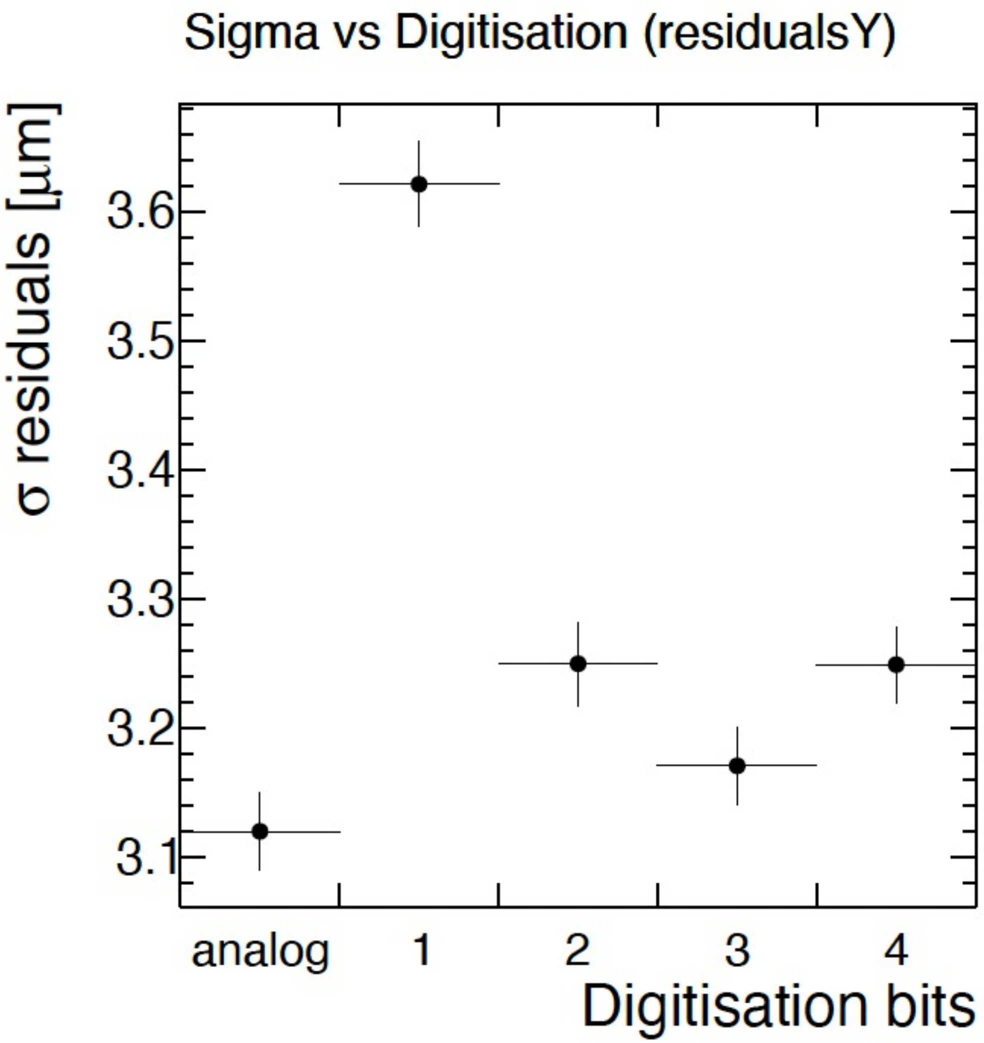


analog → red fit, 1 bit → purple fit, 2 bit → green fit

*PhD Gaëlle SADOWSKI

Digitization*: effect of Nbits





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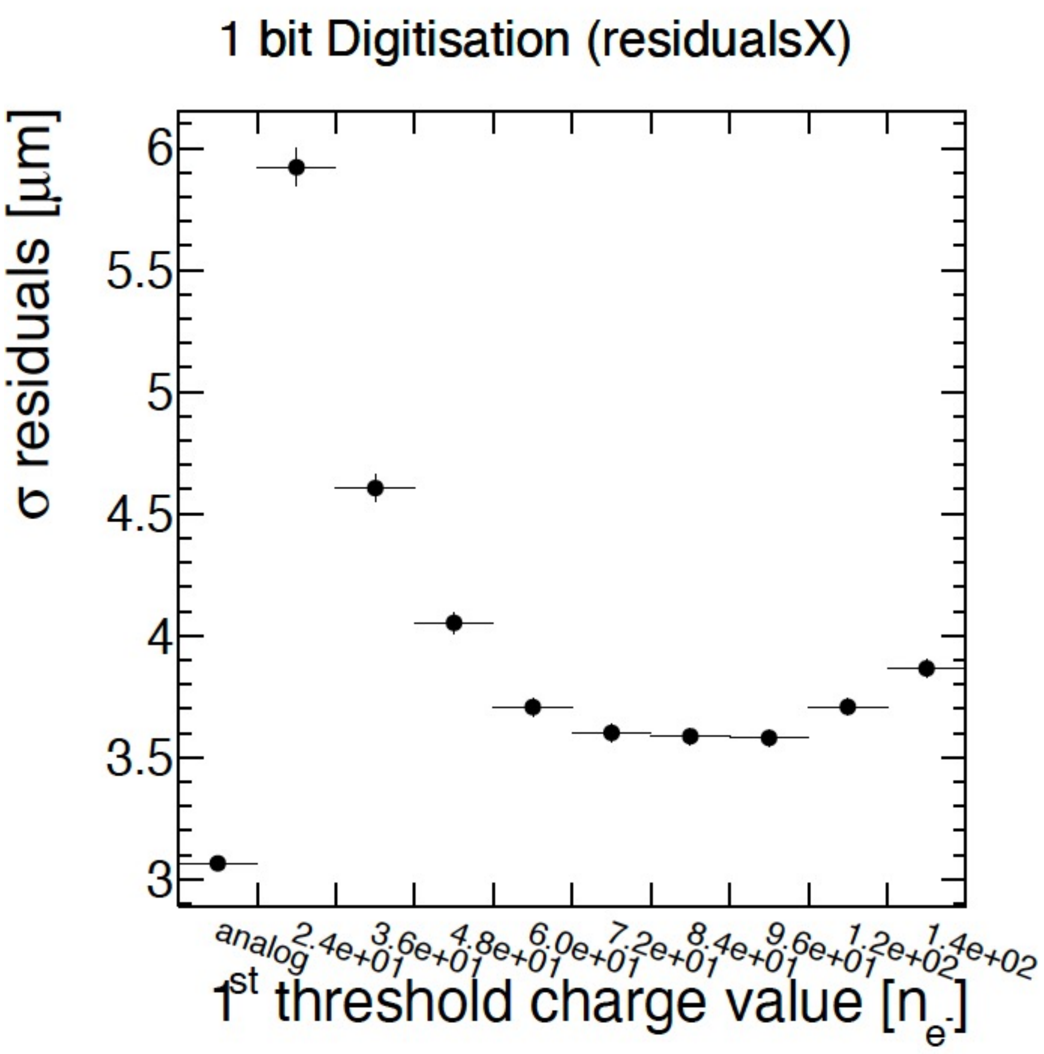
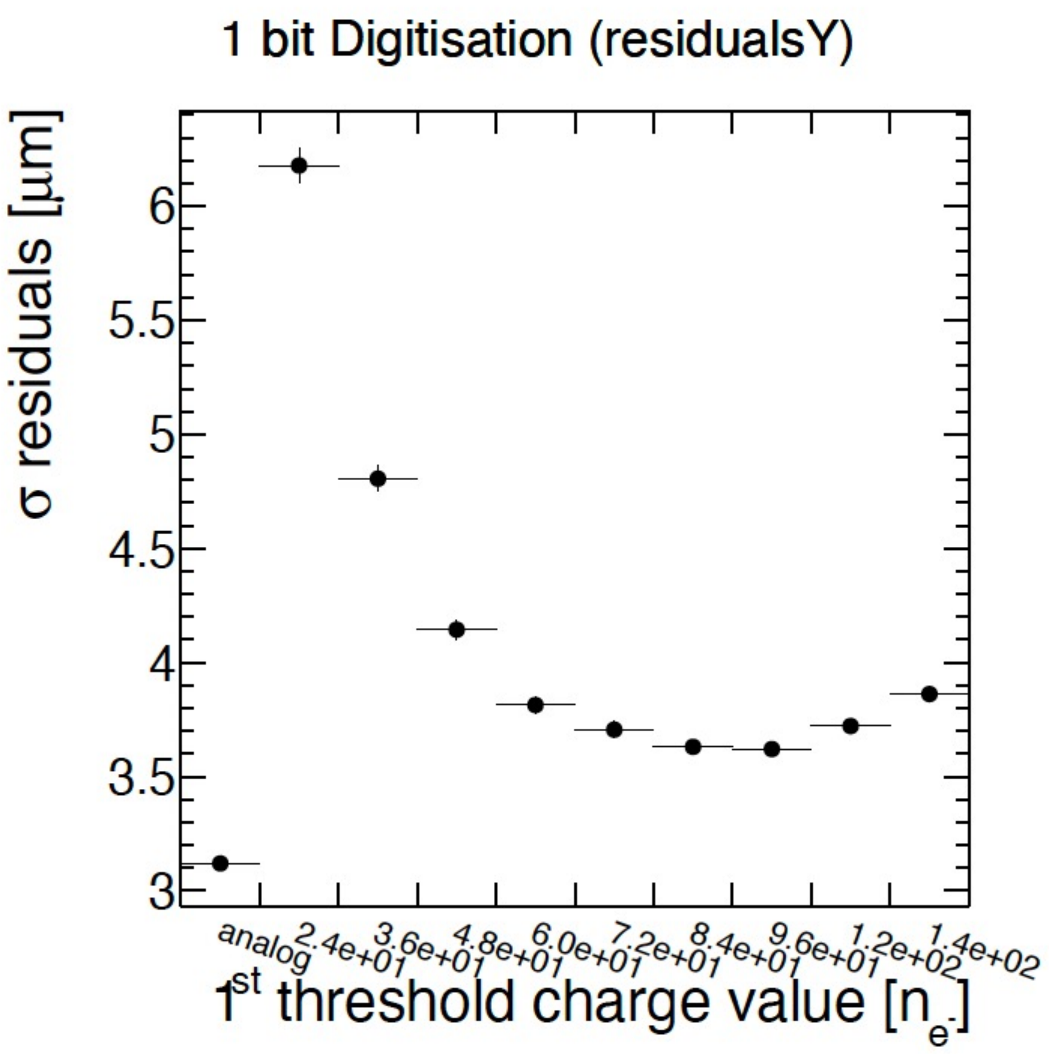
- **Restauration of analog sigma value of analog readout with 2 bits**
- **Should improve and get closer to analog value for high number of digitization bits**
- **We need to investigate the impact of the threshold value and the choice of the bin size**

Digitization: Effect of threshold value on the position residuals





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Summary

- 65 nm Technology is being scrutinized
  - ✓ Impact of pixel pitch
  - ✓ Impact of the process (std, gap, …)
  - ✓ Impact of pixel geometry

- Digitization is in progress

Thanks for your attention