Exploring ALICE ITS3 MOST: Early Results on Power Segmentation and Asynchronous Readout for Timing in a Monolithic Stitched Sensor

Mariia Selina (Nikhef) on behalf of the ALICE collaboration - PIXEL2024 - 21.11.24

ITS3 Detector Upgrade

New detector motivation

ITS detector upgrade planned in LS3 (2026-2029) for High Luminosity LHC to improve vertex precision and physics yield:

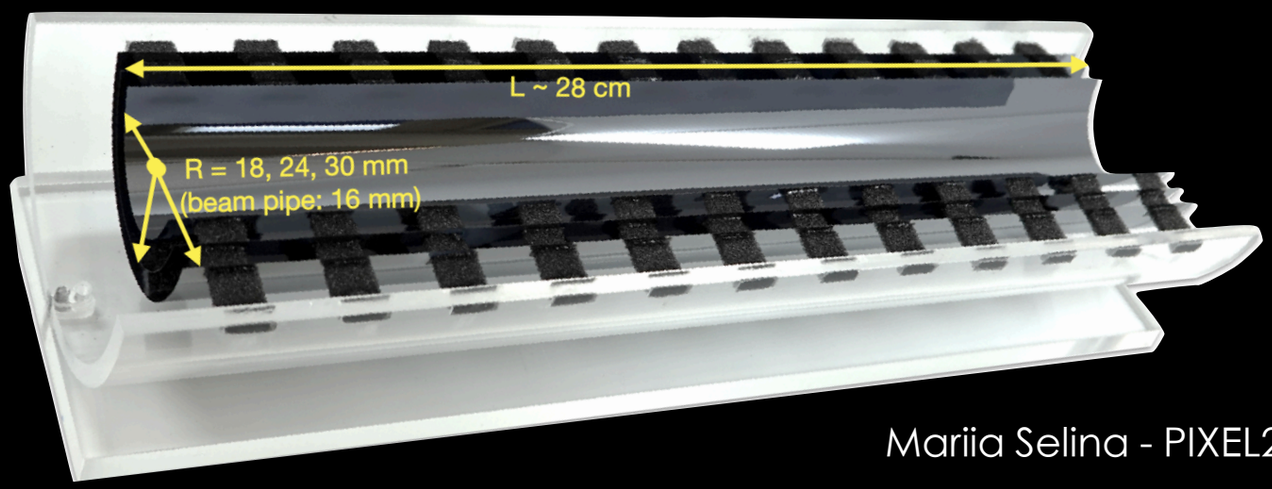
- **Detector closer to the interaction point**
- **Lower material budget to reduce particles interaction with detector material:**
  - **Remove water cooling**
  - **Remove the circuit board – Integrate data, control and power distribution on chip**
  - **Minimise mechanical support**

ITS3: wafer-scale silicon sensors bended in cylindrical layers

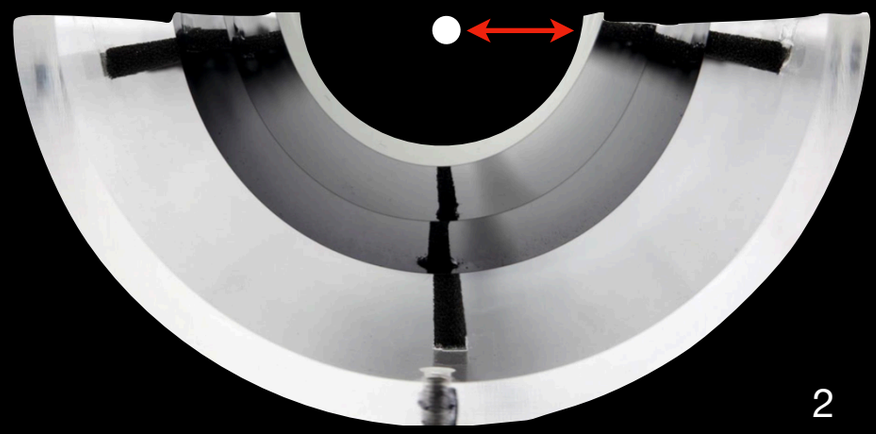
More in F. Reidt talk: ALICE Inner Tracking System 3 Overview

Material Budget:

- ITS2 $\approx 0.36\,\% X_0$-> ITS3 $\approx 0.09\,\% X_0$



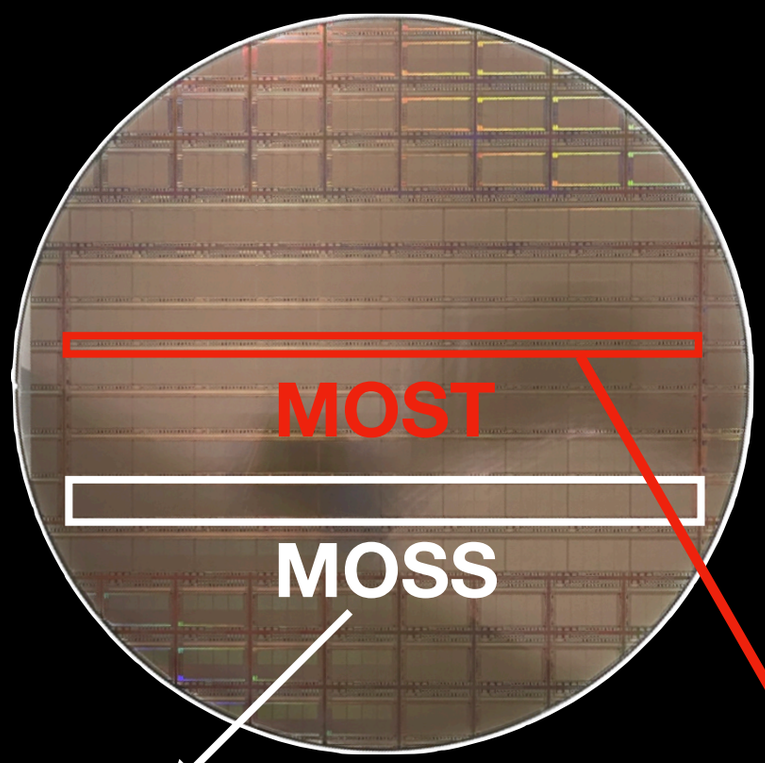
23 mm (ITS2) -> 19 mm (ITS3) from interaction point



ER1 Submission

Learning Stitching Technology

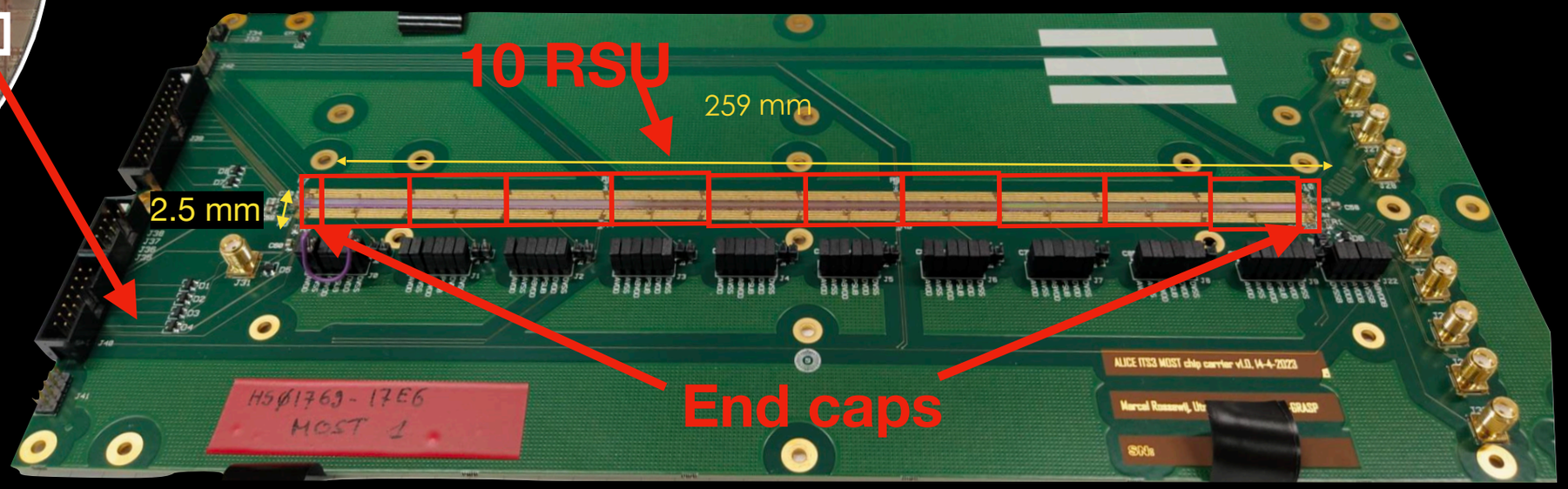
Engineering Run 1 (ER1) is the first submission of stitched chips: MOSS, MOST.



See previous talk about MOSS by Livia Terlizzi

Main differences from MOSS?:

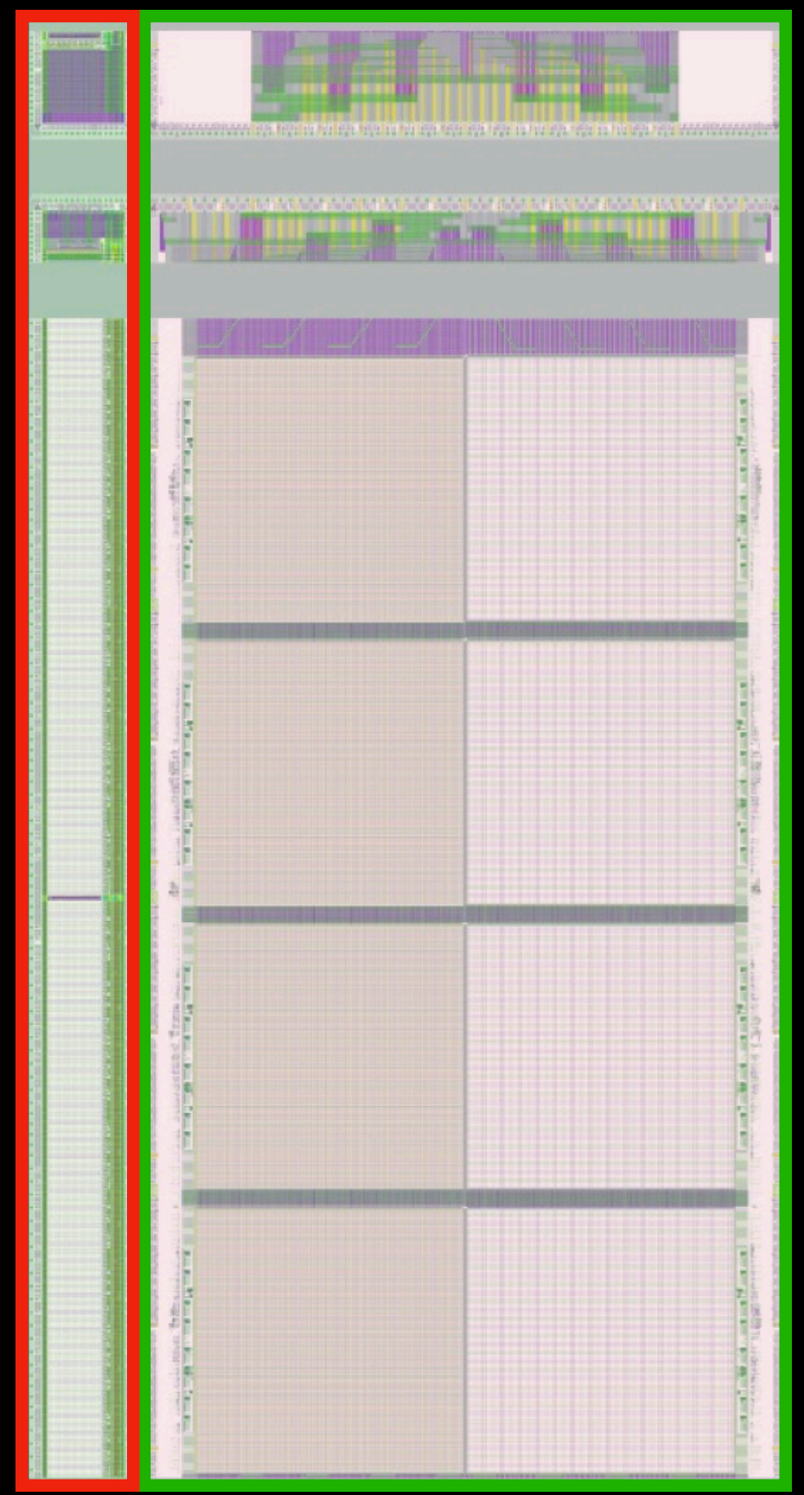
- Granular power switches, Dense matrix circuits -
  - Does this type of powering work?
  - Whats the impact on the yield?
- Asynchronous - data driven readout -
  - Can we have stitched sensor with precision timing?
- Different approach for reverse bias
  - Evaluate alternative biasing by lifting front end circuitry?



MOST Overall goal: verify different options for the stitched sensors/architectures.

Granular Power Switches

MOST special feature



Distinction from MOSS:

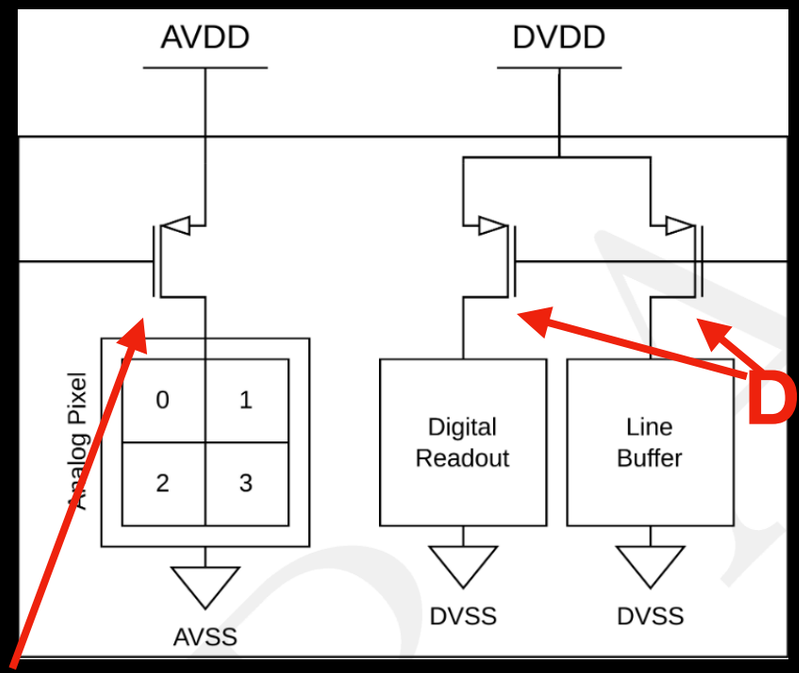
- **More densely populated matrix - what are density limits for a stitched sensor?**
  - **Minimum spacing design**
  - **Nearly continuous matrix formed over the entire chip**

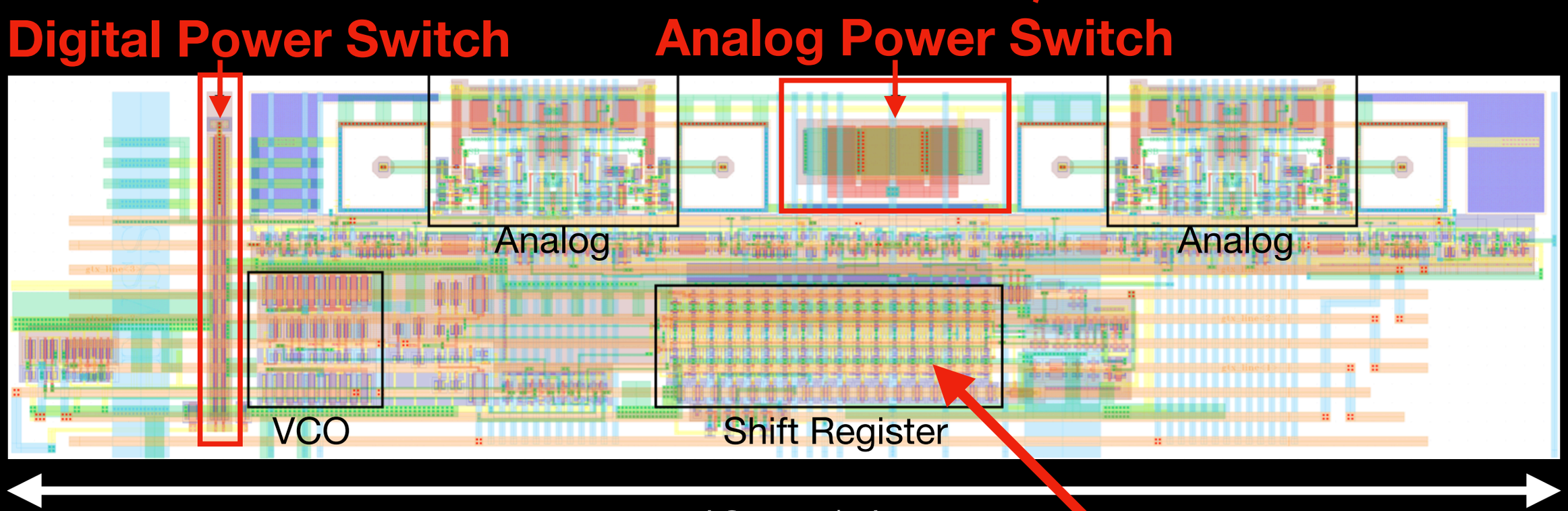
- **Fine power modularity - adopted for ITS3 but with less granularity**
  - **The denser the chip, the higher the chance of faulty areas**
  - **Powering off the faulty areas to preserve yield**

Granular Power Switches

- 1x digital switch per 352px → 2560 in total
- 1x analog switch per 256px → 3520 in total

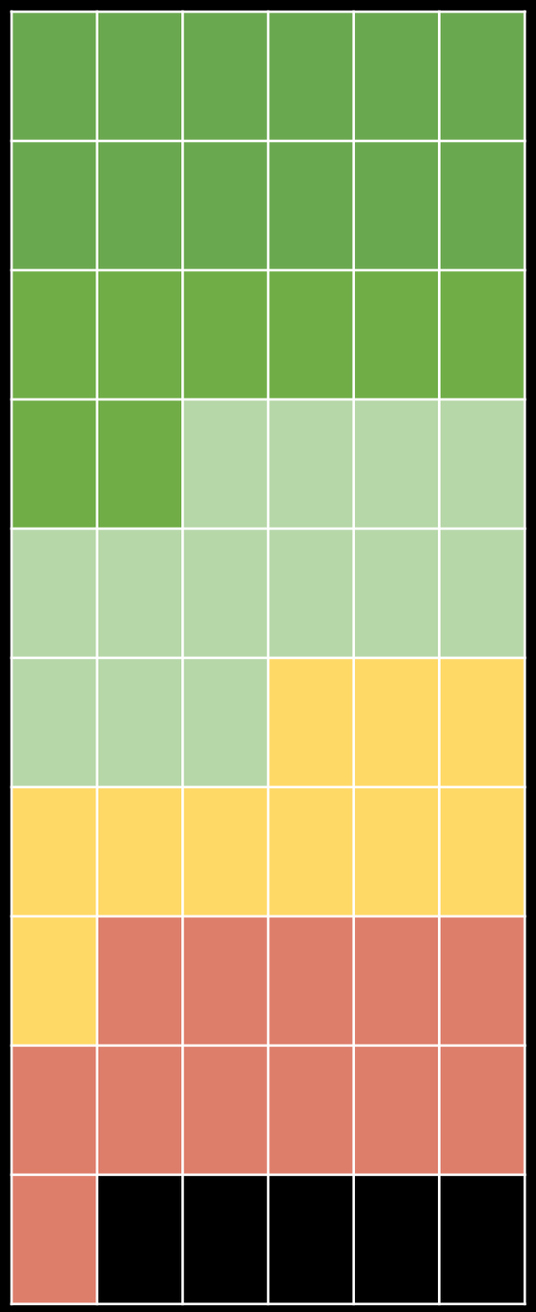
Goal: Verification of the yield for a sensor with a dense circuit design and segmented powering.





First check on yield

Power on procedure



Total of 55 chips tested:

20 (36%): **OK-I**: no trip (<25 mA)

13 (24%): **OK-II**: no trip but increased currents (<50 mA)

10 (18%): **OK-III**: increased current limit needed (<80 mA)

12 (22%): **NOK** (short, trip) -> compatible with MOSS observations

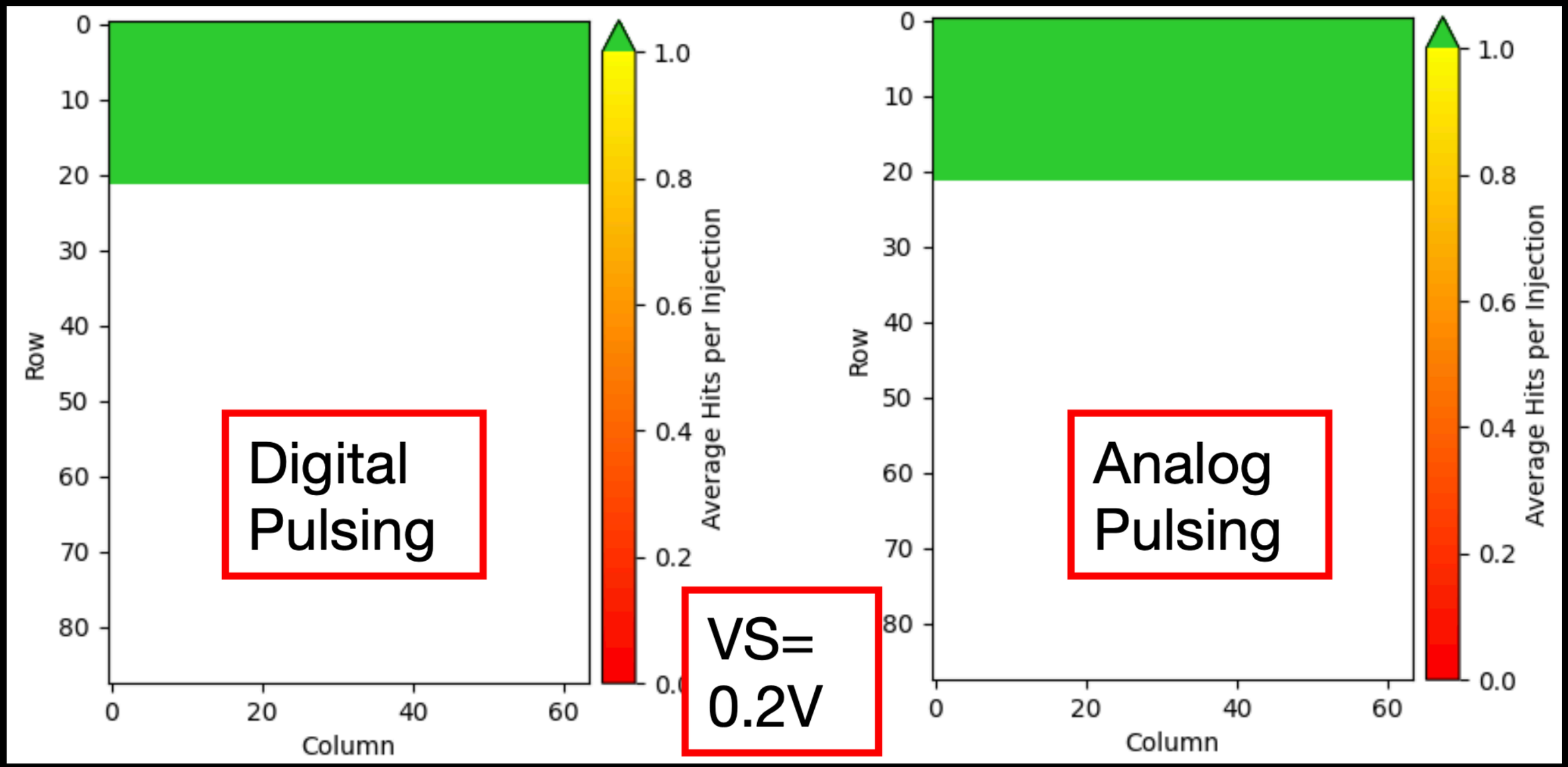
Overall yield: 78% of the chips can be powered and show functionality

In general if the chip can be powered on - it is functional

Pulsing tests (example)

What fraction of pixels is functional?

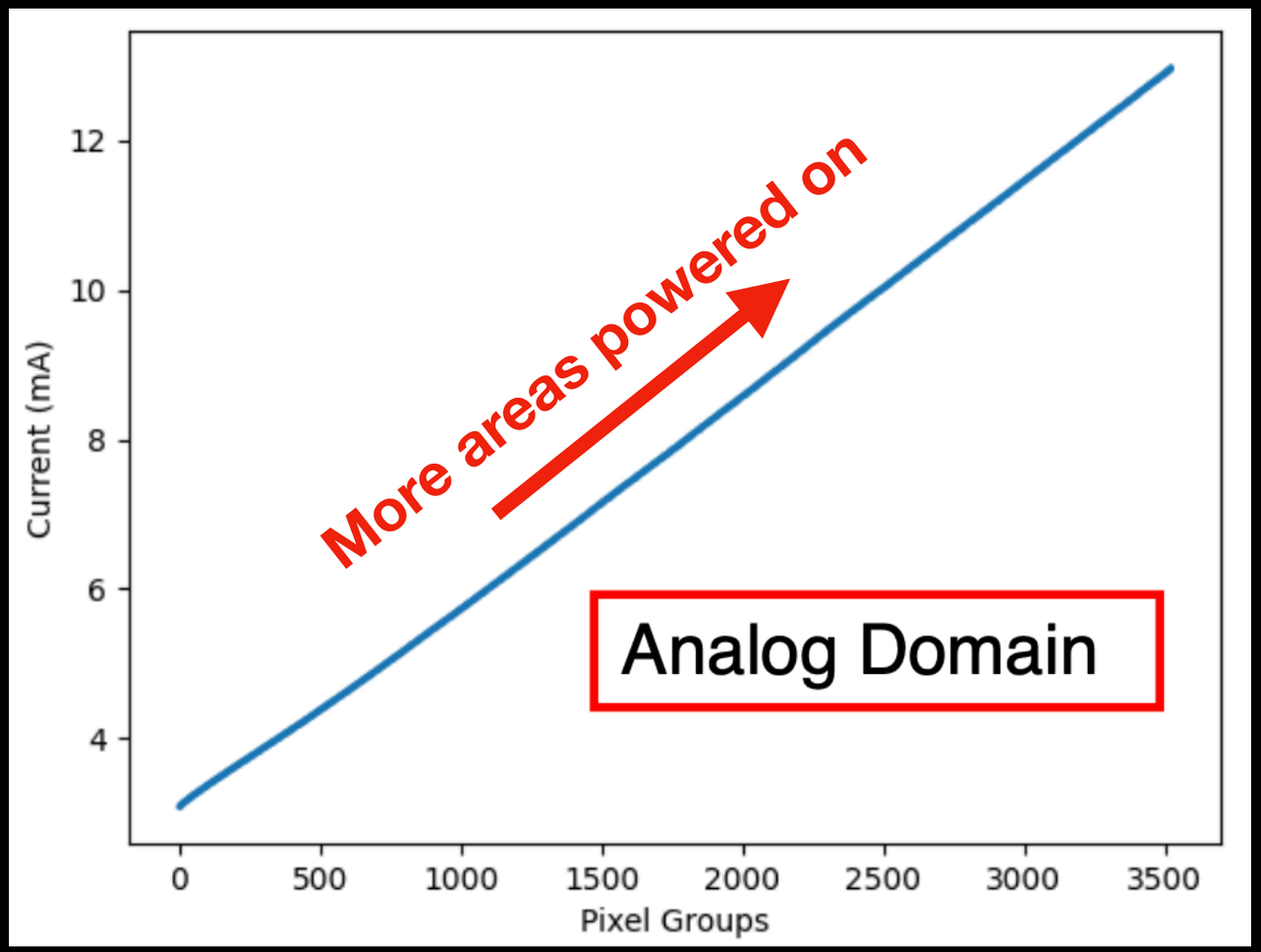
All pixels respond, but more statistics needed to evaluate the yield for the high density layout.

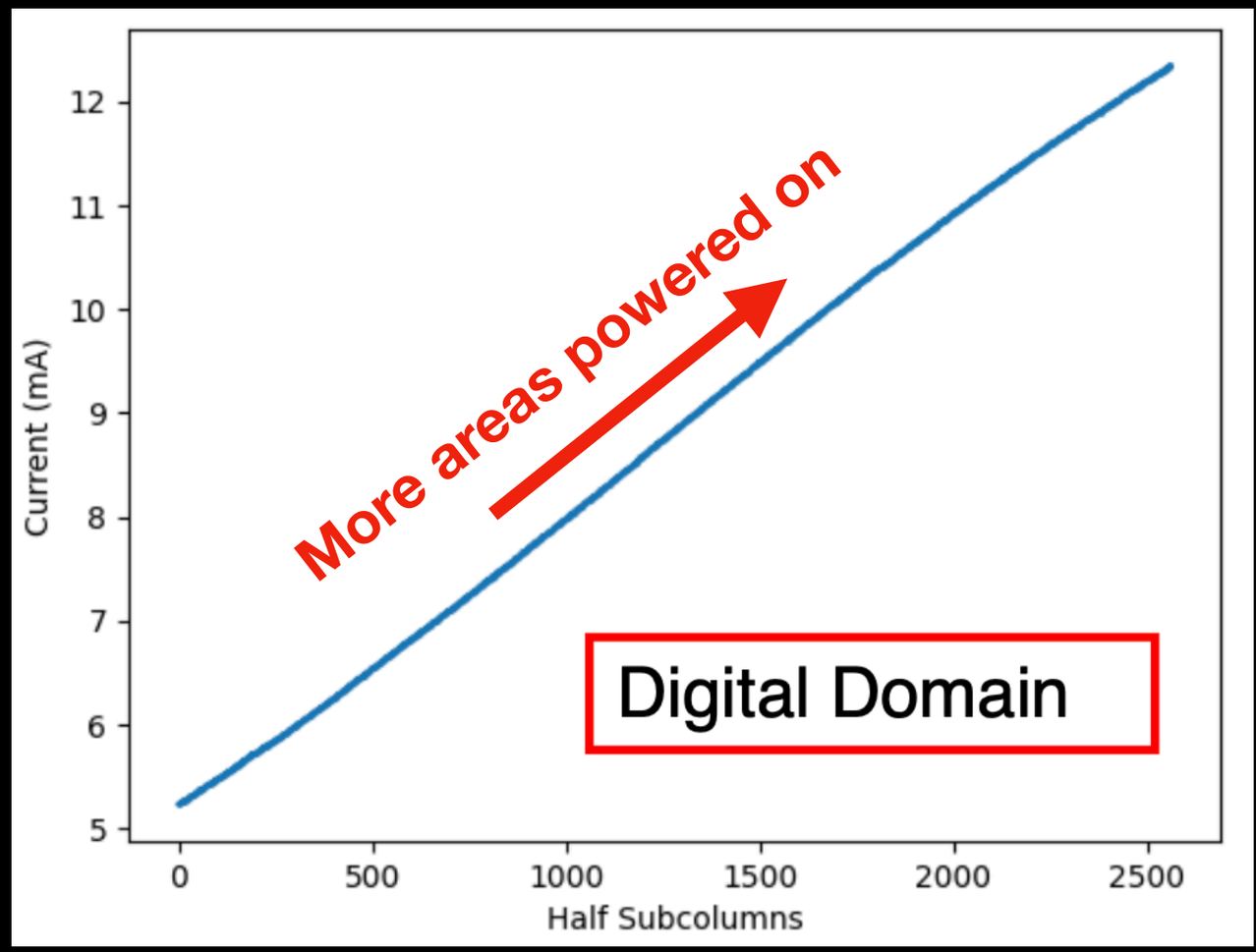


Granular Power Switches

Sequential power release

Linear power consumption increase with more areas turned on with the power switches - expected behaviour.

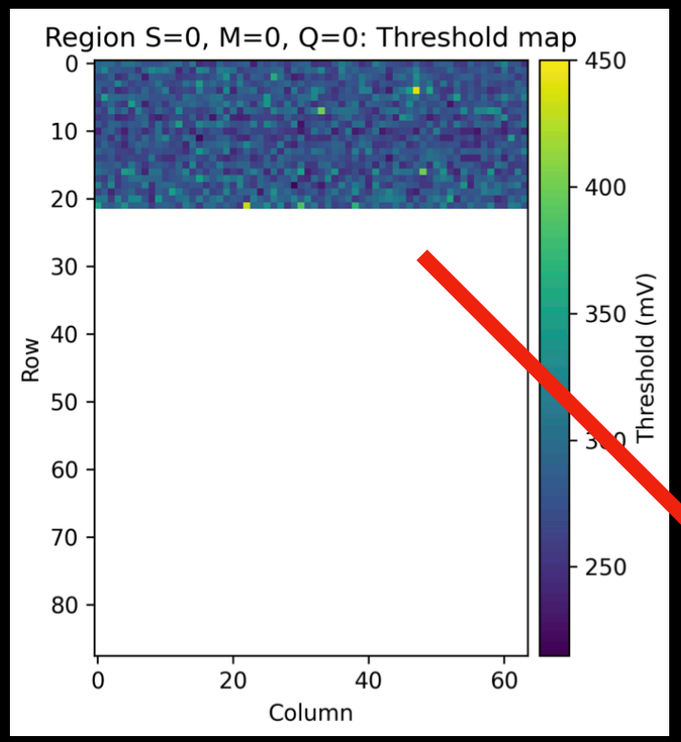


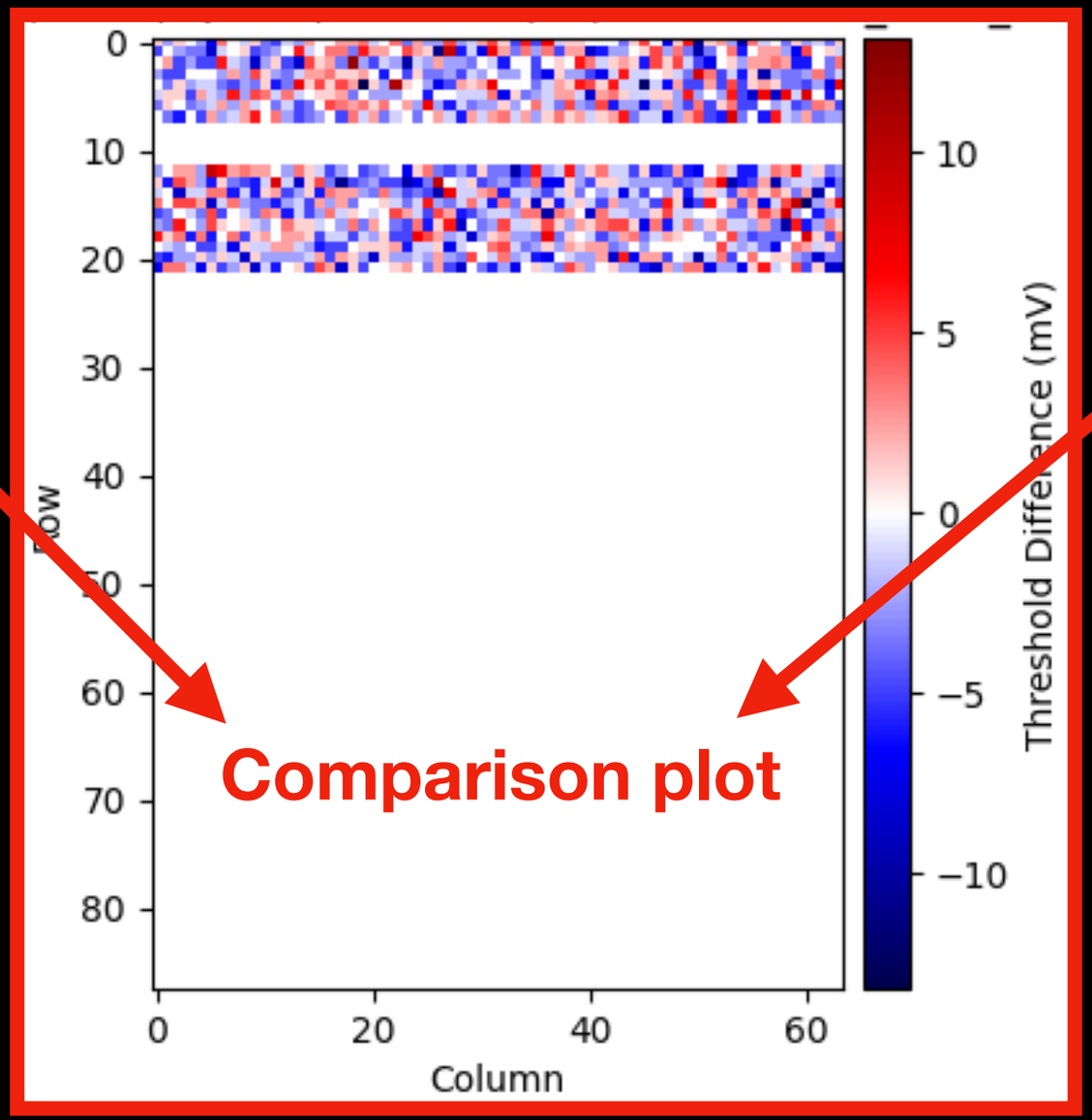


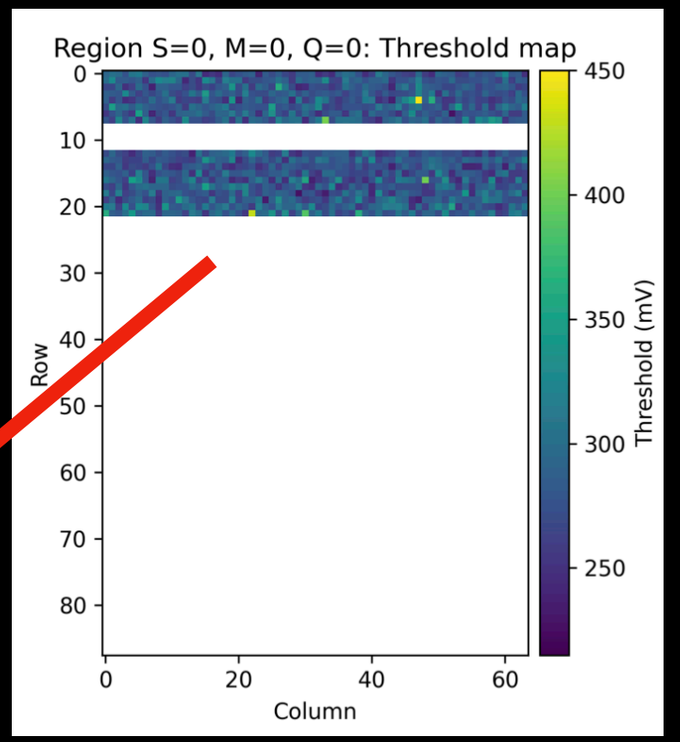
Granular Power Switches

Does switching off regions influence neighbouring regions?

- Threshold remains unchanged when neighbouring region is off
- No effect on threshold



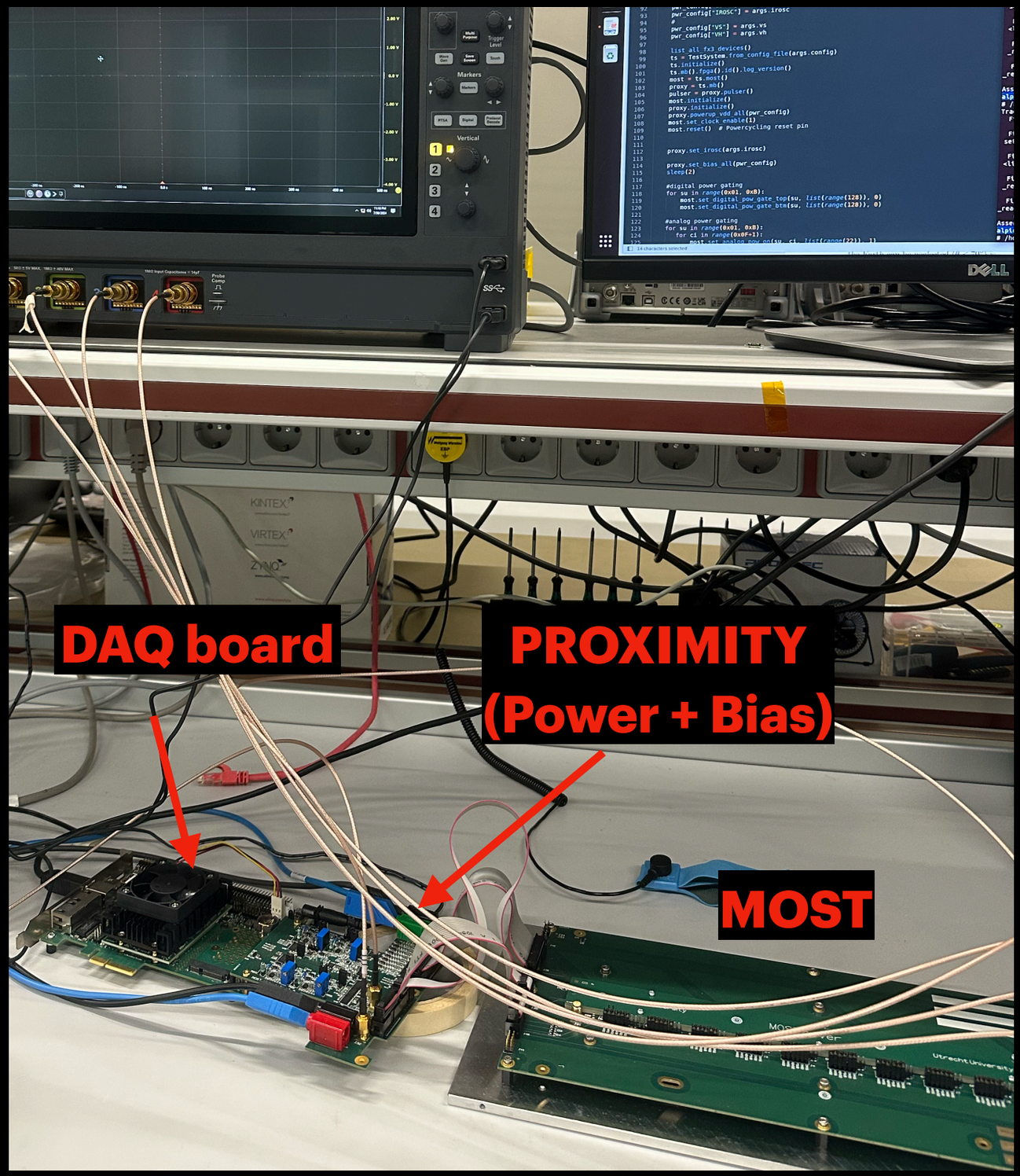




Test System

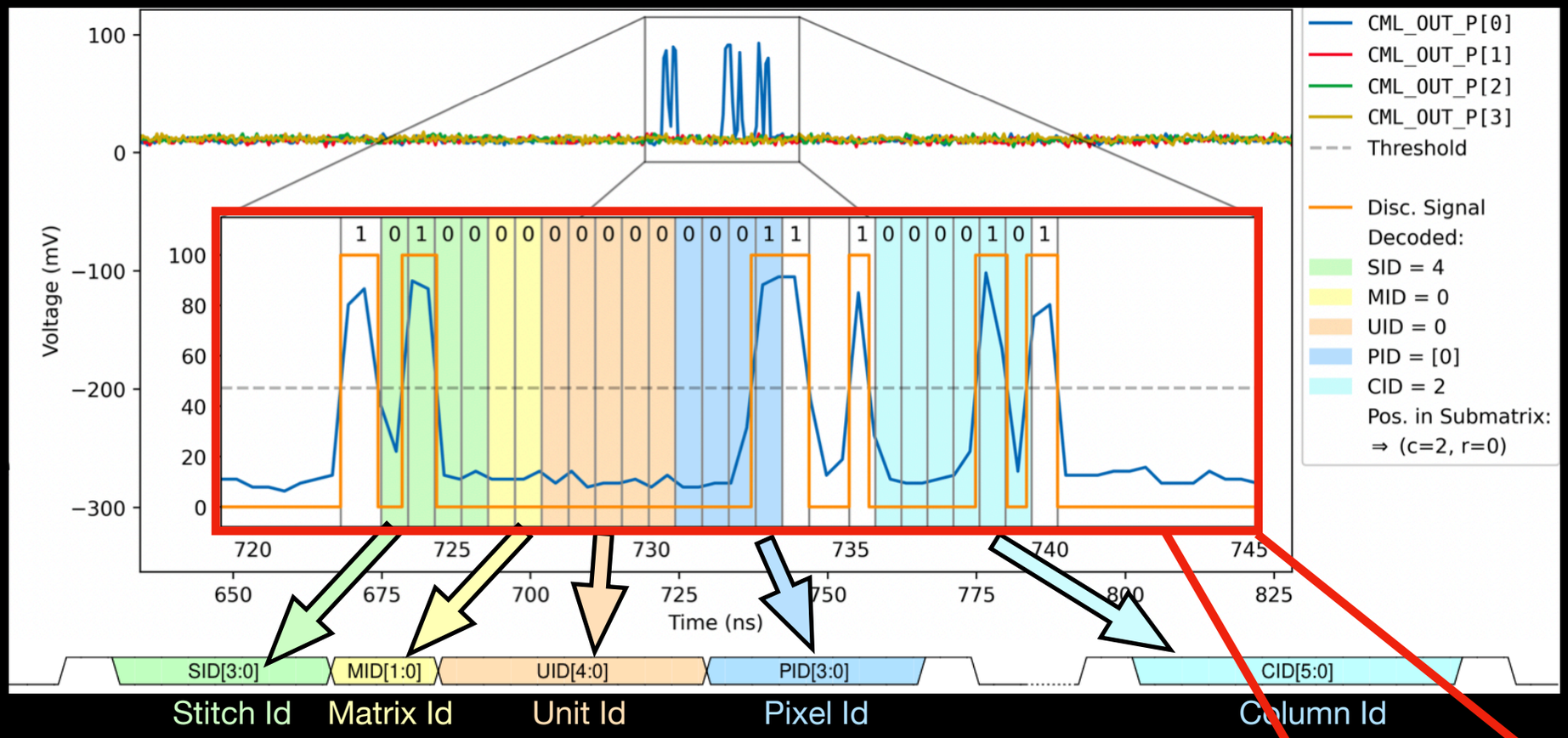
Setup

- FPGA-based DAQ board:
  - For proxy board control
- Custom proximity board for:
  - Power
  - Bias
  - Slow Control
- Readout via oscilloscope:
  - 4 channels with 6GHz, 16GS/s

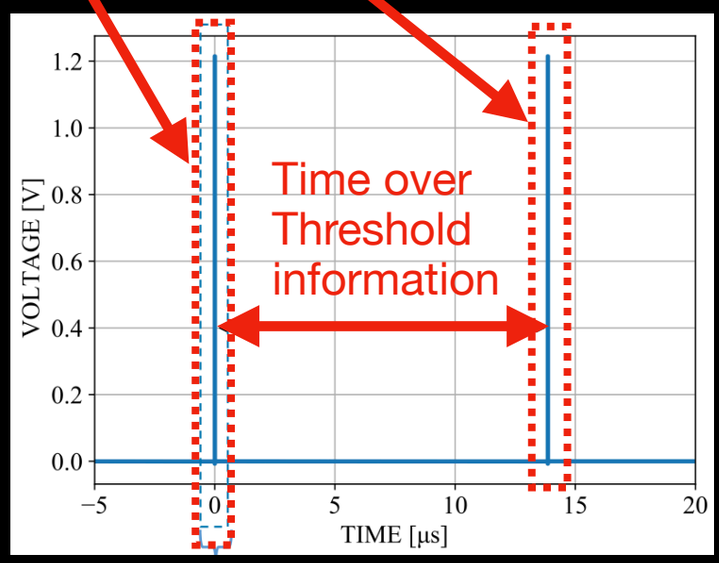


Asynchronous readout

Hit pixel location decoding from a bit sequence



1. Circuit in the pixel matrix generates a bit sequence of pixel position (groups of 4 pixels) and transmits it along the column through the whole chip
2. Bottom endcap circuit adding the column ID if activated
3. All hits go through an OR tree (logic) into 4 CML drivers



See backup slide 20 for more details

First time studies

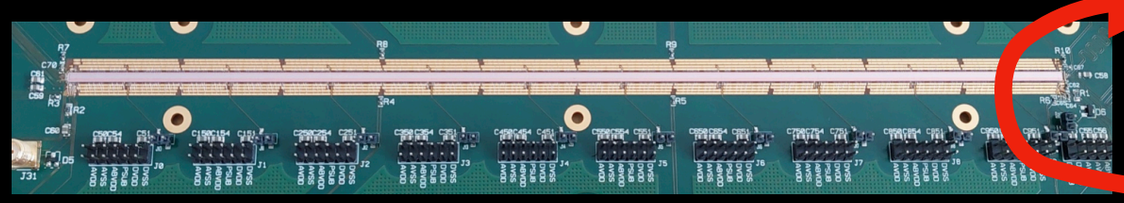
Jitter measurements

Measured the time difference between input pulse and MOST response, for full round trip:

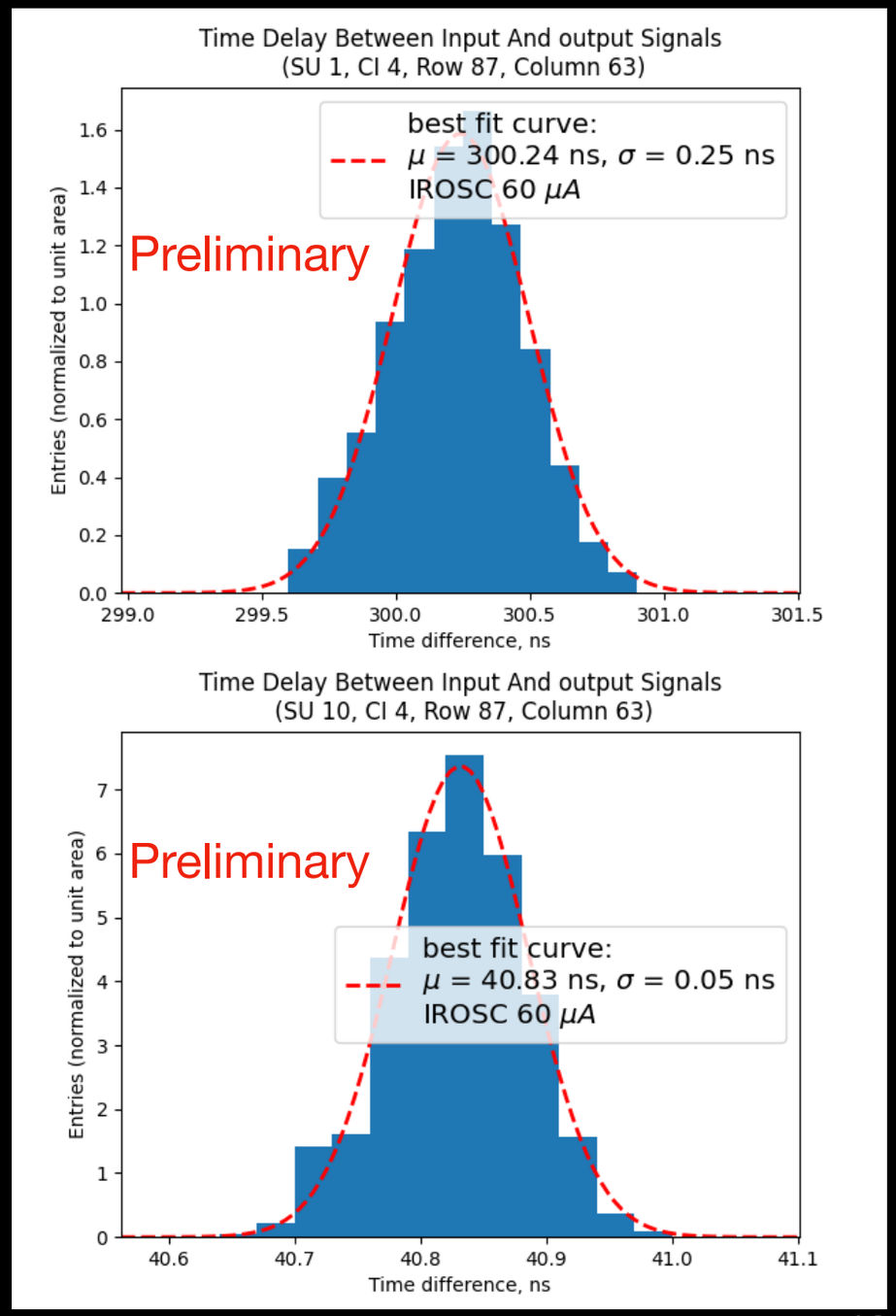
- **Time delay average is ~ 40 - 300 ns**
- **Time delay variation (jitter) ~ 50 - 250 ps**

~50 cm, ~300 ns

~4 cm, ~40 ns



Time delay linearly increasing with the distance, see slide 21 for more details

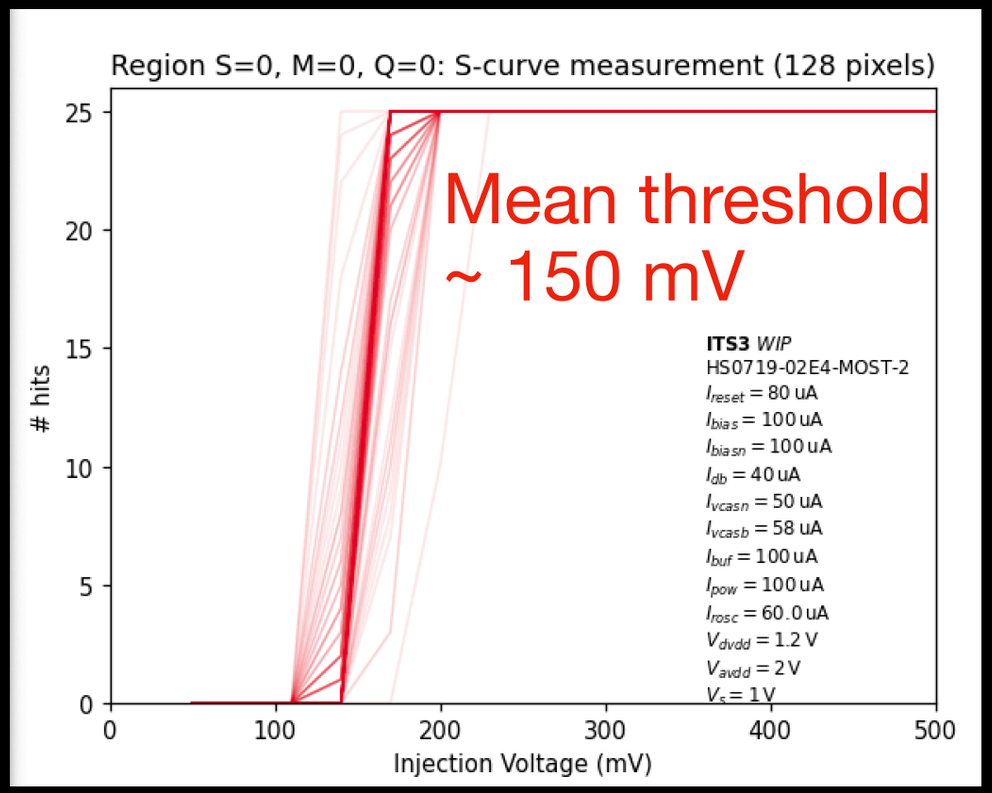


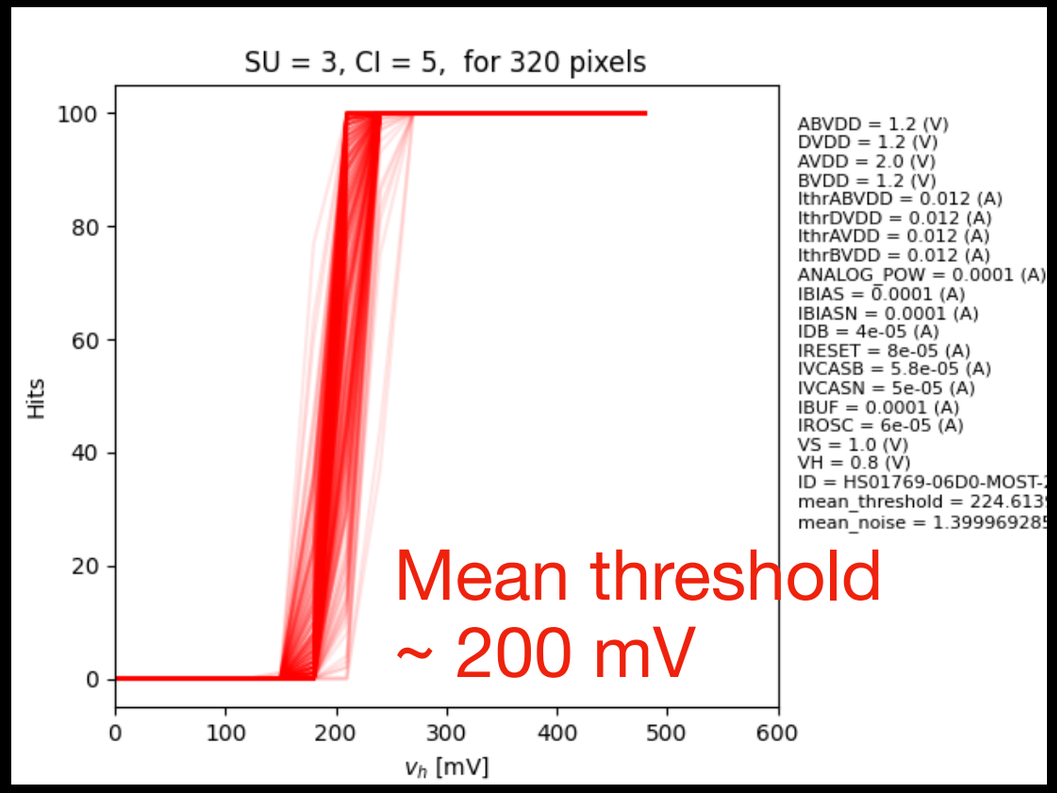
Front end and reverse bias

- Analog circuit ground is connected to the substrate
- Reverse sensor bias is applied by shifting up the potential at the input of the front end (by varying Vs)
- All pixels respond, lowest threshold found at minimum reverse bias ~ 100 mV
- Preliminary results indicate reduced noise with increasing reverse bias due to lower sensor capacitance -> work in progress on detailed analysis

See backup slide 23 for front end schematics

Example of s-curves from two different wafers (same bias parameters):



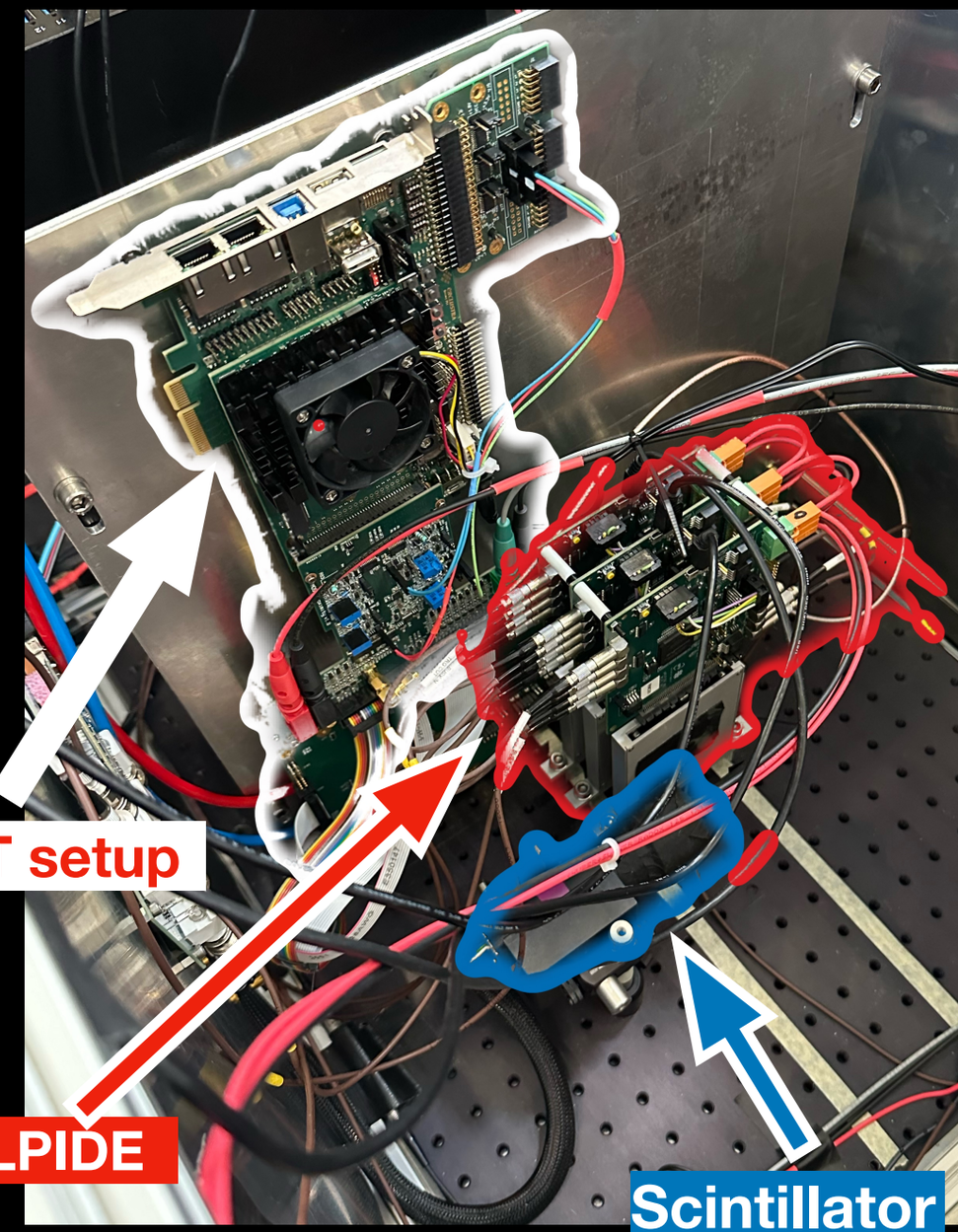


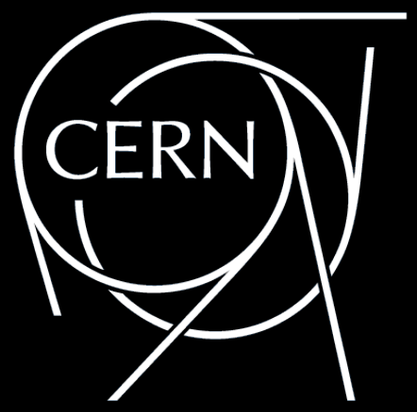
Summary

- Granular power switches, Dense matrix circuits -
  - Does this type powering work? - Yes
  - What is the impact on the yield? - Initial observations meet expectations
- Asynchronous - data driven readout -
  - Can we have stitched sensor with precision timing? - First jitter measurements are encouraging
- Different approach for reverse bias
  - Evaluate alternative biasing by lifting front end circuitry? - All pixels respond, first results show decreasing noise with VS increase

Outlook

- Test beam in September - data to be analysed
- Verify detailed yield
- Tuning of chip parameters
- Investigation of timing capabilities



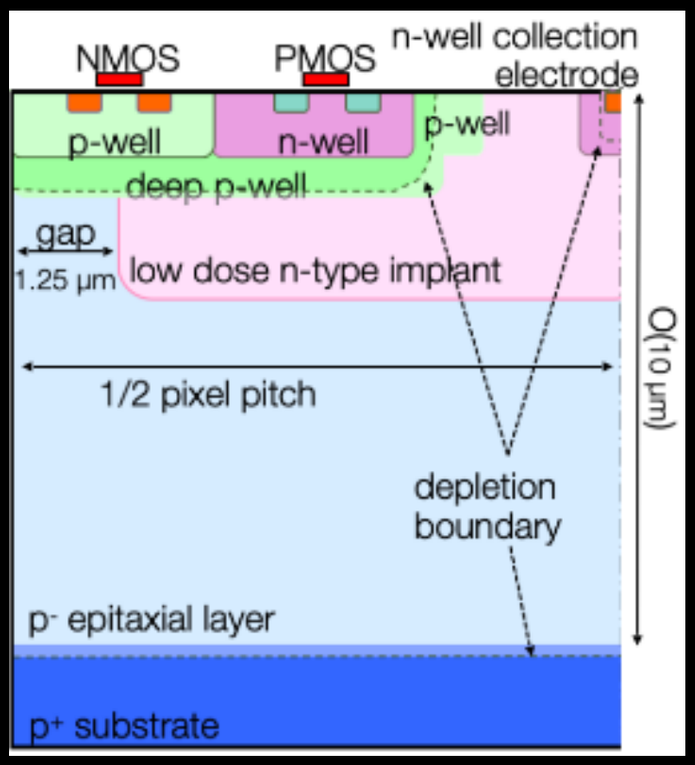


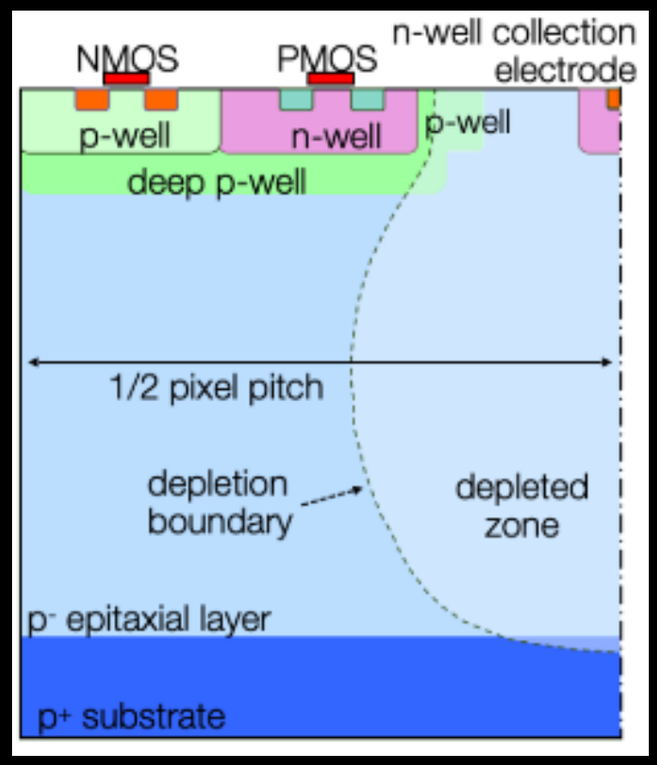
Thank you for your attention!

MOST ER1 Submission

Sensor Design

- TPSCo 65 nm CMOS Imaging Technology
- 2 pixel geometry varying by wafers: Modified with gap and Standard
- Pixel pitch: 18 um x 18 um
- 901120 pixels in total for 10 RSU

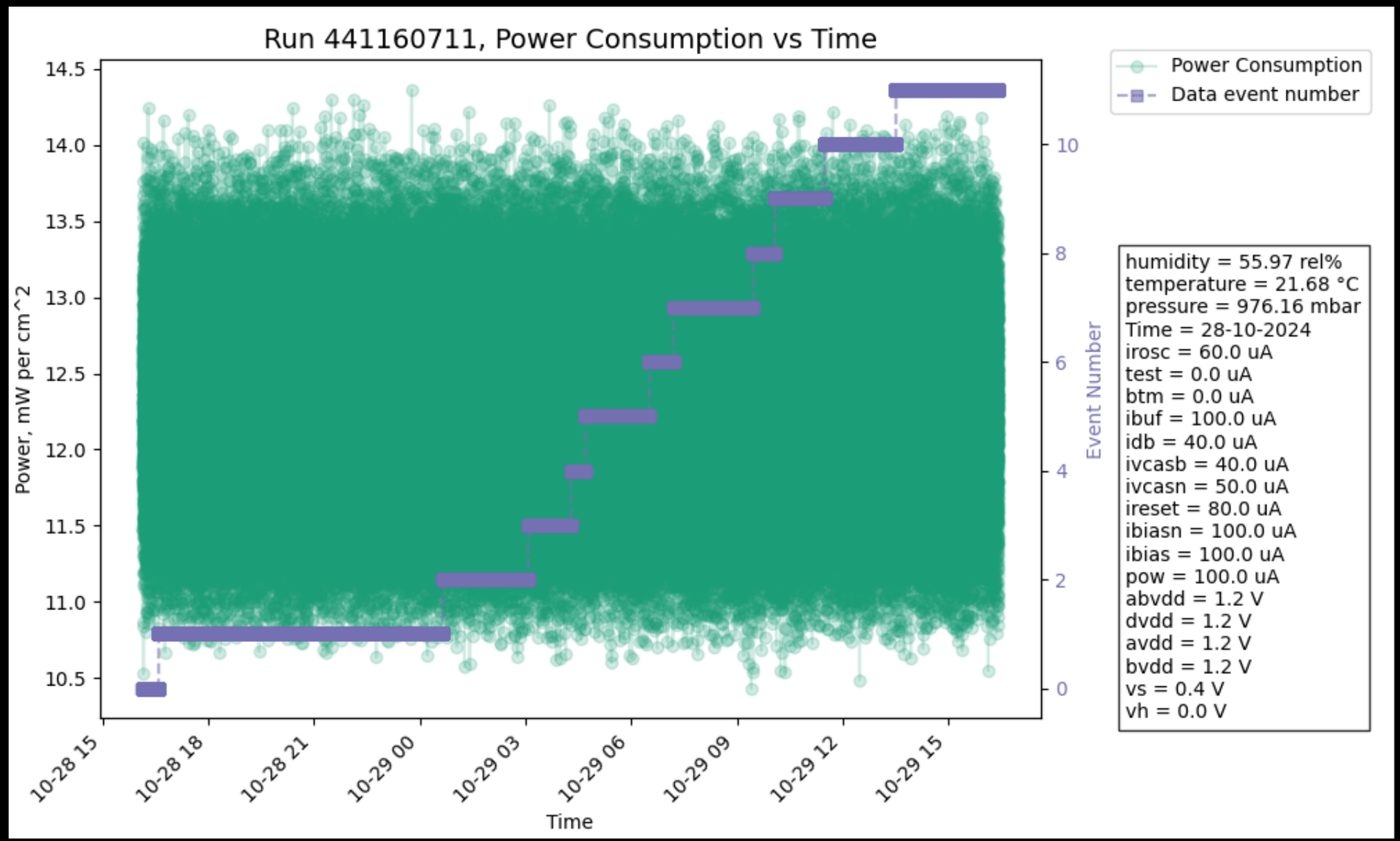




Power Consumption

Low power - less heat generated

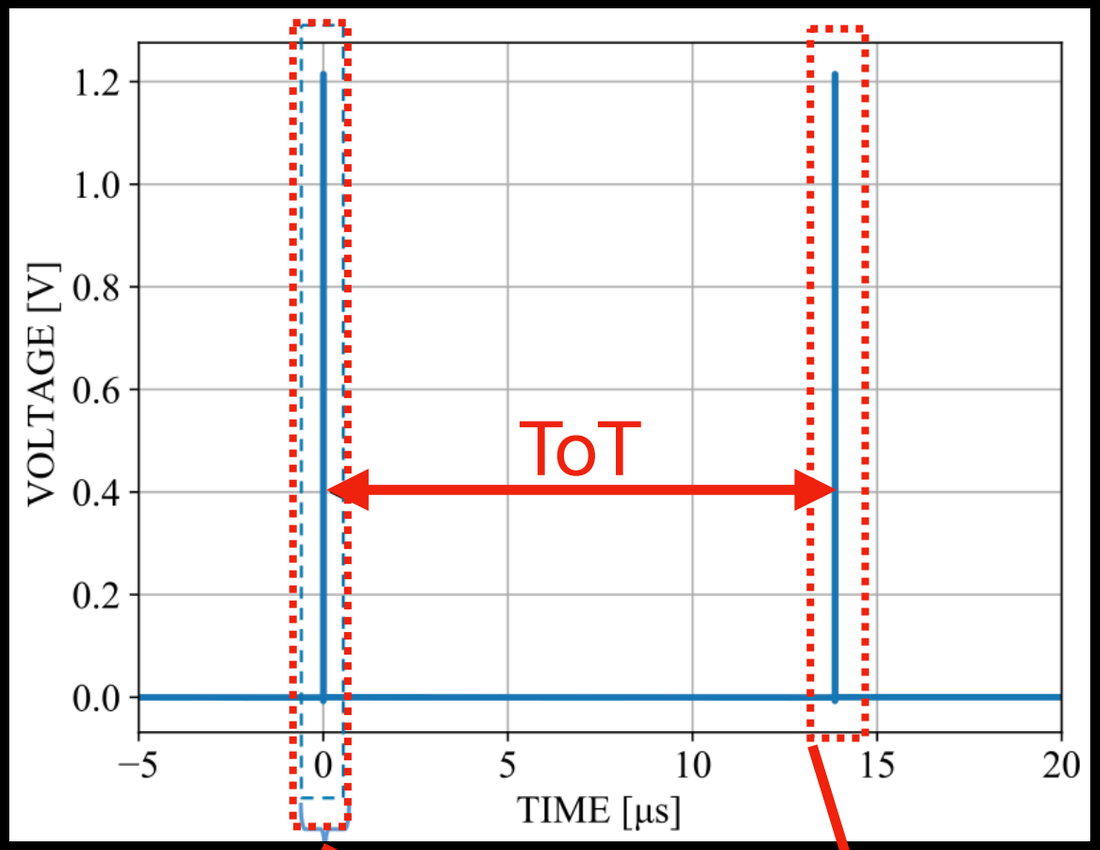
- MOST meets the air cooling requirements for the power consumption
- Average power consumption (analog+digital) with increasing number of events stays on average at 12.5 mW/cm2



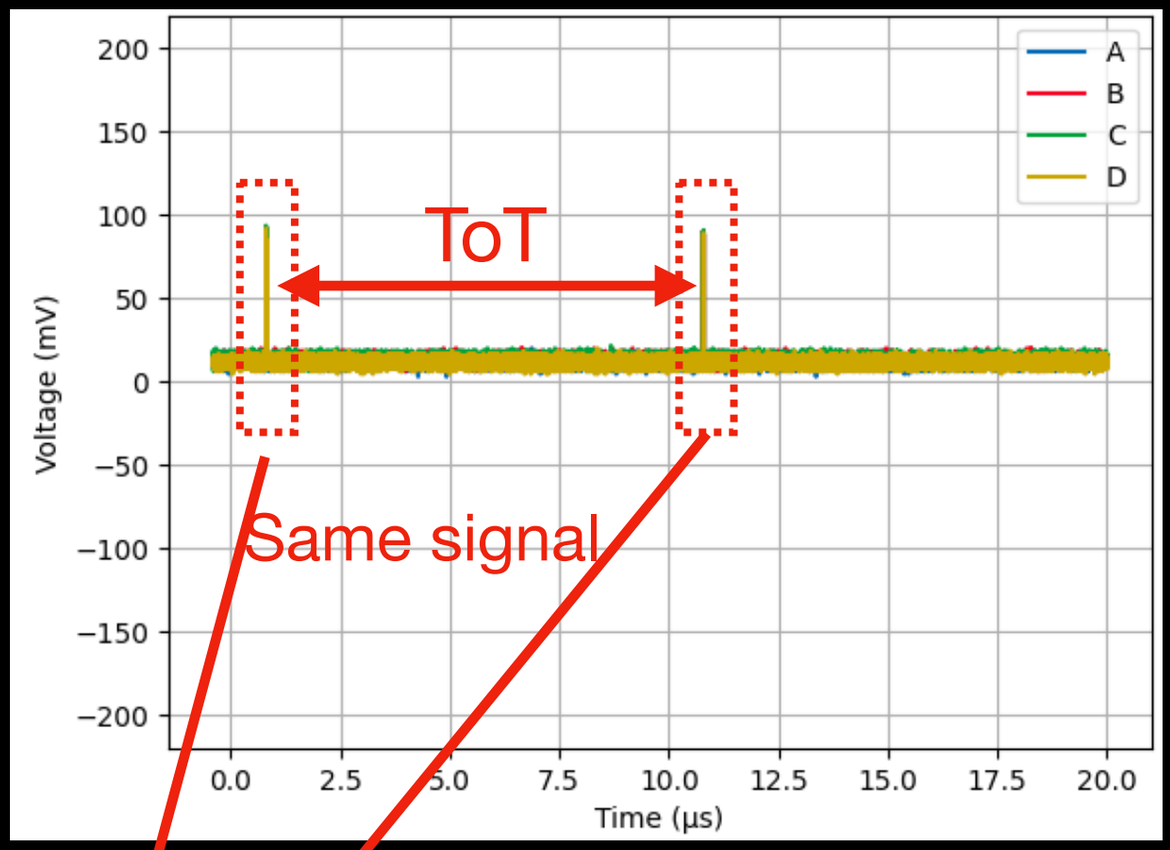
Asynchronous readout

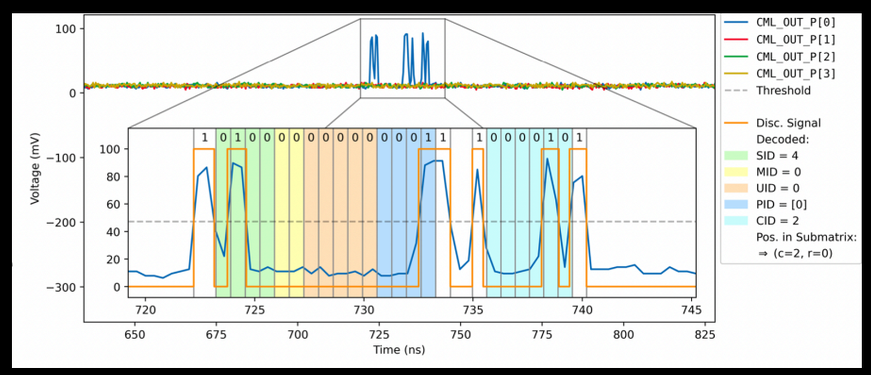
Time over Threshold (ToT) information decoding

Simulation



Real output from scope





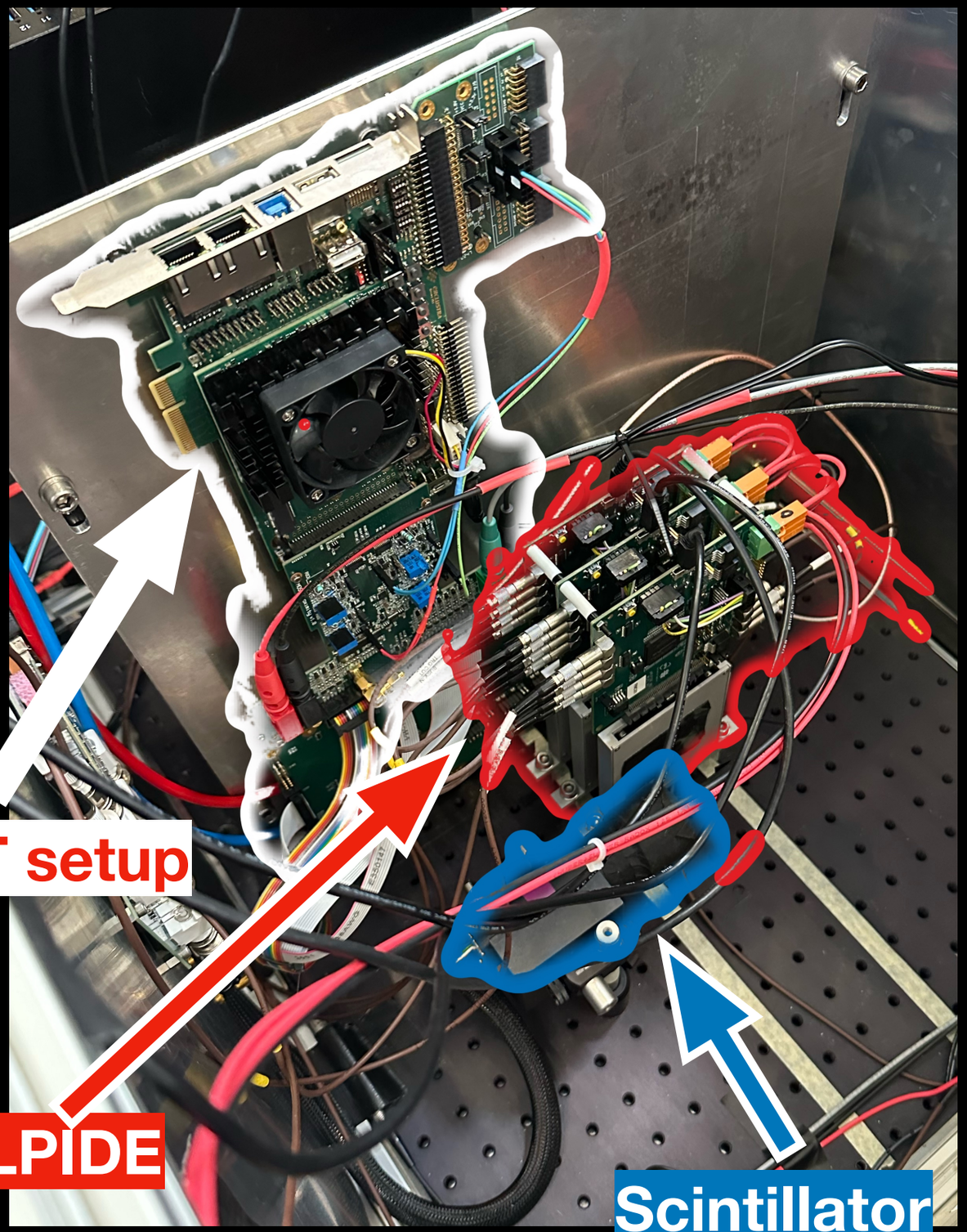
Test Beam

Analysis ongoing

- September 2024
- Parasitic user at CERN PS - Beam conditions changed frequently
- Tracking: 6 ALPIDE planes
- Trigger: 2 Scintillators + PMT
- Approx. 1 RSU in acceptance of scintillators

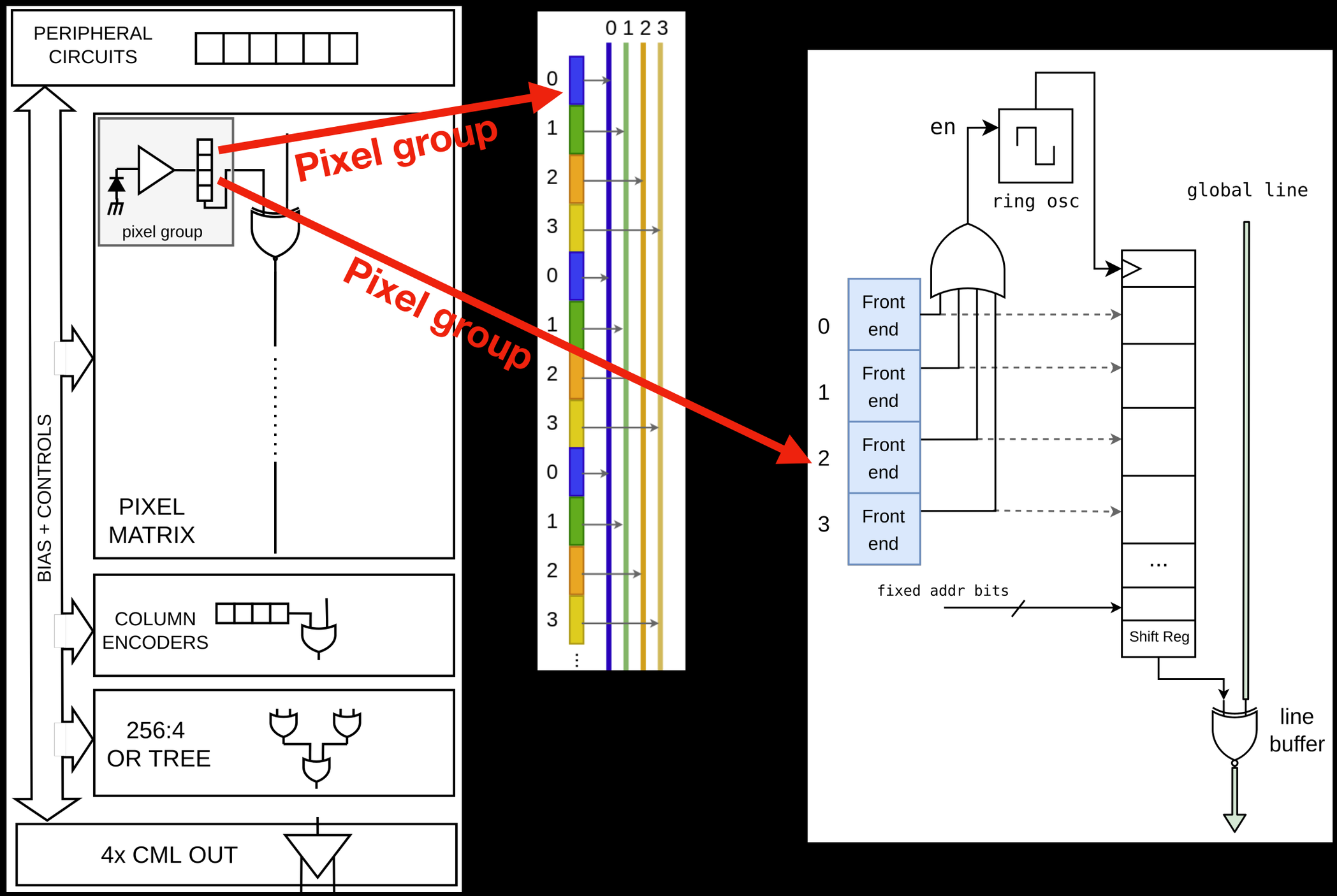
MOST detected events!!

Goal: Measure detection efficiency



Asynchronous readout

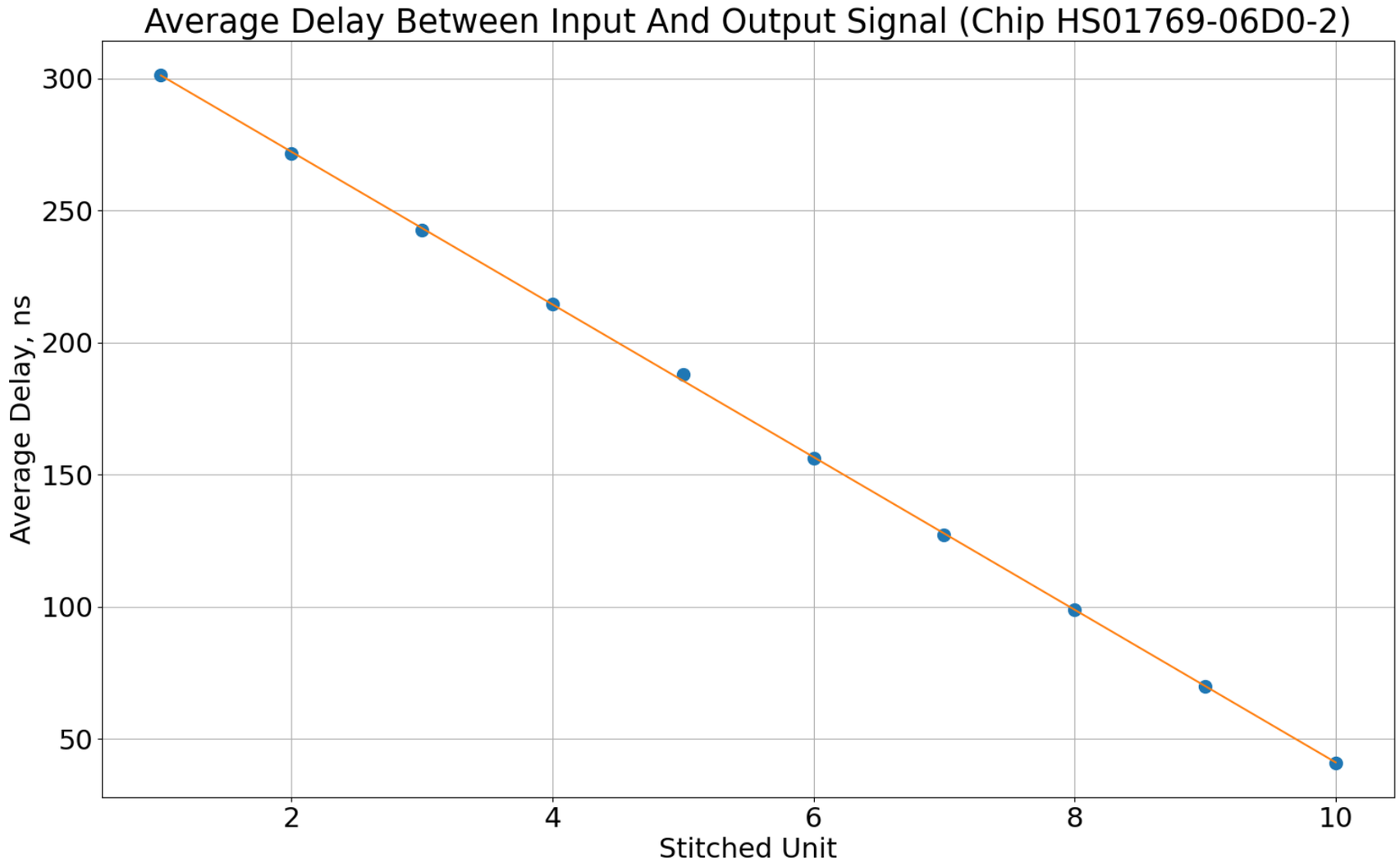
Details



First time studies

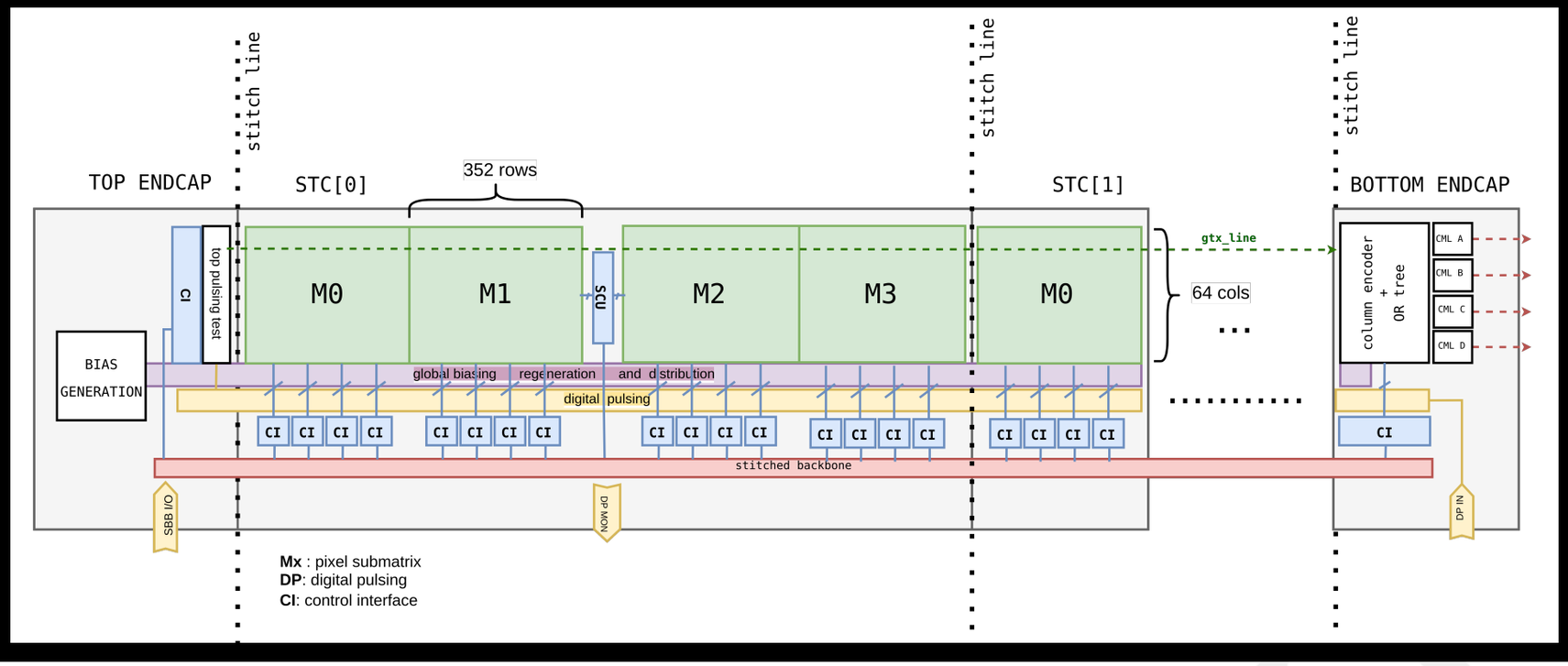
Variation of time delay with SU

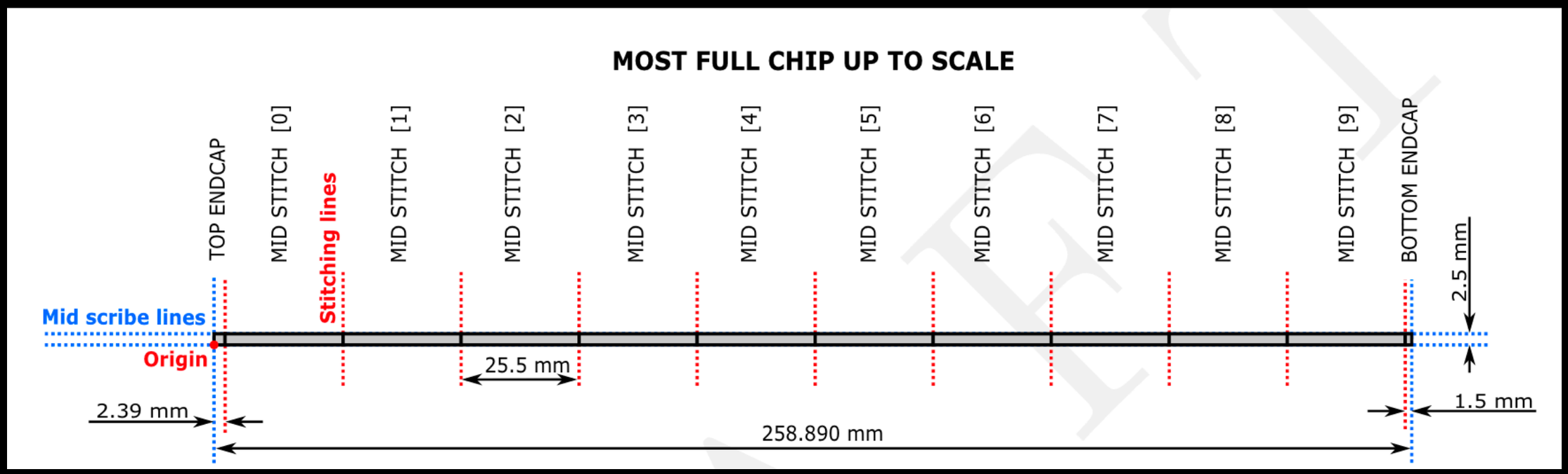
The time delay between input and output signals decreases linearly when moving closer to the nearest Stitched Unit, consistent with predictions.



MOST ER1 Submission

Stitching technology





Front End schematics

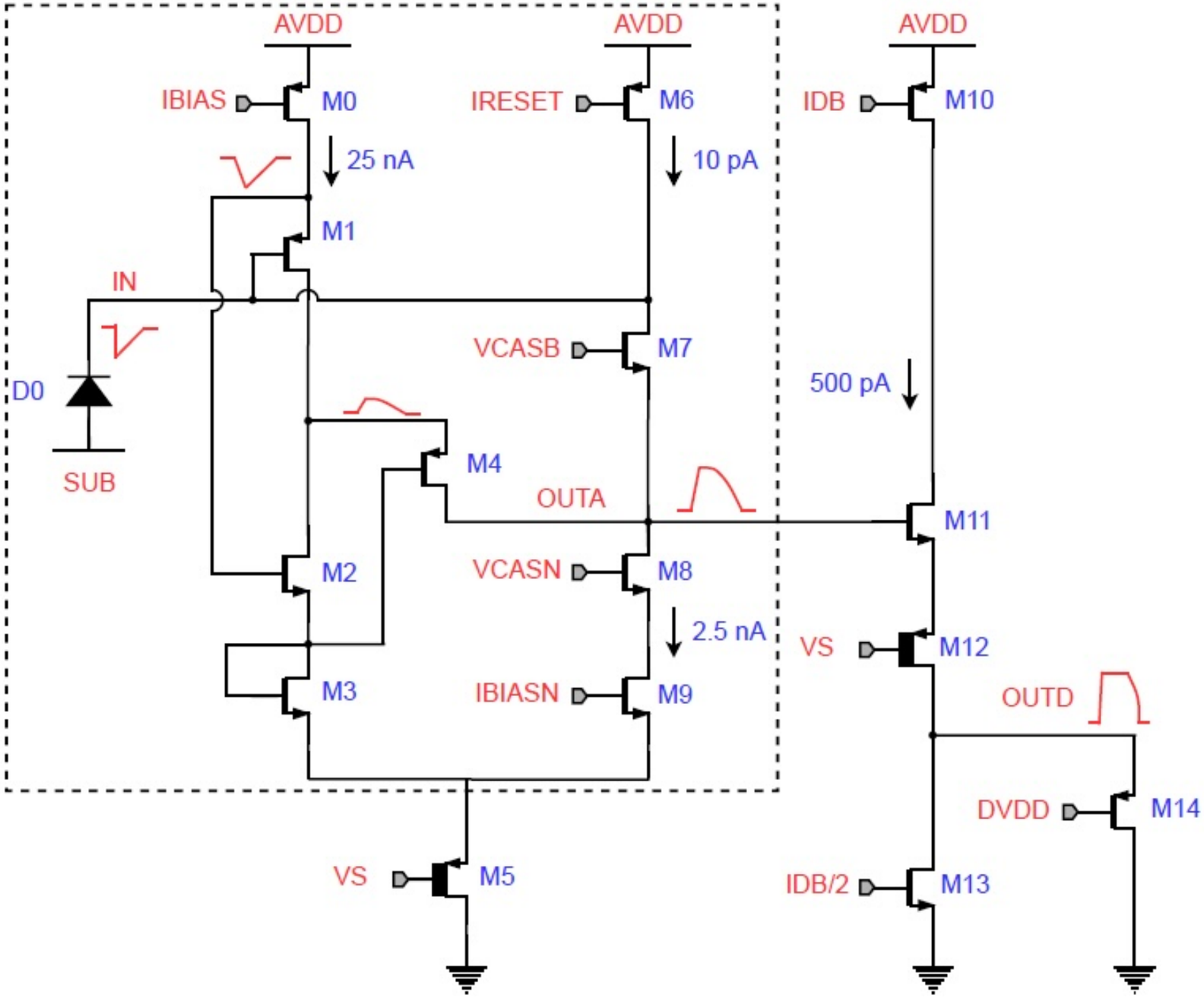
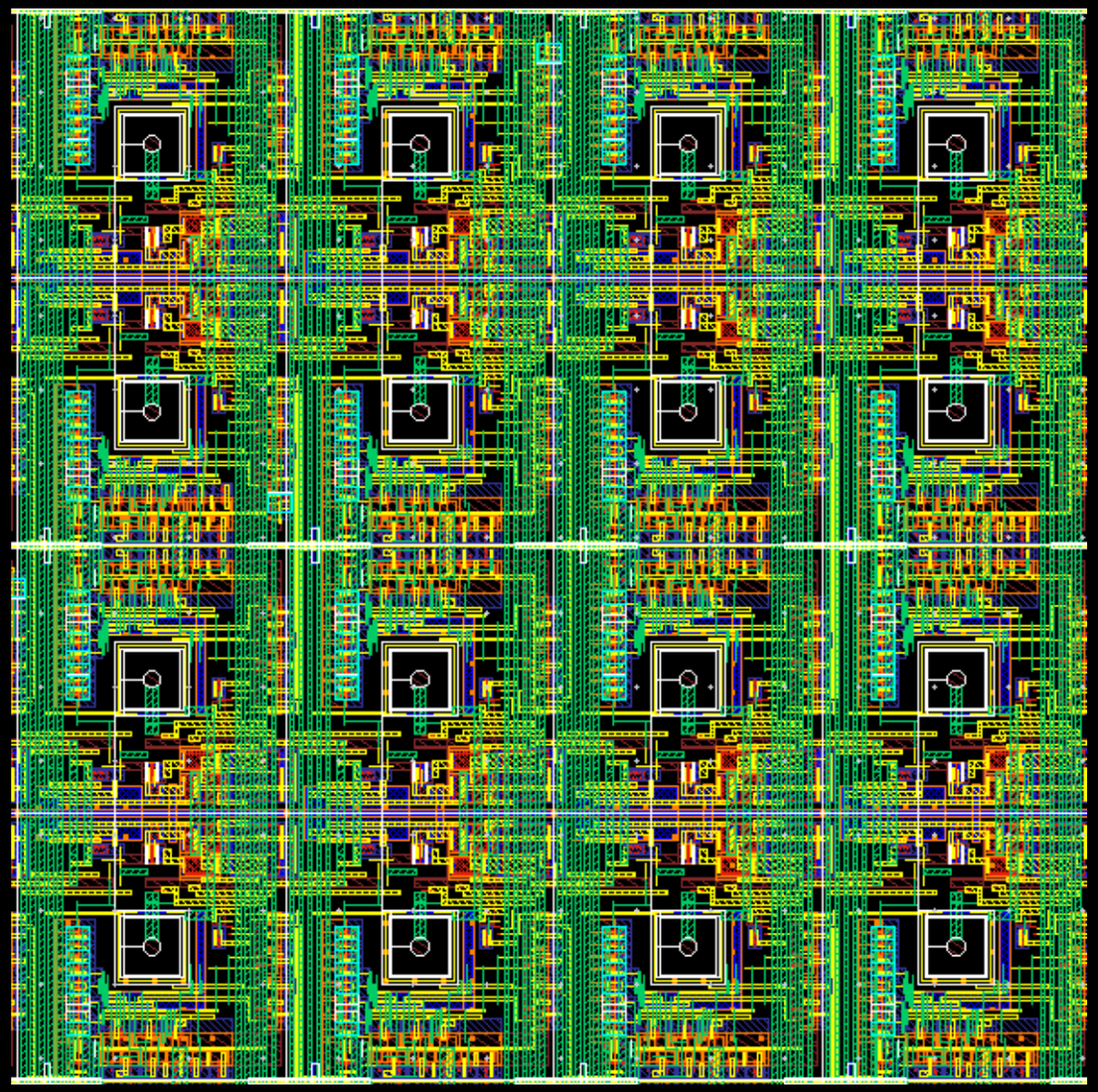


Figure 5.10: Schematic of the front-end in the MOST chip.

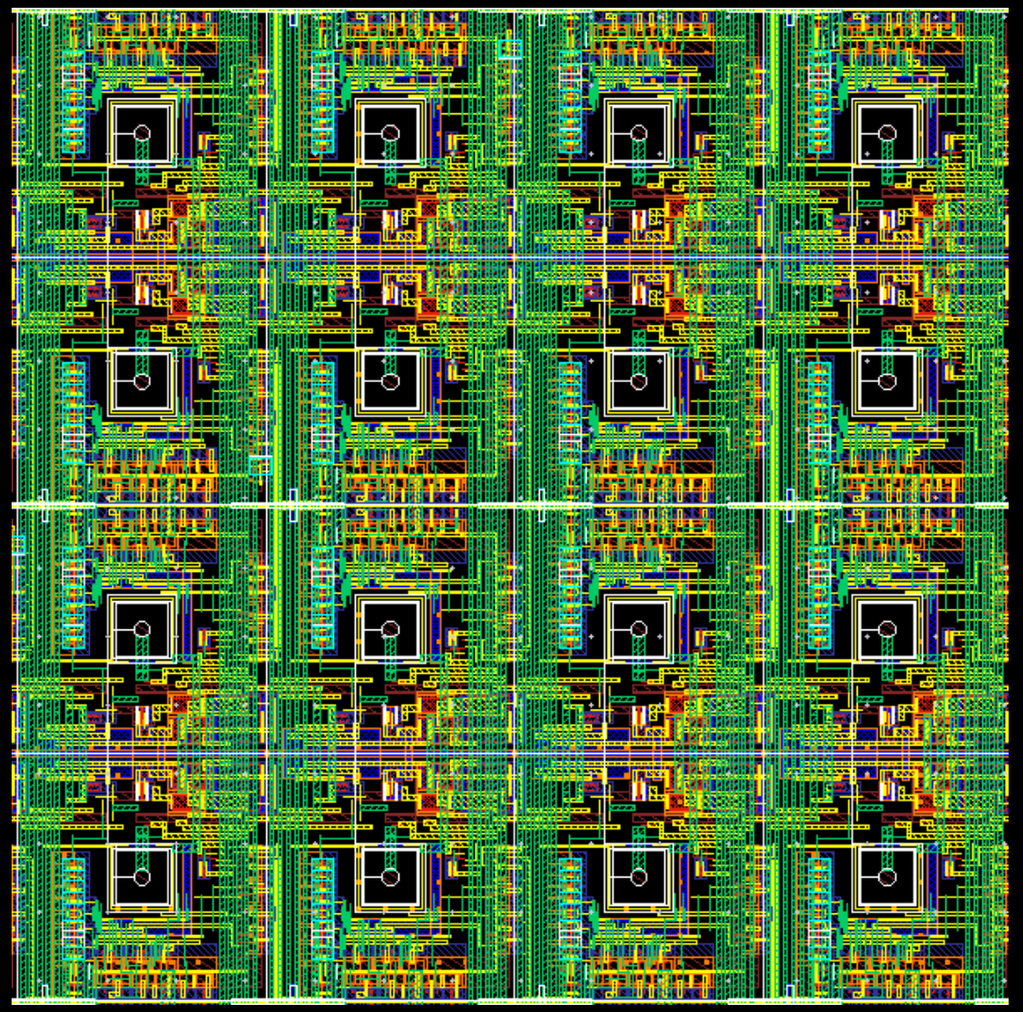
Pixel Layout

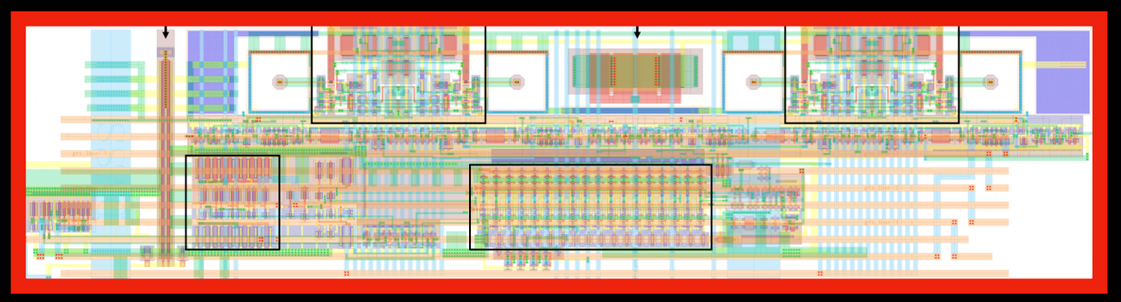
MOSS and MOST

MOSS Large Pixel Pitch 22.5 µm



MOSS Fine Pixel Pitch 18 µm





MOST Pixel Pitch 18 µm