ATLASPix3 Serial powering and multi-chip module studies for future HV-CMOS tracker

Authors:

A. Andreazza[1], R. Dong[2], H. Fox[3], Y. Gao[4], P. Gheewalla[4], **M. Huebner**[5], L. Meng[3], D. Muenstermann[3,5], I. Peric[2], F. Sabatini[1], F. Ustuner[4], R. Zanzottera[1]

[1]University of Milan, [2]Karlsruhe Institute of Technology, [3]Lancaster University, [4]University of Edinburgh, [5]RheinMain University of Applied Sciences

Motivation

Future experiments require large tracking area (~100 m^2):

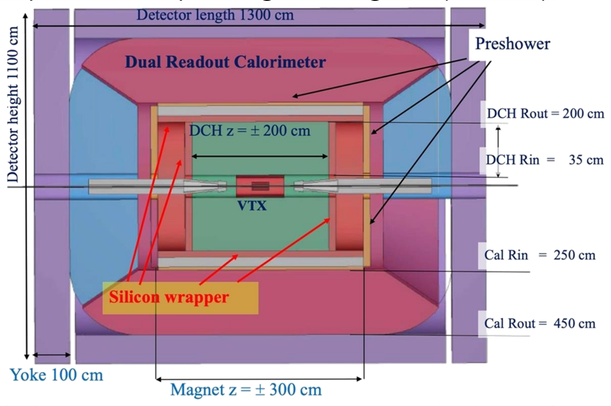

Fig. 1: IDEA detector layout for future experiments (e.g. higgs factory) [1]

- Needs relatively cheap and fast mass-production
- Modest spatial resolution and radiation requirements for the middle/outer layers
- Limited space for services (e.g. power cables)
- Material budget (weight) limited

➢ Advantages for monolithic sensors like ATLASPix3

ATLASPix3 features

- **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensor
- HVCMOS technology
- AMS/TSI 180nm process
- Substrate ~300 Ωcm
- Breakdown (unirradiated): ~-65V
- Full reticle size of 2.2 cm x 2.0 cm
  - Matrix size: 132 x 372 pixels
  - Pixel size: 50µm x 150µm
  - Pixel structure in fig. 2
- Individual amplifiers and threshold tuning circuits
  - Threshold can be tuned to 800e, with dispersion ~60e, noise ~ 70e
- Digital part separated from the analog in the peripheral
- Triggerless/Triggered readout
  - Triggered data output: up to 1.28 Gbit/s 64b/66b
  - Un-triggered data output: 1.6 Gbit/s 8b/10b
- 25ns time stamping
- Good time resolution: ~4 ns (corrected)
- Shunt-LDO (SLDO) regulators for Serial Powering
- Power consumption 140 mW/cm^2

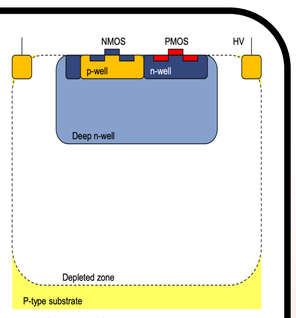

Fig. 2: Pixel structure [1]

New 2-in-1 Telescope Board

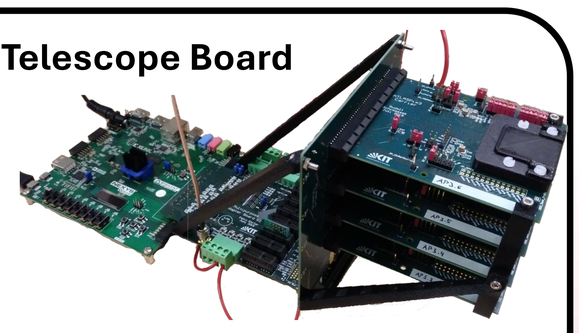

Fig. 3: Previous telescope setup
[https://gitlab.cern.ch/groups/ATLASPix3/-/wikis/telescope-revision-2-wiki-main-page]

Previous ATLASPix3 telescope:

- long traces running from Artix-7 FPGA PCB via GECCO and telescope PCBs to single carriers
- clock speed limited to 200 MHz, resulting in 400 Mbit/s data rate instead of 1.2 Gbit/s design value
- prevented us from investigating ATLASPix‘ true time resolution at full clock speed

New ATLASPix3 FMC telescope PCB designed and produced:

- combines Gecco and previous telescope board into one PCB
- shorter trace lengths
- Firmware/software modifications and testing planned for next months

➢ should allow for higher clock speeds to use full potential of ATLASPix3

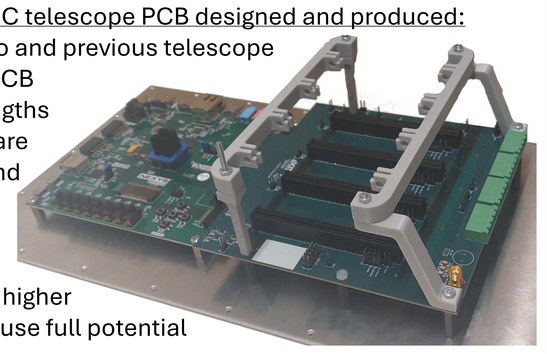

Fig. 4: New telescope setup

DESY Testbeam

- Two telescopes tested at DESY with 3-6 GeV electron beams
- associate L3 as DUT plane, other layers for alignment and track reconstruction
- selected tracks with χ^2/ndof<5
- cluster associated if within 0.6 mm from track interception

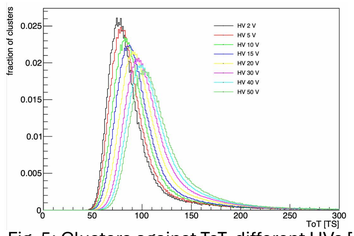

Fig. 5: Clusters against ToT, different HVs [1]

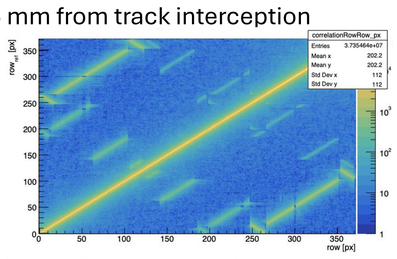

Fig. 6: Self-correlation plot [2]

- Cross-talk due to capacitive coupling limited to ~1% of hits
  - cross-talk hits show up in self-correlation plots (fig. 6)
  - contained in a low ToT peak near 0 timestamps and removed in fig. 5
- ToT increases with HV (fig. 5), cluster size moderately increases (fig. 9)
- Fig. 10 shows resolution at different HVs for 1- and 2-pixel clusters, see [2] for calculations

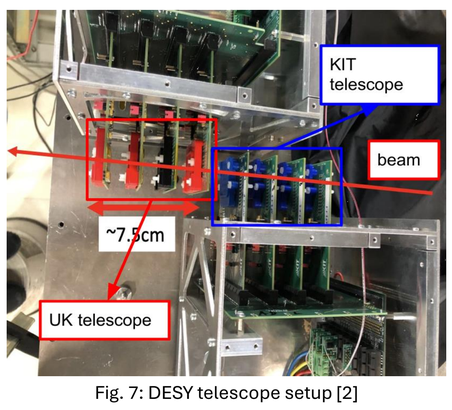

Fig. 7: DESY telescope setup [2]

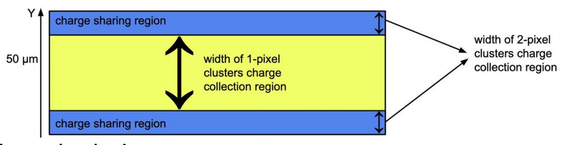

Fig. 8: Charge sharing regions [2]

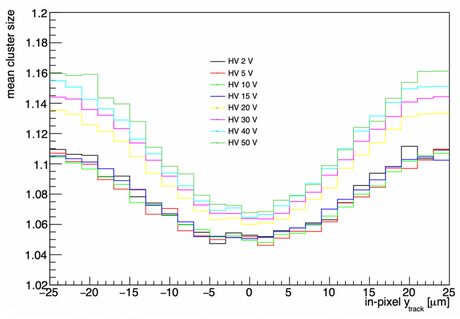

Fig. 9: Cluster size against pixel hit position for different HVs [1]

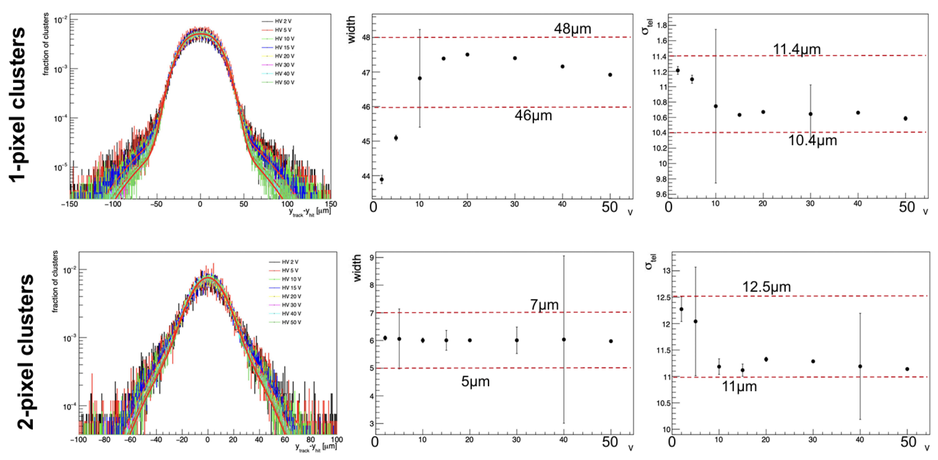

Fig. 10: Resolution for 1- and 2-pixel clusters at different HVs [2]

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). For more information see: "The DESY II test beam facility" (https://doi.org/10.1016/j.nima.2018.11.133)NIMA, Volume 922, 1 April 2019, Pages 265-28

Serial powering

- SLDO regulators for VDDD/A separately, schematic in fig. 11
- Allows for constant current operation mode
- Greatly simplifies power supply (fewer power lines and smaller current)

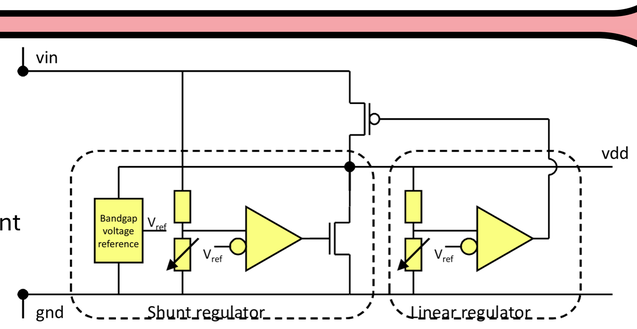

Fig. 11: Regulator circuit [1]

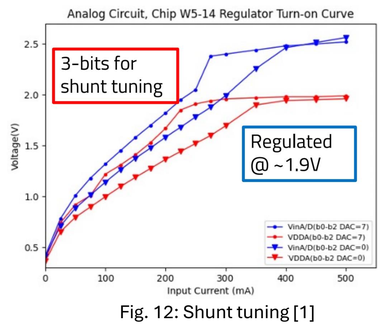

Fig. 12: Shunt tuning [1]

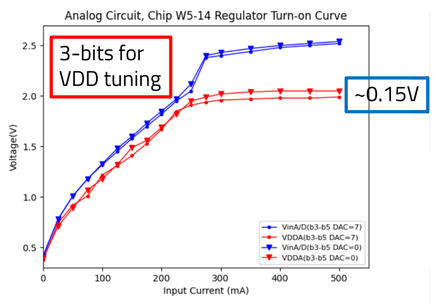

Fig. 13: VDD tuning [1]

- Current threshold can be tuned within ~50mA, ohmic behavior verified after threshold (fig. 14):

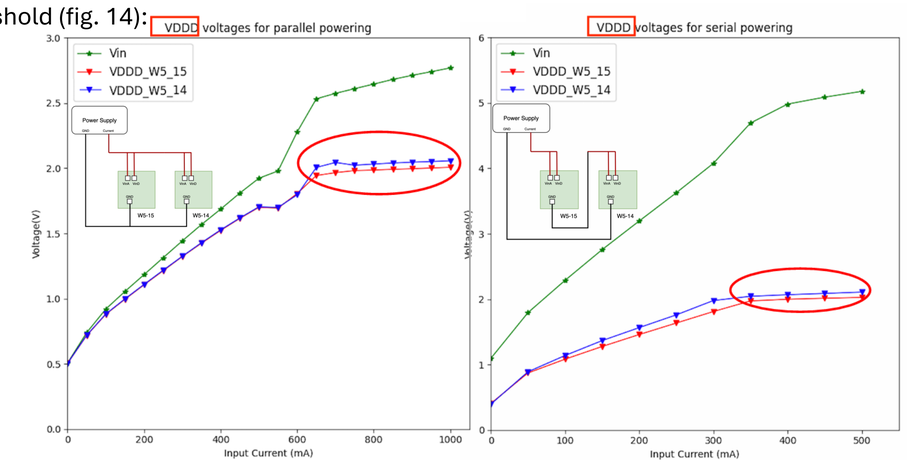

Fig. 14: VDDD for parallel (left) vs serial powering (right) [1]

- Fig. 15 and 16 show the input referred noise/threshold (using injection voltage): No performance degradation for serial, minor degradation for parallel powering

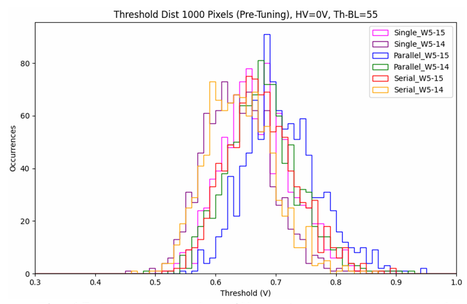

Fig. 15: Thresholds for different power schemes [1]

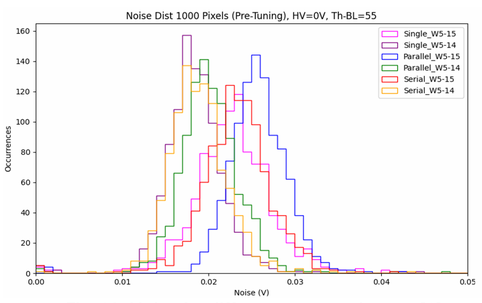

Fig. 16: Noise for different power schemes [1]

Pixel efficiency

- Efficiency = Measured hits / calculated hits. Hits are calculated by measuring particles with other telescope layers and tracing their path.
- Overall efficiency > 99 % achieved after 20 V (fig. 17) -> relatively wide operational range for bias voltage
- Efficiency in inter-pixel regions increases with higher bias voltage, see fig. 18, note the different colour gradients!

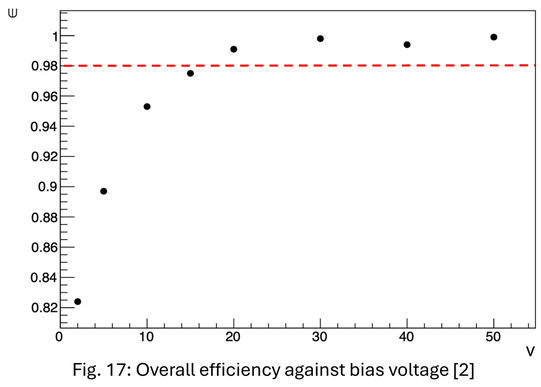

Fig. 17: Overall efficiency against bias voltage [2]

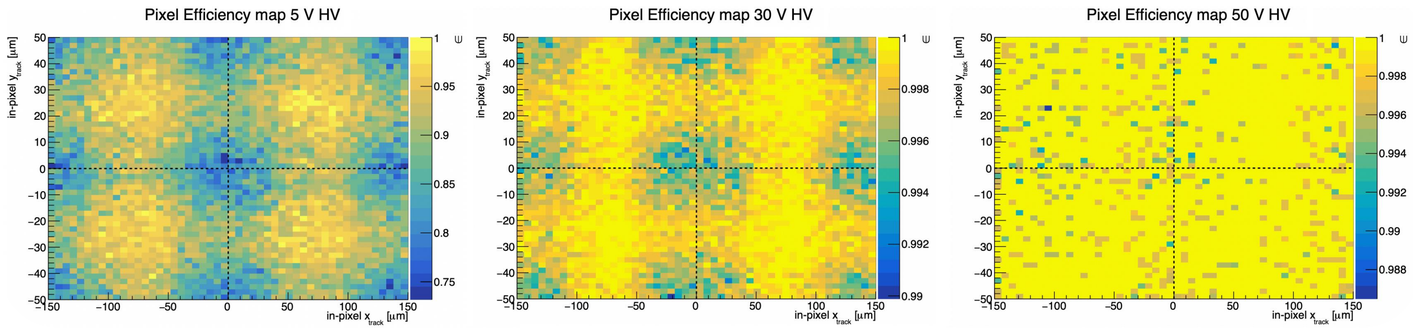

Fig. 18: Percentage of particles detected at measured in-pixel positions for different bias voltages [1]

Summary

- First quad module assembled and tested - big step towards large area application
- New quad module suitable for serial powering produced this year
- Shunt-LDO has been verified at single chip and double-chip structure
- New 2-in-1 PCB that combines Gecco and telescope board produced
- ATLASPix3 has been used in multi-chip systems as telescopes or quad modules
  - high efficiency and expected resolution for the telescope system from testbeam data
  - no degradation of performances for quad modules

Next steps

- Prototyping for mechanic and cooling are being pursued
- Tests of 2-in-1 PCB and higher clock speeds
- Assembly and tests of ~5 quad-modules, and Integration of 2-3 quad-modules on a serial-powered chain on top of a ~60cm power bus (e.g. Al flex at CERN)
- Seek funds to continue to contribute to smaller scale MPW for sensor improvements (some earlier results indicate potential to reduce significantly the power consumption)

Quad modules and serial powering chain

- 4 modules in quad share data and bias
- Serial powering chain planned with new quad module

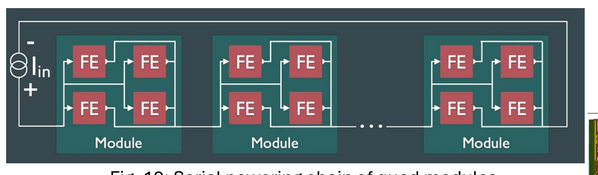

Fig. 19: Serial powering chain of quad modules
[J. Chan: Serial Powering for Atlas Itk pixel modules on Pixel 2022 conference]

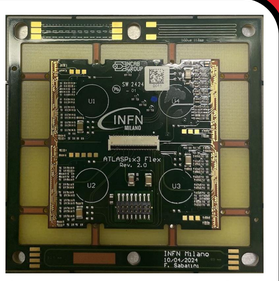

Fig. 21: New (2024) quad PCB [2]

Stave electrical bus considerations:

- Fig. 20 stave would reduce power dissipation on distribution lines and minimise number of connections
- Save material by using Aluminium as conductor

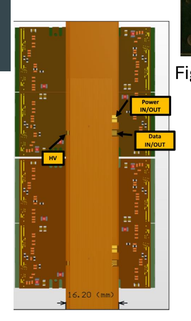

Fig. 20: Power/data stave [1]

References

[1] Large Area Low-power Monolithic CMOS Tracking Detectors for future Higgs Factory Experiments, Talk by Y. Gao at the 3rd ECFA Workshop on e+e- Higgs, Top & Electroweak Factories. 09.10.2024. With contributions from Bristol, Edinburgh, INFN Milan, IHEP, KIT, Lancaster, STFC RAL. https://indico.in2p3.fr/event/32629/contributions/142932/

[2] The ATLASPix3 CMOS pixel sensor performance, Talk by R. Zanzottera and F. Ustuner at the 42nd International Conference on High Energy Physics (ICHEP 2024). 20.07.2024. With contributions from INFN and U.Milano, KIT, IHEP, RAL, U.Lancaster, U.Bristol, U. Liverpool, U.Edinburgh, U.Tsinghua, U.South China. https://indico.cern.ch/event/1291157/contributions/5888448/

Contact: marco.huebner@hs-rm.de

Supervisor contact: daniel.muenstermann@hs-rm.de