Early evaluation of the triggering capacity of an upgraded Vertex Detector for the Belle II experiment

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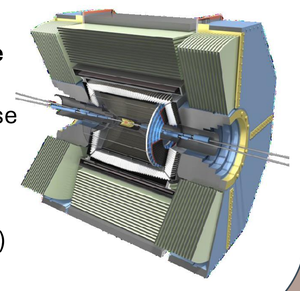
Belle II Vertex Detector Upgrade Proposal

Belle II Experiment

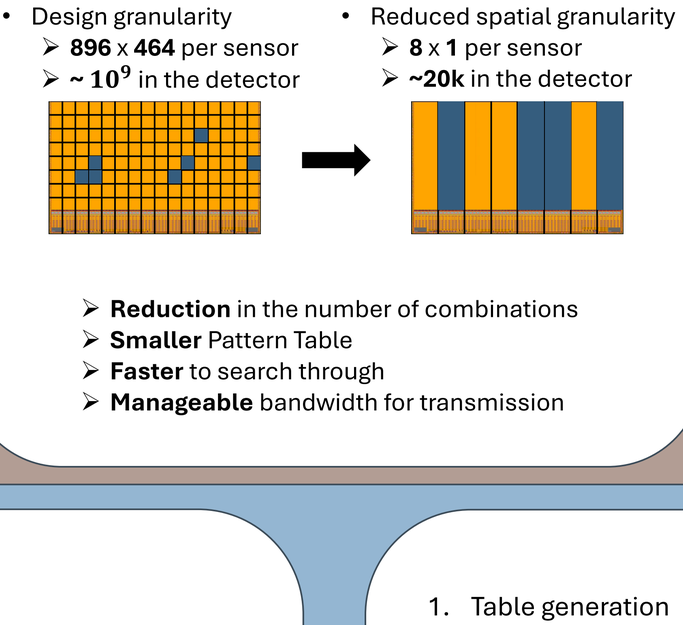
- Asymmetric e^+/e^- collision at *4/7 GeV*, $\sqrt{s} = 10,58\ \mathbf{GeV}$
- Located at SuperKEKB collider in Tsukuba, Japan
  - Highest inst. luminosity in the world : $4,7 \times 10^{34}\ \mathbf{cm^{-2}s^{-1}}$
  - ➢ Target : $6 \times 10^{35}\ \mathbf{cm^{-2}s^{-1}}$
- Improving **tracking performance** and **background rejection** needed due to luminosity increase



- Tracking trigger informations **only** from Central Drift Chamber (CDC)

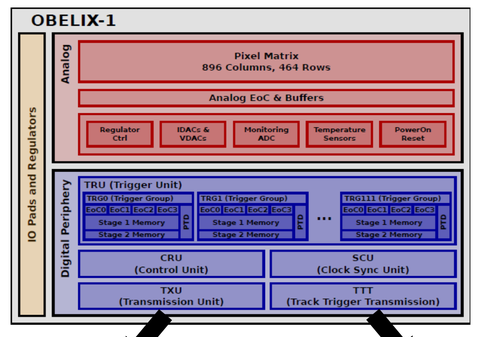
VTX Detector [1]

Current Vertex Detector **(VXD)** → New Vertex Detector **(VTX)**



- Fully pixelated detector
  - Pixel pitch : **33 µm**
- 5-6 Layers with the same DMAPS sensor : **OBELIX**
  - Pixel Matrix : **896 x 464**

OBELIX sensor [2]



Hit Data Output :
- TXU (Transmission Unit)
  - Provides pixel information
- Triggered output

Trigger Data Output :
- TTT (Track Trigger Transmission)
  - Data sent : **8 bits**
  - Frequency : **34 MHz**
- Continuous output

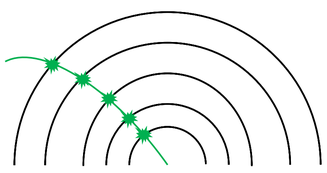
Is triggering with pixel sensor information feasible ?

Fast Track Reconstruction Algorithm

Look-Up Table

- Logic based on a **reference table** :
  1. **Pattern Table** :
     - Stored physical track patterns from simulation with their characteristics
  2. **Detector/Table pattern comparison** :
     - Triggered track if its pattern is recognized in the table

Example Pattern
$\theta = 37.2\,°, \varphi = 256{,}3\,°, p_T = 1{,}13$ Gev/c



Macropixels

Pixel :
- Design granularity
  - ➢ **896** x **464** per sensor
  - ➢ **~ 10^9** in the detector

Macropixel :
- Reduced spatial granularity
  - ➢ **8** x **1** per sensor
  - ➢ **~20k** in the detector

- ➢ **Reduction** in the number of combinations
- ➢ **Smaller** Pattern Table
- ➢ **Faster** to search through
- ➢ **Manageable** bandwidth for transmission

Patterns

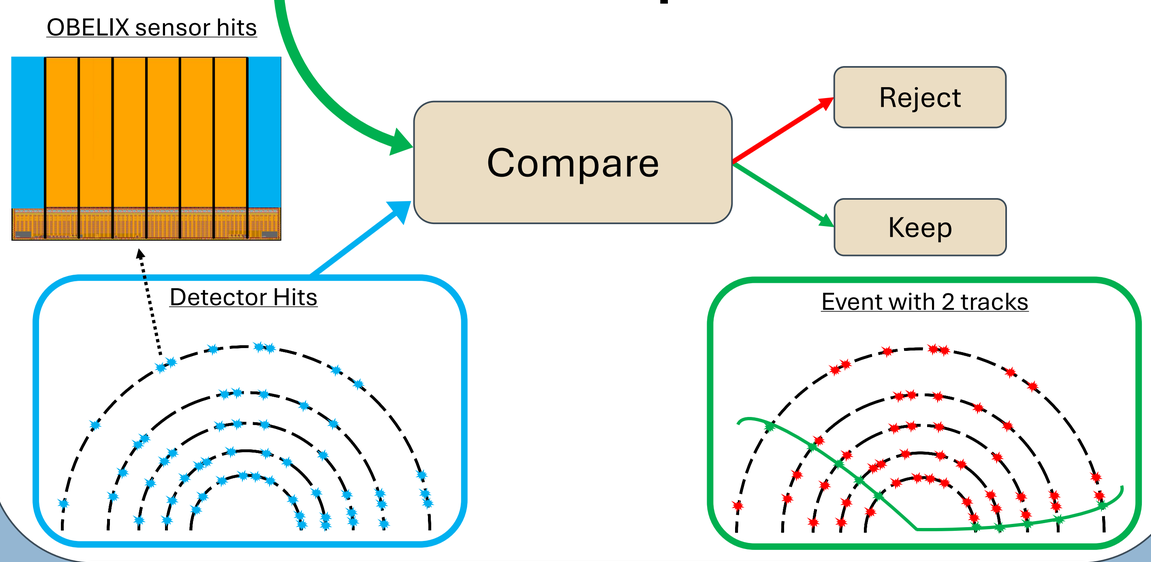
- **Pattern** : Bitword merging TTT information from all sensors
  - Current Geometry : 2552 Sensors ➡ **20416 bits**
- **LUT comparison** :

Online Hits 0011...100...110..01...1010
↕ ↕ ↕ ↕ ↕
A pattern 0010...100...010..01...0010

- **Pattern Table :**

Index	Pattern	Θ (°)	Φ (°)	p_T (GeV/c)
1	001...010....0001	67	259	1.56
2	010...010....0001	125	23	0.89
...	.....	...	...	...
126304	100...010....0100	43	344	2.34
126305	100...010...0010	175	88	1.71

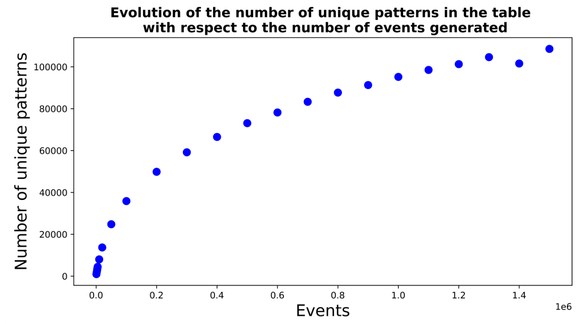
VTX TRG : In practice



Study case

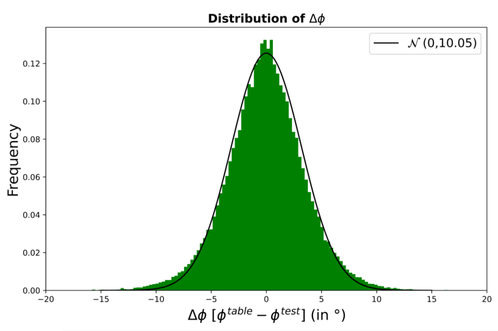
1. Table generation
   - ➢ $10^6\ \mu^{\pm}$ => With 5 Layers, ~100k unique patterns

Table event characteristics	
Production point	$(x = 0, y = 0, z = 0)$
Range of momentum	$0.2\ \text{GeV/c} \leq p \leq 3.0\ \text{GeV/c}$
Range of θ angle	$17° \leq \theta \leq 150°$
Range of φ angle	$0° \leq \varphi \leq 360°$



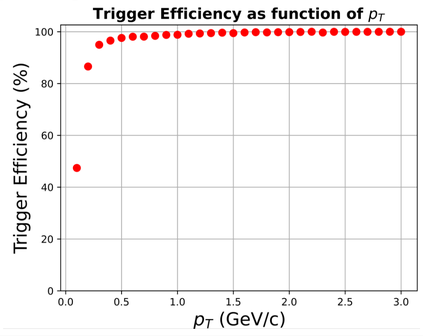
2. Test samples :
   1. Efficiency/Z-vertex acceptance : $10^5\ \mu^{\pm}$ with table characteristics / with z ∈ $[-10,10]$ cm
   2. Angle Accuracy : $10^5\ \mu^{\pm}$ with table characteristics
   3. Fake Trigger Rate : 10^6 background events, 3 BG Scenarios

Results

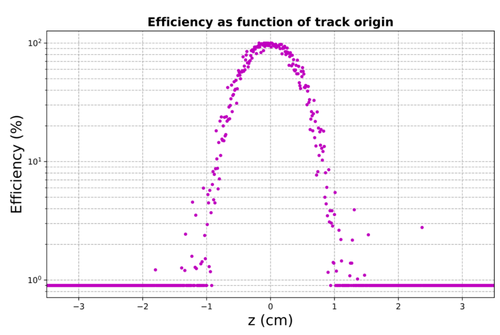


Φ Accuracy : $\pm 3,18\,°$

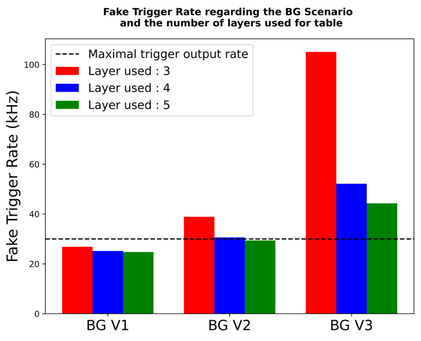
θ Accuracy : $\pm 0,34\,°$



Average Efficiency : $98,14\ \pm 0,03\ \%$



Z-vertex Acceptance : $|z| < 2,5$ cm



Cut : "Number of track > 2 & p_T > 1 GeV"

Best Case Fake Rate : **23 kHz**
- ➢ Investigate better cuts

Conclusion

- Excellent preliminary results
  - VTXTRG in agreement with TRG requirements
- More complete studies to be conducted
  - Different Macropixel segmentation (4/16/32)
  - BG Analysis Code for standalone mode
  - Other VTX Geometries (6 Layers / staggered)
- Implementation firmware to be studied
  - Constraints from TRG FPGAs and OBELIX design

Acknowledgement

This work has been conducted thanks to the help of Tomoyuki Shimasaki, Maximilian Babeluk, Jérôme Baudot, Taichiro Koga, and the comments provided by the Belle II TRG and VTX group

References

- [1] : Aihara et al., *"Belle II Detector Upgrades Framework Conceptual Design Report"*, 2024, arXiv : 2406.19421
- [2] : Babeluk et al., *"CMOS MAPS upgrade for the Belle II Vertex Detector"*, 2023, DOI : 10.1016/j.nima.2023.168015