Upgrade of the Belle II Vertex Detector with depleted monolithic active pixel sensors

Alice Gabrielli on behalf of the Belle II VTX collaboration

Eleventh International Workshop on Semiconductor Pixel Detectors for Particles and Imaging

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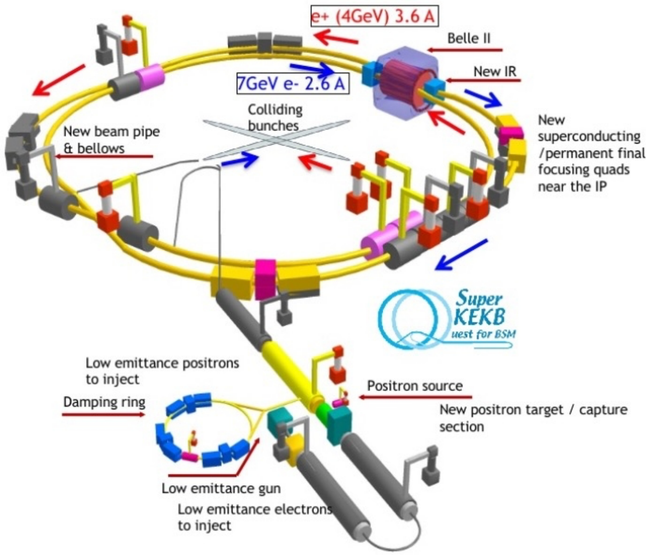
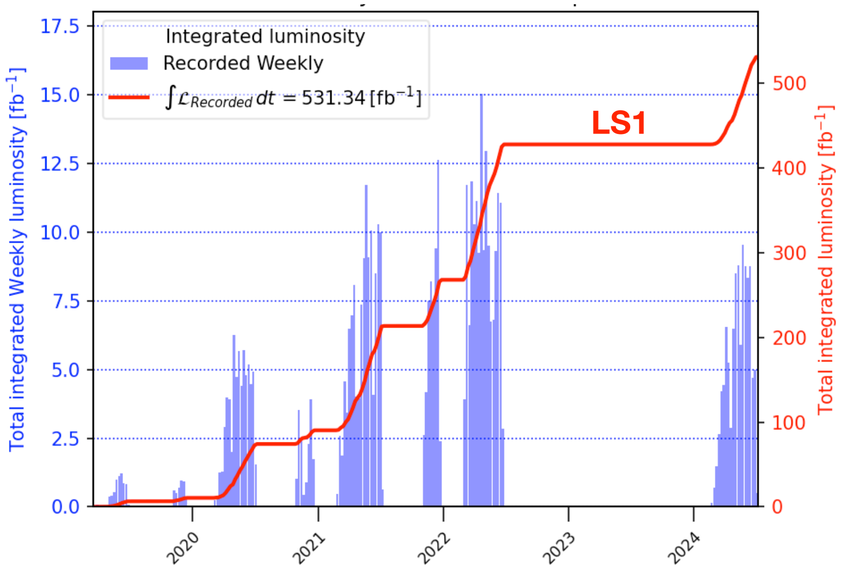
Belle II experiment at SuperKEKB

- Belle II searches for new physics beyond standard model at luminosity frontier
- SuperKEKB collider: asymmetric e^+e^- collisions at $\Upsilon(4S)$ resonance at 10.58 GeV

  ⇒ aims at reaching higher luminosity but with challenging background conditions





Achieved

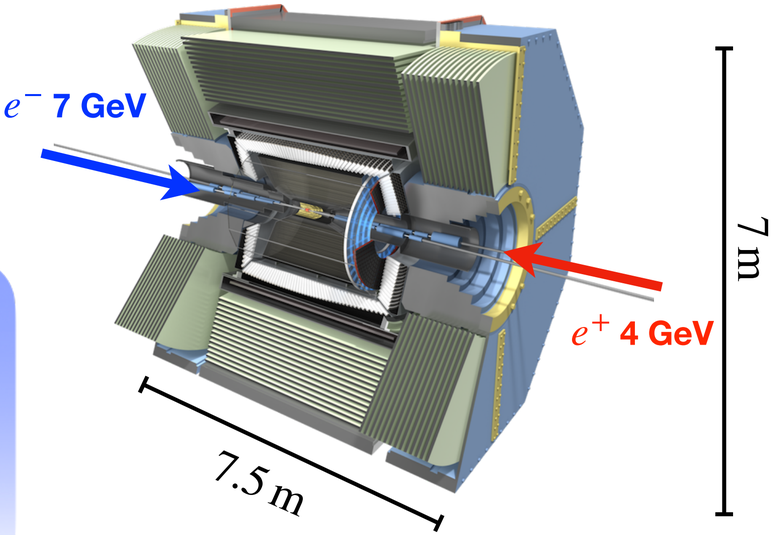
$$\mathscr{L} = 4.7 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$$

$$\int \mathscr{L}\,dt = 530\,\mathrm{fb}^{-1}$$

Target

$$\mathscr{L} = 6 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$$

$$\int \mathscr{L}\,dt = 50\,\mathrm{ab}^{-1}$$



⇒ Require an upgrade of accelerator complex to reach the target luminosity, which may include a major redesign of the Interaction Region (IR)

The current Vertex Detector (VXD)

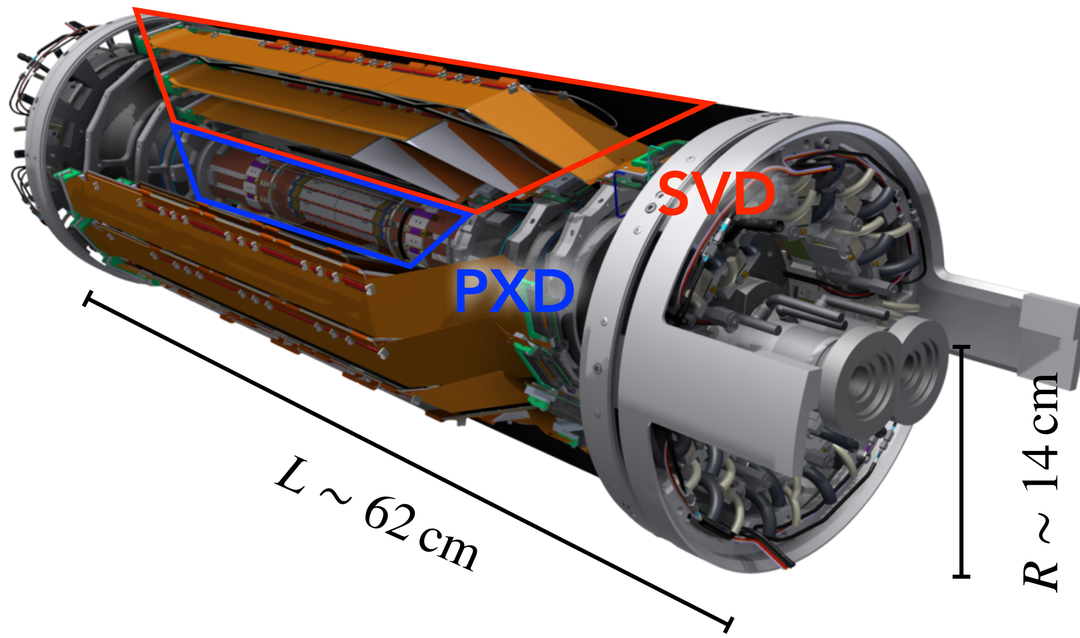
⇒ 2 inner layers of Pixel Detector (PXD) → *talk by F. Becherer*

- **DEPFET pixel** thin sensors (75 μm) & N_2+CO_2 cooling → 0.25% X_0/layer
- Small pitch of 50-70 μm but long integration time of 20 μs
- Occupancy limit 3%
- Cannot contribute to track findings

⇒ 4 layers of Silicon Vertex Detector (SVD)

- **Double-sided strip** 300 μm thick & 2-phase CO_2 cooling → 0.75% X_0/layer
- Excellent time resolution of 3 ns but strip length up to 12 cm
- Occupancy limit 6%, using hit-time for BG rejection
- Trigger latency limited to 5 μs by readout

⇒ *Total material budget of 3.5% X_0*

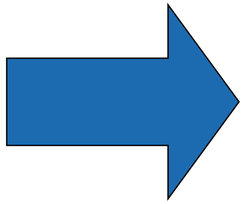


Excellent performance for current occupancy <1%

Upgrade of the Belle II VXD

Motivations for the upgrade

- Large uncertainty on background extrapolation at target luminosity and with a possible upgrade of the IR: 3 possible background scenarios [*ref. CDR*]
- Limited safety margin and performance degradation in high background scenario.
  - PXD layer1: up to 2% occupancy ($32\,\mathrm{MHz/cm^2}$)
  - SVD layer 3 up to 9% occupancy ($9\,\mathrm{MHz/cm^2}$)



Upgrade requirements:

- Hit rate up to 120 MHz/cm^2
- Fast time stamping 50-100ns
- Resolution <15μm → pitch of 30-40μm
- Aiming power dissipation ≤200mW/cm^2
- Operation simplicity and reduced services
- Radiation levels:

  TID ~ 100 Mrad

  NIEL ~ 5×10^{14} neq/cm^2

- At target luminosity we may reach the limits of current detector ⇒ need higher granularity and time resolution in all layers
- Prepare spares in case of accidents or unforeseen degradation

⇒ Depleted Monolitich Active Pixel Sensors (DMAPS)

VTX proposal

Concept = 5 straight layers with DMAPS pixel sensors

- Higher space-time granularity & lower material budget
- Reduce occupancy to improve tracking in high background
- Better tracking & vertex resolution at low momentum
- Adaptable to potential changes of Interaction Region

Technical choices

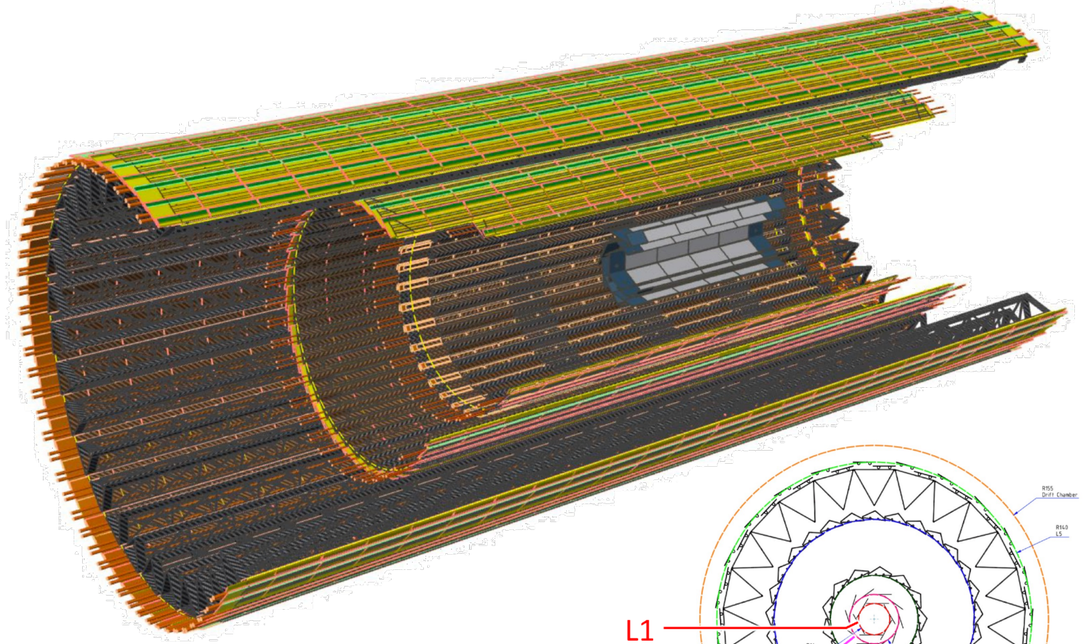
- Identical pixel sensor on all layers:
  Optimized BELle II pIXel (OBELIX) chip
- VTX design → *talk by J. Baudot*:

  iVTX (L1 & L2): all-silicon, self-supported, air cooled
  → 0.2 % X_0/layer

  oVTX (L3 to L5): carbon fiber frame, water cooled
  → 0.3 - 0.8% X_0/layer

  ⇒ Total material budget reduced to 2.4% X_0

Baseline VTX layout with 5 layers



R: 1.4 - 14 cm
max length 70 cm -> 1m

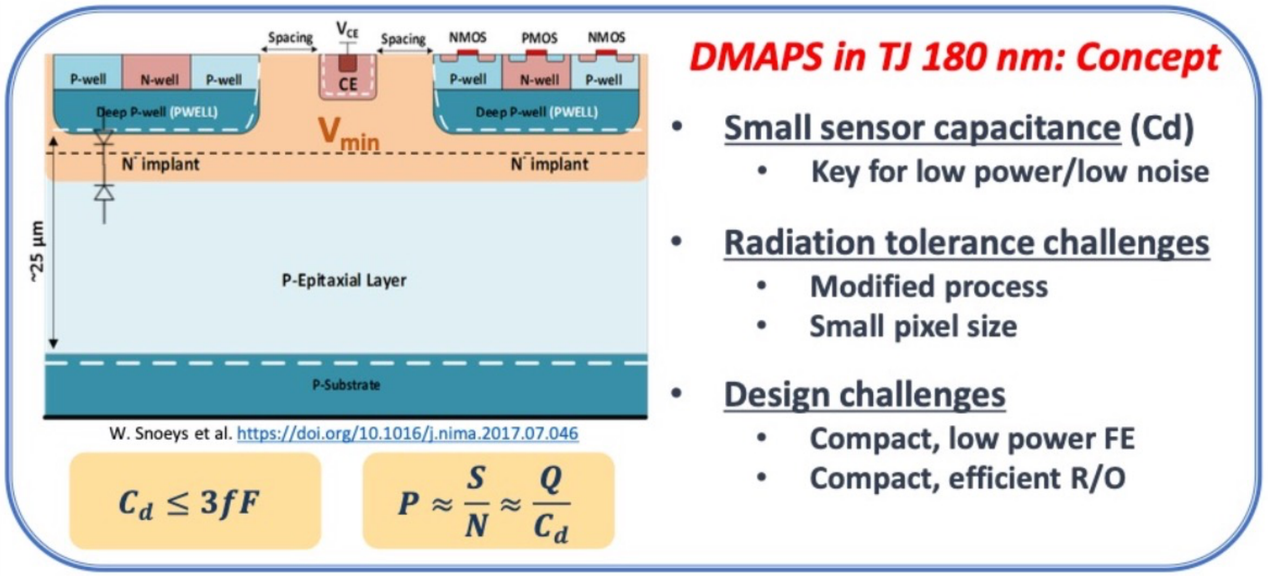
	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	17	40	31	
# Sensors	4	4	7	16	2 x 24	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	% X_0

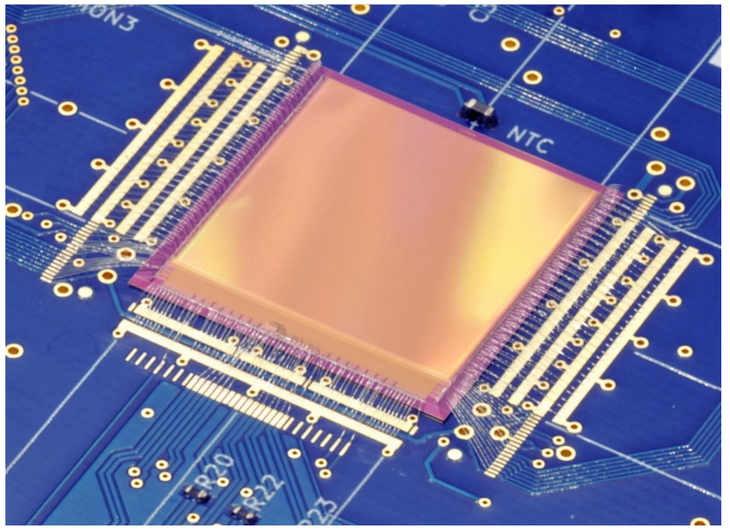
**Large uncertainty on BG extrapolation/possible changes in IR region*

TJ-Monopix2 (TJMP2) as forerunner of OBELIX

Developed for ATLAS (ITK outer layers), DMAPS Tower Semiconductor **180 nm CMOS process** but modified process to improve rad-hardness & faster readout

- 33x33 μm^2 pitch, 25 ns integration, large matrix 512×512 pixels (2×2 cm^2)
- 7 bit ToT information, 3 bit in-pixel threshold tuning
- Column drain readout capable to handle >> 120 MHz/cm^2 → triggerless in TJMP2
- Various sensing volume thicknesses (epi-30 μm, CZ-bulk)
- 4 front-end flavors with differences in the amplifier and detector input coupling (AC or DC)





TJ-Monopix2 sensor bonded on a test board

TJMP2 characterisation in the lab

Detailed characterisation of TJ-Monopix2 (all FE) to validate key performance crucial for OBELIX design

- **Threshold and noise:**

  ⇒ stable operation down to THR~250e^- (MIP signal in 30 μm Si MPV~2500e^-)

  ⇒ THR dispersion 17e^-, Noise ~8e^-

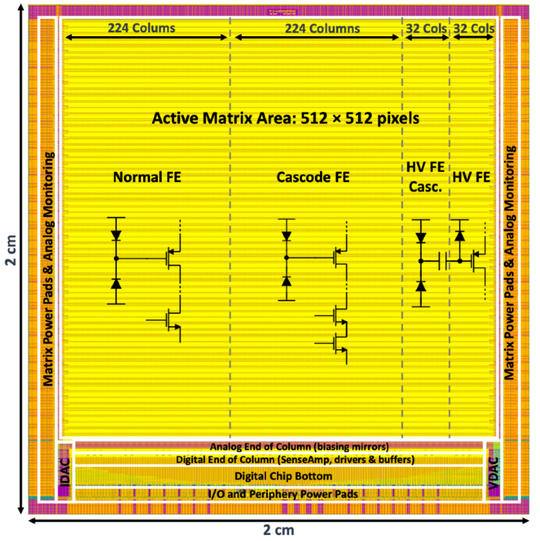
- **Time Over Threshold (ToT) calibration, Fe55**
- **Comparison with measurement and simulations**

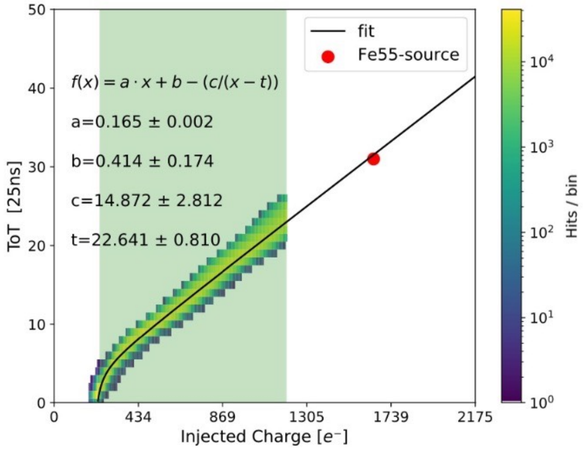
  ⇒ Measurement from monitoring pixels of the analog output signal after the FE amplifier

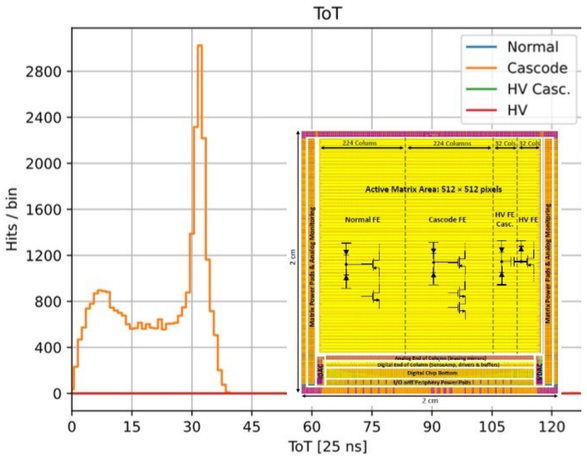
- **Test on p-irradiated sensor ongoing**

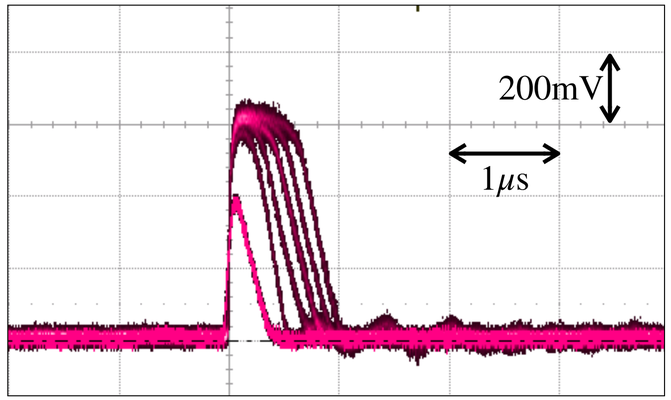
  ⇒ THR and noise evolution with temperature, in-pixel threshold tuning power

Layout of TJMP2 sensor: divided in 4 regions with different FE









DC cascode FE: Signal after the amplifier for different injected charges

TJMP2 Test Beam

Several beam test campaigns (DESY, 3-5 GeV electrons)

- July 2022: non-irradiated sensors and high threshold 500e^- (un-tuned chips)

  → Efficiency ~99% and position resolution ~9 μm

- July 2023: low threshold 250-300 e^- and irradiated sensor $5 \times 10^{14}\,\mathrm{neq/cm^2}$ with 24 MeV protons

  → Confirmed good performance and high efficiency after irradiation, increasing bias

- July 2024: repeat on p-irradiated sensor with high fluence $5 \times 10^{14}\,\mathrm{neq/cm^2}$ & TID 100 Mrad

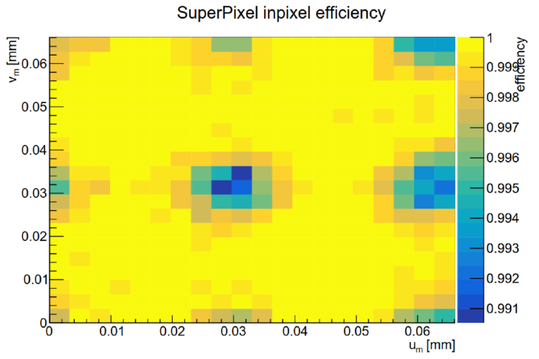
  → *TID 100Mrad*: both DC and AC cascode efficiency 99.9%

  → *NIEL* $5 \times 10^{14}\,\mathrm{neq/cm^2}$: slightly worse efficiency than in TB 2023 (effect of higher T and higher leakage current is the explanation)

  - DC cascode efficiency>99.5% but ~3% of masked pixels
  - AC cascode efficiency ~98.5%

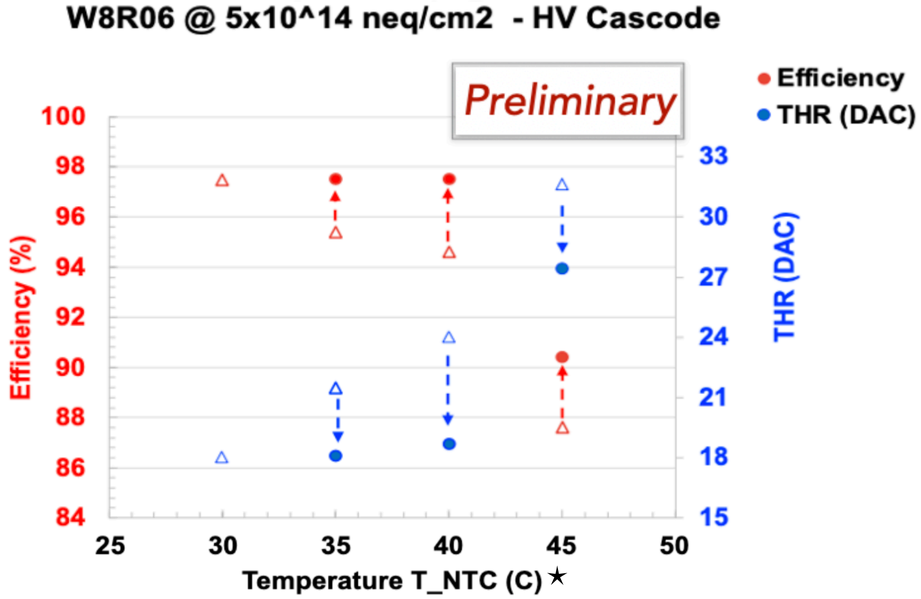
Results TB July 2023

FE amplifier	Coupling	Efficiency [%]
Normal	DC	99.99
Cascode	DC	99.79
Normal	AC	98.11
Cascode	AC	99.13



Results TB July 2024

After p-irradiation, with chip temperature $\geq 40\,\mathrm{C}$ (T_{room}), both threshold and noise increase, with a drop in efficiency.



★ chip temperature ~10/15°C higher than NTC temperature

TJMP2 Test Beam

Several beam test campaigns (DESY, 3-5 GeV electrons)

- July 2022: non-i
(un-tuned chips)
→ Efficiency ~99
- July 2023: low
5×10^{14} neq/cm
→ Confirmed g
irradiation, increa
- July 2024: repe
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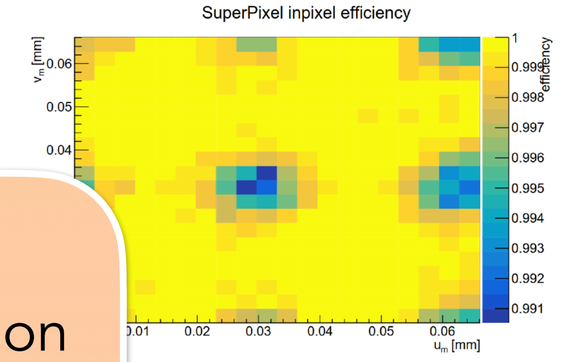
→ *TID 100Mrad*:
→ *NIEL* 5×10^{14} n
(effect of higher T
  - DC cascode efficiency>99.5% but ~3% of masked pixels
  - AC cascode efficiency ~98.5%

- Several cooling options for iVTX now under evaluation considering OBELIX power consumption with high hit rate & performance deterioration with high Temperature after irradiation with NIEL fluence of $5 \times 10^{14}\,\mathrm{neq/cm^2}$

⇒ Another TB planned for 2025 to explore lower temperature ranges and study the performance for irradiated sensors at different NIEL fluences

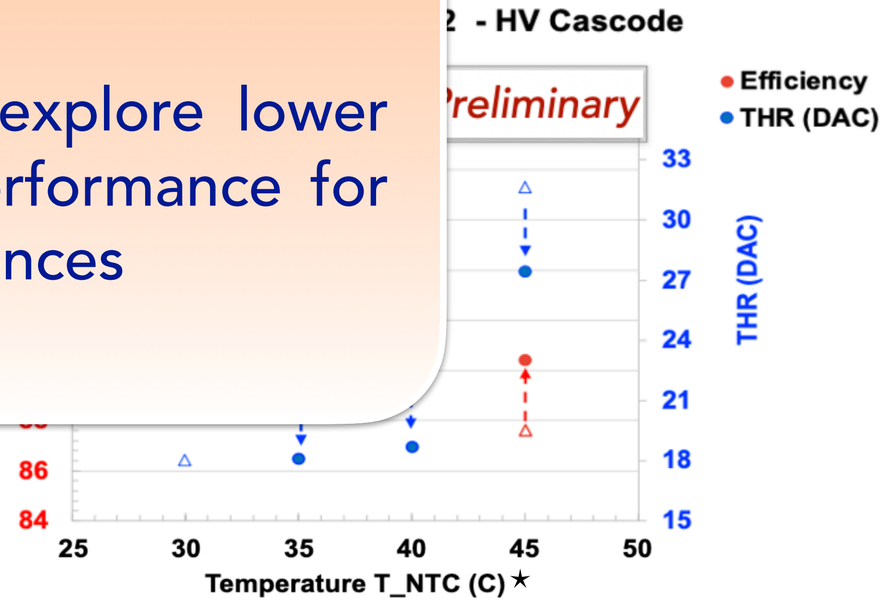
Results TB July 2023

FE amplifier	Coupling	Efficiency [%]
Normal	DC	99.99



2024

temperature ≥ 40 C
noise increase, with a

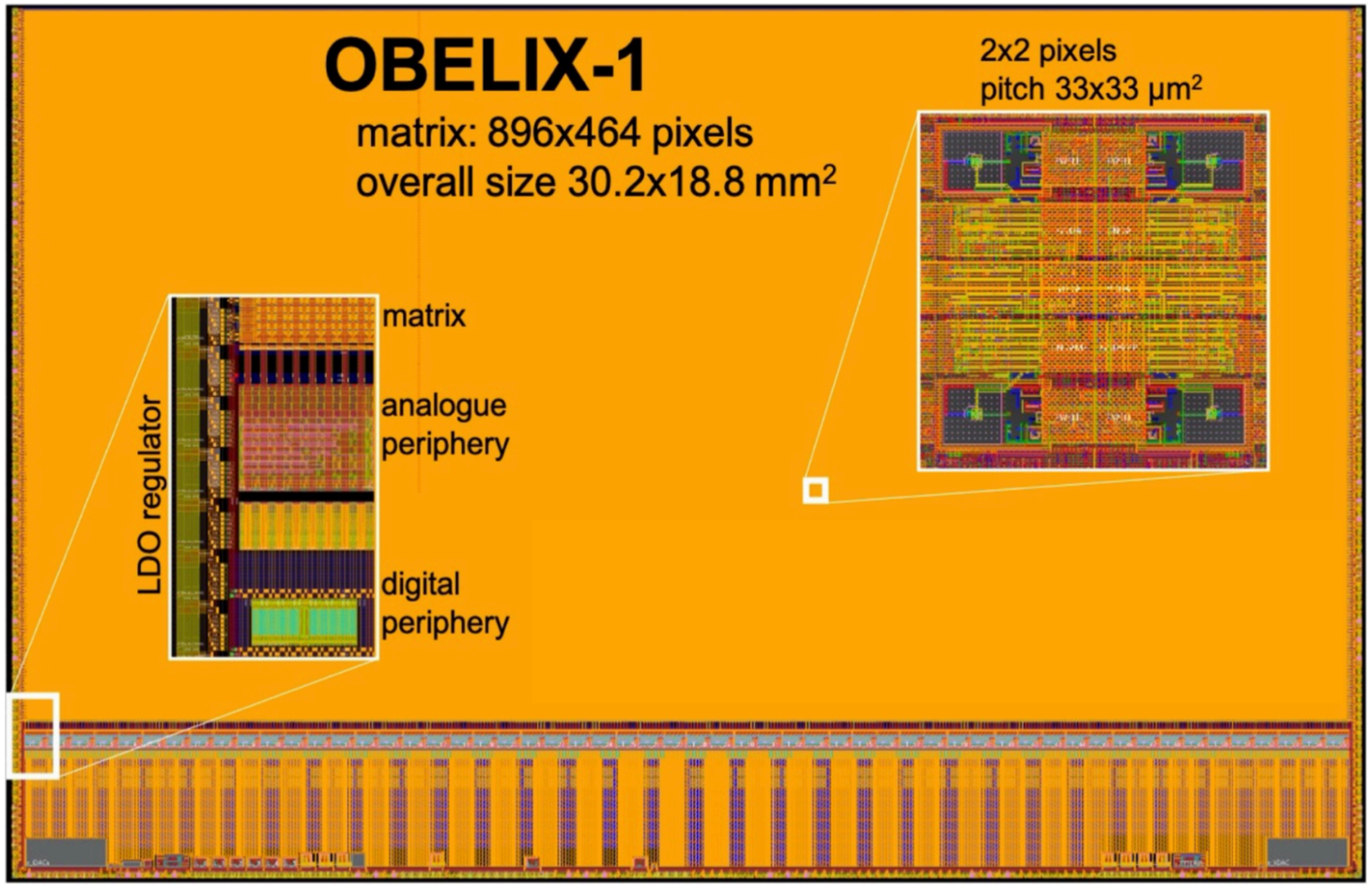


★ chip temperature ~10/15°C higher than NTC temperature

OBELIX specifications

Pitch	33 μm
Signal ToT	7 bits
Time stamping	50 to 100 ns
Fine time * stamping	~5 ns for hit rate <10 MHz/cm²
Hit rate max for 100% eff.	120 MHz/cm²
Trigger handling	30 kHZ with 10 μs delay
Trigger * output	~10 ns resolution with low granularity
Power (with hit rate)	200 to 300 mW/cm² (1 to 120 MHz /cm²)
Bandwidth	1 output 320 MHz

** optional features*



Matrix inherit from TJ-Monopix2, size adjusted

⇒ Values obtained from post-layout simulations

OBELIX sensor design

- Based on current characterisation results on TJMP2, 2 FE flavors are chosen for OBELIX on equal area
- OBELIX design with new digital periphery with trigger logic for Belle II and optional features to allow Track Trigger capability and finer time-stamping for outer layer hits (low rate)
- First full scale prototype OBELIX-1sensor ~ ready submission in spring 2025

Analog:

- Column drain architecture from TJ-Monopix2
- Monitoring ADC
- Temperature sensors

Power pads:

- On-chip LDOs voltage regulators

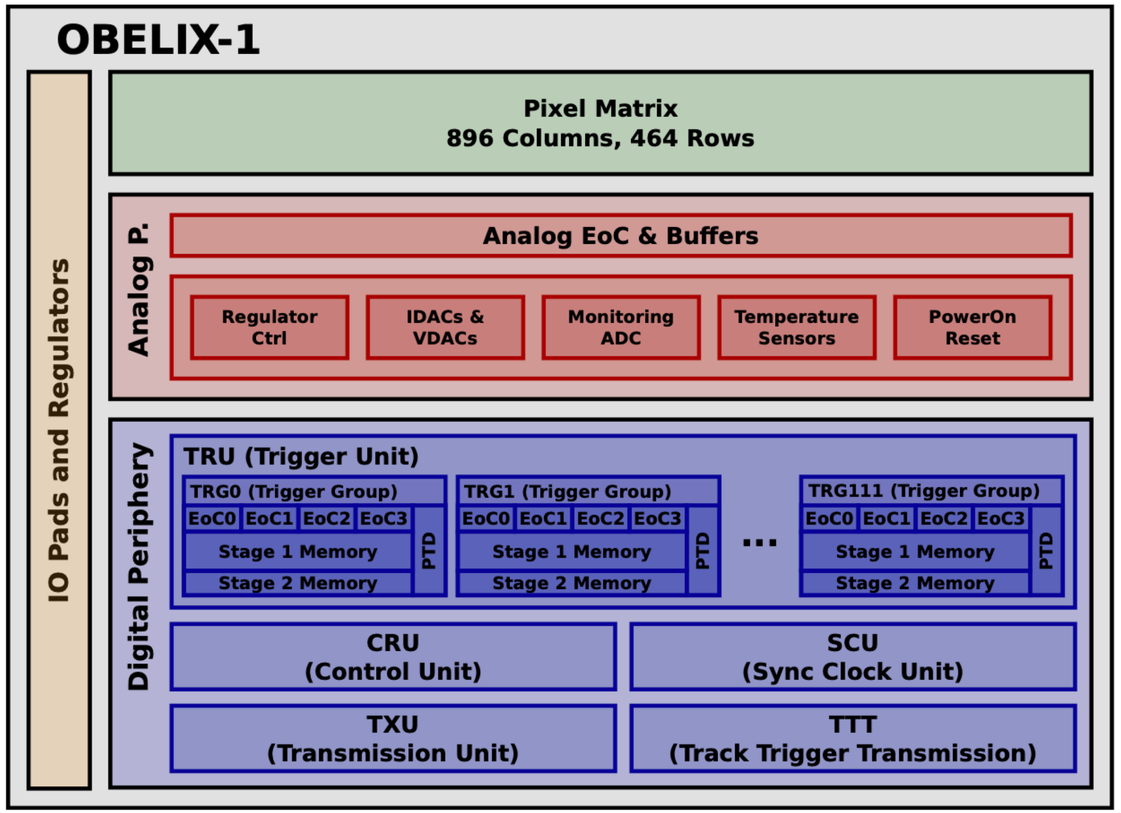
Digital periphery:

- Two new modules adapted for Belle II trigger:

  ⇒ TRU: Pixel readout, trigger processing

  ⇒ TTT: Fast transmission in parallel

OBELIX functional block diagram



Summary

- SuperKEKB will need an upgrade to reach the target luminosity $6 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, including a possible major redesign of the Interaction Region (IR)
- Current VXD has excellent performance now, but limited safety margin in the high BG scenario

  ⇒ upgrade vertex detector (VTX) based on DMAPS pixels, more performant and resilient against higher background
- OBELIX sensor based on TJMP2 matrix with new digital periphery
- Lab testing and TB campaigns on TJMP2 to validate key performance crucial for OBELIX design
- First full scale prototype OBELIX-1sensor ~ ready submission in spring 2025

VTX collaboration

IGFAE, Santiago
University of Bergamo
IUniversity of Bonn
University of Dortmund
University of Göttingen
Jilin University
KIT, Karlsruhe
IPMU, Kashiwa
Queen Mary University of London
CPPM, Marseille
IJCLab, Orsay
RAL, Oxford
INFN & University of Pavia
INFN & University of Pisa
IFCA (CSIC-UC), Santander
IPHC, Strasbourg
University of Tokyo
KEK, Tsukuba
IFIC (CSIC-UV), Valencia
HEPHY, Vienna

BACKUP

iVTX

All-silicon module < 0.2% X_0/layer

- 4 contiguous OBELIX sensors diced as a block from the wafer, thinned to 50 μm, except in some border area ~400 μm thick, to ensure stiffness
- Post-process redistribution layer for interconnection

Prototypes:

- Thermal and electrical tests on first real-size ladder with resistive heaters and two redistribution layers

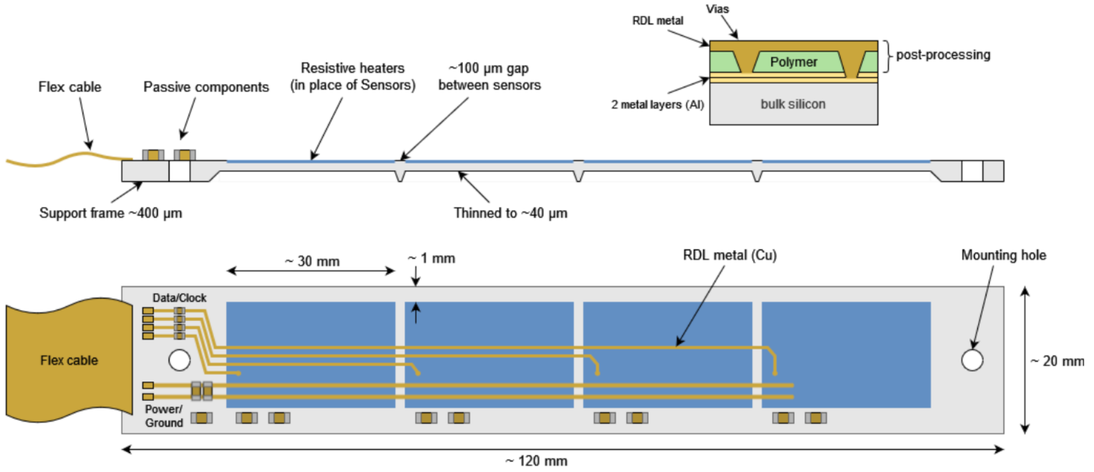
  ⇒ temperature on top of metal layers of 53°C for 1.5 W dissipated/sensor

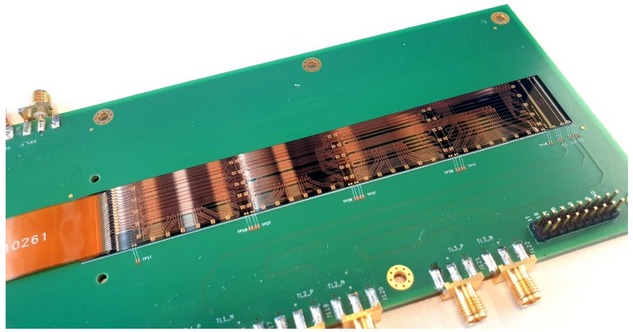
Preliminary cooling simulation results

- Non uniform power: matrix ~100 mW/cm^2, digital periphery depending on hit rate

  ⇒ average power ~ 300 mW/cm^2 @ hit-rate of 120MHz/cm^2
- Air cooling alone might be marginal

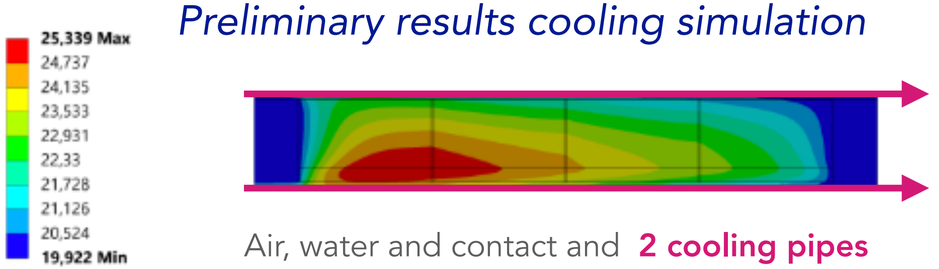
  ⇒ several cooling options under evaluation, based on power consumption and chip temperature limits (both max temperature and temperature gradient in the matrix)





iVTX ladder demonstrator tested

Preliminary results cooling simulation



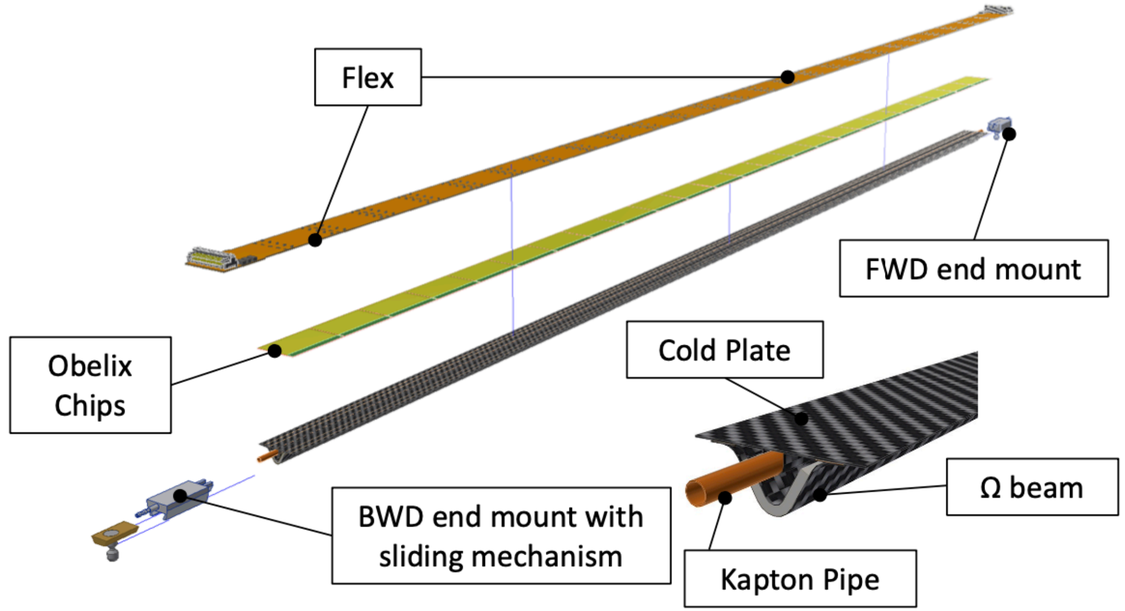
Air, water and contact and **2 cooling pipes**

	Max T [°C]	T range [°C]
Contact + air	49	29
Contact + water	26	6
Contact+air+water	25	5

oVTX

Ladder structure (ALICE ITS2-inspired):

- Carbon Fiber support structure (Ω beam), cold-plate with pipes (2 or 1 pipe) with liquid cooling
- Sensor glued on cold plate, flex cables connecting each half ladder

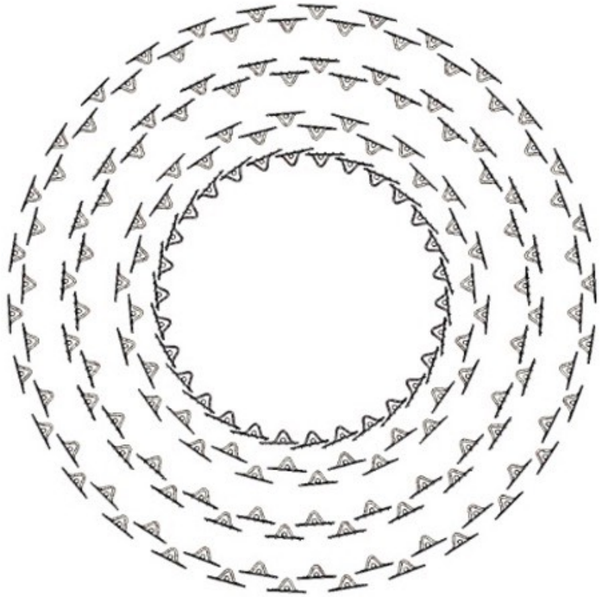


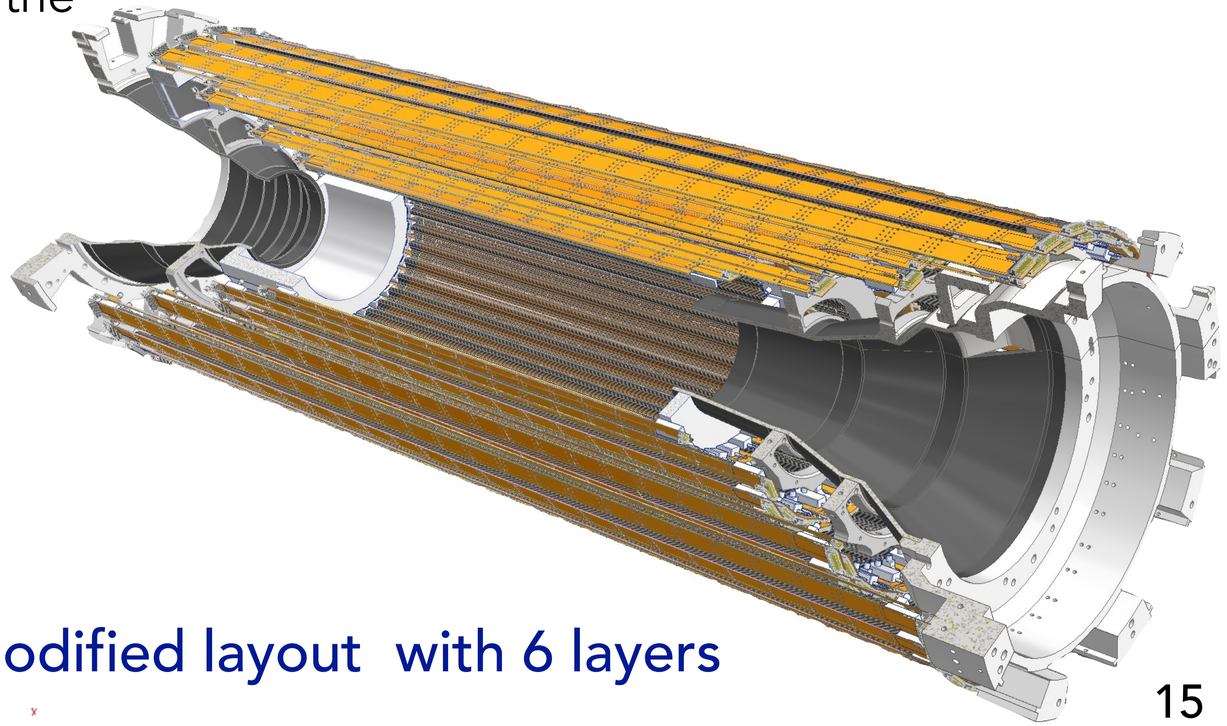
Prototypes:

- Mechanical and thermal characterisation done for the longer ladder ~70 cm (outermost layer)

Mechanical design already advanced:

⇒ now also exploring a 6 layers option, with more compact ladder design





Modified layout with 6 layers

TJMP2 Test Beam

Several beam test campaigns (DESY, 3-5 GeV electrons)

- July 2022: non-irradiated sensors and high threshold 500 e^- (un-tuned chips)
  → Efficiency ~99%
  → Position resolution ~9 μm

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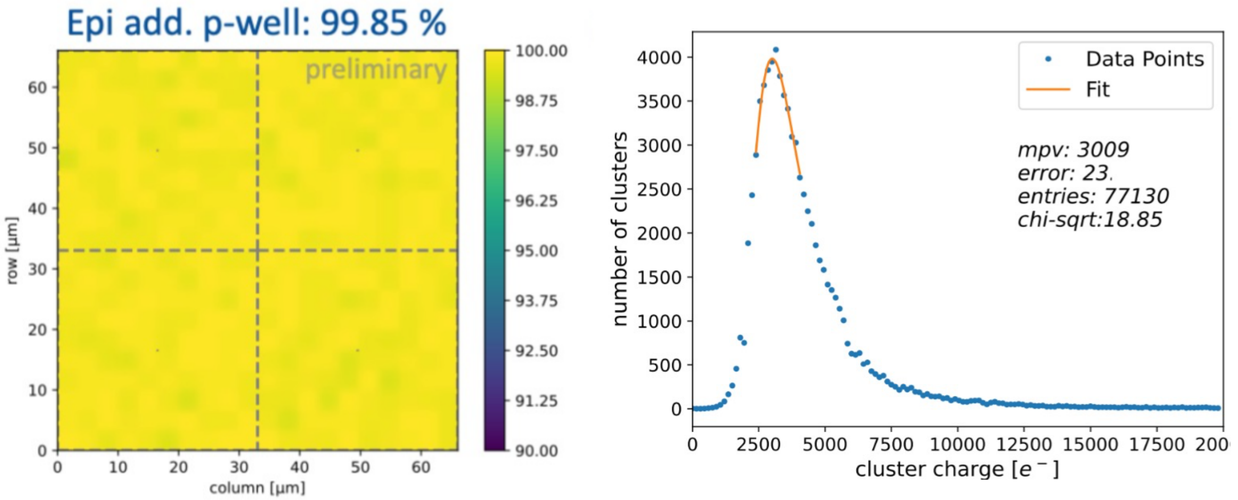
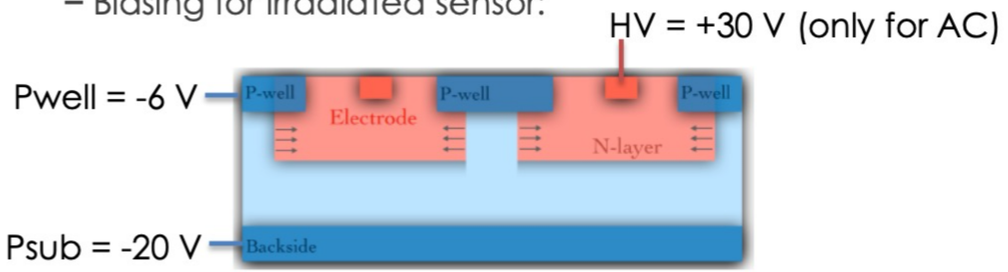
  → Confirmed good performance and high efficiency after irradiation, increasing bias

Results TB July 2022



– Biasing for irradiated sensor:



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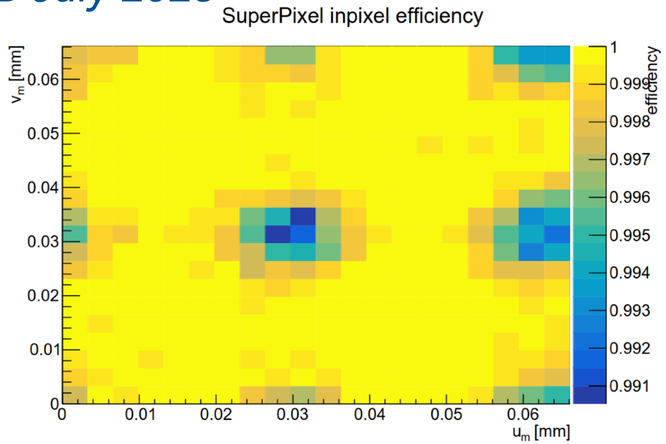


TJMP2 Test Beam

Results TB July 2024

- July 2024: repeat on p-irradiated sensor with high fluence 5×10^{14} neq/cm^2 & TID 100 Mrad

  → TID 100Mrad results

  ▸ Both DC and AC cascode: efficiency 99.99%

  → NIEL 5×10^{14} neq/cm^2 results slightly worse than in TB 2023 (effect of higher T and higher leakage current is the current explanation)

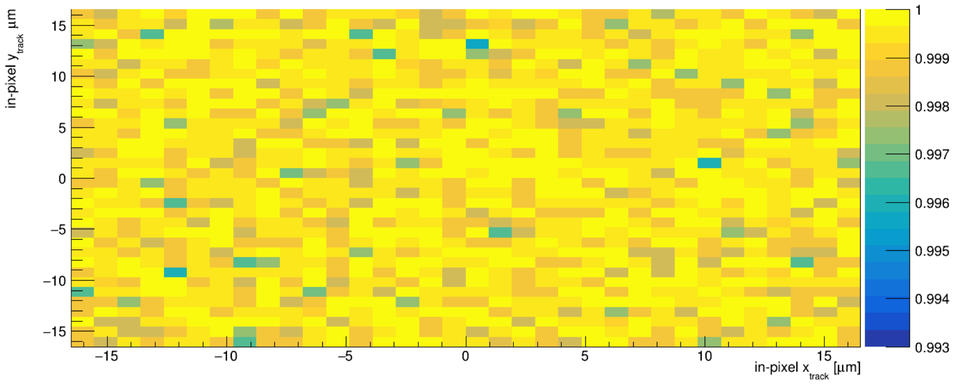
  ▸ DC cascode FE: efficiency>99.5% but with ~3% of masked pixels

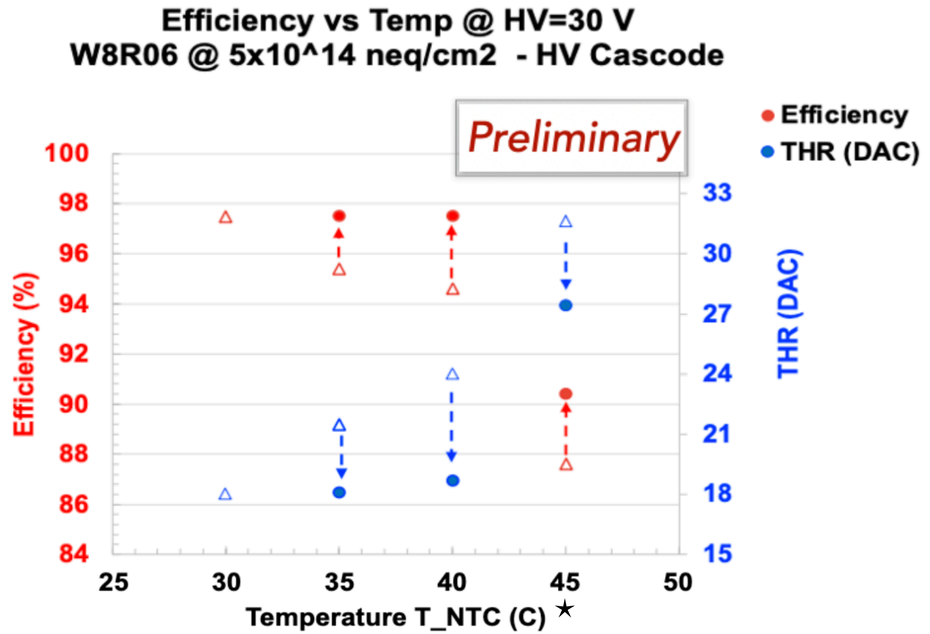
  ▸ AC cascode FE: efficiency ~98.5%

  → After p-irradiation, with chip temperature $\geq 40\,\mathrm{C}$ (T_{room}), both threshold and noise increase, with a drop in efficiency

  → Possible tuning to reduce threshold but less powerful at higher temperature

TID - inpixel efficiency HV cascode





★ chip temperature ~10/15°C higher than NTC temperature