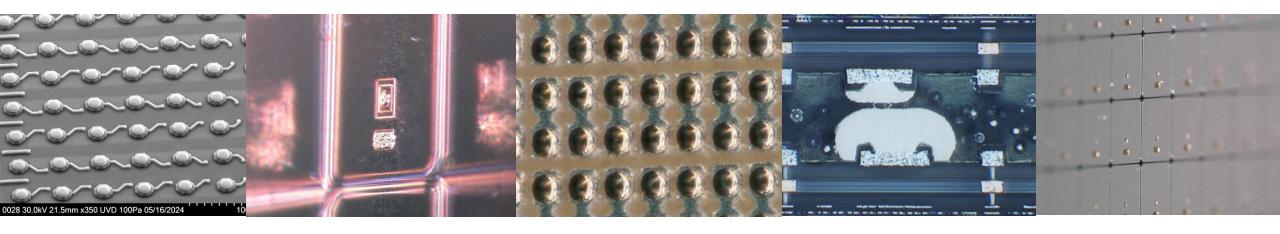


Pixel detector hybridization with ACA Anisotropic Conductive Adhesives



PIXEL 2024

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- 1: CERN 2: Hamburg University 3: LPNHE-Paris, Centre National de la Recherche Scientifique
- 4: Universite de Geneve 5: KIT Karlsruhe Institute of Technology 6: FBK

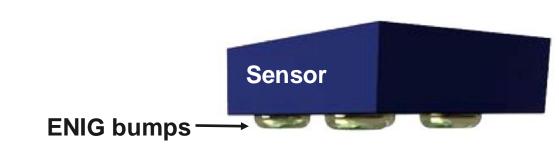
Introduction

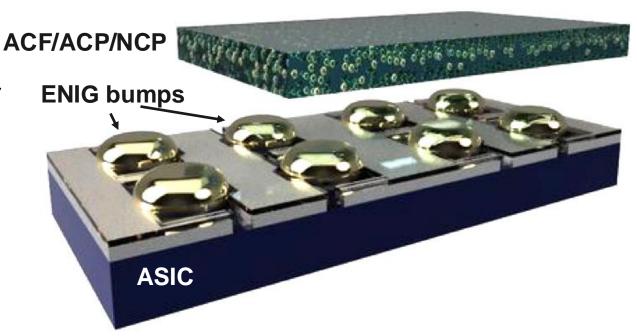
Development of an in-house module hybridization technique in two main steps:

- Creation of bumps on the pads of Sensor and ASIC with ENIG plating
- 2. Flip-chip assembly with an anisotropic conductive layer or non-conductive layer between the chips

Advantages:

- Single die processing
- Adaptable to the application
- Low temperature process
- Maskless
- In-house (short turnaround time, quick adjustments)





- ENIG: Electroless Nickel Immersion Gold
- ACF: Anisotropic Conductive Film
- ACP: Anisotropic Conductive Paste
- NCP: Non-Conductive Paste

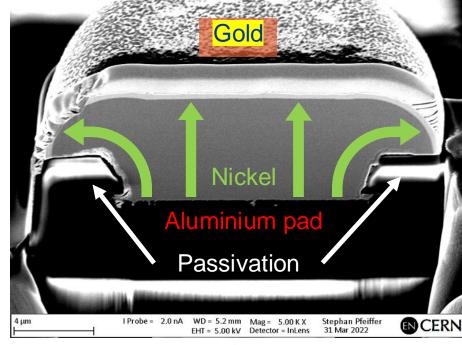


1) Creation of bumps on the pads of chips with ENIG plating

Introduction

3 main steps for Electroless Nickel Immersion Gold (ENIG) plating:

- 1. Pre-treatment and zincation of the aluminium pad
- 2. Electroless Nickel deposition (creation of the bump)
 - Self-catalytic reaction on pad surface, bump height controlled by immersion time
- 3. Immersion Gold
 - Corrosion protection, bondable surface, very thin layer (< 1 μm)



FIB cross-section of an ENIG bump on an aluminium pad

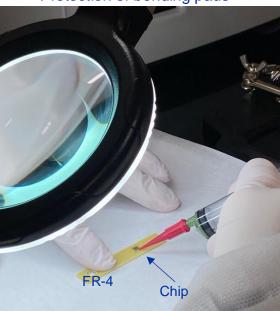


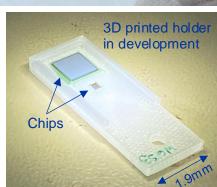


Sample preparation

Samples preparation:

- Gluing the chip on holder
- Protection of bonding pads





Challenges for the preparation of small-sized chips (handling, gluing, protection of bonding pads)





Development of a microdispenser

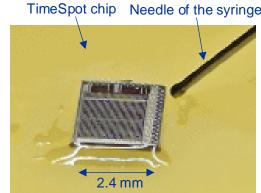










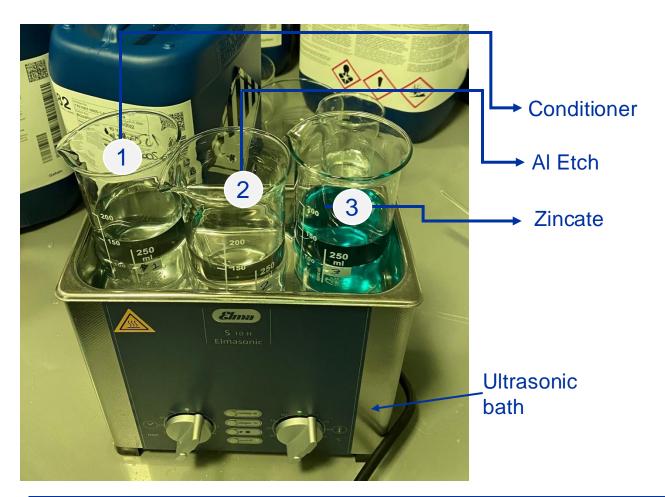


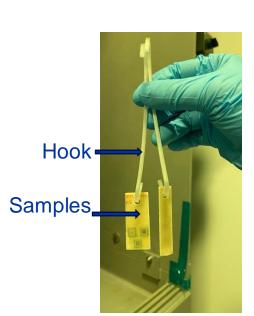




Pre-treatment setup

<u>Pre-treatment</u>: ultrasound + manual movements





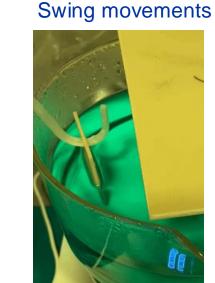


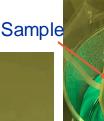




Nickel Plating setup







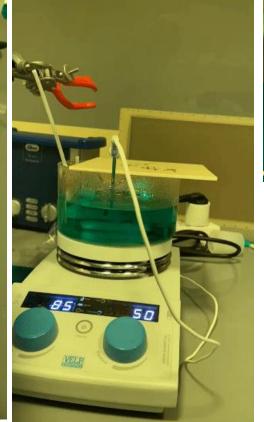
Sample

Stirring magnet

Hook-

Sample

Hot plate



Bubbles removal from surface of chip



Frequent calibration

- pH metre
- Temperature probe
- Micropipette



Avoiding crosscontaminations









ENIG plating results on test structures

Timepix3 type daisy-chain test structures, 22x22 µm pads and 55 µm pitch

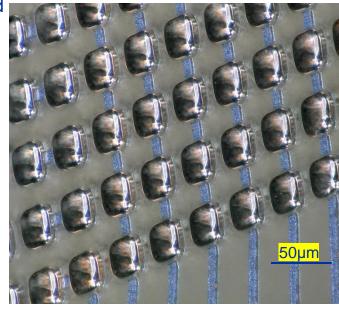


Timepix 3 type daisy-chain device test structure (14x14mm)

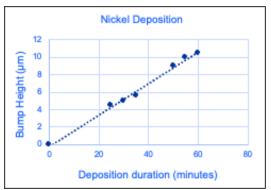
Good bump homogeneity

Excellent ENIG results:

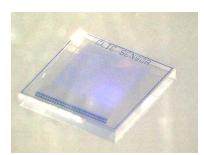
55min deposition



>99% of 65536 pads correctly Bumps height: $10 \mu m (\pm 0.5 \mu m)$



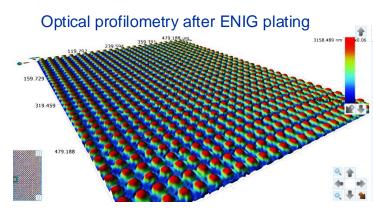
Small pitch/small pads test structures, 20 µm pitch, 10x8 µm rectangular pad size (High connection density)



Small pitch/small pads test structures test structures (3.2x3.2mm)

Excellent ENIG results:

- Good bump homogeneity
- >99% of 16384 pads correctly plated
- Bumps height: 4.5 µm (± 0.2 µm) 25min deposition







plated



TimeSpot ASIC Functional chip 55μm pitch, <u>19μm</u> pads

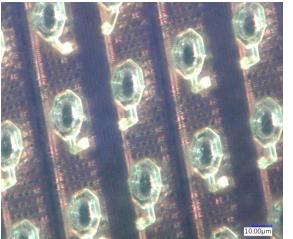
Excellent ENIG results:

- 100% of pads correctly plated (1184 pads)
- Pads height: 10 µm $(+/-0.5 \mu m) 1h$ deposition

Collaboration with INFN Cagliari (Angelo LOI, Adriano

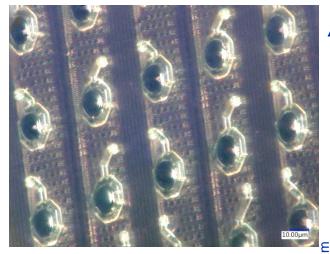
https://web.infn.it/timespot/

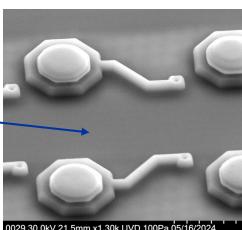
Before plating, optical microscope



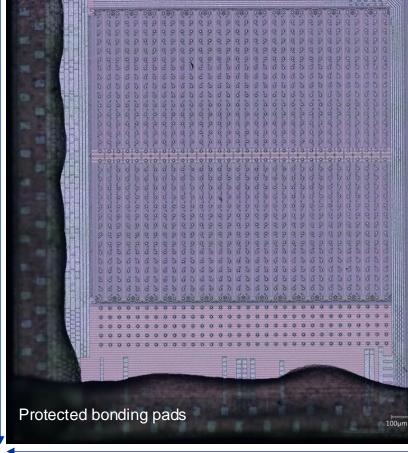
After plating, SEM

After 1h plating, optical microscope











2.4 mm



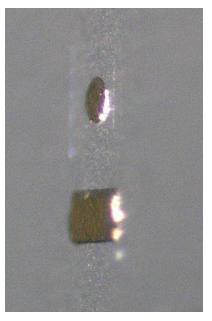


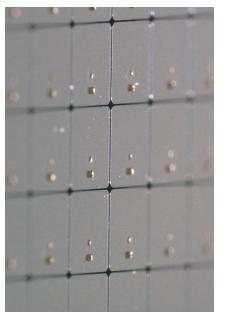
ATLAS HGTD LGAD sensors <u>Functional chips</u> 1.3mm pitch, 90 µm diameter pads

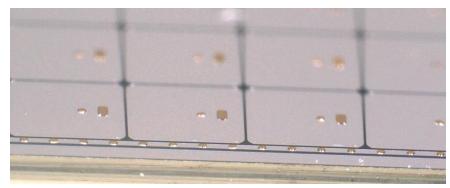
Good ENIG results:

- Homogeneity of bumps achieved with no overplating
- No skipped pads
- Bumps height: 8.5 μm (± 0.7 μm) (1h deposition)

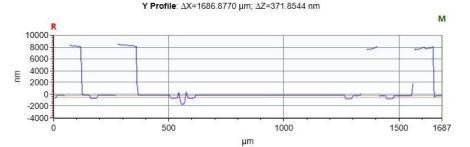
Optical microscope, 62° tilt

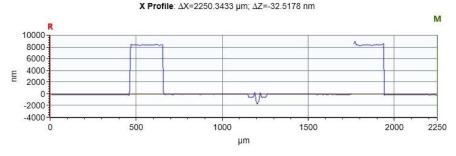


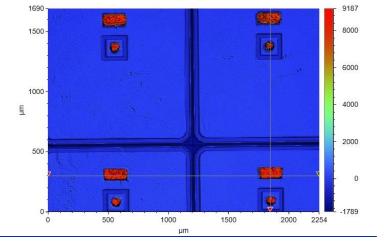




Optical profilometry after ENIG plating











KEK AC-LGAD Sensors and ASICs

Functional chips 100 µm pitch, 40 µm diameter pads

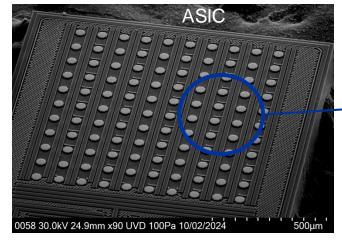
Good ENIG results:

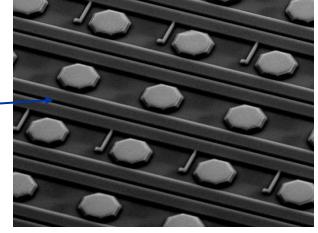
- Homogeneity of bumps achieved with no overplating
- No skipped pads
- Bumps height: 8.5 μm (± 0.6 μm)

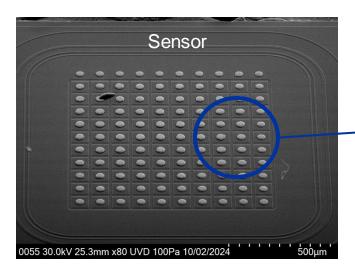
Collaboration with KEK (Koji NAKAMURA) and University of Geneva (Lorenzo PAOLOZZI)

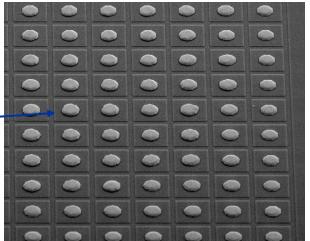
Tomoka Imamura, Sayuka Kita, Koji Nakamura, and Kazuhiko Hara, "Development of HPK Capacitive Coupled LGAD (AC-LGAD) detectors", PoS, vol. VERTEX2023, pp. 032, 2024

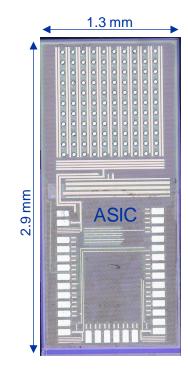


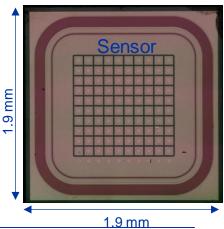
















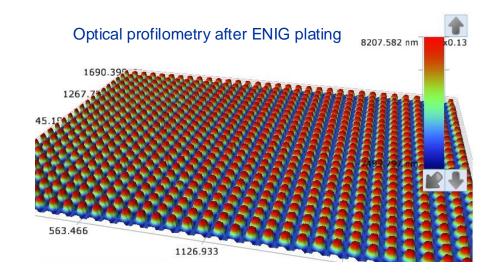
ColorPix2 <u>Functional</u> chips 70 µm pitch, 40 µm pads

Good ENIG results:

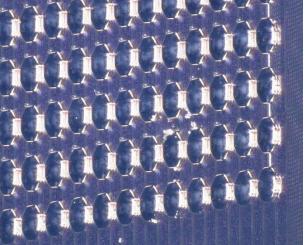
- Homogeneity of bumps achieved with no overplating
- No skipped pads
- Bumps height: 11 μm (± 0.5 μm) 1h deposition

"Color imaging of Xrays", FNSPE CTU in Prague

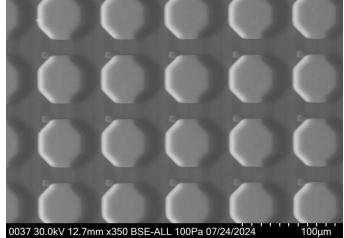
https://indico.cem.ch/event/829863/contributions/5053901/attachments/2567463/4426692/PIXEL2022_poster.pdf



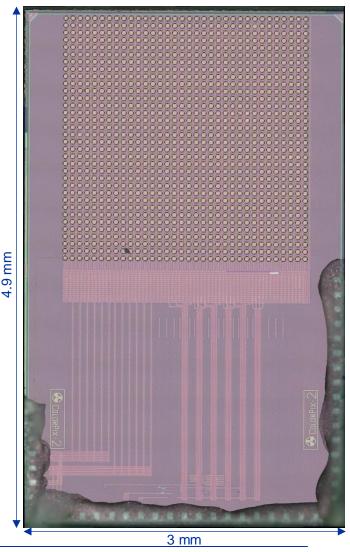
Optical microscope, 61° tilt



After plating, SEM



Optical microscopy after ENIG plating







Conclusion for ENIG plating

Optimised ENIG plating:

- Reproducibility
- Almost no skipped pads
- No overplating
- Uniformity (even at the edge of the chips)

Tested on different configurations:

- High pad density (20 μm pitch) and small pads (10 μm)
- Low pad density (1.3 mm pitch) and large pads (90 μm)
- Successful plating of functional chips TimeSpot, ColorPix,
 KEK AC-LGAD ASICs and sensors, and LGAD sensors for ALTIROC3

	Pad size	Pitch	ENIG height	Chip size
"Timepix3" daisy-chain test structures	12-22 µm	55 µm	10 μm	14x14 mm
"Small pitch" daisy-chain test structures	10x8 µm² (rectangular)	20 μm	4.5 μm	3.2x3.2 mm
TimeSpot ASIC	19 µm	55 µm	10 µm	2.4x2.7 mm
ATLAS HGTD LGAD sensors	90 µm	1.3 mm	8.5 µm	20x22 mm
KEK AC-LGAD Sensor and ASIC	40 μm	100 μm	8.5 µm	ASIC 1.3x2.9 mm Sensor 1.9x1.9 mm
ColorPix2	40 µm	70 µm	11 µm	3x4.9 mm





2) Flip-chip assembly



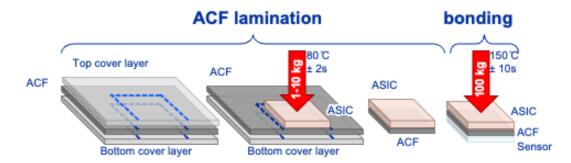
Bonding with Anisotropic Conductive Adhesive (ACA)

Bonding done at Geneva University using semi-automatic flip-chip bonder

- Precise temperature, pressure and alignment control
- Heating up to 400°C and force applied up to 100 kgf
- Available for bonding with Anisotropic Conductive and Non-conductive Film/Paste ACF/ACP or NCF/NCP

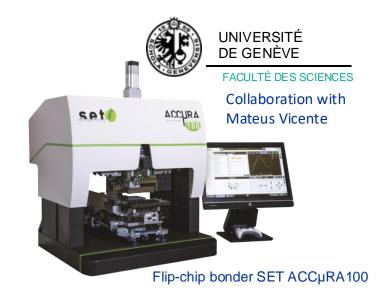
ACF bonding has two steps: lamination and bonding

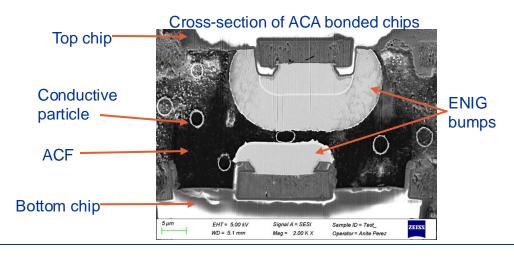
- ACF lamination at 80°C, ≈ 5 kg/cm2
- Bonding at 150°C, ≈ 50 kg/cm2



ACP bonding has three steps:

- Mixing the micro-particles with the liquid adhesive
- Dispensing the mix on the bottom chip
- Flip-chip bonding

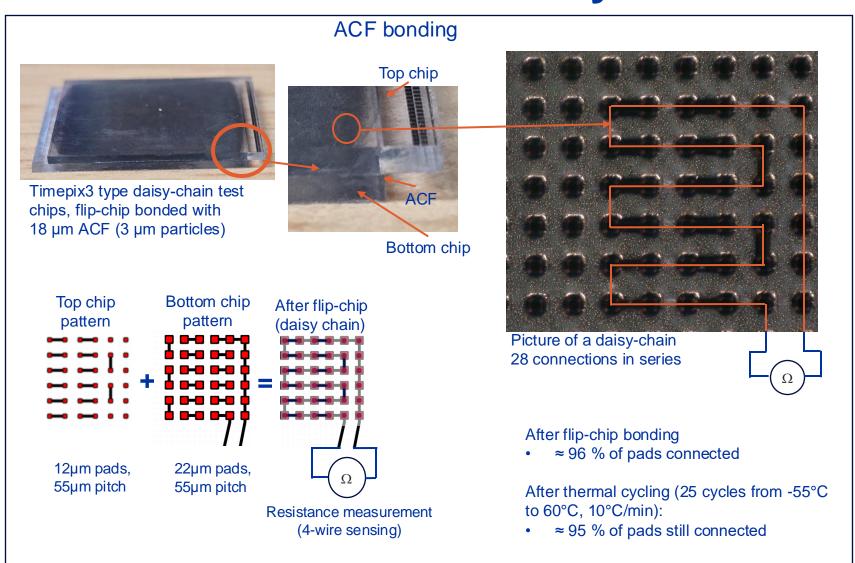








Characterisation of daisy-chain test structures

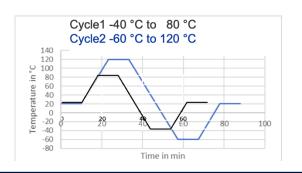


ACP bonding

Daisy-chain test chips with 10x10 connections, 300 µm pads, 1 mm pitch, flip-chip bonded with ACP (20 µm Ag particles)



- · 97.1 % of pads connected
- After thermal cycling (20 cycles from -40°C to 80°C): 94.5 % pads still connected
- After thermal cycling (20 cycles from -60°C to 120°C): 91.7 % pads still connected



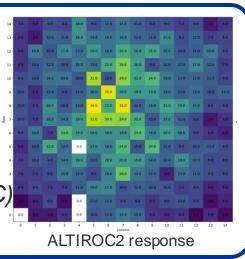




Hybridisation and characterisation of functional chips

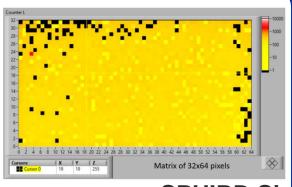
ALTIROC2/3

- 15x15 pixels, 1300 µm pitch
- LGAD sensor
 - ACP with 10 µm particles
 - 98.2% yield
 - Tested by A. Wang (USTC)



SPHIRD

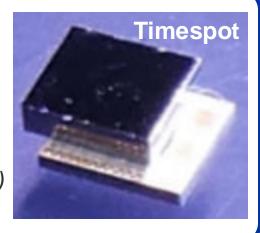
- 32x64 pixels, 50 µm pitch
- Si planar sensor
 - ACF 14 µm thick
 - 85% yield (+7% weak response)
 - Tested by M. Ruat (ESRF)



SPHIRD Si response

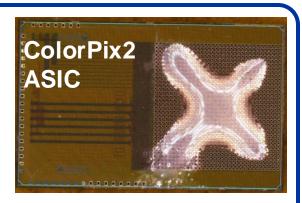
Timespot

- 32x32 pixels, 55 µm pitch
- Si 3D trench sensor
 - ACF 18 µm thick
 - 85% yield
 - Provided by A. Loi (INFN)



ColorPix2

- 32x32 pixels, 70 µm pitch
- CZT sensor 1.8 mm thick
 - NCP
 - around 70% yield
 - Tested by J. Jirsa (FNSPE CTU)





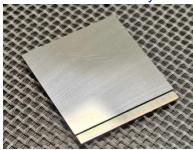


Gold-stud hybridisation of ALTIROC3/A and LGAD sensors

- Using ALTIROC3/A ASICs and LGAD sensors from ATLAS High-Granularity Timing Detector (HGTD) to develop new in-house bonding process for sensor and ASIC qualification
- Single and stacked double gold studs used for the connections between the chips, epoxy underfill for bonding
- Used for radiation-hardness qualification of LGAD sensors
- Low temperature process (60°C) to avoid uncontrolled annealing

Process tested with unirradiated and irradiated sensors, excellent interconnect yield achieved for both single and double gold studs. Impact of thermal cycling on interconnects to be studied.

ALTIROC/LGAD Hybrid



Gold stud

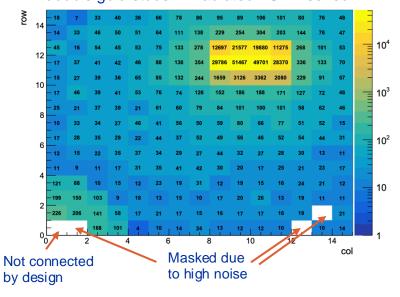


Pictures from Hybrid SA



Preferred this solution to increase the gap between ASIC and sensor from 20 µm to 35 µm and thereby decrease coupling between them

Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor



Confirmation of good inter-connection with occupancy map (≈ 100%)

Gold-stud hybridisation process suitable for large pitch (>100µm), large pads (>80µm) chips



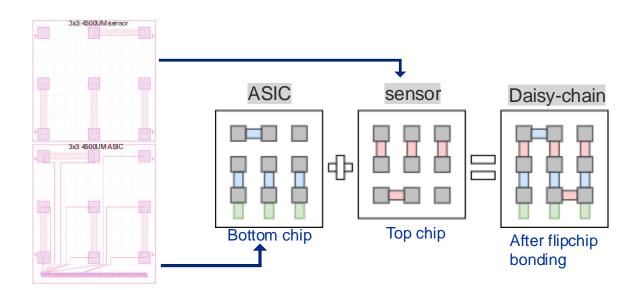


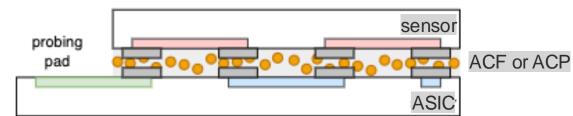
Conclusion

- Optimised ENIG plating tested on many different configurations
 - Dummy test chips, functional chips, with different pad size, pitch, chip size...
- Different approaches studied for hybridisation
 - ACF, ACP, NCP, Gold Studs
- Successful flipchip bonding of different chips with different sizes
 - Optimisation of bonding parameters (pressure, time, temperature)
- Reliability tests in climate chamber (ongoing)
 - Good results for both the ACF and the ACP



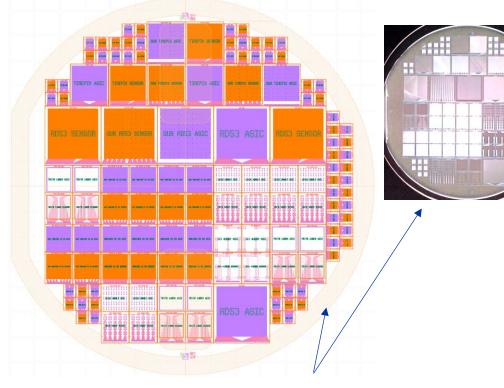












Daisy chain devices produced at FBK

Designed to validate interconnect yield, electrical resistance, thermo-mechanical stress

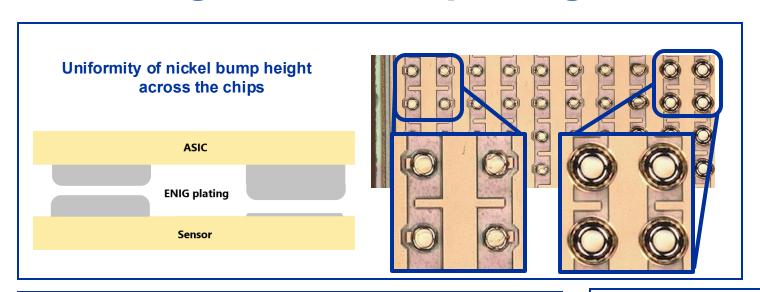
- 6" glass wafers, 625 µm thick
- Varying Bonding area, pad size and pitch, matching different target applications

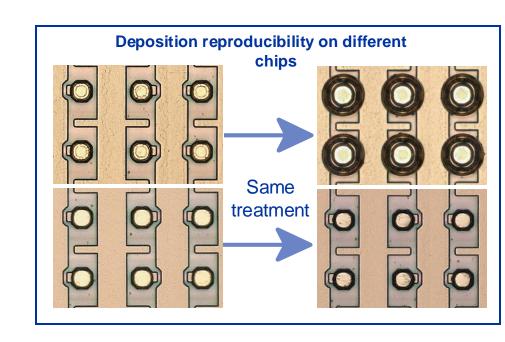
https://zenodo.org/records/7310324

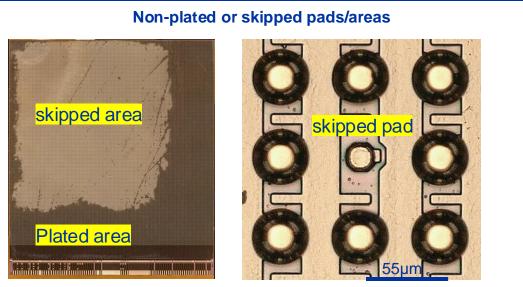


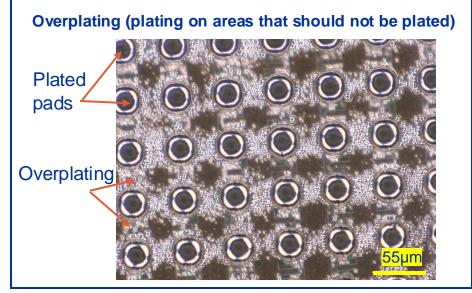


Challenges of initial platings









ENIG plating on high connection density chips (ex: CLICpix2, 12µm pads; 25µm pitch) !!





Characterisation of ENIG plating

Keyence optical microscope Optical profilometer Mechanical profilometer SEM **Bruker Contour** Hitachi SU5000 Bruker Dektat XT Stylus





Process flow documentation

