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## Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations

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Monolithic Active Pixel Sensors (MAPS) offer the possibility to integrate sensors and readout electronics on the same chip in a standard CMOS process. This significantly reduces the material budget while maintaining good spatial resolution, making MAPS an attractive solution for High Energy Physics (HEP) applications. A prominent example of MAPS in HEP applications is the new ITS3 vertex detector of the ALICE experiment at the Large Hadron Collider (LHC) at CERN [1]. This chip will be located at less than 20 mm from the interaction point and is planned to be installed in 2026, during the LHC Long Shutdown 3 period.

This work focuses on the optimization of the pixel sensor for the new ITS3 vertex detector and future monolithic chips for HEP applications. In the framework of the CERN Experimental Physics Research & Development Work-Package on monolithic sensor (EP-R&D WP1.2) and in synergy with the ALICE experiment and the ITS3 upgrade, an extensive 3D TCAD simulation campaign was conducted to optimize the sensor for both higher performance and better radiation tolerance.

Performance of the sensor is evaluated based on the sensor capacitance  $CS$ , the total charge collected, and the collection time in both cases where a particle crosses either the center or the corner of the pixel.

Given the proximity of the sensor to the interaction point, ensuring its radiation tolerance is essential. While sensors in ITS3 must endure a fluence of  $1 \times 10^{13}$  1MeVneq/cm<sup>2</sup>, fluences in other applications can be significantly higher, sometimes exceeding  $1 \times 10^{16}$  1MeVneq/cm<sup>2</sup>.

This optimization acts on the implants of the TPSCo 65nm CMOS commercial imaging process used to realize the sensor. The TPSCo 65nm technology has been qualified for HEP and this further optimization aims at reducing  $CS$ . Smaller  $CS$  result in a higher signal for the same charge, increasing the operating margin for a given power consumption or reducing the power consumption for a given operating margin. A large part of simulations focused on the relevant practical situation of a sensor biased at only  $V_B = -1.2V$ , a requirement for ITS3. This work is a continuation and further improvement of the work presented in [2].

The optimized version of the process presented in this work demonstrates a reduction in sensor capacitance of more than two orders of magnitude in comparison to the standard process. Compared to the work in [2],  $CS$  was reduced by more than a factor of 4, maintaining very similar timing and radiation hardness. This result is extremely relevant for the design of the front-end circuit. The extensive simulations (more than 300GB) are used to explore the limits of the sensor operating point to ensure sufficient operating margin.

The simulations were extended to higher reverse-bias voltages to explore the possibility of improving the radiation tolerance of the sensors for applications operating at fluences higher than ITS3. The data presented here contribute to demonstrate that higher reverse-biases are necessary for designing sensors capable of withstanding fluences above  $1 \times 10^{15}$  1MeVneq/cm<sup>2</sup>.

[1] TDR ALICE-ITS3. No. CERN-LHCC-2024-003. 2024

[2] C. Lemoine et al 2024 JINST 19 C02033

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