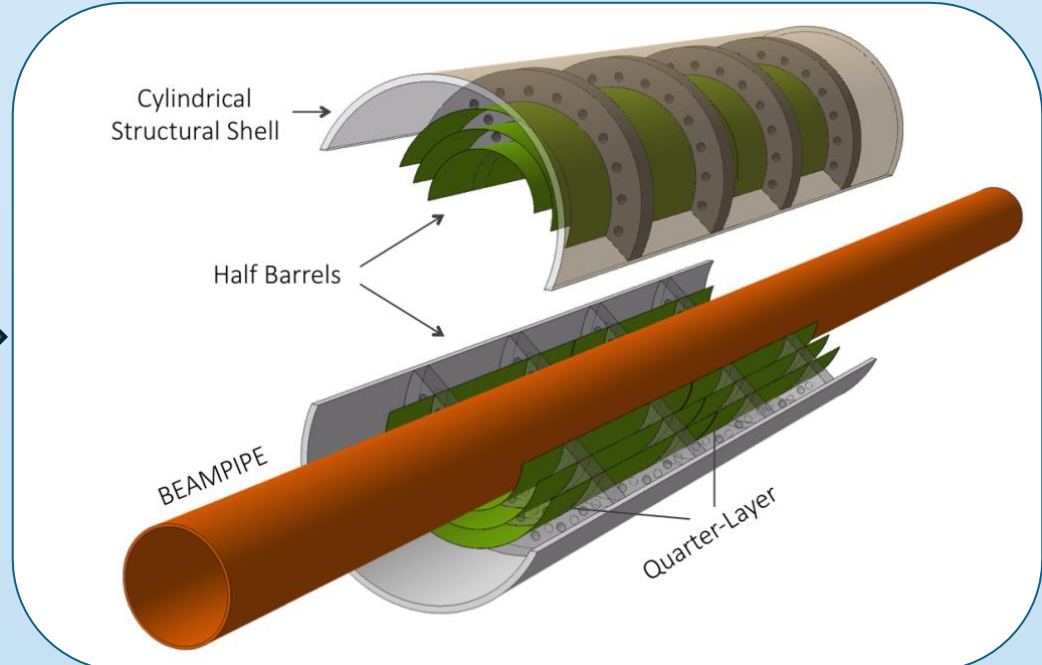
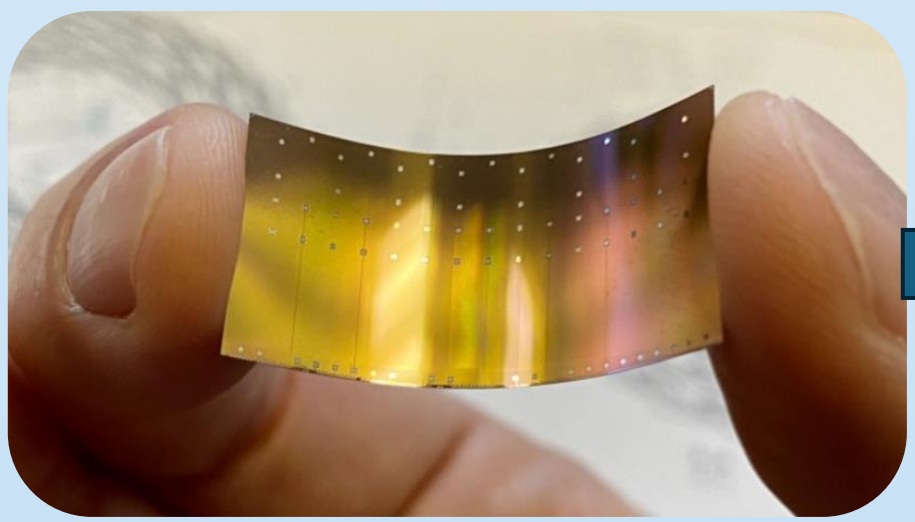


Study of the global and in-pixel efficiency and resolution of different variants of the CE-65v2 MAPS

ALICE ITS3

- Upgrade of the Inner Tracking System, installation in 2027-30
- Three innermost layers of ITS2 will be replaced with wafer-scale, thin, bent sensors
- Ultra-light design to minimise multiple Coulomb scattering



Requirements	ALICE ITS3	FCC-ee vertex
Sensor spatial resolution	5 μm	3 μm
Material budget per layer [X_0]	0.07%	< 0.3%
Radiation tolerance [$1\text{MeV } n_{\text{eq}}/\text{cm}^2$]	10^{13}	$\sim 10^{14}$ per year
First layer radius r_{min}	19 mm	13.7 mm
Power density	40 mW/cm^2	$\lesssim 50\text{mW}/\text{cm}^2$
Partial hit density	8.5 MHz/cm^2	$\sim 250\text{MHz}/\text{cm}^2$

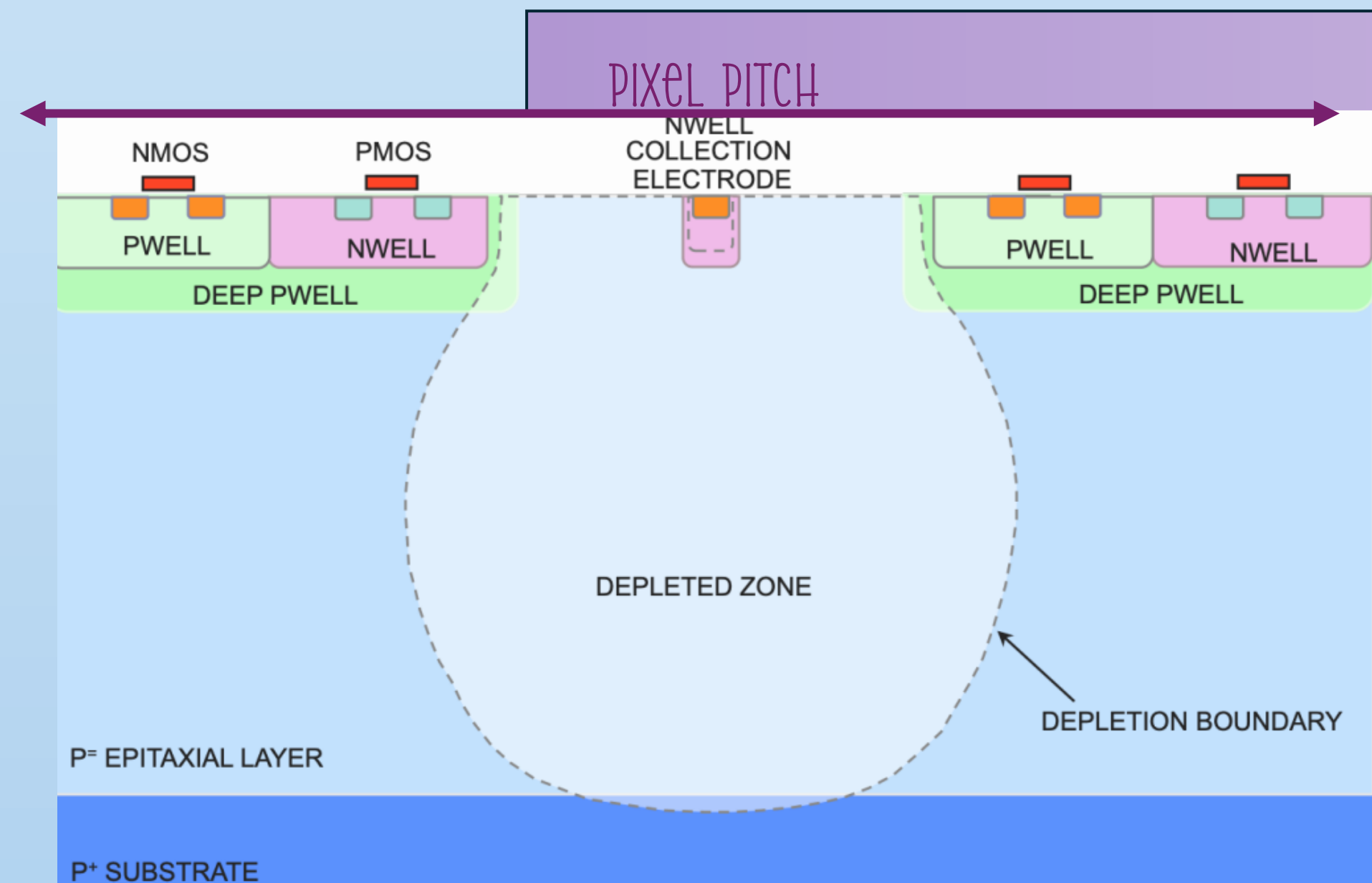
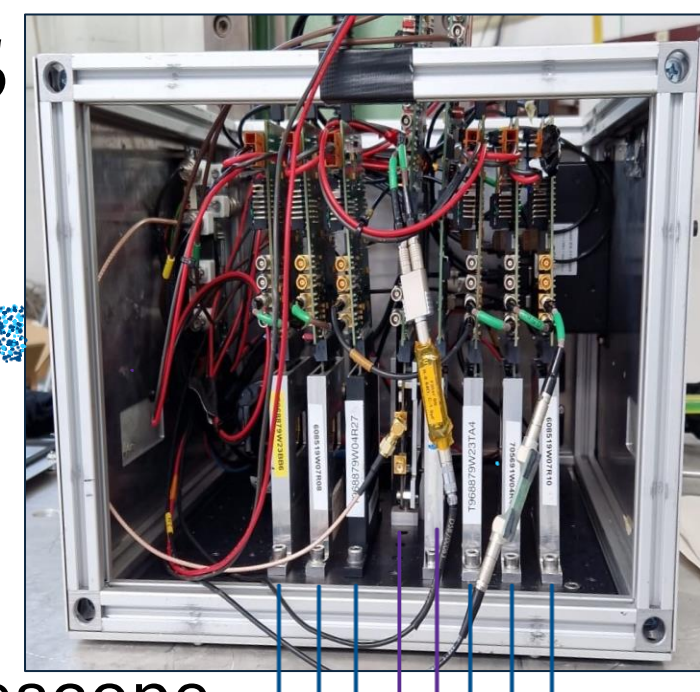


Testbeam at CERN SPS

Mixed hadron beam

Telescope consists of:

- 6 ALPIDE planes
- DPTS as trigger
- 2.2 μm resolution of telescope



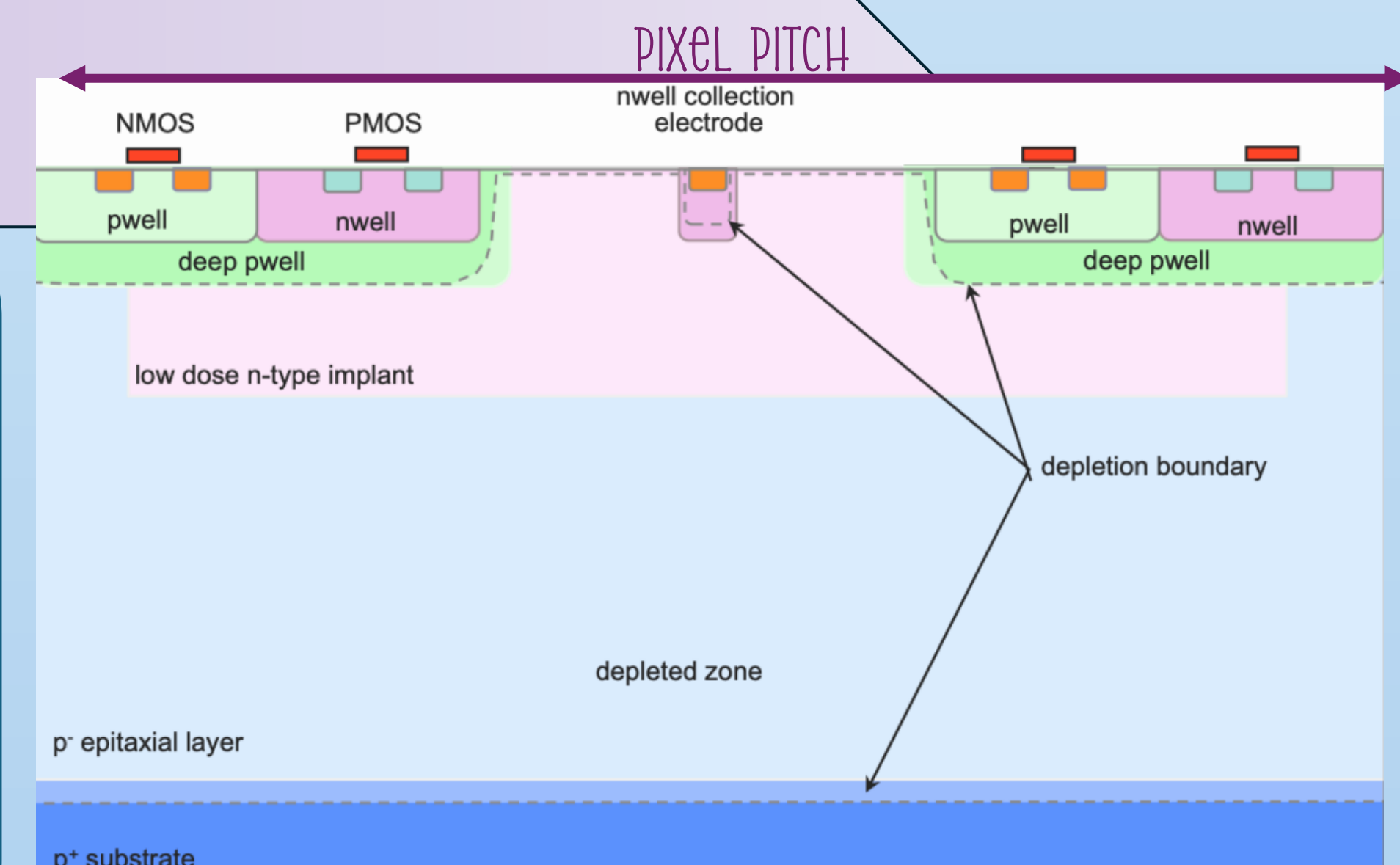
Faster charge collection, better efficiency

Standard process

- High charge sharing between neighb. Pixels
- Slow charge collection
- subject to charge trapping, less radiation tolerant

Modified with gap process

- Low charge sharing
- Even at the edges fast charge collection
- More radiation tolerant



Electric field expands laterally due to gap in low dose n-type implant at pixel edges
→ Charge collection is drift-dominated

More charge sharing, better resolution

Undepleted regions at the pixel edges
→ Charge collection is diffusion-dominated

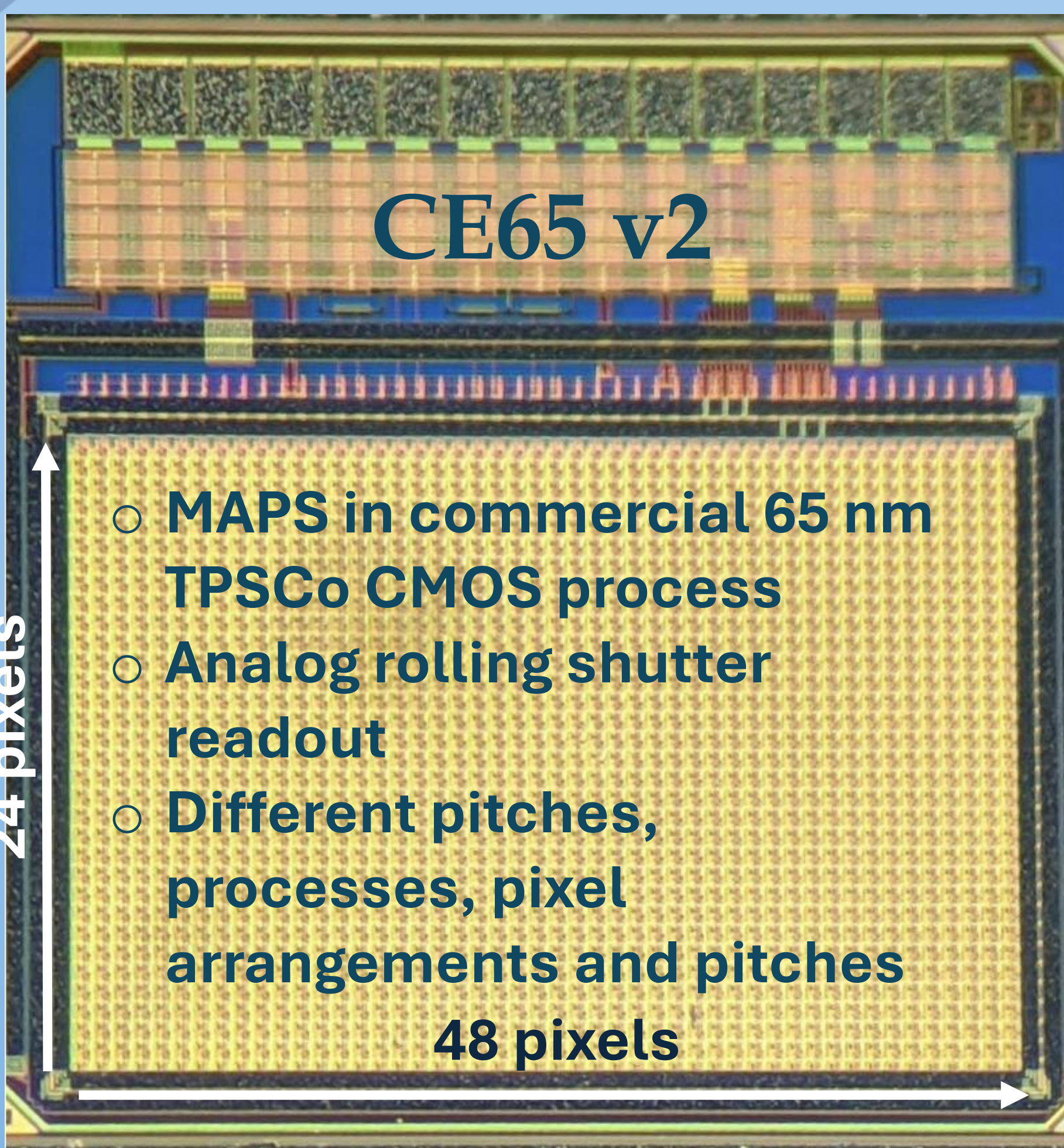
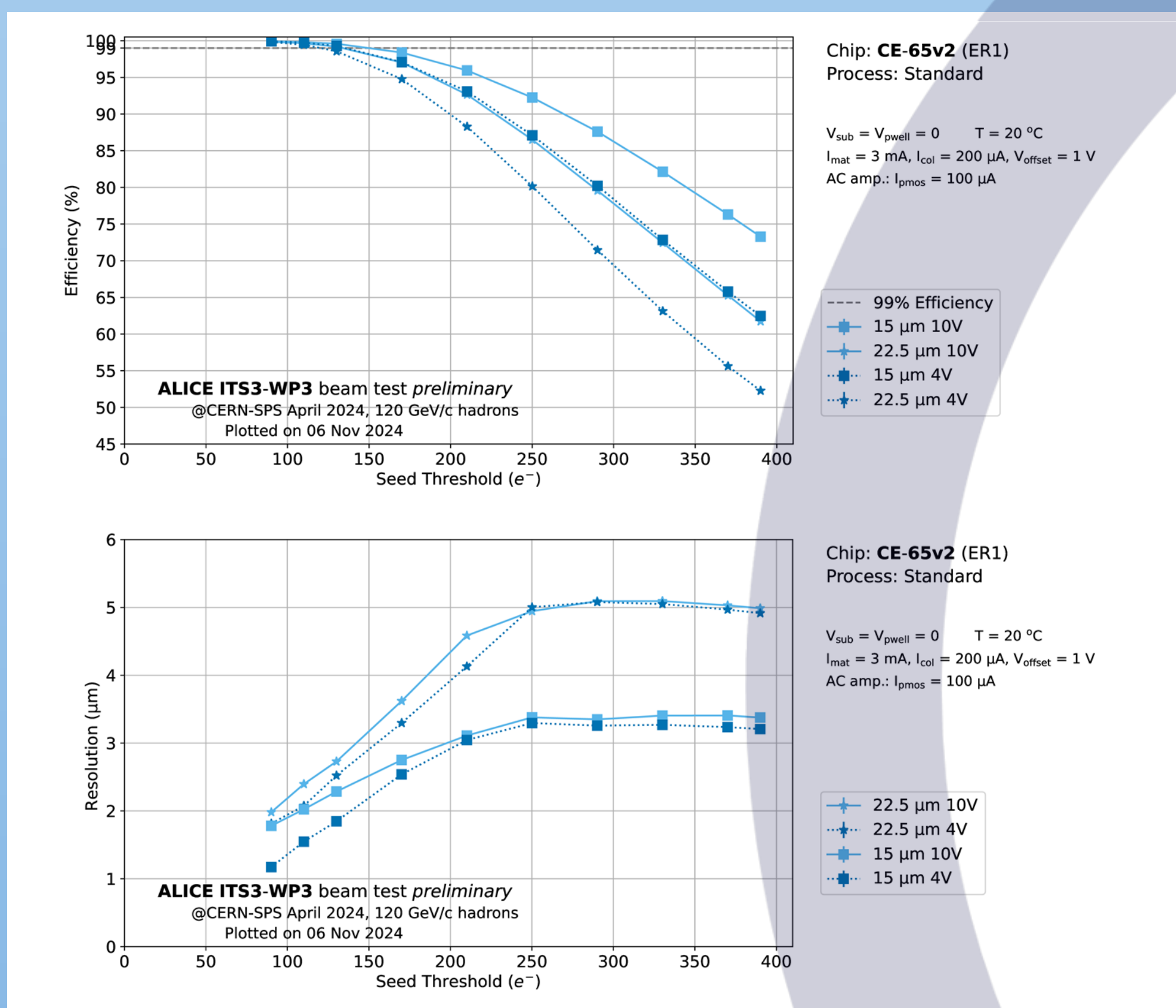
Standard process

- Mask noisy pixels on reference and DUT
- Telescope pre-alignment and alignment
→ DUT pre-alignment and alignment → Analysis

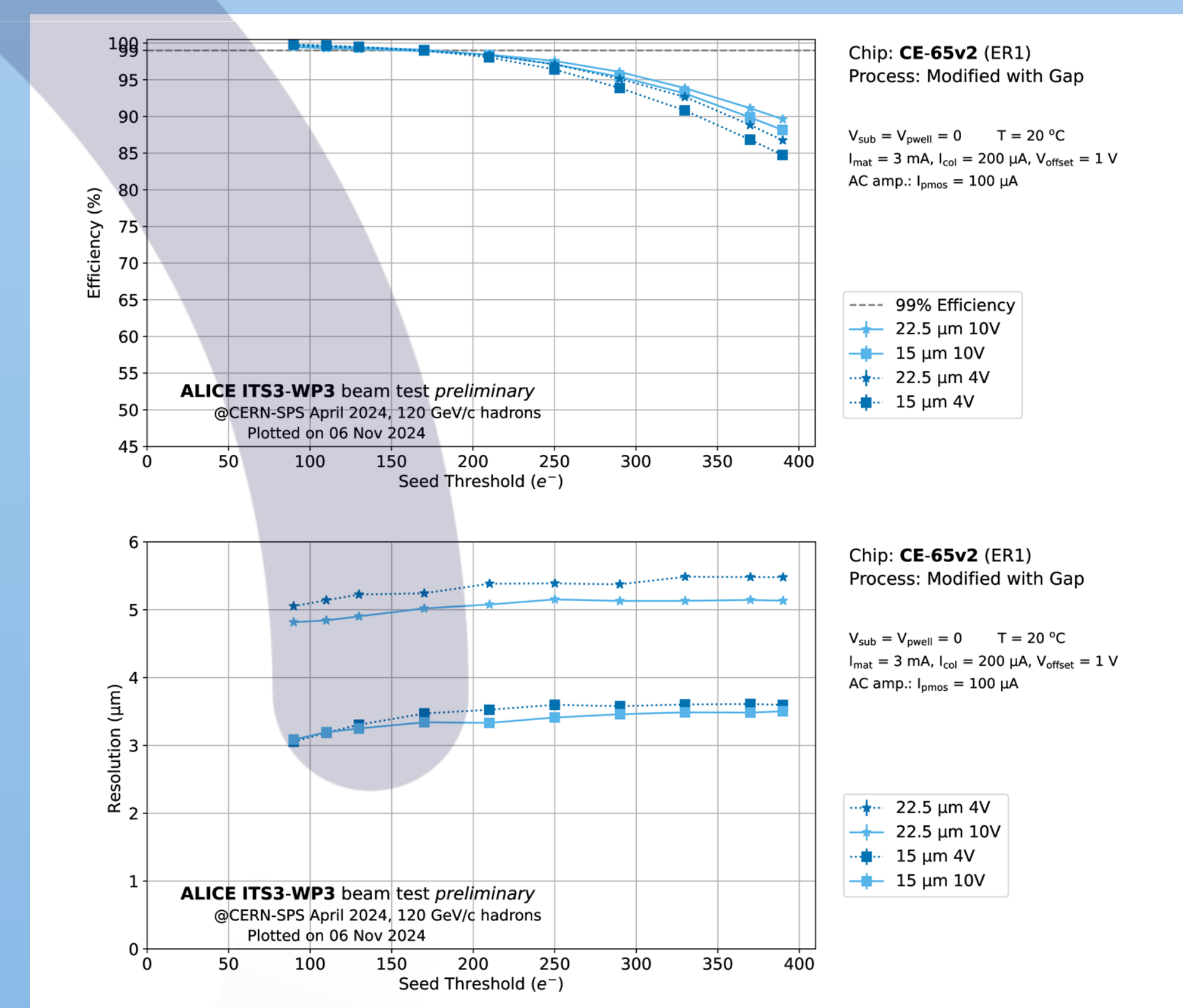
Test beam data analysis details

- Cluster method with threshold_{neighbour} = threshold_{seed}
- First seed threshold at 3 x RMS noise
- Subtract telescope resolution in quadrature

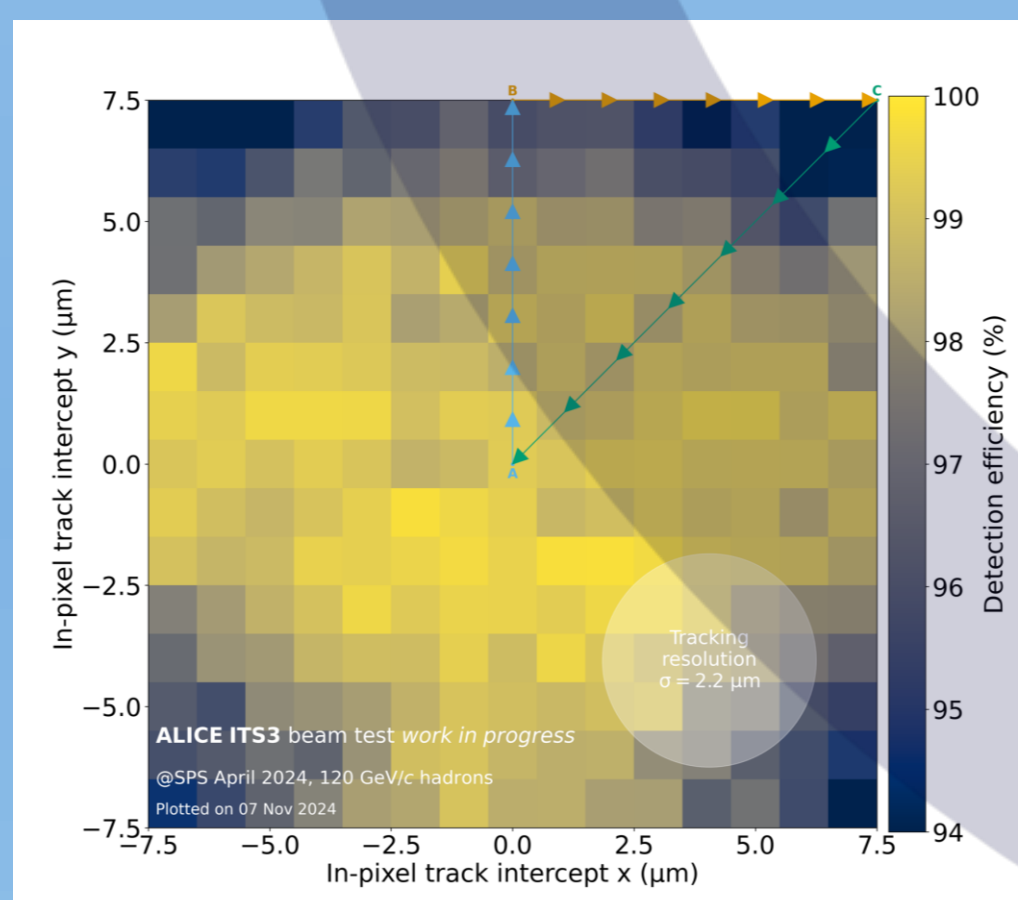
Modified with gap process



- MAPS in commercial 65 nm TPSCo CMOS process
- Analog rolling shutter readout
- Different pitches, processes, pixel arrangements and pitches



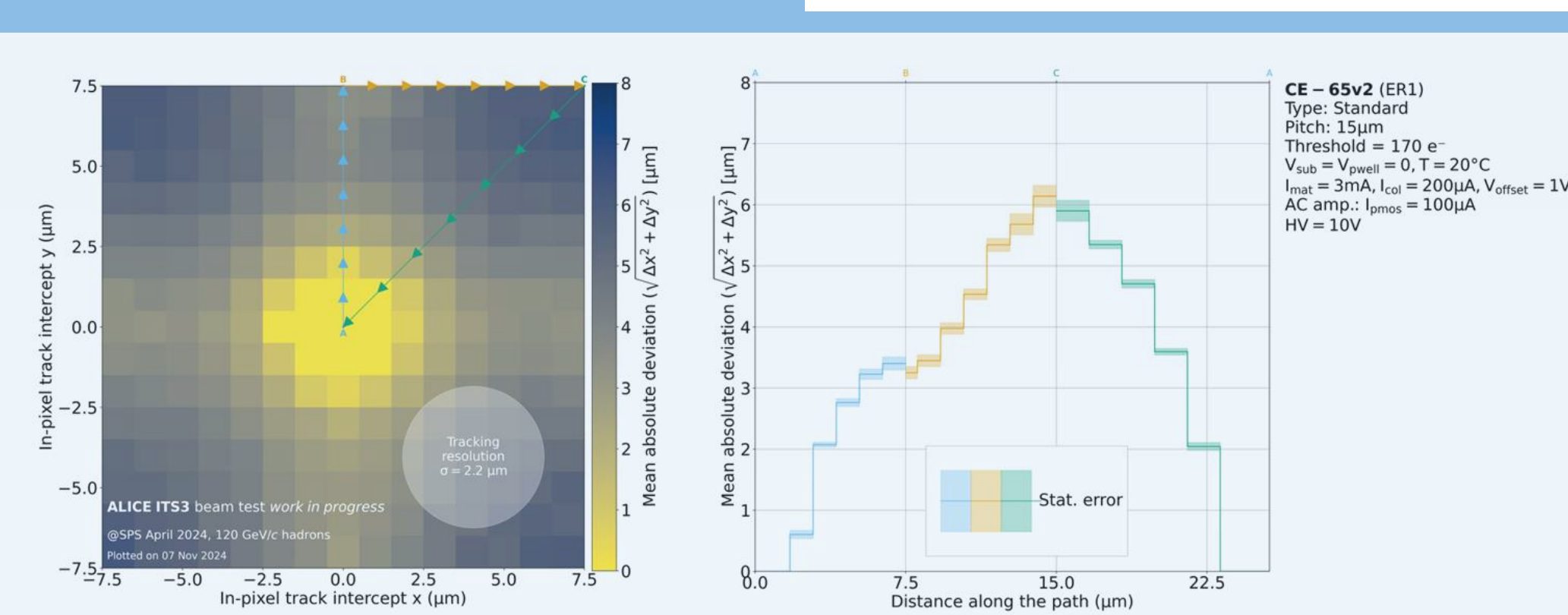
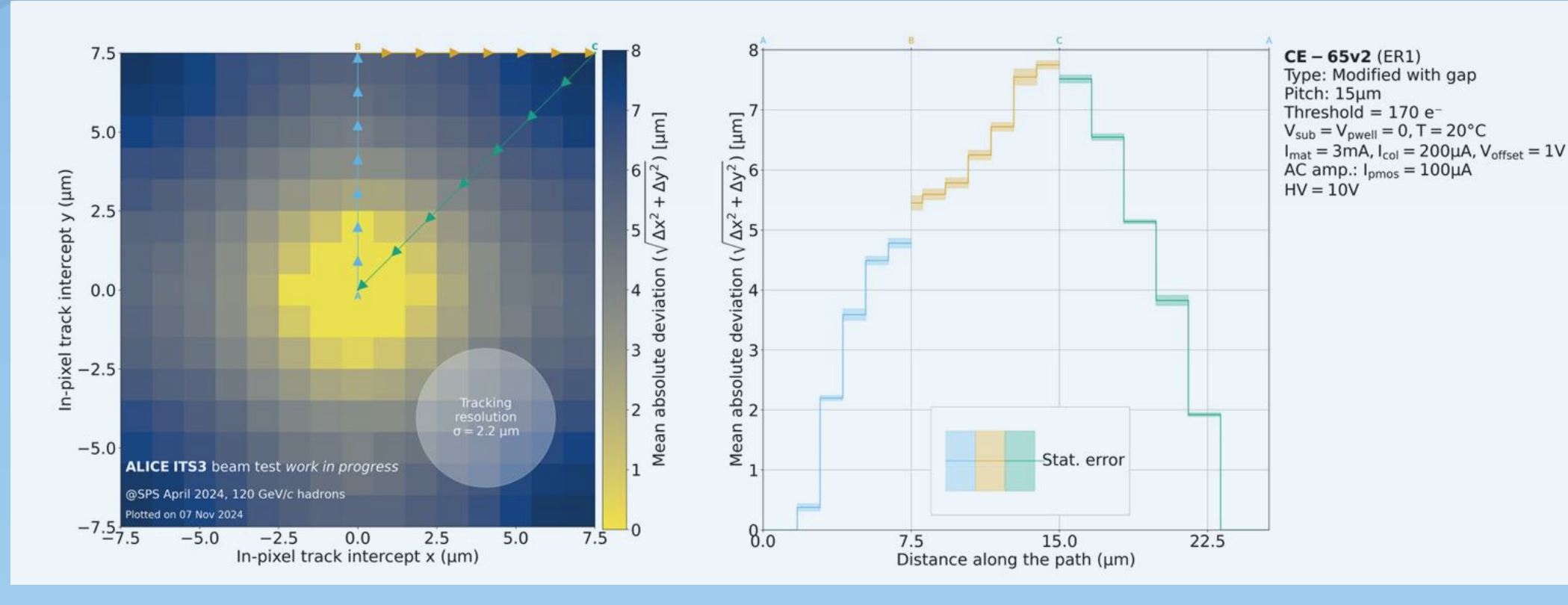
- ### Standard
- Better efficiency for 10V than 4V
 - < 2.5 μm and < 3.5 μm resolution for 15/22.5 μm pitch at efficiencies > 99%



Pitch [μm]	Process		
	Standard	Modified	Mod w. GAP
15			
18			
22.5			

The blue figures represent chips discussed on the poster

- ### Modified with Gap
- Negligible impact of higher voltage
 - < 3.5 μm and < 5.5 μm resolution for 15/22.5 μm pitch at efficiencies > 99%



In-pixel discussion

- Modified with gap process has higher efficiency at edges and corners, slightly worse in the centre
- Better resolution in standard process comes from edge and corner regions, thanks to charge sharing

Outlook and Conclusion

- Resolution < 3.5 μm resp. < 5.5 μm , efficiency greater than 99% at thresholds larger than 3 x RMS noise
 - Compatible with FCC-ee spatial resolution requirement. Further development needed to fulfil other requirements
- Detailed in-pixel studies possible thanks to large matrix size. Result confirming previous findings on process variations
- CE-65 v2 characterisation almost finished
 - Radiation tolerance of CE-65 under investigation (May 2024 test beam at DESY)
 - Request for SPS test beam in 2025 to test 18 μm pitch and modified process in detail

Bibliography

- The ALICE collaboration, Technical Design report for the ALICE Inner Tracking System 3 - ITS3 ; A bent wafer-scale monolithic pixel detector, (2024).
- Full report on the FCC Feasibility Study mid-term review. Scientific Policy Committee - Three-Hundred-and-Thirty-Sixth Meeting, (2023).
- S. Bugiel et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **1040**, 167213 (2022).