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Testing the Limits of ITkPixV2: the ATLAS Inner Tracker Pixel Detector Readout Chip

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The ITkPixV2 readout chip is the production readout chip for the ATLAS Phase 2 upgrade for the High-Luminosity LHC of the ATLAS inner detector, scheduled for commissioning at the start of 2029. The innermost layers of the ATLAS ITk pixel detector are expected to reach maximum hit rates of $3\text{GHz}/\text{cm}^2$, a total radiation dose of 1 GRad, and data readout rates of 5Gbps, with an operational lifetime of over a decade.

In order to ensure continuous operation of the ATLAS pixel detector, it is critical to perform rigorous testing of the ITkPixV2 readout chip and the accompanying Data Acquisition (DAQ) system. To perform this testing, we utilize the YARR DAQ system, which is designed to support the readout of ATLAS ITk Pixel and Strip detector modules on a variety of hardware platforms. For readout hardware, we use the YARR PCIe firmware, which employs Simple PCIe Carrier (SPEC) cards to readout Pixel detector modules.

In this talk, we present the development towards and results of several such tests done in the past year in test beam campaigns, Single Event Effect (SEE) facilities, X-ray irradiation machines, and simple bench testing, as well as the DAQ development done concurrently in YARR software and firmware to facilitate these tests. These results present the closest test yet of ITkPixV2 chips to their target nominal operational conditions in the upgraded ATLAS detector at the HL-LHC. This includes reaching the highest hit rates and trigger frequencies measured to date, along with simultaneous development of the YARR DAQ software and firmware to be able to handle continuous stable operation, automatic chip error handling, and online data processing at these rates.

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