The MiniCactus sensor development line : towards HV-CMOS Monolithic sensors with 20 ps resolution

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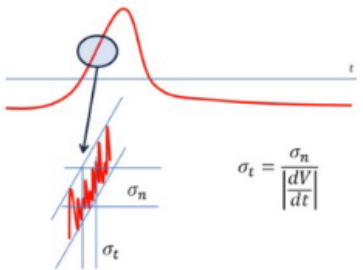
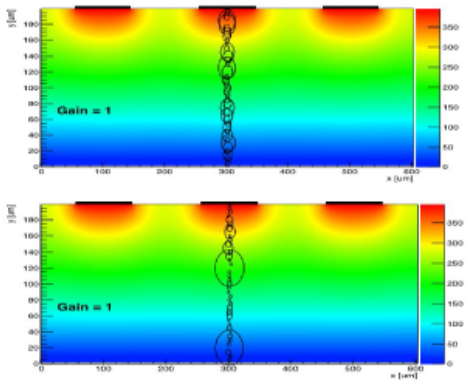
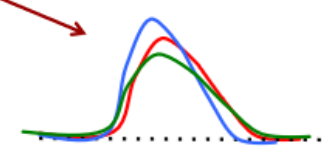
Time resolution ingredients

$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$



"Jitter" term





Signal shape is determined by Ramo's Theorem

$$i \propto qvE_w$$

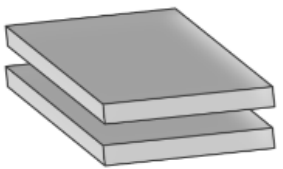


Illustration taken From N. Cartiglia (VCI 2022)

Small noise → choice of technology, small detector capacitance
High dv/dt →
High electric field (but Vd saturates around 1 V/μm)
Intrinsic amplification

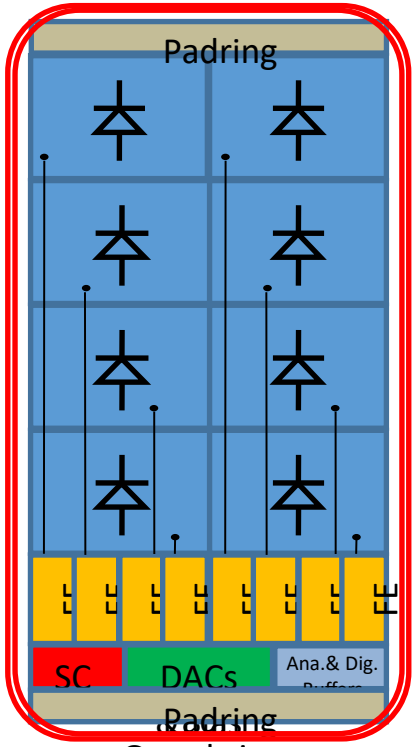
Amplitude variation → Timewalk, corrected offline

Non-homogeneous energy deposition → cannot be corrected, minimized by design

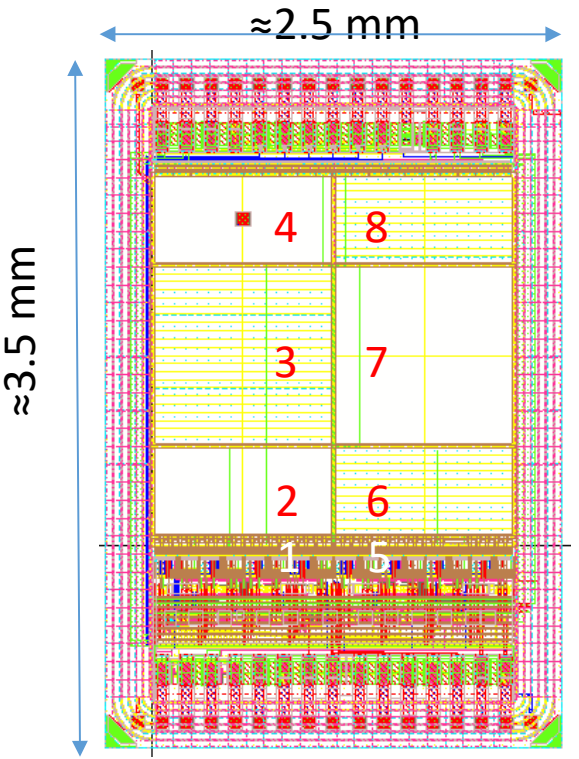
Saturated drift velocity in sensor volume → Uniform weighting field

Parallel plate geometry, easier for big pixels → Large electrode designs

MiniCACTUS V1 Sensor Chip



Block diagram of the MiniCACTUS chip (not to scale)

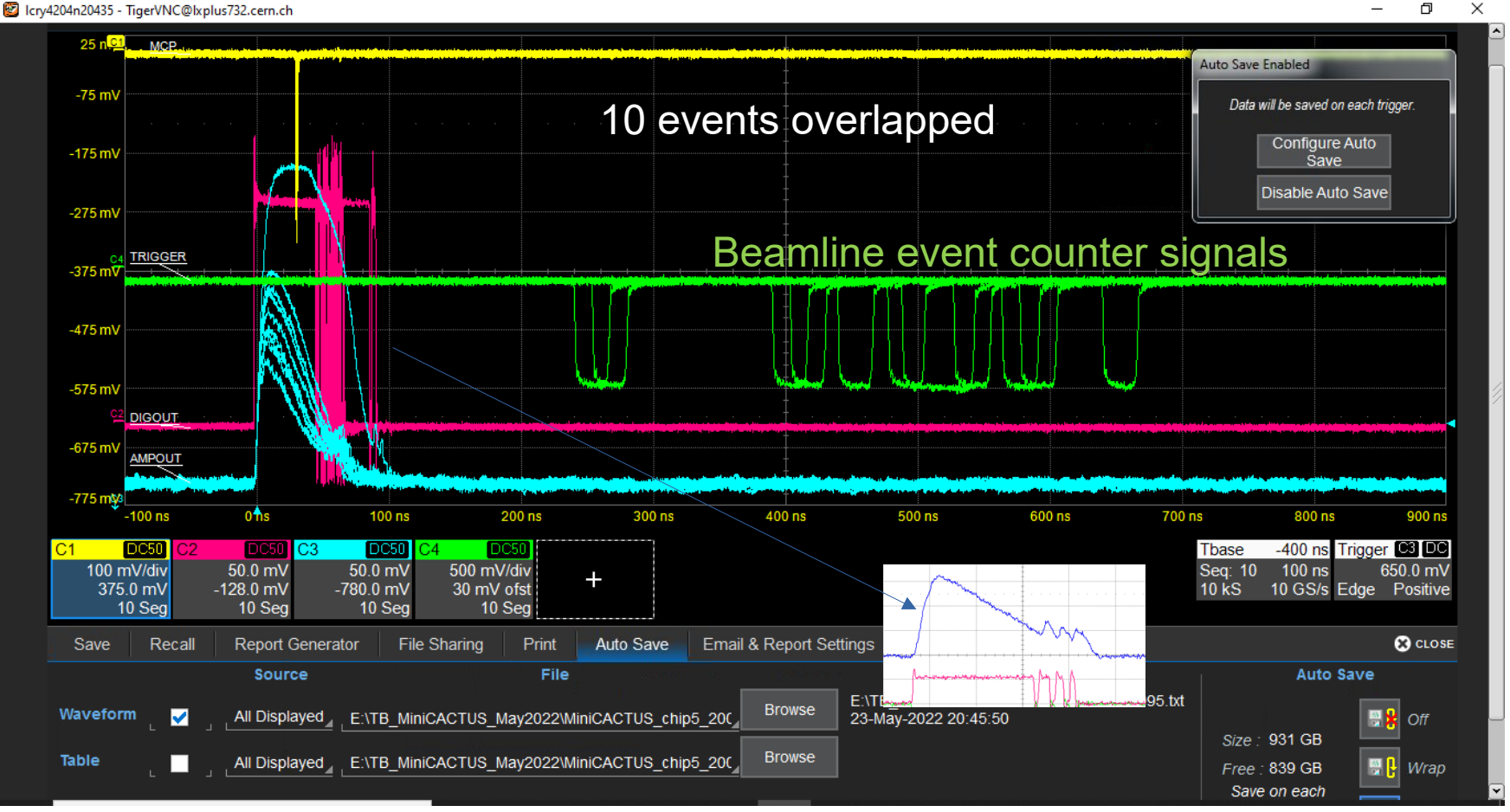


Layout of MiniCACTUS

Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel

- **MiniCACTUS** is a small detector prototype designed in order to address the *low S/N issue* observed on previous CACTUS large size demonstrator
- FE integrated at column level, pixels mostly passive
- On-chip **Slow Control**, **DACs**, **bias circuitry**
- 2 discriminated digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns
- 2 small pixels implemented as test structures to study charge collection (*FEs not power optimized*)
- Some detectors thinned to 100, 200, 300µm and than post-processed for backside polarization after fabrication

TYPICAL WAVEFORMS OBSERVED DURING TESTBEAM

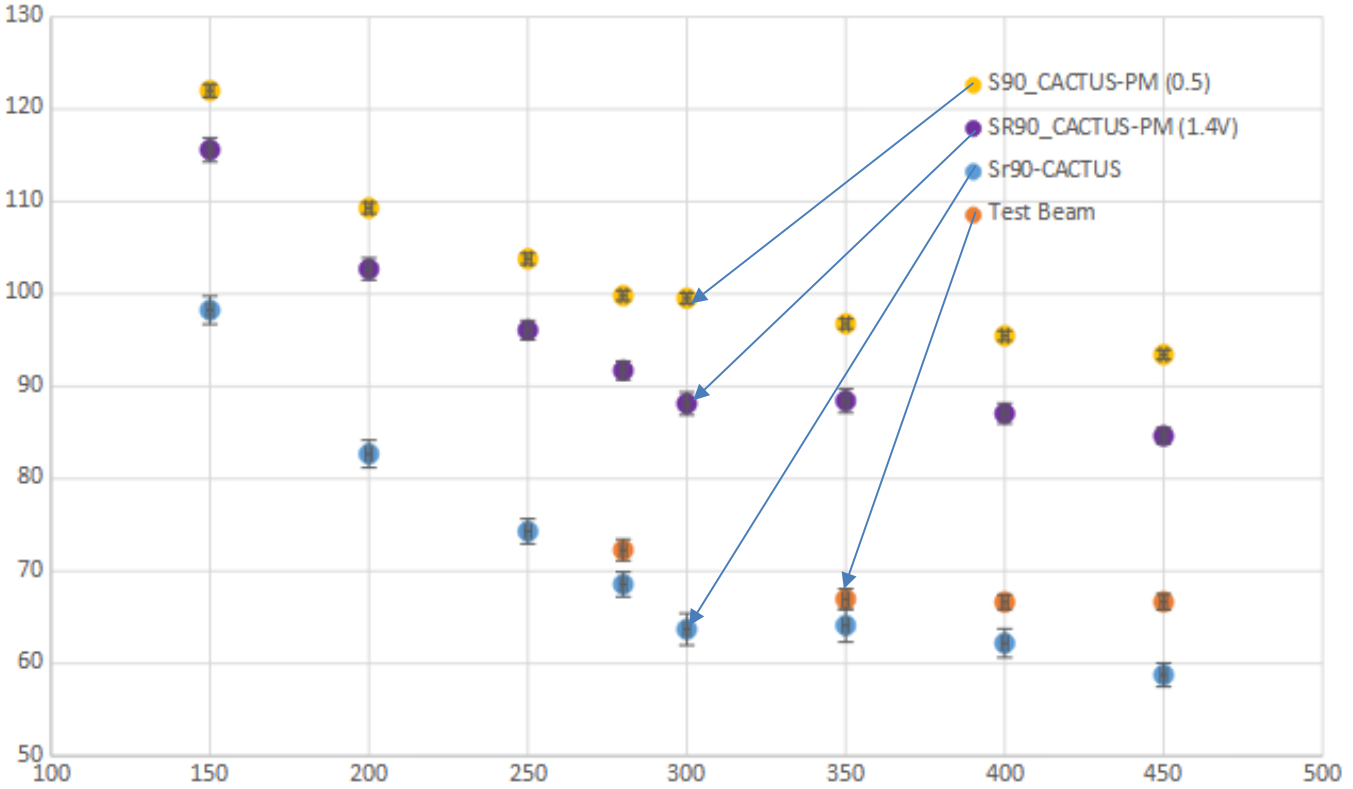


→ Ringing on Digital Output due to coupling from the digital buffers (known problem from in-lab tests, negative impact on TW corrections from digital ToT)

180 GeV/c muon data taken at CERN/SPS EHN1, H4 beamline (parasitic to RD51/DRD1)

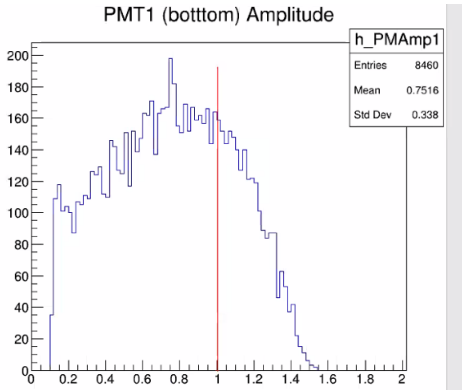
TIMING MEASUREMENTS COMPARISON : PMT+^{90}Sr SOURCE/TESTBEAM

MiniCactus v1, Chip#6, pixel 8, **0.5 x 1 mm², 200 µm**



Bias Voltage (V)

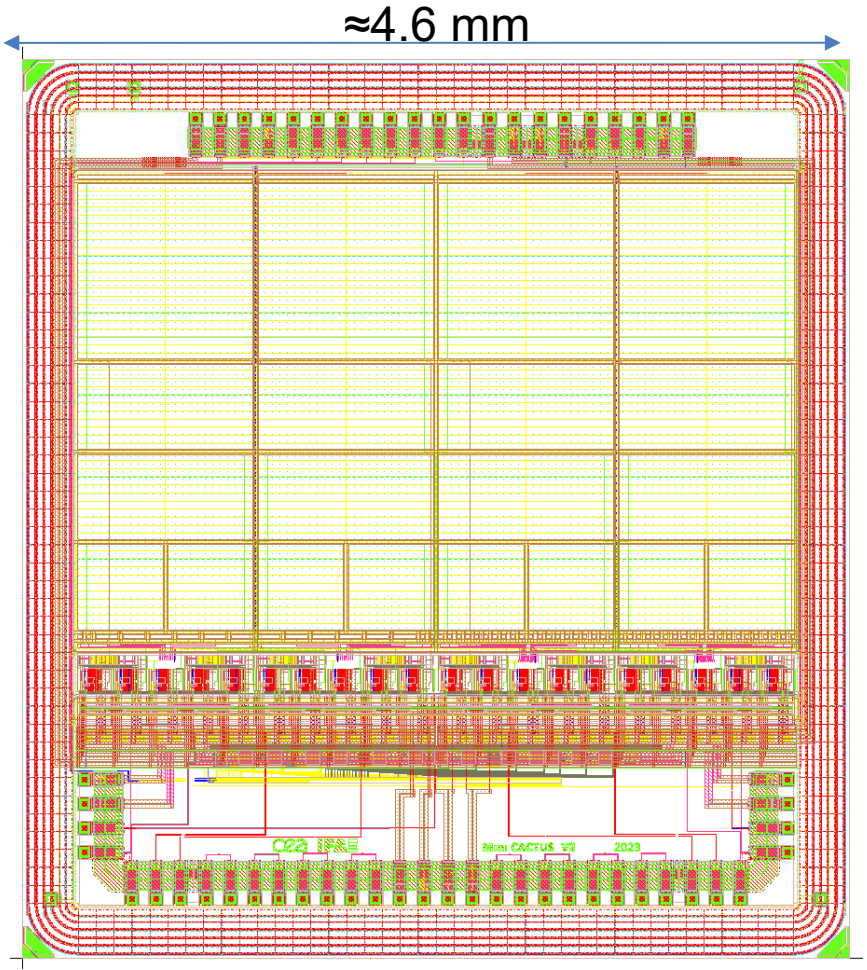
→ In-lab measurements with 90Sr betas allow to predict actual performance with MIPs



Have to select MIP-like betas by cutting out low energy deposits in PMT

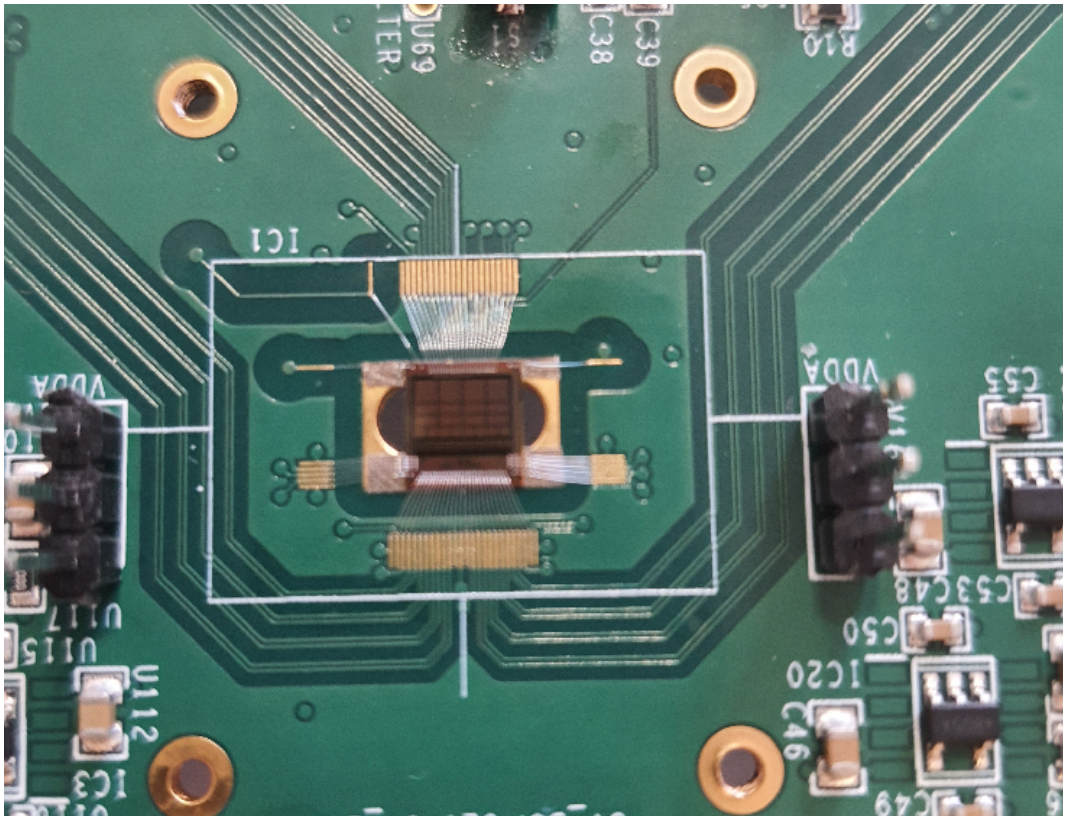
MiniCACTUS_V2 Sensor Chip

Irfu : Yavuz Degerli, Fabrice Guilloux, Jean-Pierre Meyer, Philippe Schwemling
IFAE : Raimon Casanova, Yujin Gan, Sebastian Grinstein



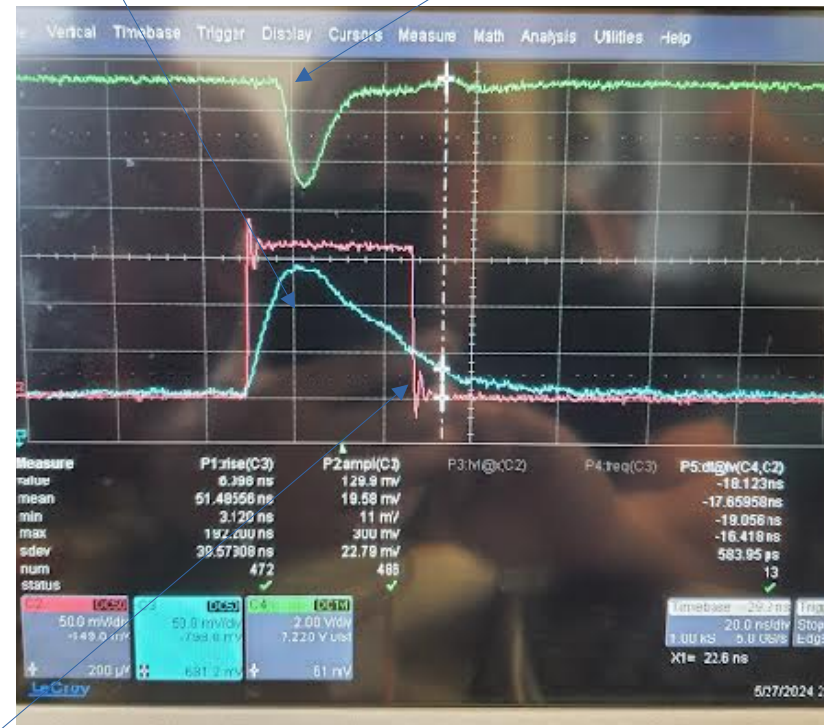
- ~ 2 times larger than MiniCACTUS
- 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm diodes
- 50 µm x 150 µm and 2 50 µm x 50 µm small test diodes
- 3 different preamps
- New multistage discriminator with **programmable hysteresis**
- Improved layout for better mixed-signal coupling rejection
- **CEA-IRFU** & **IFAE-Barcelona** coll.
- Submitted in May 2023, chips came back from post-processing end May 2024

First look at MiniCactus v2



PMT

Analog

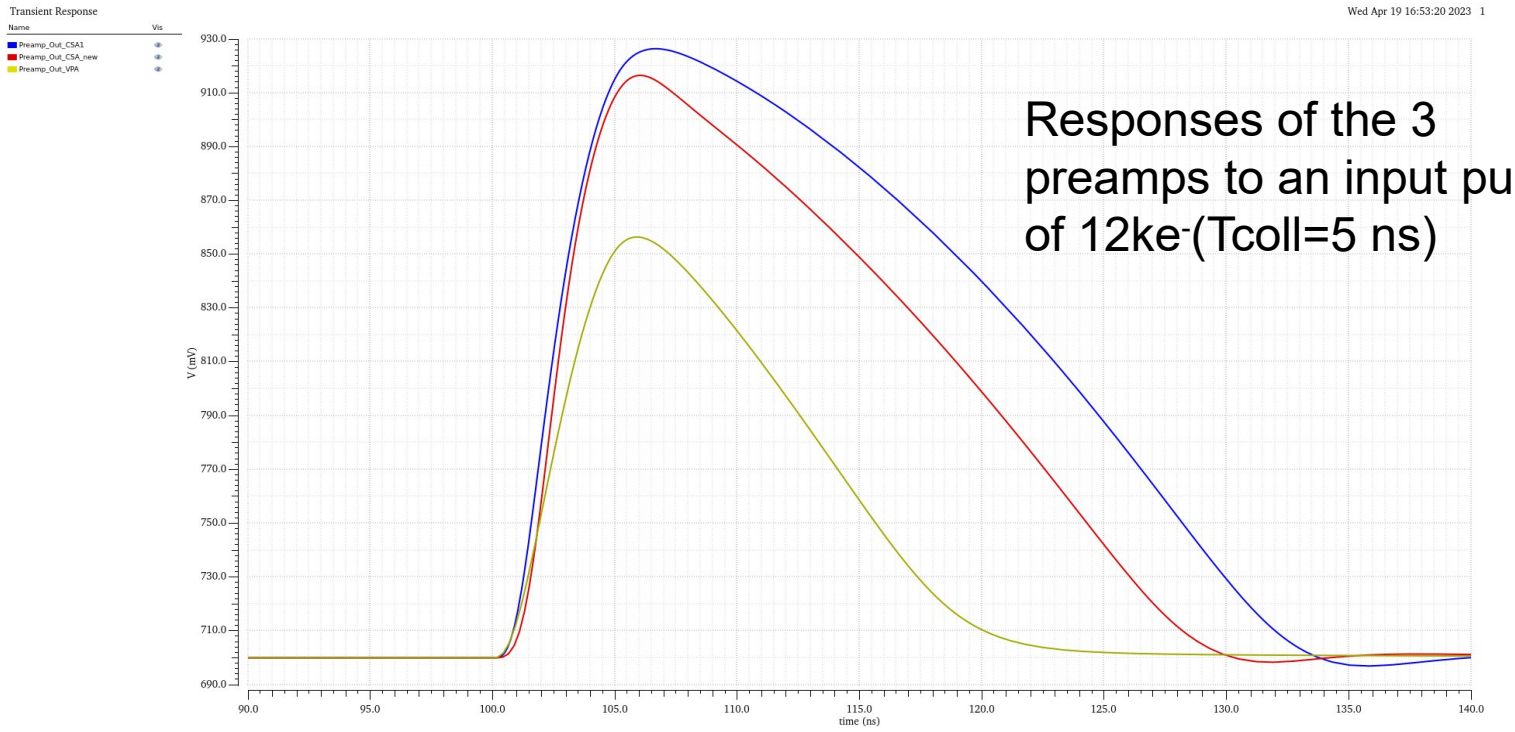


Digital

Analog/Digital couplings are gone !

MiniCACTUS_V2 Sensor Chip

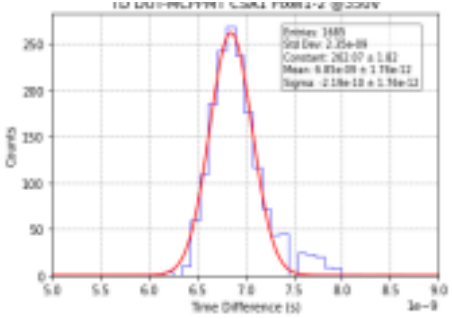
- 3 different preamps implemented in MiniCACTUS_V2
- 2 new preamps (CSA_new and VPA) designed by **IFAE-Barcelona** for better jitter and reduced ToT

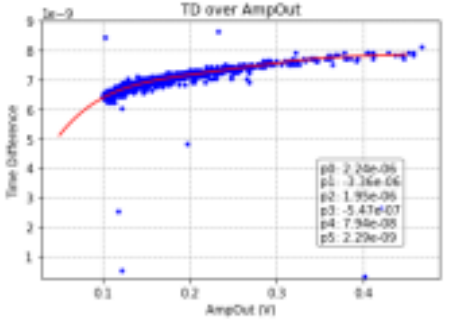


Responses of the 3 preamps to an input pulse of 12ke$^-$(Tcoll=5 ns)

- CSA1 : MiniCACTUS_V1 charge sensitive preamp
- CSA_new : new charge sensitive preamp
- VPA : new voltage preamp

June-July 2024 first testbeam results





175 μ chip, 0.5 mm x 0.5 mm pixel, 300 V

- Data cleaning (cut the noise)
- Sigma before time walk correction: 219 ps
- Sigma matrix after time walk correction:

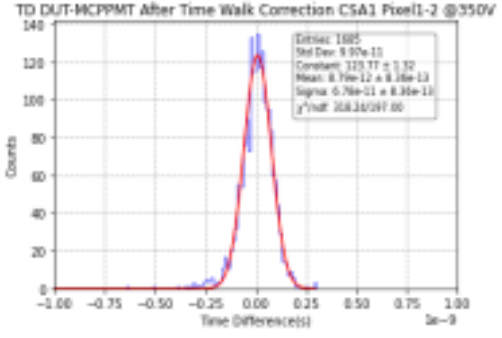
Sig(DUT-MCP)	Sig(DUT-PMT)	Sig(MCP-PMT)
67.8 ps	88.1 ps	72.3 ps

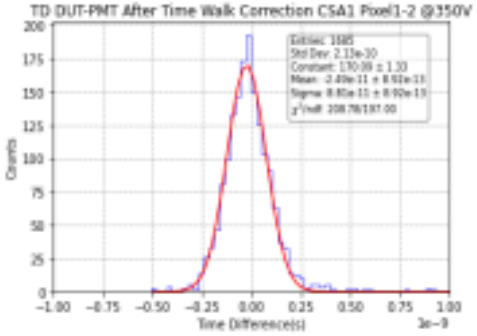
- Reverse the matrix to get the sigma of the devices:

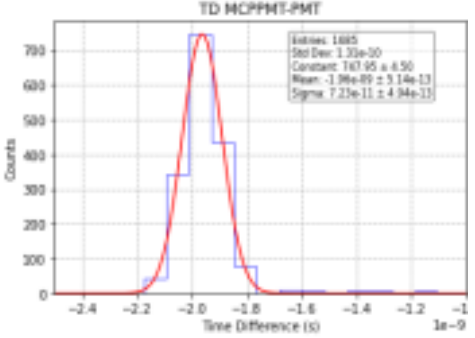
Sig(DUT)	Sig(PMT)	Sig(MCP)
59.9 ps	64.4 ps	32.5 ps

Testbeam setup has three time measurement devices : Beamline MCP, MiniCactus v2, PMT → can extract time resolution of the three devices

Best result obtained so far
Improvements to be expected from higher HV data and FE parameter optimisation

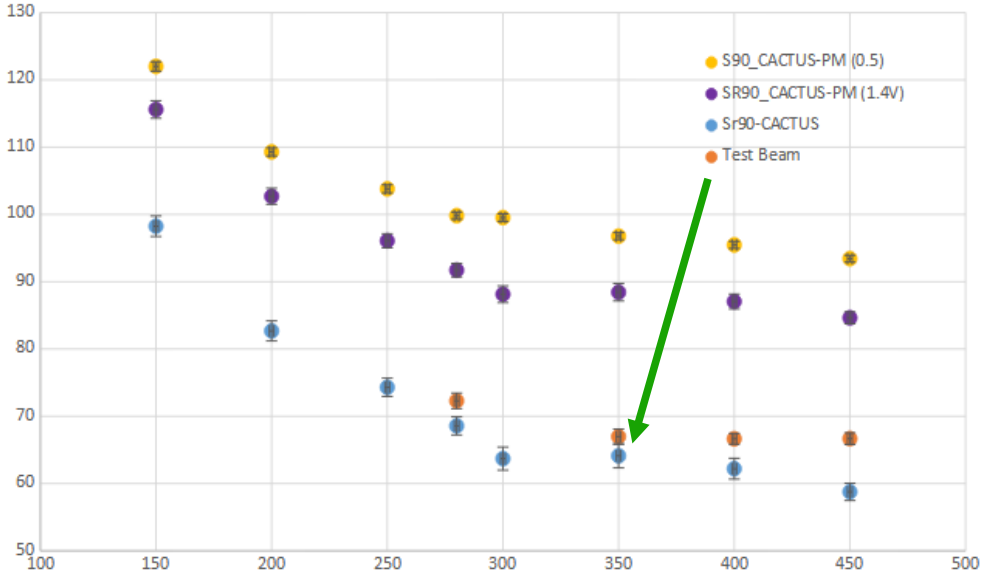


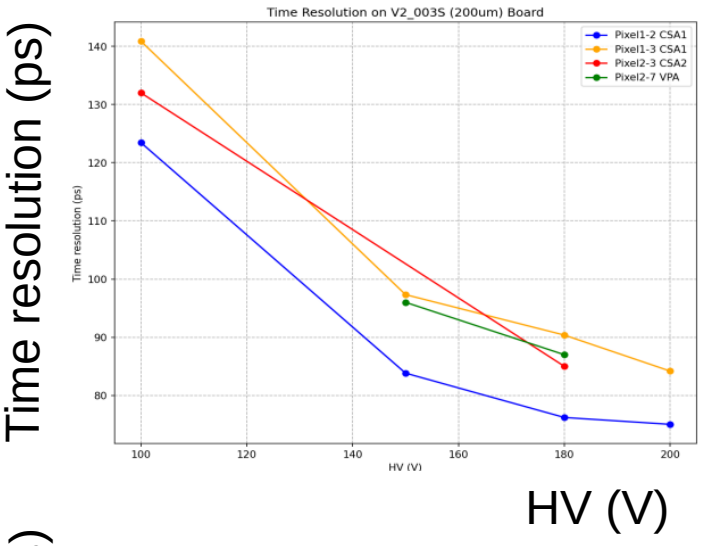


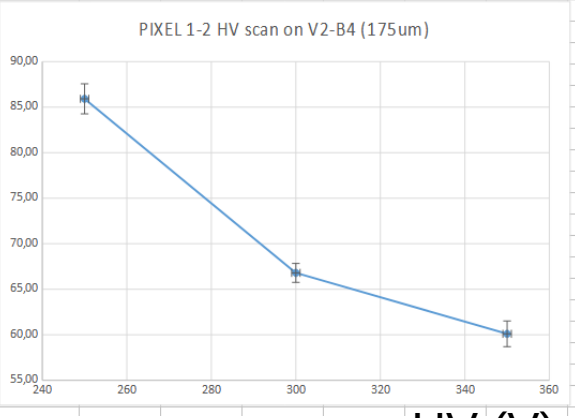


MiniCactus v1/v2 comparison

Time resolution (ps) MiniCactus v1



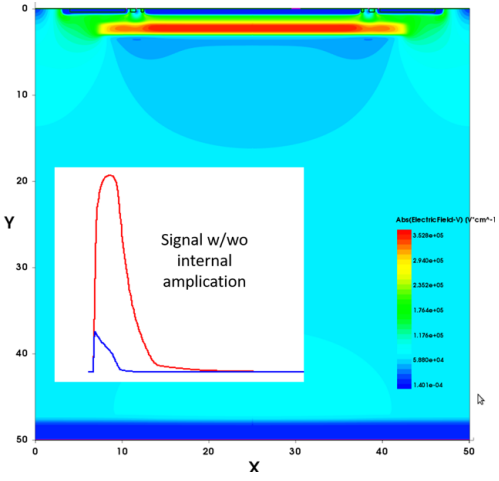




- Time resolution of v1 and v2 similar for same pixel geometry and identical thickness
- New front-ends have similar performance (before optimization) to old front-end
- 0.5 mm x 0.5 mm better than 0.5 mm x 1 mm pixels
- Best result so far on 0.5 x 0.5 mm pixel, thickness 175 μ

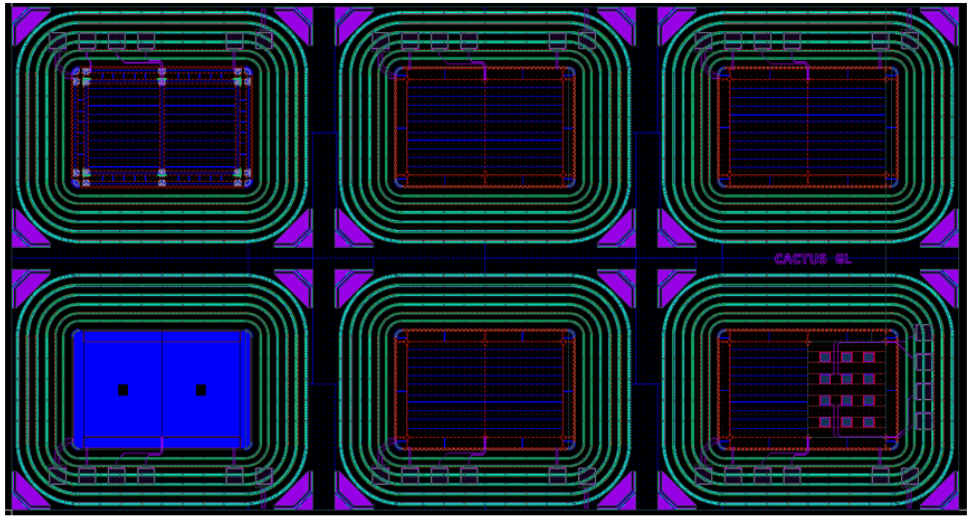
How to improve further ?

- Add intrinsic gain to :
  - Improve S/N → Improve on time resolution
  - Reduce FE power consumption
  - Reduce pixel pitch
- Ultimate long term goal is reaching 20 ps resolution

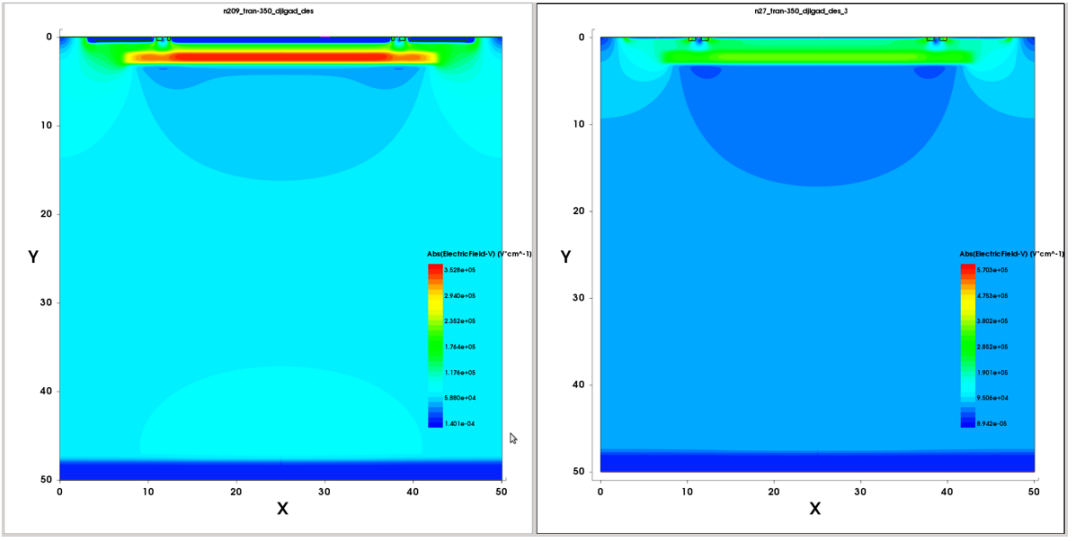


TCAD simulation of structures with gain layer

MiniCACTUS-GL Layout



Electric field for one diode with external rings

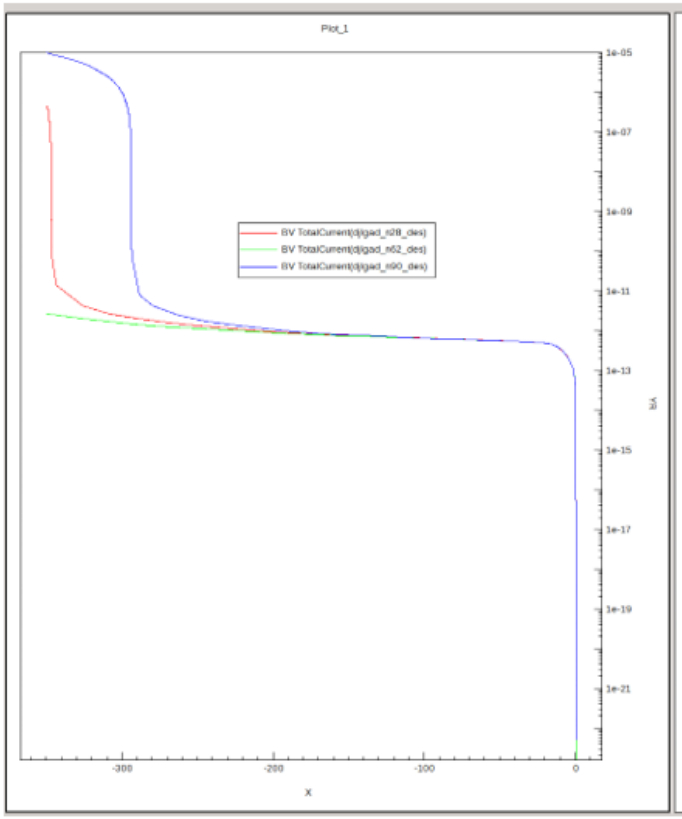


NW diode

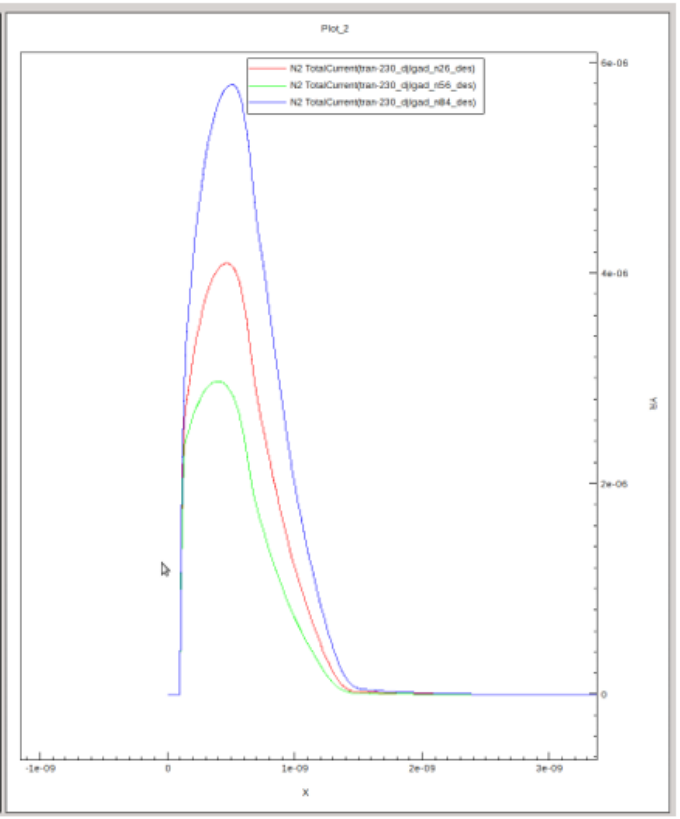
N+ diode

- DJ-LGAD concept (buried PN-junction implemented by the foundry)
- Total area = 10 mm², 6 different chips with different diodes

Optimization of Buried PN-Junction Parameters



I-V curves



Transient signal

P dose
High
Medium
Low

- Gain ≥ 10 seems possible

Submission status

- Test structures (passive sensors) have been submitted in May 2024 LF15A MPW
- Six different layouts, identified as promising by TCAD
- Production implied only minimal modifications to LF15A standard process
  - Changes of implant energies for two layers
  - Addition of one Customer Reserved Layer
- HR wafers (same as MiniCactus) → postprocessing underway
- 30 u epi wafers → hope is to get rid of postprocessing, diced chips being shipped
- Expect to have HR chips back from dicing/postprocessing by end of 2024

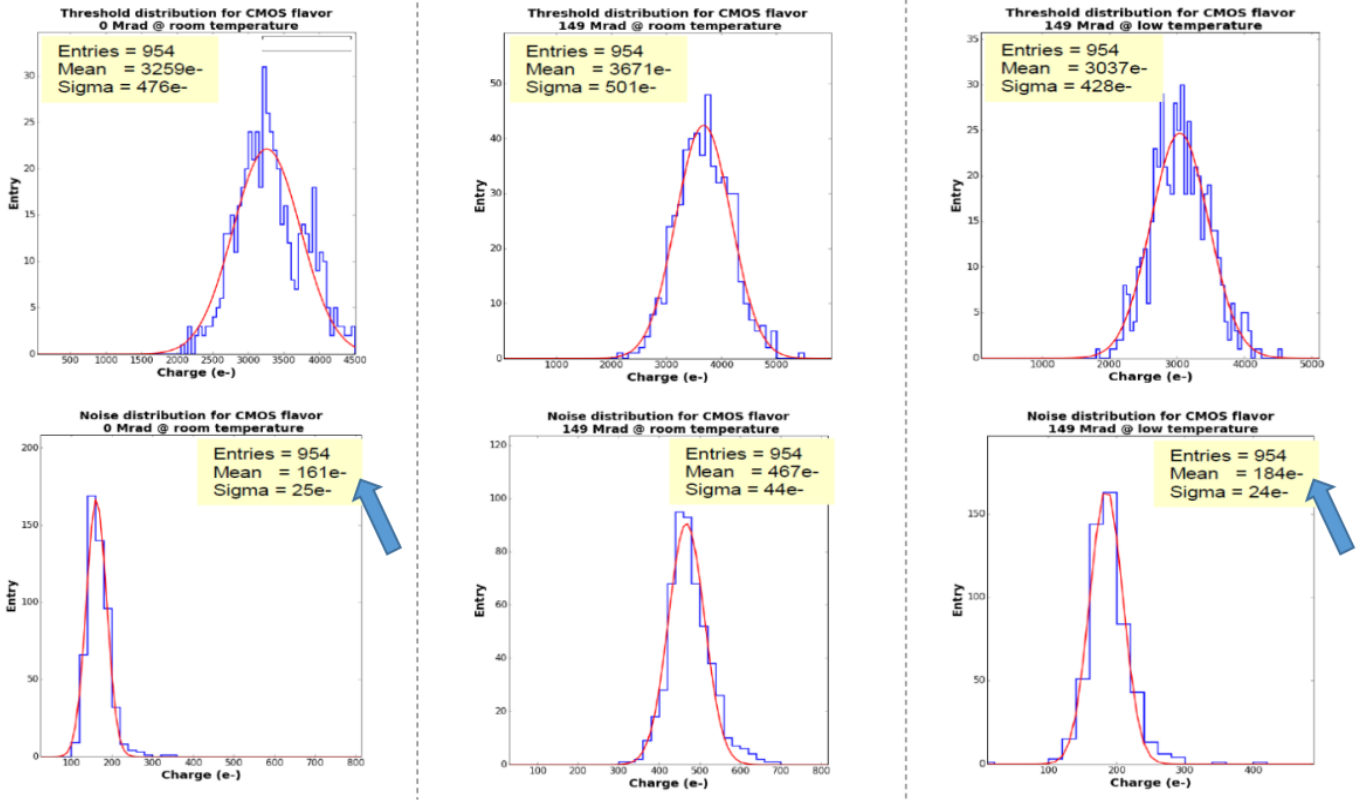
Conclusions and perspectives

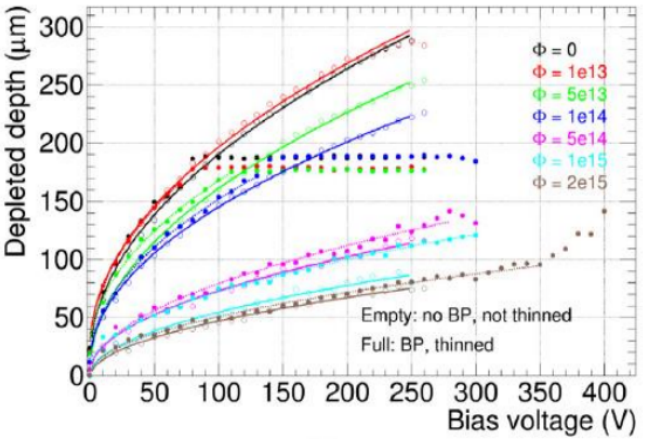
- Short term : In-lab and test-beam tests of MiniCactus v2
- Medium term : investigate test structures with integrated gain layer.
- If test structures work, integrate front-end, and submit a MiniCactus like design in LF15A (end 2025 ?)
- Publications :
  - MiniCACTUS: A 65 ps Time Resolution Depleted Monolithic CMOS Sensor (arXiv:2309.08439, NSS 2022 conference)
  - MiniCACTUS: Sub-100 ps timing with depleted MAPS, Nucl.Instrum.Meth.A 1039 (2022) 167022, VCI 2022 conference)
  - CACTUS: A depleted monolithic active timing sensor using a CMOS radiation hard technology (arXiv:2003.04102, JINST 15 (2020) 06, P06011)

Backup

LF15A radiation hardness

0 Mrad @Room Temp **149 Mrad @Room Temp** **149 Mrad @Low Temp -15°C**





[I. Mandic et al. NIM A 903, 2018]

→ Radiation tests at CERN-SPS with **proton** beam on **LF-CPIX** chip (**CPPM**)

→ 14% increase of noise after irradiation with cooling

Comparison of time resolution of unirradiated and 10^{14} 1 MeV neq chips

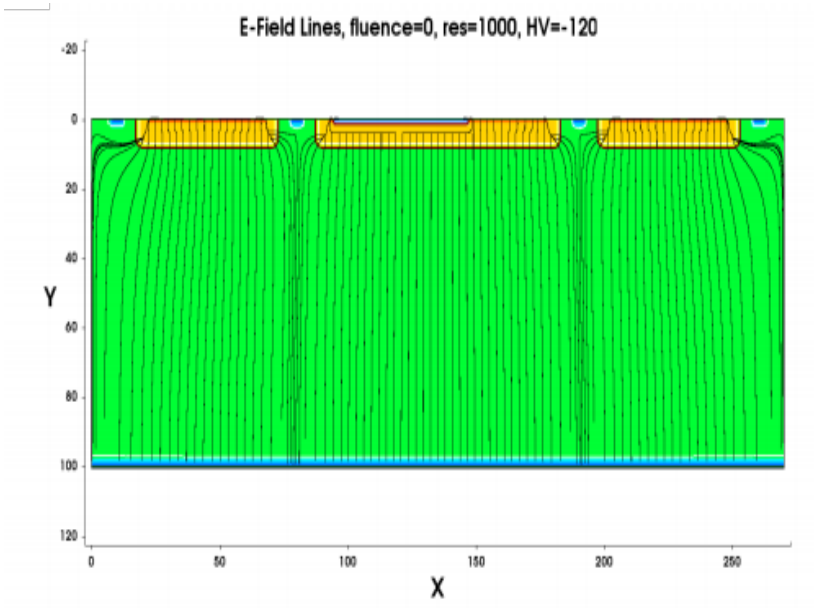
Sensor	HV bias (V)	Conditions	Temp. (°C)	Time res. (ps)	MPV (mV)
Unirradiated 300 u	400	testbeam, MCPMT time reference	room	78.97 ± 1.36	201.9 ± 0.5
Unirradiated 300 u	400	90Sr, PMT time reference*	room	104.5 ± 2.30	195.7 ± 2.3
Unirradiated 300 u	280	testbeam, MCPMT time reference	room	89.11 ± 1.56	200.9 ± 0.5
Irradiated 300 u	280	90 Sr, PMT time reference	20	108.2 ± 3.2 (PMT subt.)	108.2 ± 3.2
Irradiated 300 u	320	90 Sr, PMT time reference	20	132.9 ± 5.0 (PMT subt.)	113.5 ± 0.8
Irradiated 300 u	320	90 Sr, PMT time reference	-15	87.9 ± 4.7 (PMT subt.)	132.7 ± 0.6

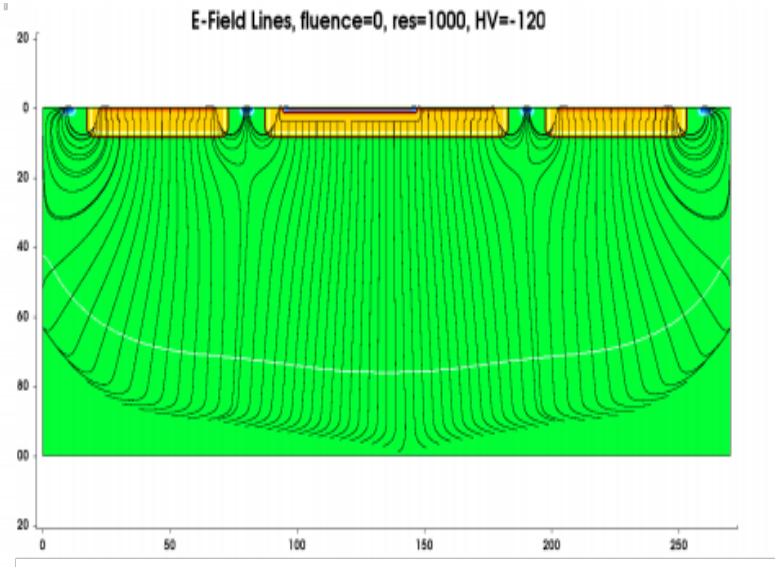
Irradiation at 10^{14} n_{eq} worsens time resolution by 18 % w.r.t. unirradiated at 20 °C

Cooling at -15°C brings time resolution more or less back to unirradiated performance (less dark current fluctuations)

*PMT resolution for 90 Sr betas estimated to be 71.3 ps ± 1.7 ps

ELECTRIC FIELDS





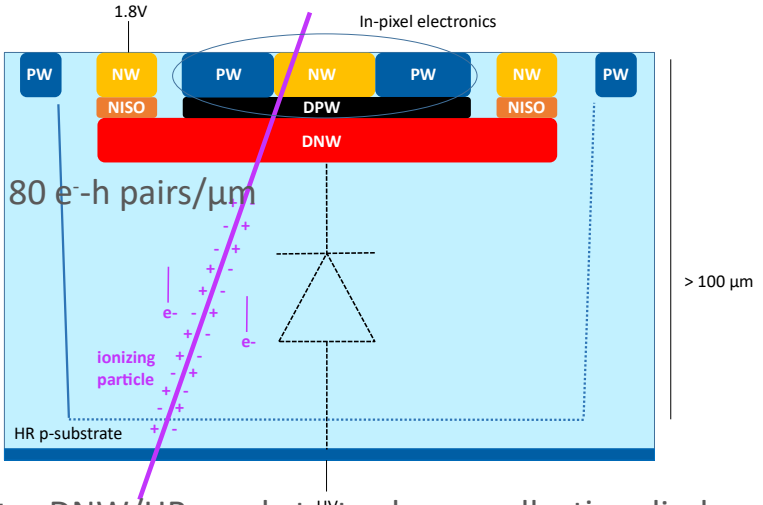
Backside versus top biasing → Need backside polarization to ensure best charge collection and signal shape uniformity!

TIMING WITH HV-CMOS/DMAPS*

*Depleted **MAPS**

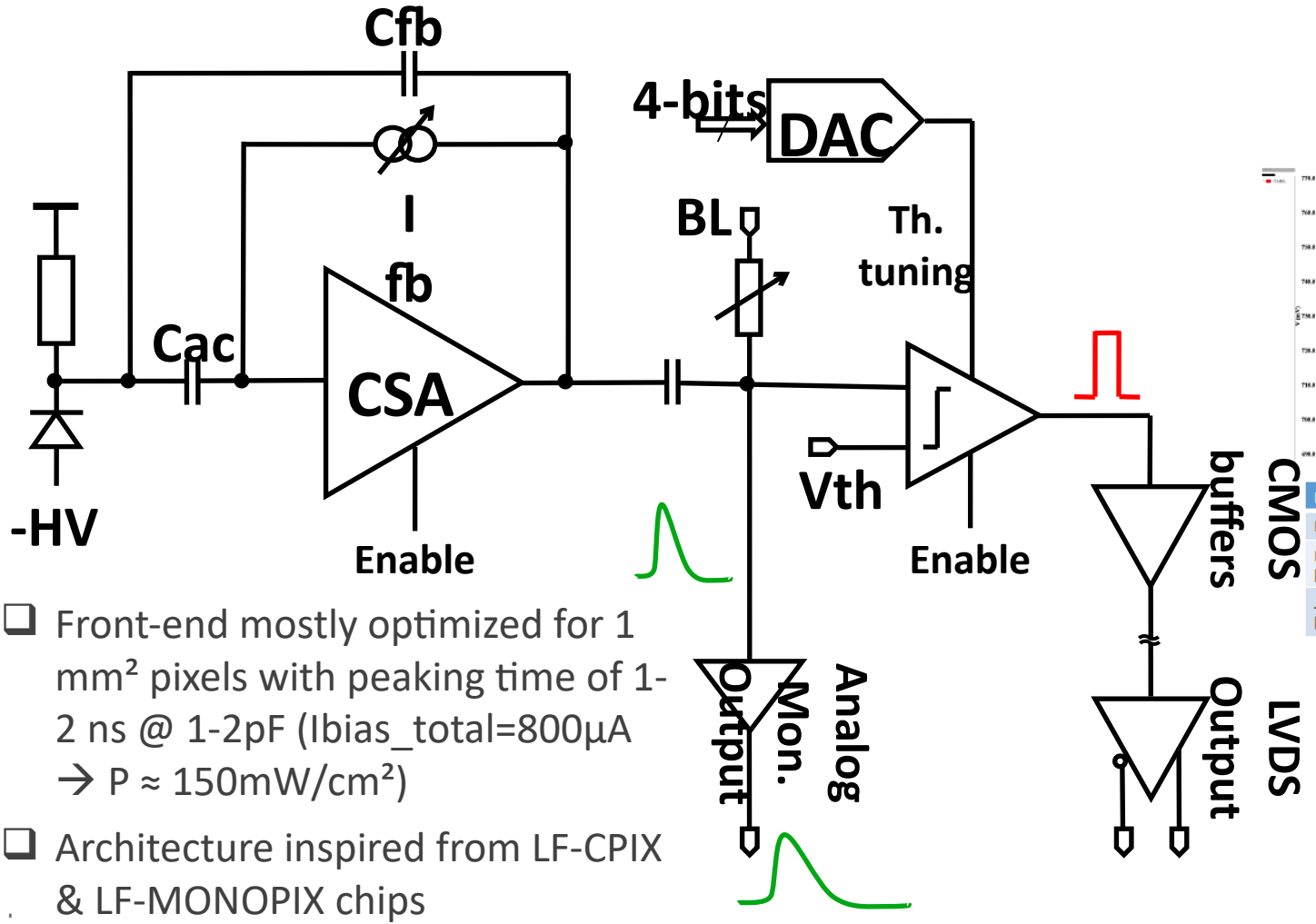
- The objective of our R&D is the development of a **monolithic timing sensor** in a **commercial HV-CMOS process** for future high energy physics experiments or for LHC upgrades (timing detectors, after phase 2 upgrades)
- **LFoundry 150 nm** HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (**LF-CPIX**, **LF-MONOPIX1**, **LF-MONOPIX2**) in this process with proven **radiation hardness** (Bonn, IRFU and CPPM coll.)

HV-CMOS Sensor Pixel



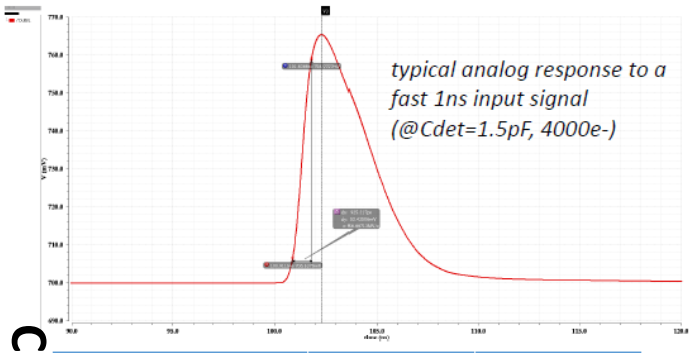
- DNW/HR p-substrate charge collection diode
- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 µm)
- **Charge collection by drift (fast)**
- **No internal amplification**
- Electronics can be integrated inside charge collection diode

ON-CHIP FRONT-END



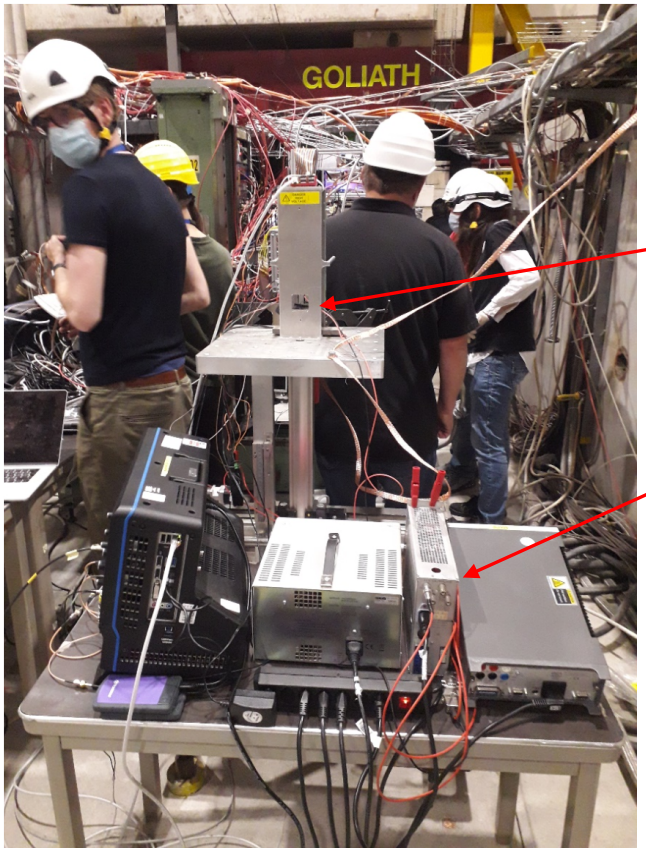
- Front-end mostly optimized for 1 mm² pixels with peaking time of 1-2 ns @ 1-2pF (Ibias_total=800µA → P ≈ 150mW/cm²)
- Architecture inspired from LF-CPIX & LF-MONOPIX chips

Typical CSA transient simulation result



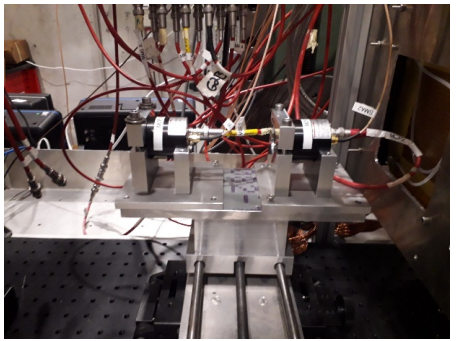
Parameter	1.5 pF	1 pF
Rise Time (from 10% to 90%)	~ 0.9 ns	~ 0.8 ns
Input Referred Noise [estimated from AC simulations]	~ 290 e-	~ 220 e-
Jitter [estimated from $t_r/(S/N)$]	~ 67 ps	~ 44 ps

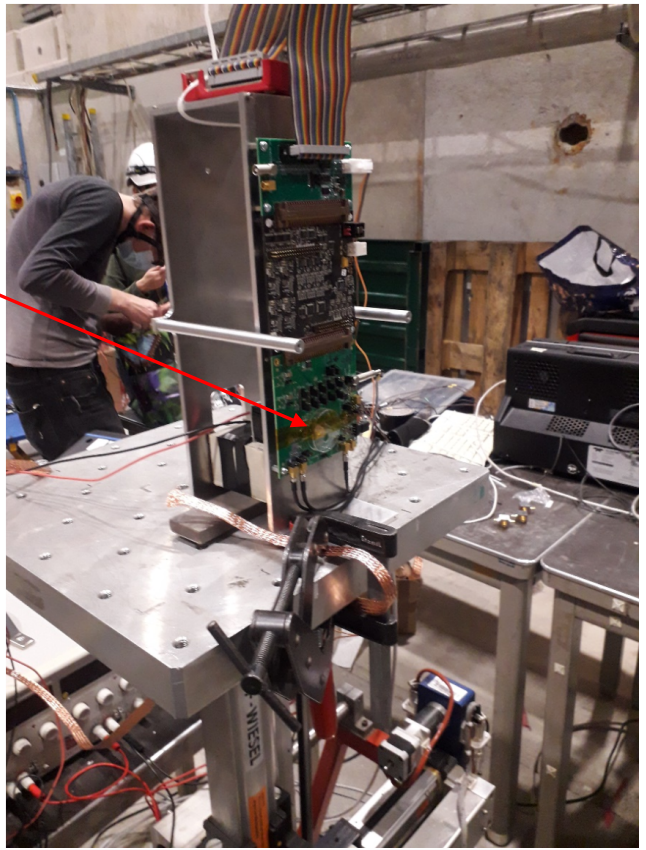
TESTBENCH OF MINICACTUS IN TESTBEAM



MiniCACTUS

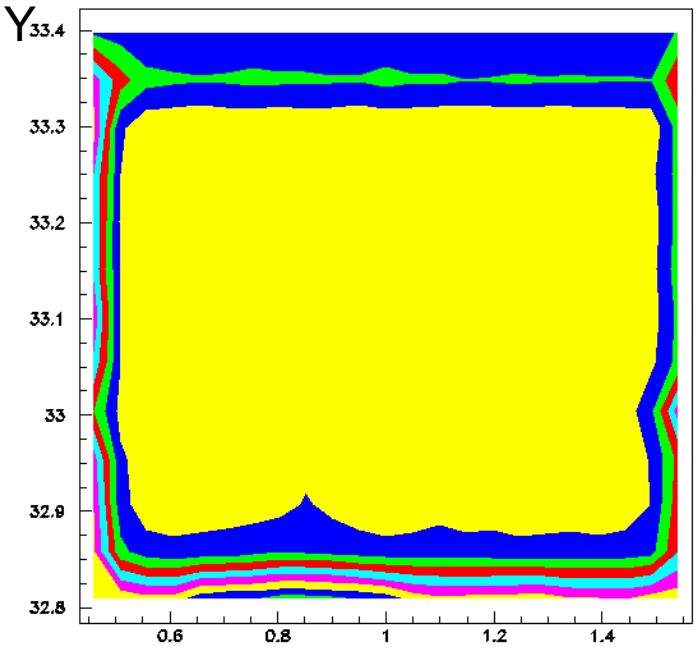
Power Supplies
(LV and HV)



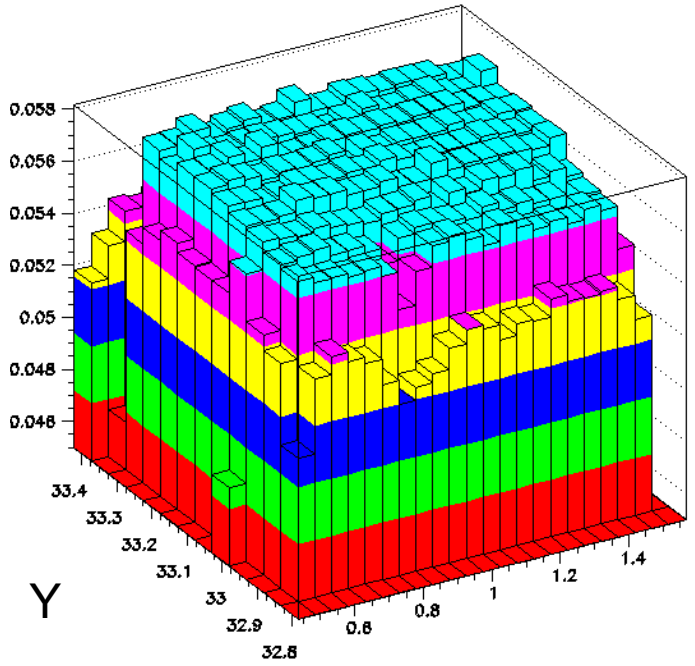


Time reference
RD-51 MCPs (resolution < 10 ps)

Pixel position scan at 20 keV with photons (data taken at Synchrotron Soleil)



Amplitude



Pixel has very good uniformity

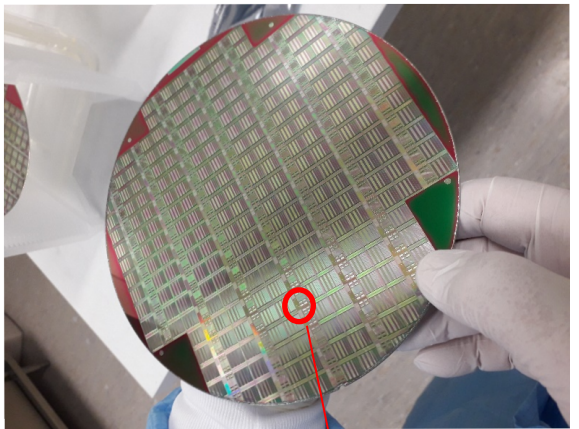
Used a pencil beam (50 microns by 50 microns) to scan pixel surface

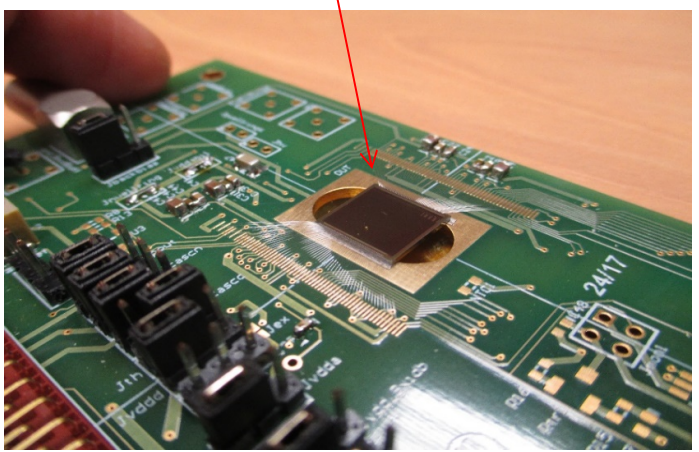
No non-uniformity found

CACTUS* DEVELOPMENT

*CMOS ACtive Timing µSensor

- The first demonstrator called **CACTUS** for timing in LF 150 nm process designed in 2019
- The front-end in CACTUS is based on an **in-pixel fast preamplifier** followed by a **leading edge discriminator**
- Time walk corrections done off-line by **ToT measurement**
- Expected timing resolution from Cadence & TCAD simulations: 50-100 ps





The CACTUS demonstrator on PCB
(chip size : 1 cm x 1 cm)