

First Experience with the Mu3e Vertex Detector Construction

Luigi Vigani University of Heidelberg Pixel 2024 22/11/2024



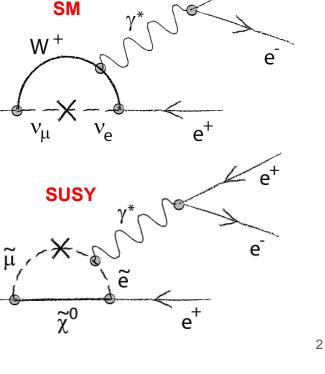


Mu3e: Physics Motivation

- Search for $\mu \rightarrow eee$
 - Standard Model: BR ($\mu \rightarrow eee$) < 10⁻⁵⁴
- New physics might enhance BR
- Current limit:
 - BR (μ → eee) < 10⁻¹² (SINDRUM, 1988)

 μ^+

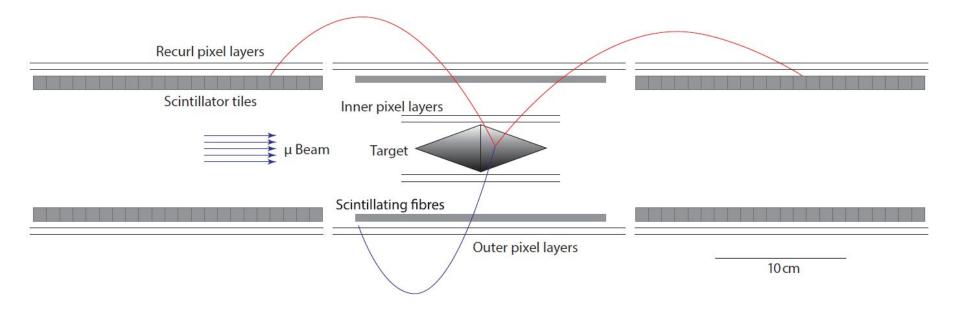
- Aimed single-event sensitivity:
 - BR (μ → eee) < 2 · 10⁻¹⁵ (Phase 1)
 - BR (μ → eee) < 10⁻¹⁶ (Phase 2)
- Location: PSI muon beamline
- Phase 1: under construction
- Phase 2: PSI High Intensity Muon Beamline





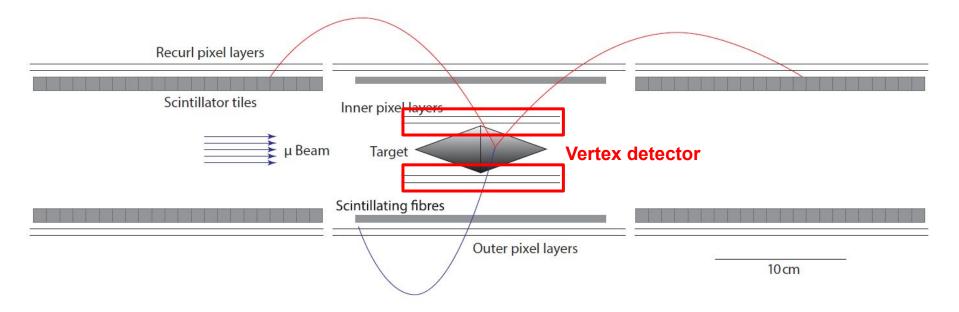


- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)



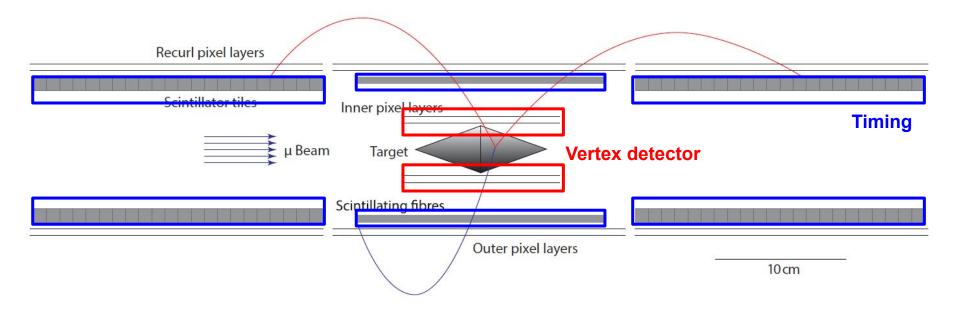


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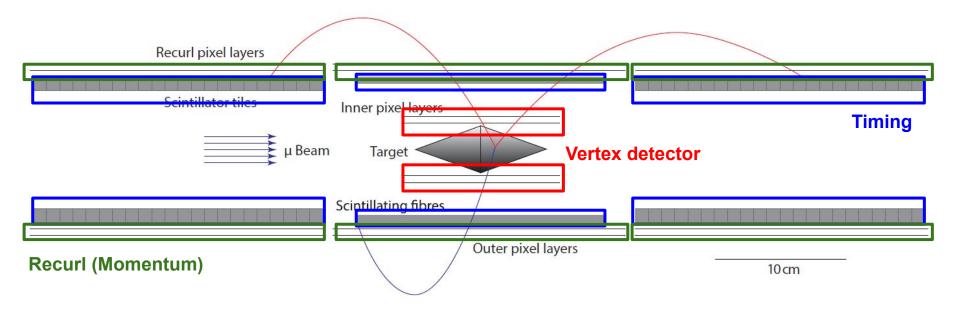


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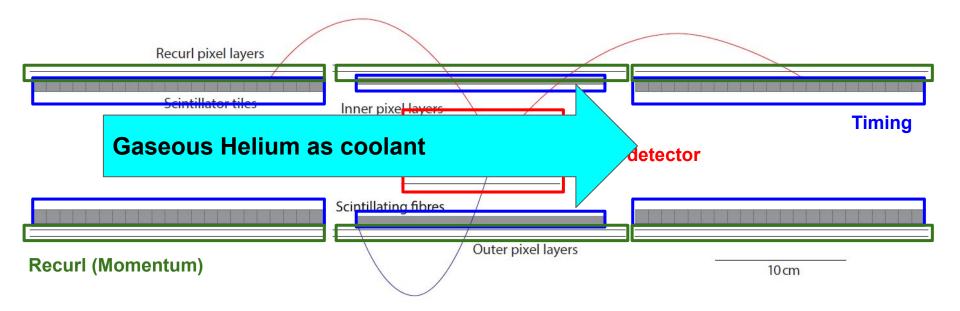


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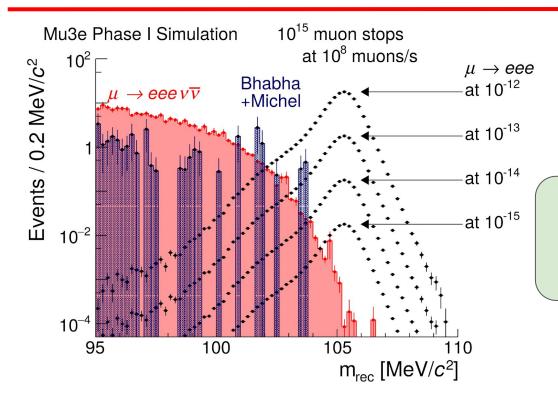




- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)



Experimental sensitivity



Invariant mass of signal decay, radiative decay and accidental background (Bhaba+Michel)

Momentum resolution crucial for detecting the peak at muon mass...

Material budget is key factor!

1 MeV resolution with 0.1% * X/X $_0$ per layer

Mu3e TDR at Nucl.Instrum.Meth.A 1014, 165679



Experimental sensitivity

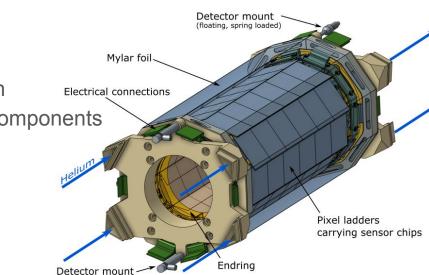




Invariant mass of signal decay, radiative decay and accidental background (Bhaba+Michel) [Mu3e TDR] Mu3e Collaboration Meeting Wengen 2024

Construction challenges for the pixel detectors

- Thin chips
 - Post-processing and qualification
 - Handling
 - QC
- Thin Aluminum-Kapton HDIs
 - Both electrical and mechanical integration
 - Reduced number of lines, no electronic components
- Compact design
 - Cabling and routing
- Helium cooling system [not in this talk]
 - ~250 mW/cm²
 - Helium plant
 - Flow control



Mu3e Vertex Detector

Vertex collaboration: Uni-Heidelberg, Uni-Zurich, PSI

(fixed)



10

Thin chips

0

10

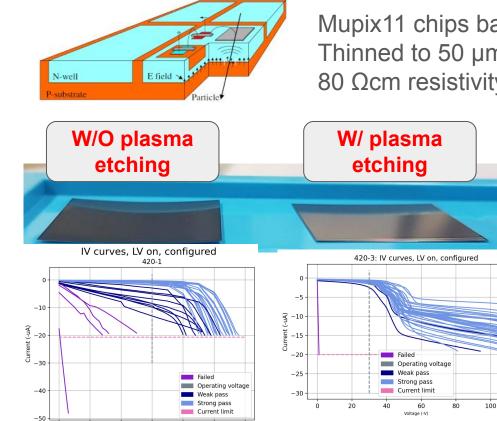
20

30

Voltage (-V)

50





Mupix11 chips based on HV-CMOS technology Thinned to 50 μm (Vertex) 80 Ωcm resistivity (380 Ωcm for first prototype modules)

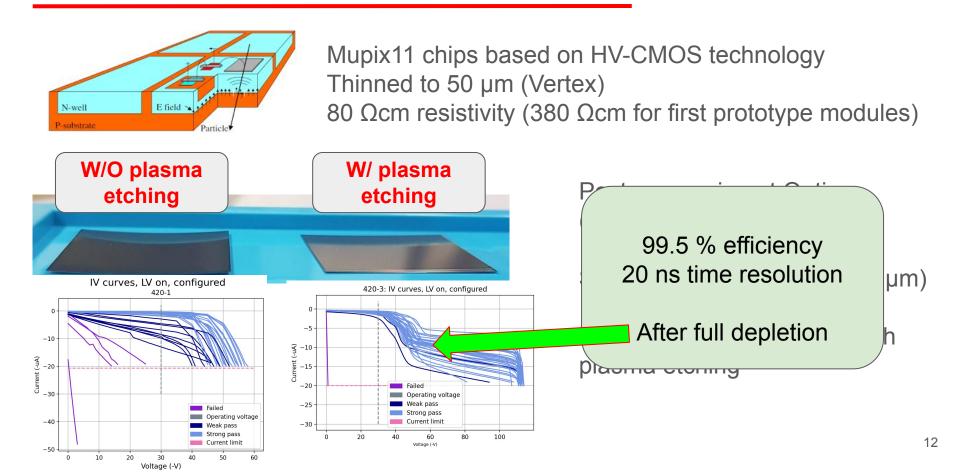
Post processing at Optim (Marseillle, France)

Small tolerance in dicing (11 µm)

Significant improvements with plasma etching

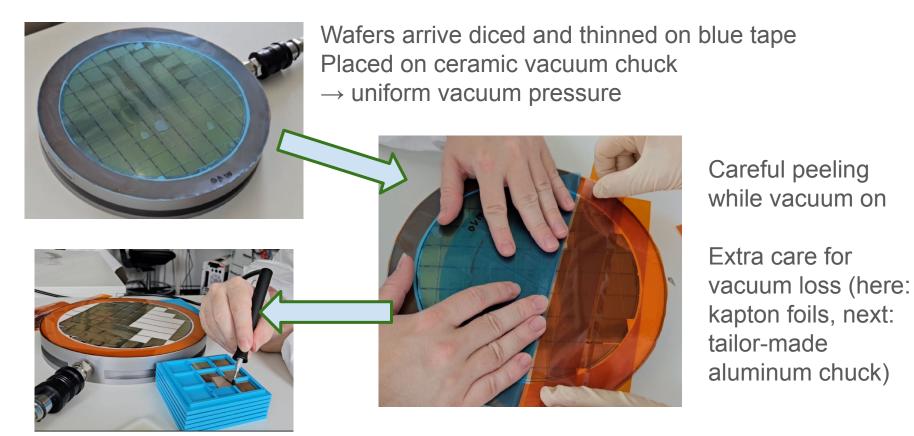
Thin chips





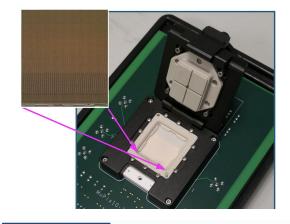
Thin chips: handling

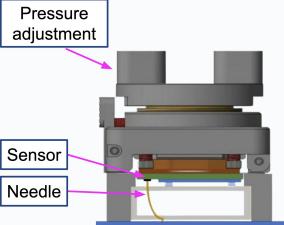




Thin chips: QC







Probe card with manual actuator developed for the task

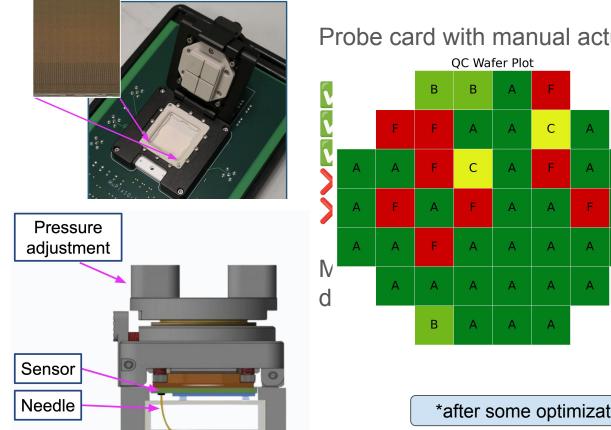
Table-top system
 No dependency on probe stations
 Easy to transfer between institutes
 Manual procedure (training required)
 Slow throughput (2-3 minutes to replace chips)

Note: Mu3e Vertex detector consists of only 108 chips and is developed between Heidelberg and PSI

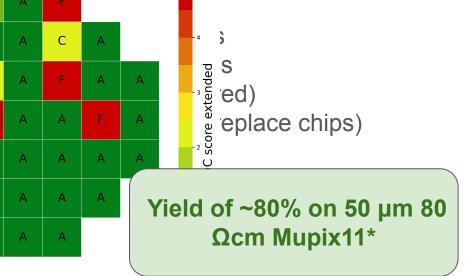
Several operational aspect investigated (IV curve, powering, link stability, noise profile,...)

Thin chips: QC





Probe card with manual actuator developed for the task



*after some optimization iteration

16

Thin HDIs

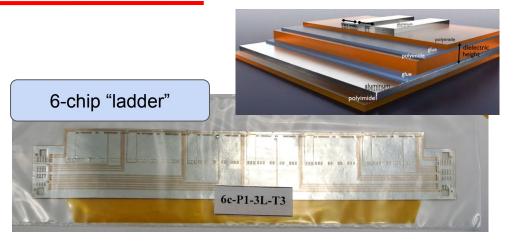
Katpon-Aluminum flexes produced by LTU (Kharkiv)

2 layers + spacer: stack and traces geometry optimized for LVDS transmission

HDIs for multiple purposes: power, HV, signal in, data out, mechanical support

HDI + 6 chips + connecting flex = "Ladder" (see poster by T. Senger, with QC)

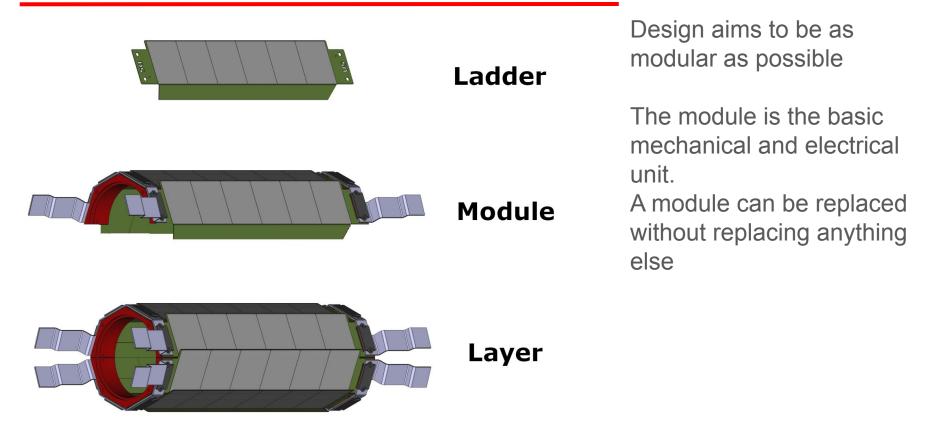
Long design and qualification stage needed.





Modules

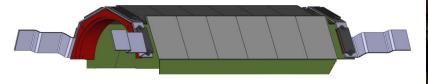


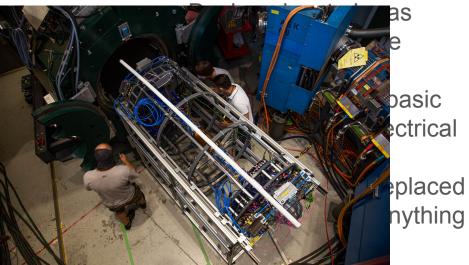


Modules











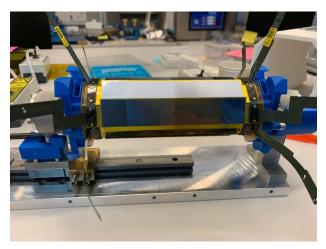
Layer

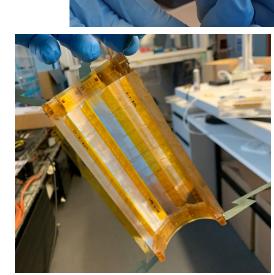
Note: Mu3e sits at ground level, relatively easy to access

Thin HDIs: mounting

Manual procedures:

- Aligning chips
- Glueing
- HDI overlay
- TA-Bonding
- Module assembly





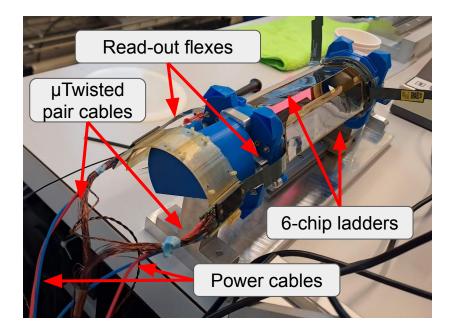




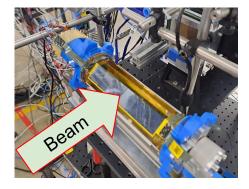
Thin HDI qualification



In the lab



In the testbeam area

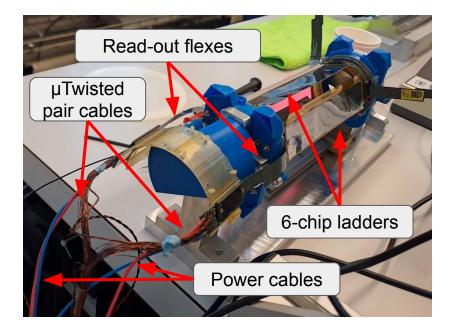




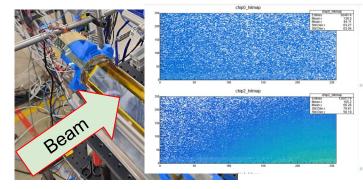
Thin HDI qualification



In the lab

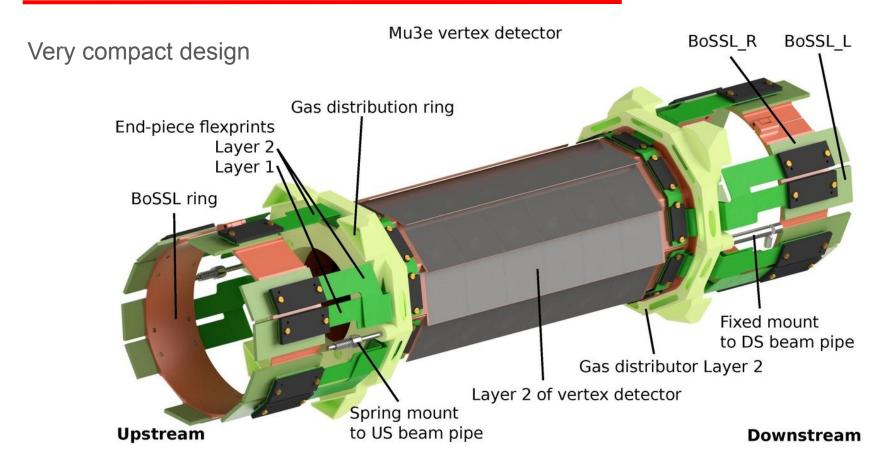


In the testbeam area

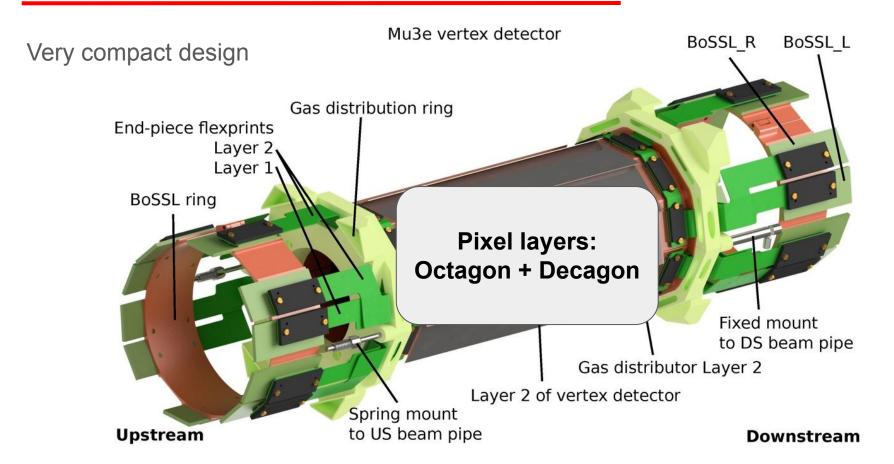




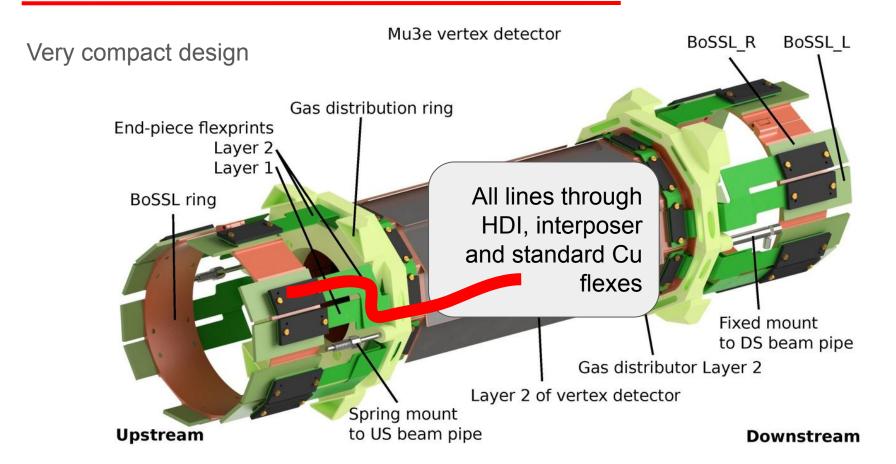




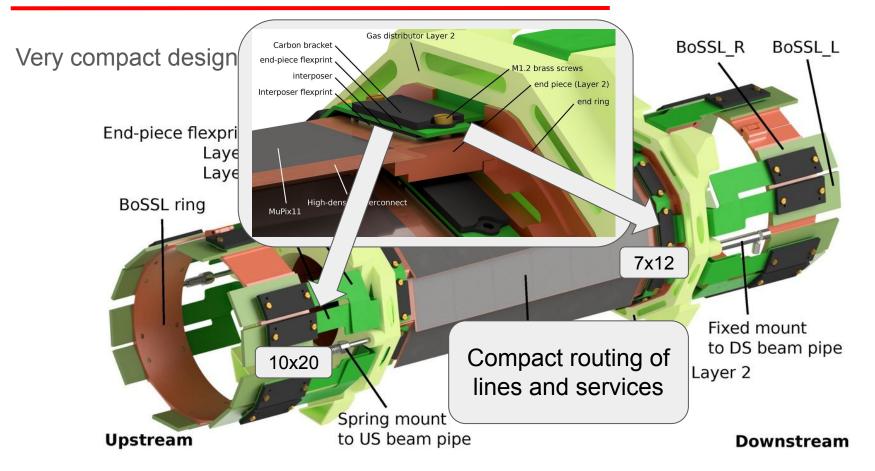




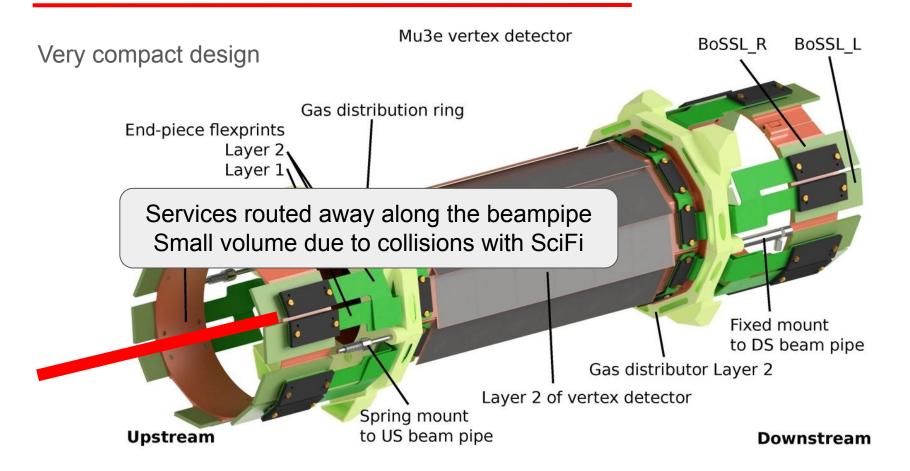




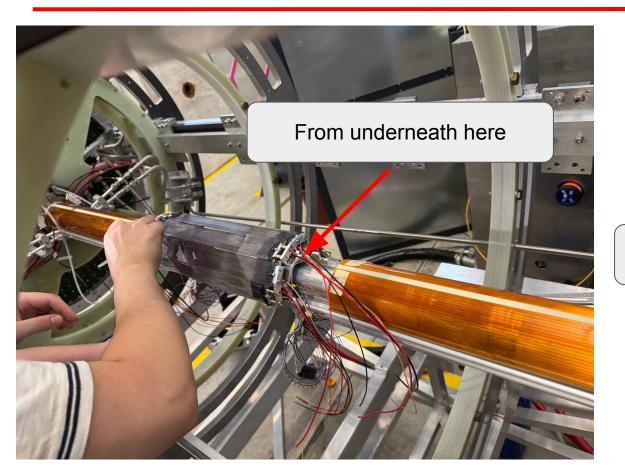


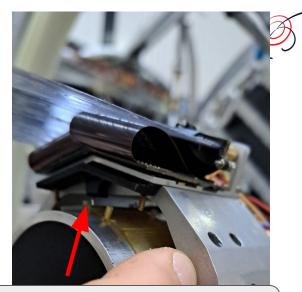






26



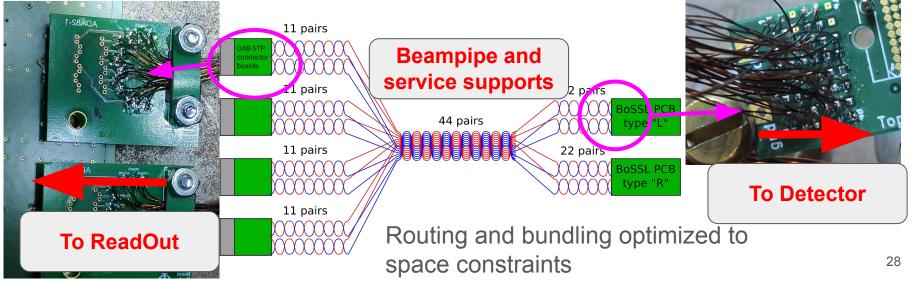


24 differential lines + 8 sense To be squeezed here



Solution:

- Micro-twisted pair cable bundles
 - 127 um copper, 25 μm polyimide, 30 μm extra distance for impedance matching
- Wires stripped and soldered directly on connector boards





Vertex Status



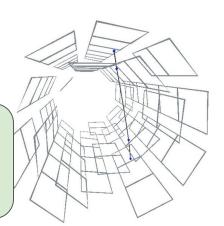
- Production almost finished
 - All chips qualified
 - \circ All ladders produced \rightarrow to be qualified
 - Module+layer assembly to follow
- Services currently mounted on cage
 - Cables + infrastructure + DAQ + cooling pipes + ...
- Vertex to be mounted by beginning of next year

Vertex Status

- Production almost finished
 - All chips qualified
 - \circ All ladders produced \rightarrow to be qualified
 - Module+layer assembly to follow
- Services currently mounted on cage
 - Cables + infrastructure + DAQ + cooling pipes + ...
- Vertex to be mounted by beginning of next year
- Qualification with cosmic run to follow



Performed previously with a Mupix10 Vertex prototype (slides from Vertex22)



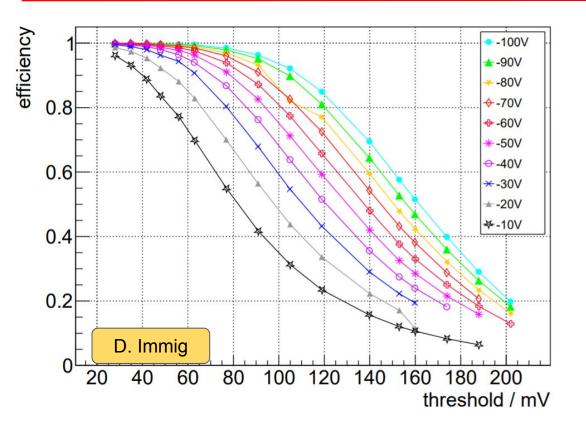


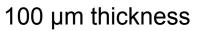
Backup



pixel size [µm ²] sensor size [mm ²] active area [mm ²] active area [mm ²] sensor thinned to thickness [µm] LVDS links maximum bandwidth [§] [Gbit/s] timestamp clock [MHz]	$ \begin{array}{r} 80 \times 80 \\ 20 \times 23 \\ 20 \times 20 \\ 400 \\ 50 \\ 3 + 1 \\ 3 \times 1.6 \\ \geq 50 \end{array} $
RMS of spatial resolution [µm] power consumption [mW/cm ²] time resolution per pixel [ns] efficiency at 20 Hz/pix noise [%] noise rate at 99% efficiency [Hz/pix]	$ \leq 30 \\ \leq 350 \\ \leq 20 \\ \geq 99 \\ \leq 20 $

MuPix10: results





110 V breakdown

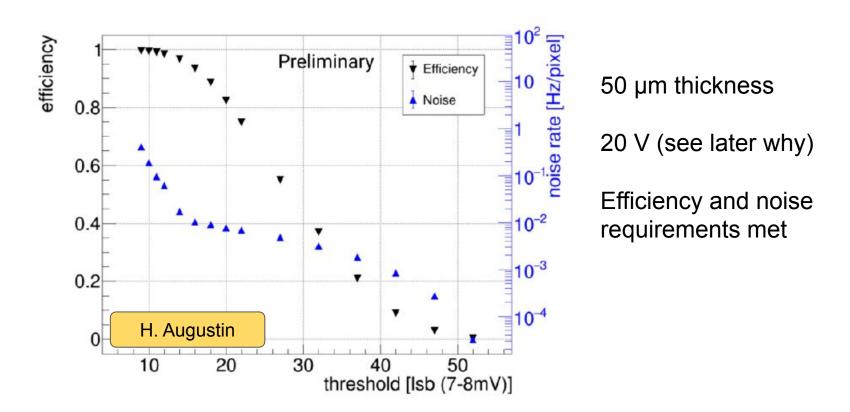
Efficiency plateau well defined above 20 V





MuPix10: results





Mupix10 detailed studies



Testbeam at DESY

Alpide telescope

6 layers

5 µm resolution

EuDAQ + Corryvreckan



Mupix10 detailed studies



99.92%

99.85%

99.77%

99.69%

99.61%

99.53%

99.45%

99.38%

99.30%

98.82%

97.58%

96.33%

\$6.09%

93.84%

92.59%

91,35%

90.11%

88.85%

20

20

30

in-pixel xtrack [µm]

30

in-pixel xtrack [µm]

-60 V

0 V

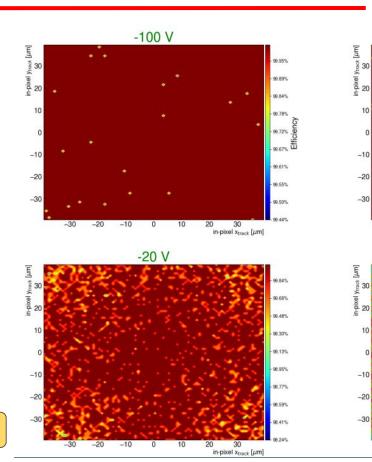
-30

-20

In-pixel efficiency

100 μm thick

43 mV threshold

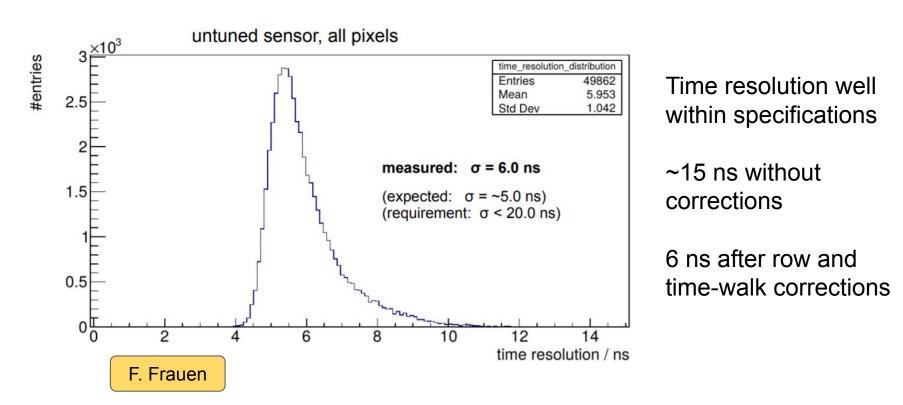






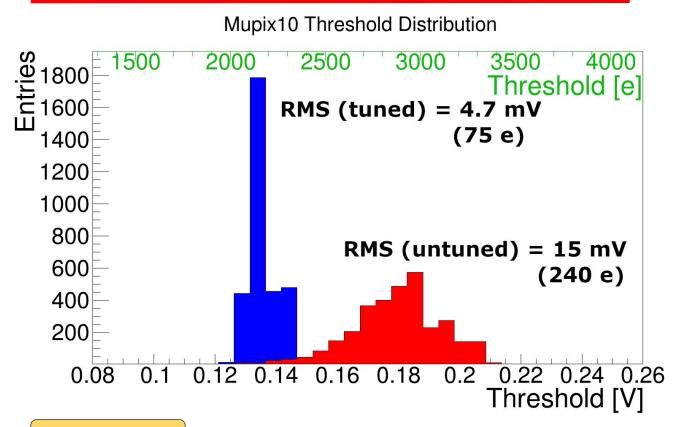
MuPix10: results





MuPix10: results





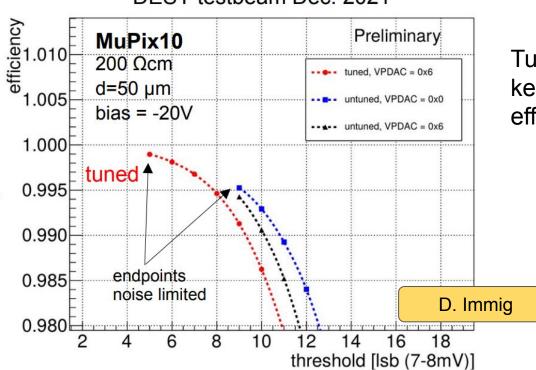
Tunable threshold for each pixel

Tuning with threshold scans:

Low threshold dispersion

MuPix10: results



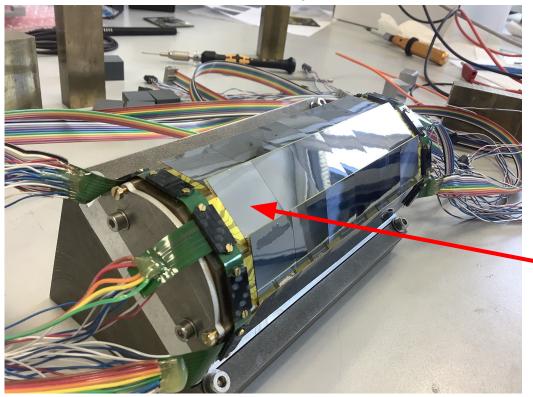


DESY testbeam Dec. 2021

Tuning by lowering threshold while keeping noise constant: maximize efficiency!



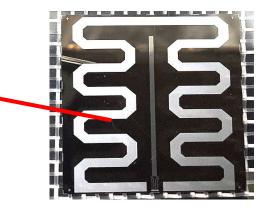
Thermo-mechanical stability



Silicon heater prototype

Reproduction of inner tracker with same materials and connections

Chips are just passive silicon heaters



Thermo-mechanical stability



Silicon heater prototype

Test stand with Helium cooling system



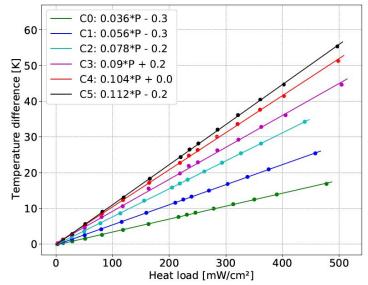
Thermo-mechanical stability



- Temperature difference linearly depending on heat dissipation
- Expected ΔT < 70 K for 350 mW/cm² (conservative limit)
- Cooling concept works 🔽
- More detailed studies to come

Silicon heater prototype

Temperature to power relation for Layer 0 Ladder 1

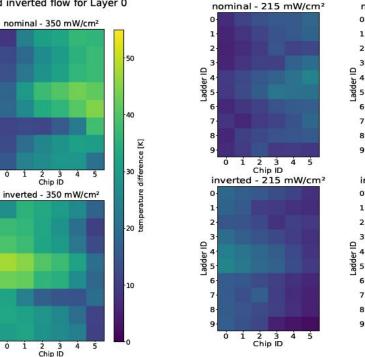


42





Thermo-mechanical stability



Comparison of nominal and inverted flow for Layer 0

0

2

Ladder ID

5

0

2

A w

5 6

0

Ó

5

5

nominal - 215 mW/cm²

0

1

2

Ladder ID

Ó

0

1

2

tadder ID

0

2

2 3

Chip ID

Chip ID

inverted - 215 mW/cm²

Silicon heater prototype

10

-50 Ladder 40 o temperature difference [K] 0 1 2 3 4 5 Chip ID inverted - 350 mW/cm²

3

ò

1

2 3 4 5

Chip ID

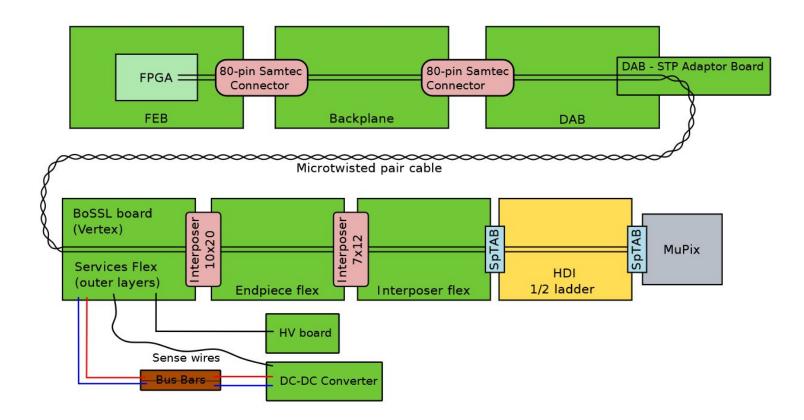
Comparison of nominal and inverted flow for Layer 1

n

nominal - 350 mW/cm²

Vertical slice breakdown





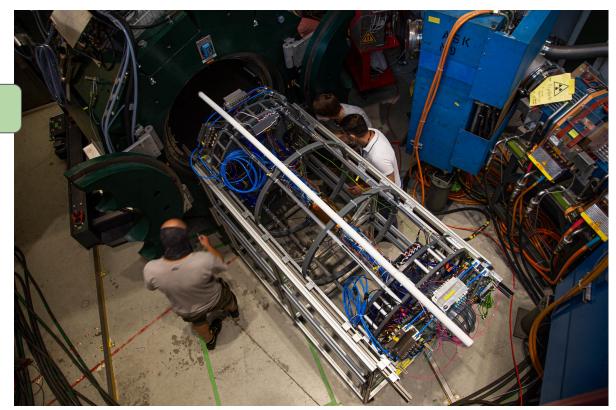
Operation in experimental conditions

Mag

DAQ and experimental concept

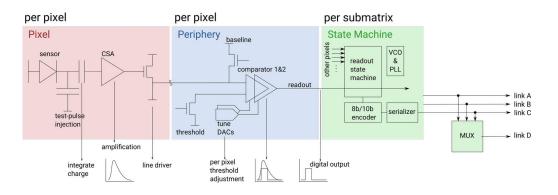
Inside Magnet

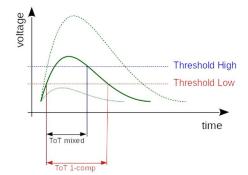
More pics at https://www.flickr.com/pho tos/nberger/albums/72157 719305216074/page1/





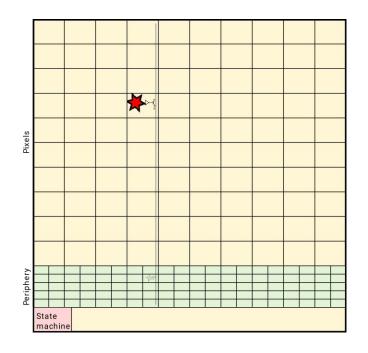
MuPix Architecture





- Clear separation of analog and digital electronics
- 2 comparator design
- Tuning/Trimming and masking available
- Priority encoder / column-drain readout
- Chip sub-divided into 3 matrices \rightarrow 1 Data link each + 1 multiplexed link

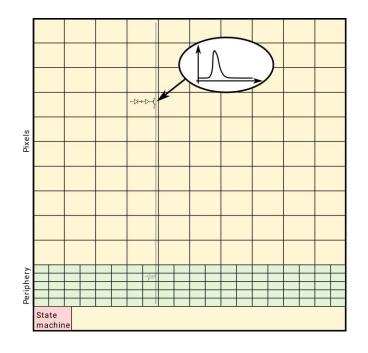




- Deposited charge amplified by in-pixel amplifier
- Source follower drives the signal to the periphery
- Digitisation in periphery
- . Timestamp sampling
- Readout statemachine manages
 column-drain readout
- Data is send out via a 1.25 Gbit/s differential link

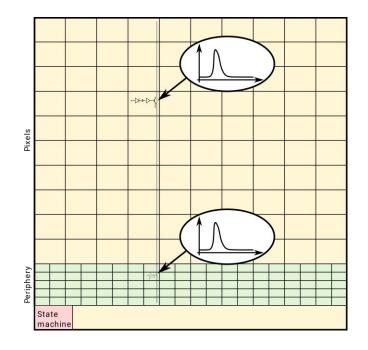
Courtesy: Frank Meier





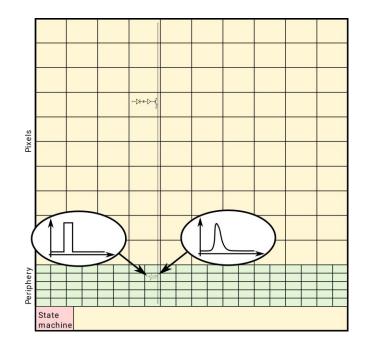
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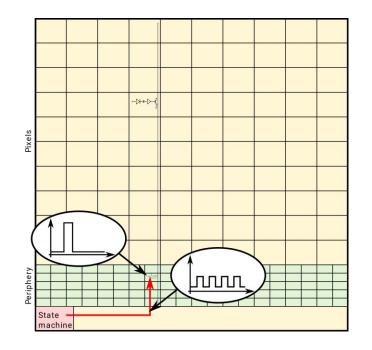
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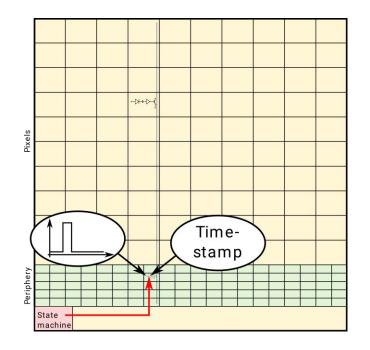
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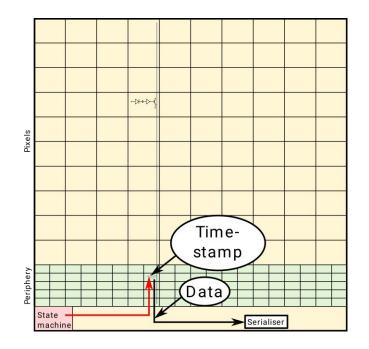
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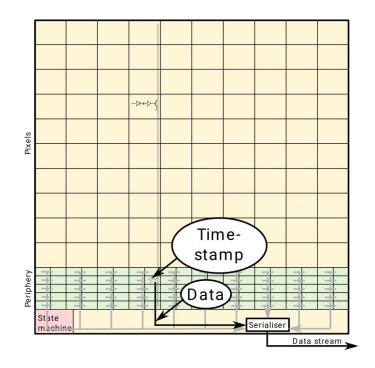
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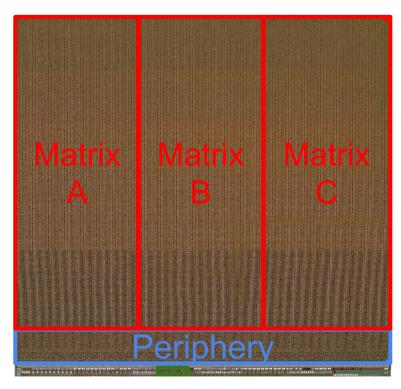




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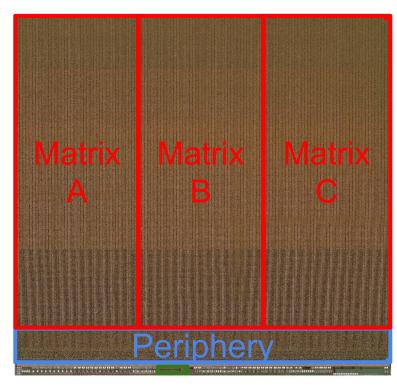
MuPix10 & MuPix11



Pixel size [µm²]	80 x 80
Sensor size [mm ²]	20.66 x 23.18
Active size [mm ²]	20.48 x 20.0
Pixel matrix	256 x 250
Thickness [µm]	50, 70
Substrate [Ωcm]	80, 370
Data links	3+1
Data speed [Gbit/s]	1.25
Time-of-arrival [bits]	11
ToT [bits]	5
TS binning [ns]	8 (option for 1.6)



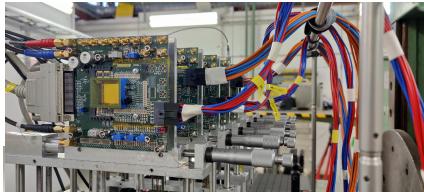
From MuPix10 to MuPix11



- Removal of R&D features
 - → More pads for powering
- Improvement of powering grid
 - Less on-chip voltage drop
- Buffering of data lines
 - Full speed readout
 30 MHits/s per sub-matrix
- Re-synthesis of State machine
 - ➡ Fast configuration interface available
- Re-done pixel point-to-point connection
 - Reduced delays and parasitic couplings



Sensor Characterisation



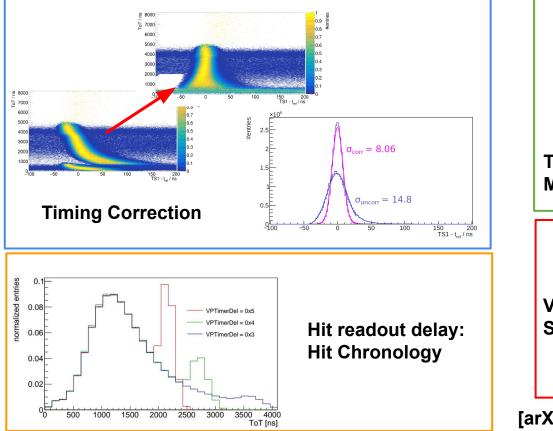


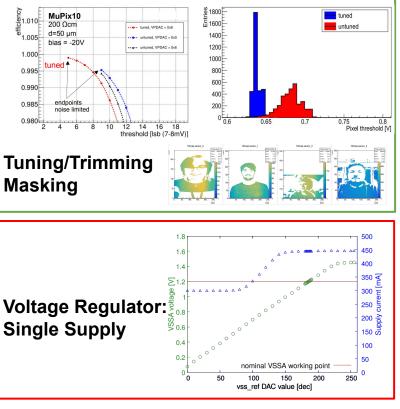


- Lab commissioning
- Lab optimisation: Radioactive sources: ⁵⁵Fe, ⁹⁰Sr Time coincidence
- Testbeam Campaigns: DESYII (Hamburg, GER) MAMI (Mainz, GER) PSI piM1 (Villigen, CH)
- MuPix-Telescope
- Mimosa/Alpide-Telescopes



Summary - Results MuPix10

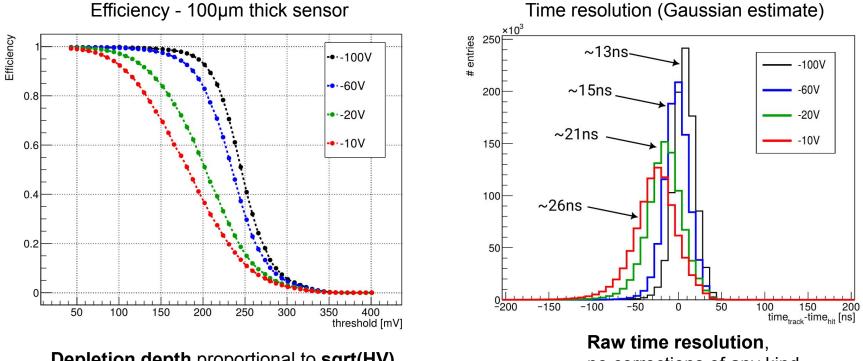




[arXiv:2012.05868] & VERTEX2022

MuPix11 - First Light

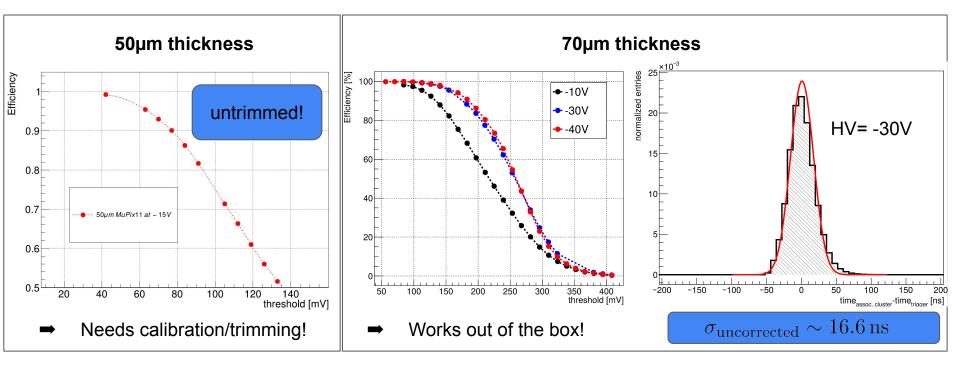




no corrections of any kind

Depletion depth proportional to sqrt(HV)

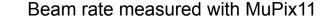
MuPix11 - Efficiency for 50 and 70 μm

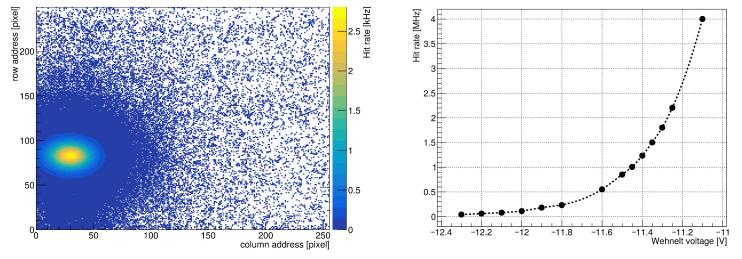


Mu3e: 50µm sensors for the vertex detector (~100 Sensors) 70µm sensors for the outer layers (~3000 Sensors)





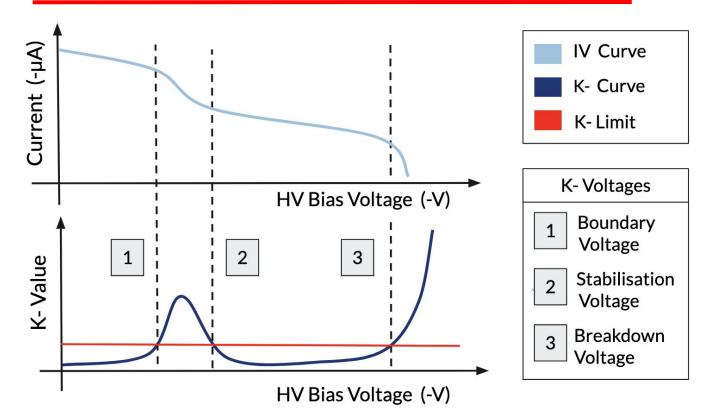




No Readout saturation visible @ 4 MHz Hitrate

Average Rate on "Hottest" Sensor 6 MHz

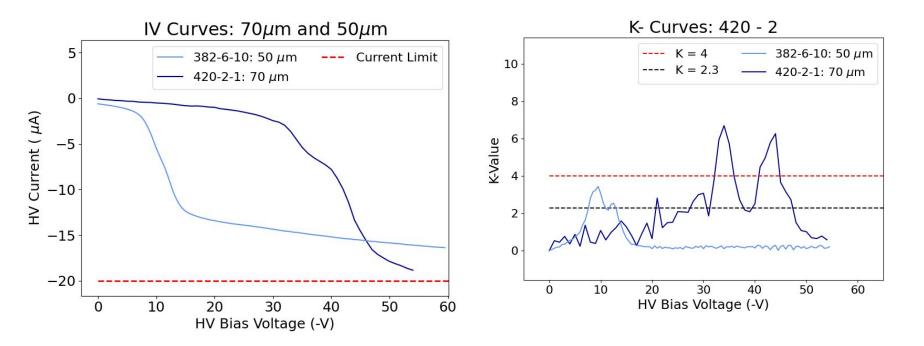
IV issues





IV issue





IV issues



