

Integration Concept of the CBM Micro Vertex Detector

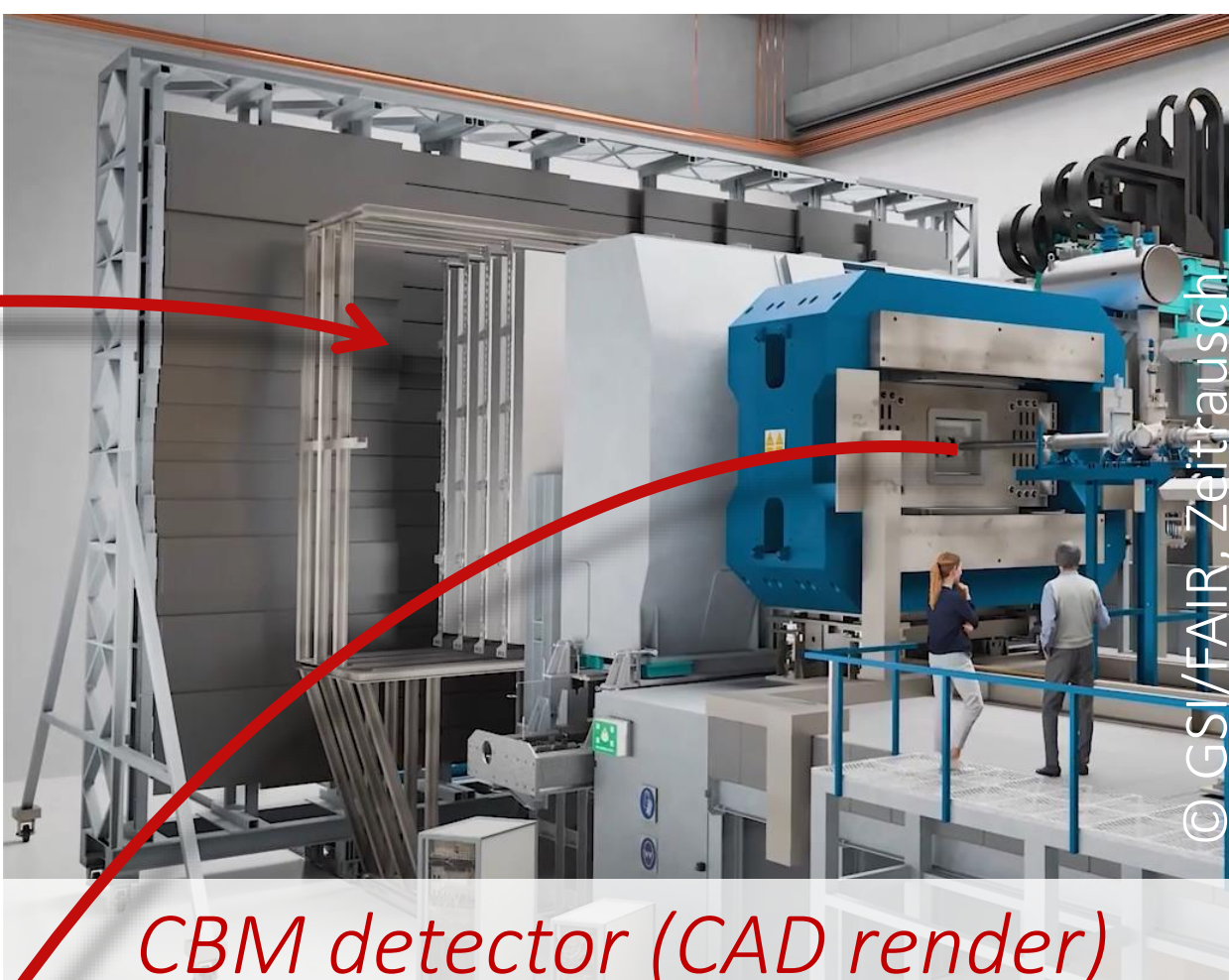


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The Compressed Baryonic Matter Experiment at FAIR

CBM at FAIR & Its CMOS MAPS-based Micro Vertex Detector

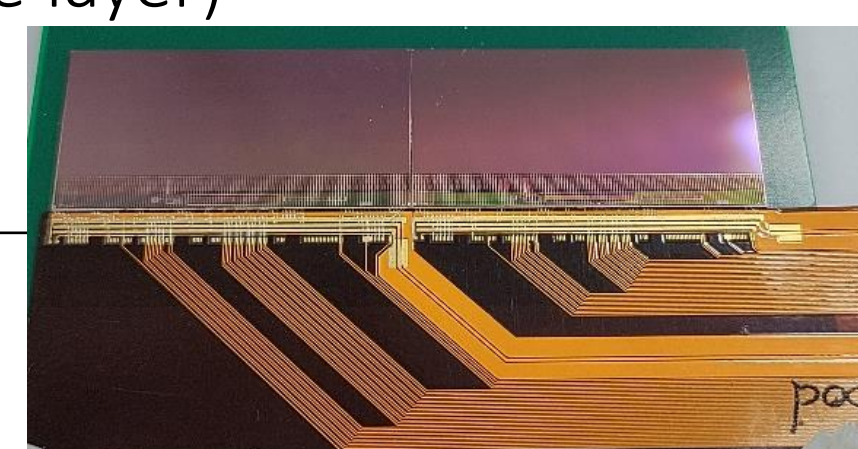
Compressed Baryonic Matter (CBM)
Fixed-Target heavy ion experiment at FAIR
 $\leq 10^7$ reactions/s at $\sqrt{s_{NN}} = 2.9 - 4.9$ GeV
High μ_b , moderate T
Electron and Muon Setup
Multi-differential measurements, rare probes
Trigger-less free-streaming readout
Online event selection, 4-D event reconstruction



Micro Vertex Detector (MVD)
4 planar layers at $z = 8 - 20$ cm
 $2.5 - 25^\circ$ azimuthal acceptance
In vacuum, mounted to 'front flange'
Inside 1 T-m magnet dipole field
 ≈ 0.15 m² area, 288 sensors, 150M pixels
CMOS MAPS (MIMOSIS; TJ180 nm)
 $\approx 0.3\% - 0.5\% X_0$ per layer

Electrical Integration

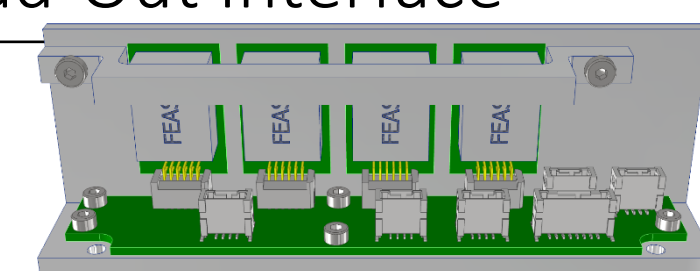
Sensor FPC (R&D phase)
Power, Bias, SC, Data connection
Baseline: 12 μ m Cu-traces (ILFA)
 $\approx 0.05\% X_0$ (single layer)
2 sensors per FPC
R&D on Al FPCs



Front-End Board - FEB (R&D phase)
GBT-SCA for SC
Power, Bias, SC, Data interface

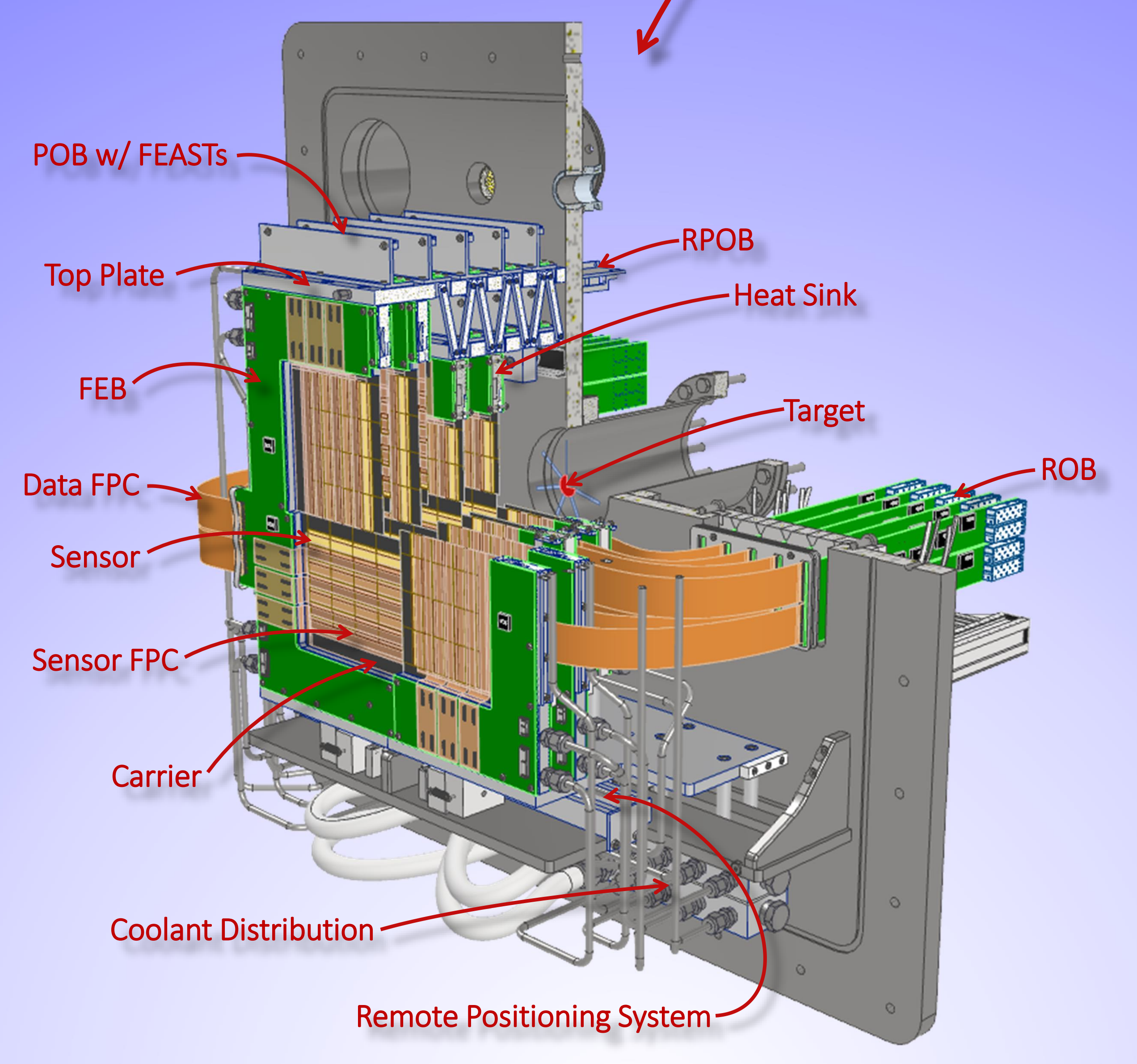
Data FPC (R&D phase)
Clock, Data connection
3 layers, 18 μ m Cu-traces

Read-Out Board - ROB (Design Phase)
GBTx, SCA, VTTx, VTRx
30 uplinks per ROB (844 links total)
Connects Common Read-Out Interface



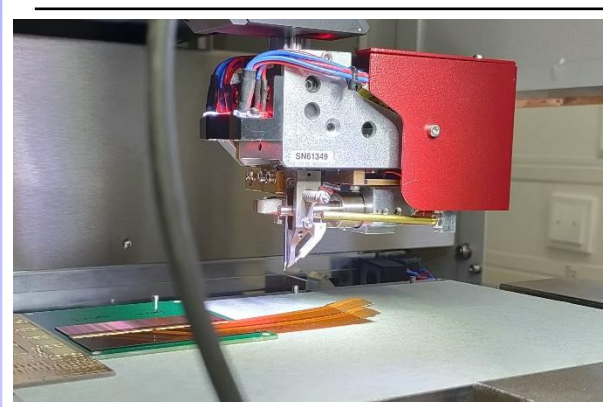
Power Boards - POB (R&D phase)
PCBs w/ 4, 5, or 6 FEASTMP
Sensor and ROB powering
Liquid/Air cooled (in-/outside vacuum)

Specifications
31.15 x 17.25 mm², 1024 x 504 pixels
70 (50) μ m thick with 50 (25) μ m epi-layer
AC and DC pixels, Std. (ALPIDE) and p-Stop epi
Back bias up to 6 V, HV up to 20 V
20 (80) MHz/cm² mean (peak)
Priority encoding, on-matrix clustering



Mechanical Integration

Carrier (ready for pre-production)
Thermal Pyrolytic Graphite (TPG)
 $\approx 0.2\% X_0$ (380 μ m), $>1500_{xy}$ W/mK
Mechanical support and cooling
Cut and μ -structured with laser ablation
Parylene-C coating + plasma activation



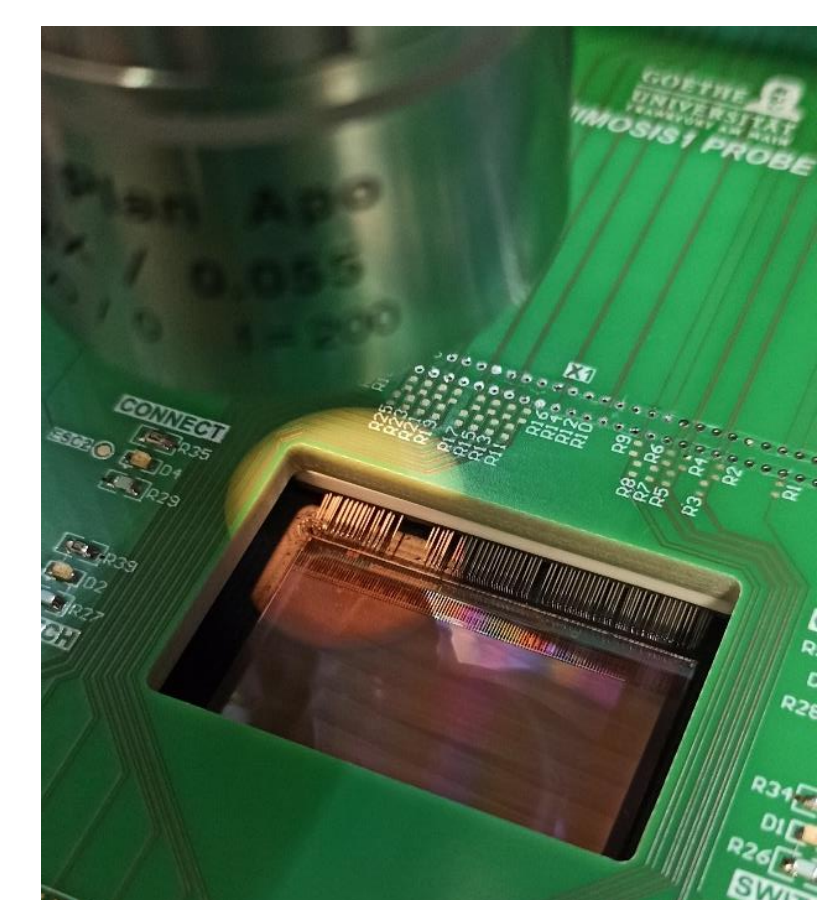
Double-sided Integration
Full coverage of geometric acceptance
Double-sided wire-bonding (25 μ m Al)
EpoTek 301-2 low-viscosity epoxy (sensors)
3M™ Tape 9461P (FPCs)

Cooling (ready for pre-production)
Conductive inside, active outside acceptance
Mono-phase liquid 3M™ Novec 649 ($\approx -20^\circ$ C)
Heat sinks: integration jigs and detector frame
Upstream electronics air cooled



Remote Positioning System
Safe position 5 cm lateral displacement
Two independent, rigid half-detectors
Pneumatic motor, rail system
Adjustable end stops

MIMOSIS CMOS MAPS



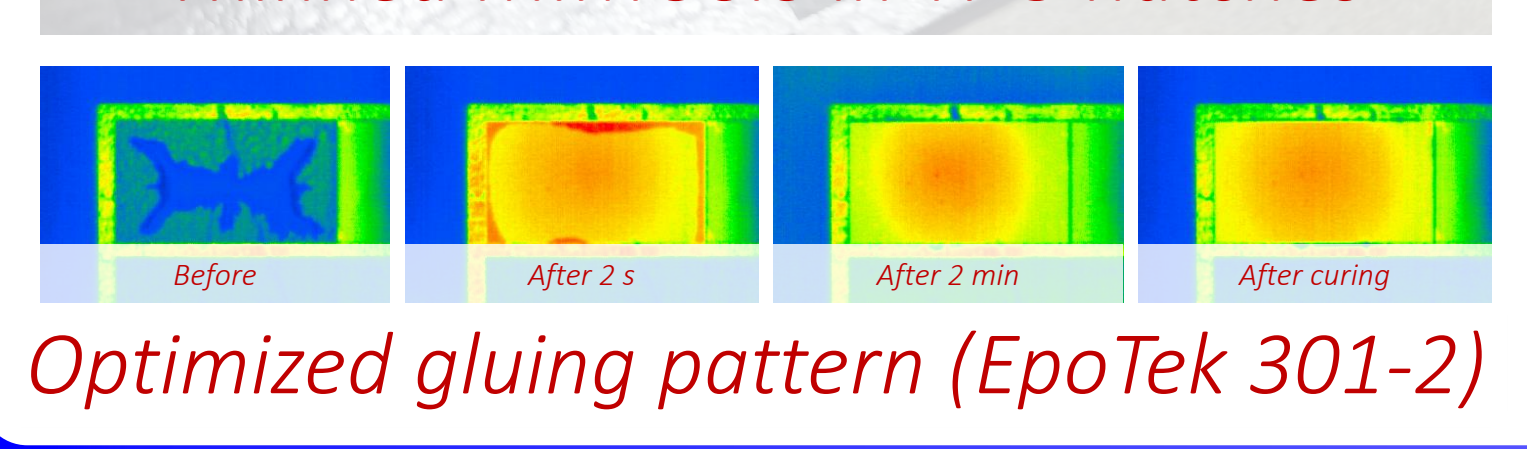
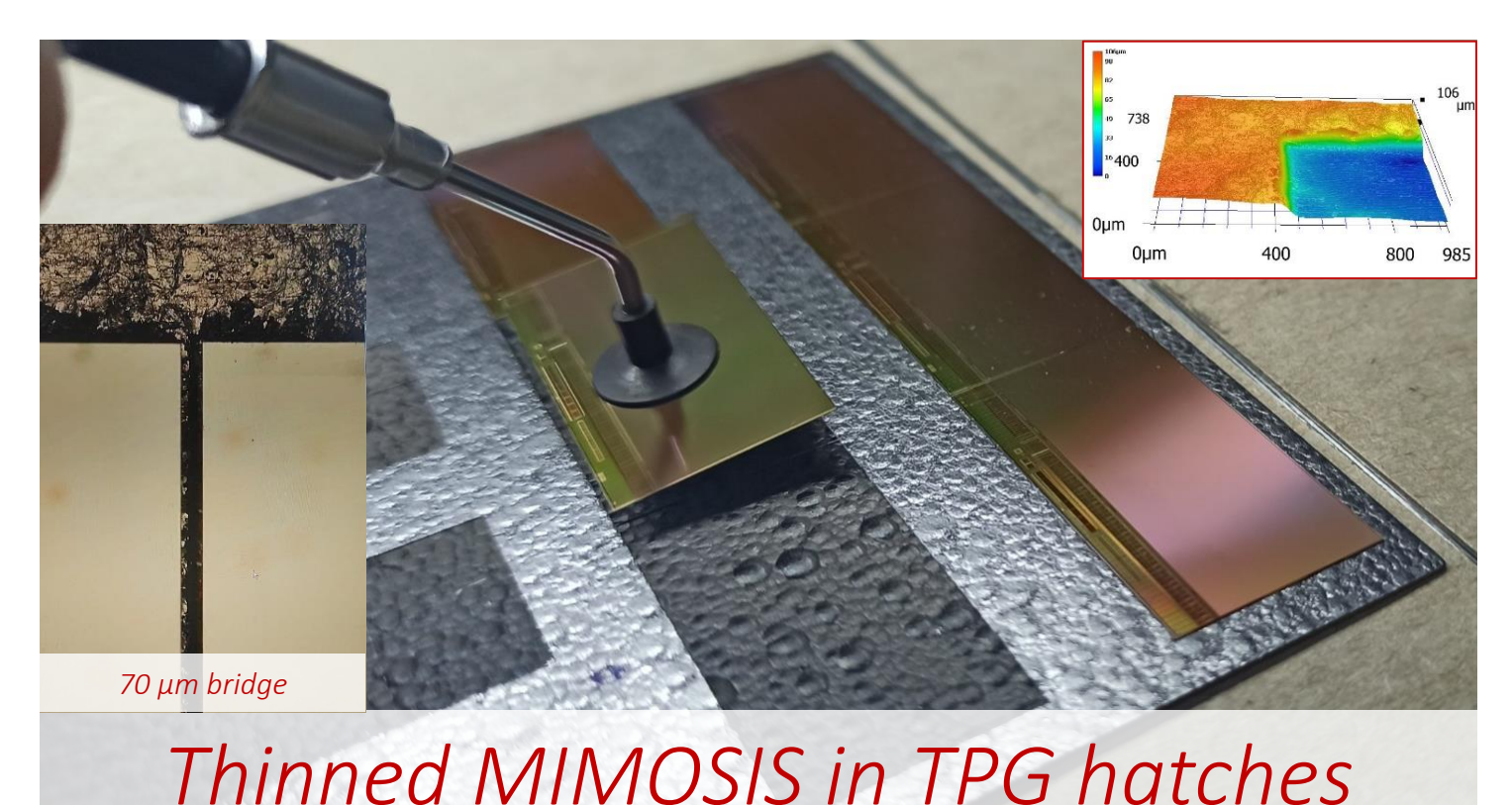
QA (Probe Testing)	
Analog and digital power	Data output mode
Back bias sweep	DAC scan
Register addressing, crosstalk, r&w	Analog scan (pulsing)
Chip ID	Threshold scan (S-curves)
	Dead, noisy pixels



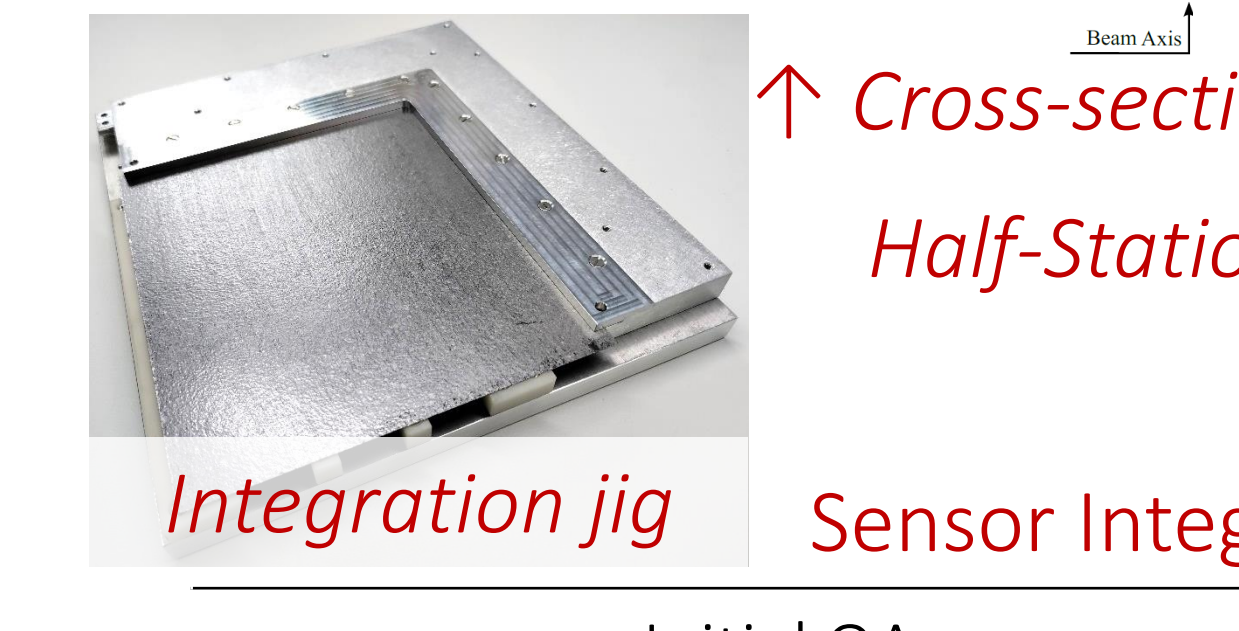
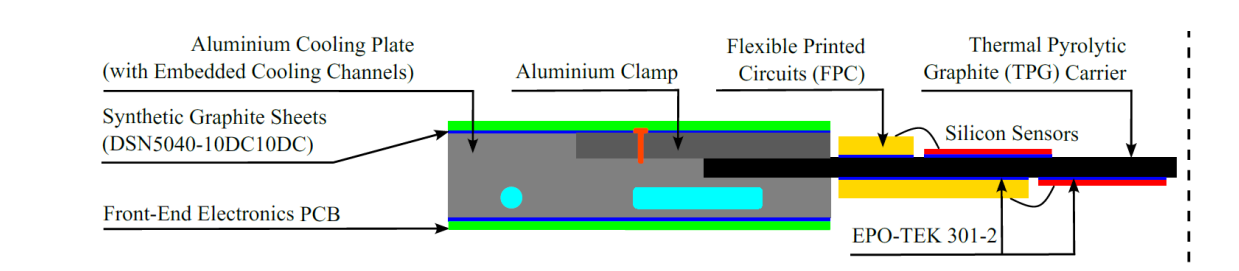
Performance
Power density $p \ll 75$ mW/cm²
GMDS ≥ 80 e, efficiency $\gg 99\%$
 $\sigma_{xy} = 6 \mu$ m ($\sigma_z = 70 \mu$ m), $t_{frame} = 5 \mu$ s
MIMOSIS-2.1: Irradiation campaign ongoing
MIMOSIS-2.1: No LU for LET ≤ 50 MeV cm²/mg (preliminary)
MIMOSIS-1: In specs up to 10^{14} n_{eq}/cm², 5 Mrad (preliminary)

Aspects of Integration

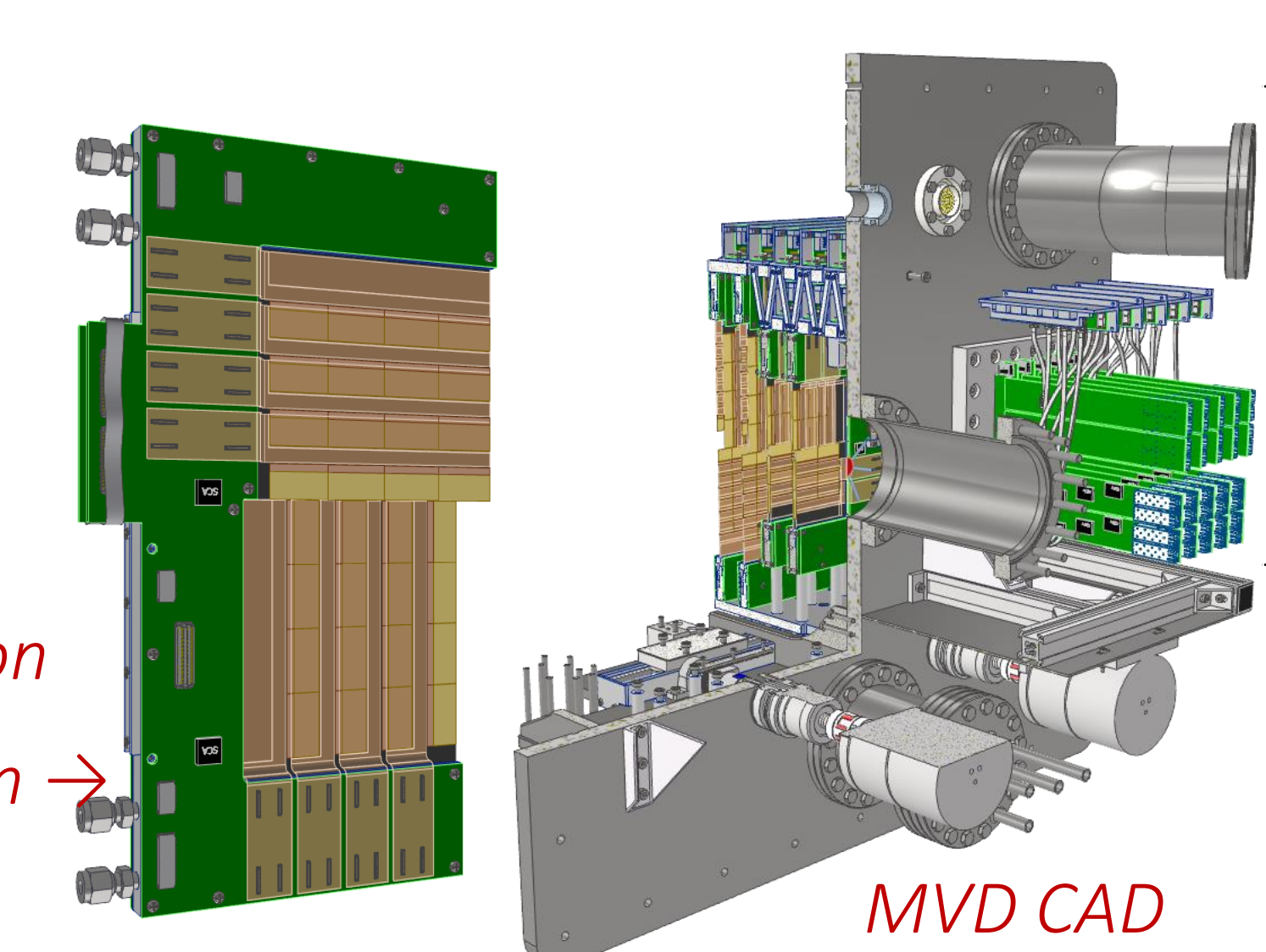
Sensor Integration
Jigless; μ -structured carrier
→ laser-ablated pockets ('hatches')
Mechanical & thermal connection Sensor/Carrier
Mechanical connection FPC/Carrier
Electrical connection: Full-automatic wire-bonding



Double-sided Integration
Concept validated in R&D phase
Dedicated support jig
QA + reworkability to ensure yield



Sensor Integration Flow (Draft)
Initial QA
Carrier cutting & hatching
Coating (QA), plasma activation
Assembly of carrier & FEB in heat sink
FPC tape gluing (QA, rework)
Sensor gluing (QA, rework)



Metrology
FPC gluing (QA)
Wire bonding (row-by-row, QA)
Electrical characterization
Mounting to Half-Stations
Final QA, storage

Detector Integration
Mounting and Remote Positioning System
LV distribution
Readout system
Cooling system
Detector control system (EPICS)
Assembly optimized w/ full-scale prototype

