

# Design and performance of the gaseous beam monitor for the CSR external-target experiment

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On behalf of the CEE Beam Monitor Group

Central China Normal University

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for Particles and Imaging

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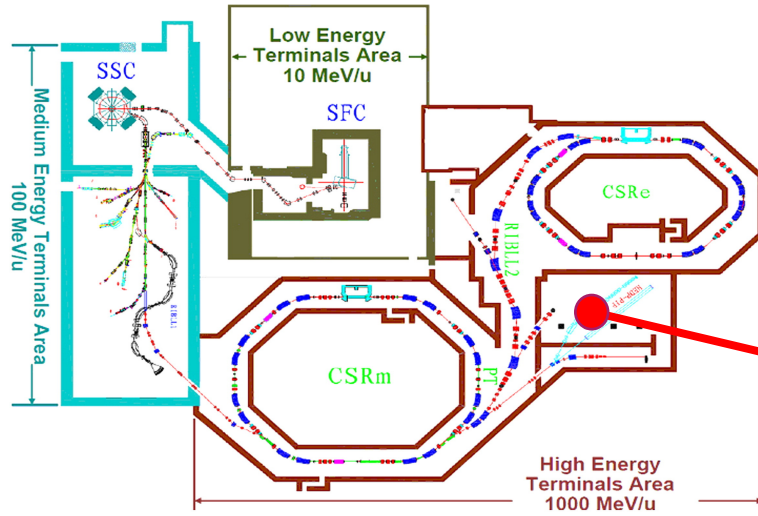
# Outline

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- Introduction
- Beam Monitor of CEE
- Topmetal-CEEv1/v2 chips
- Summary and Outlook

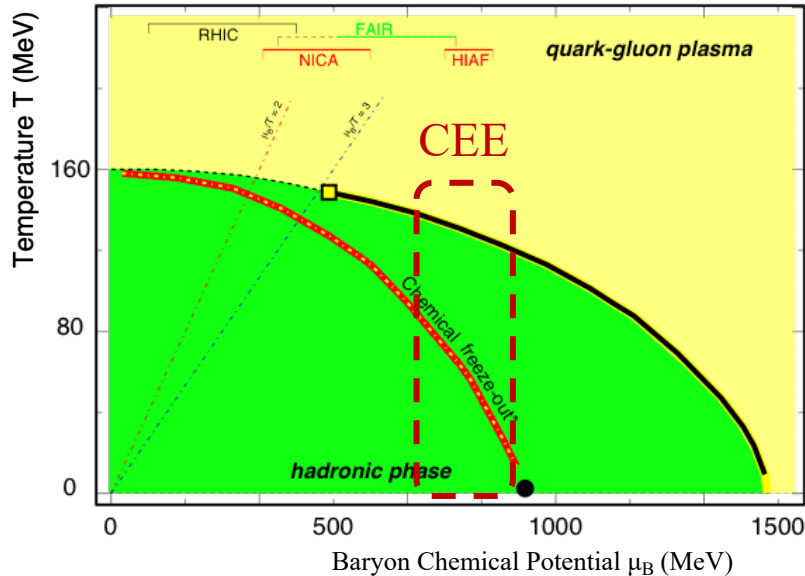
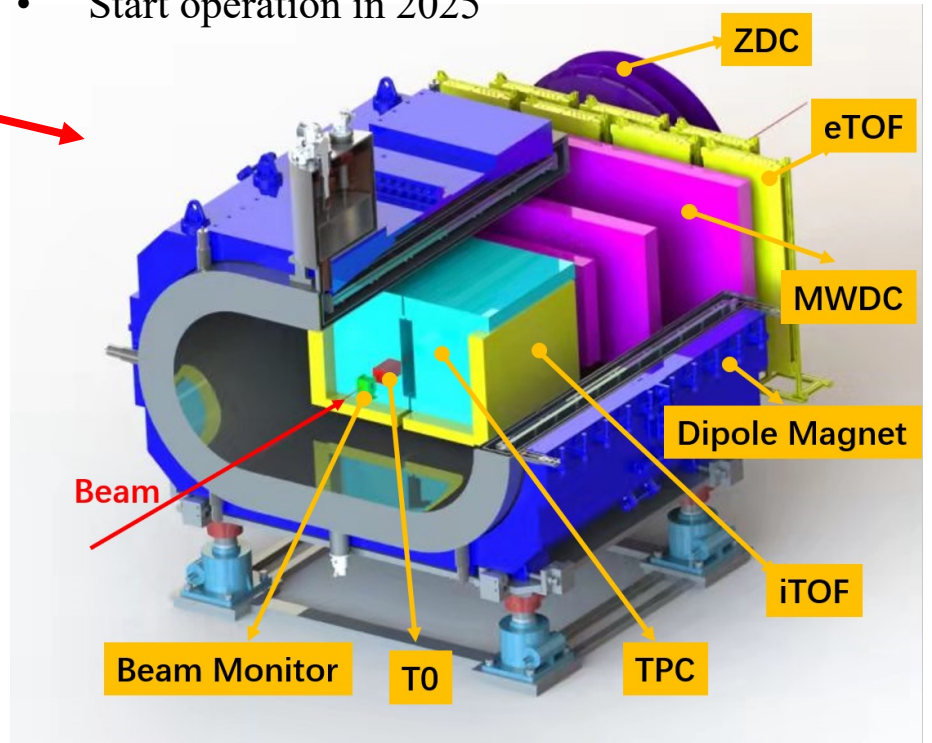
# CEE at HIFRL-CSR

## Heavy Ion Research Facility in Lanzhou Cooling-Storage-Ring system



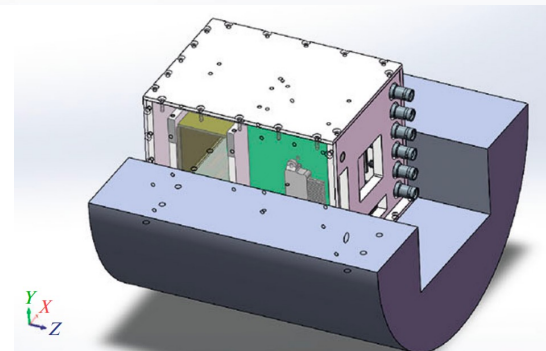
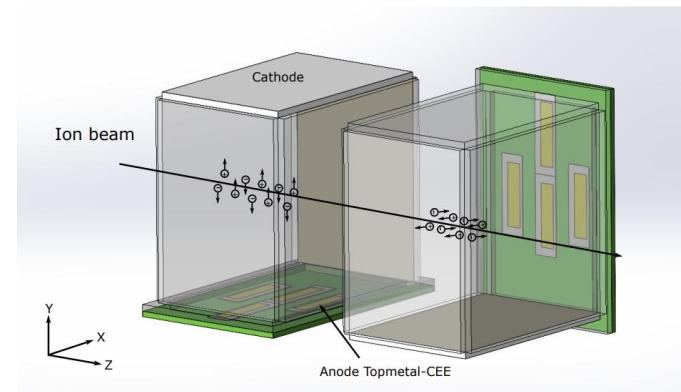
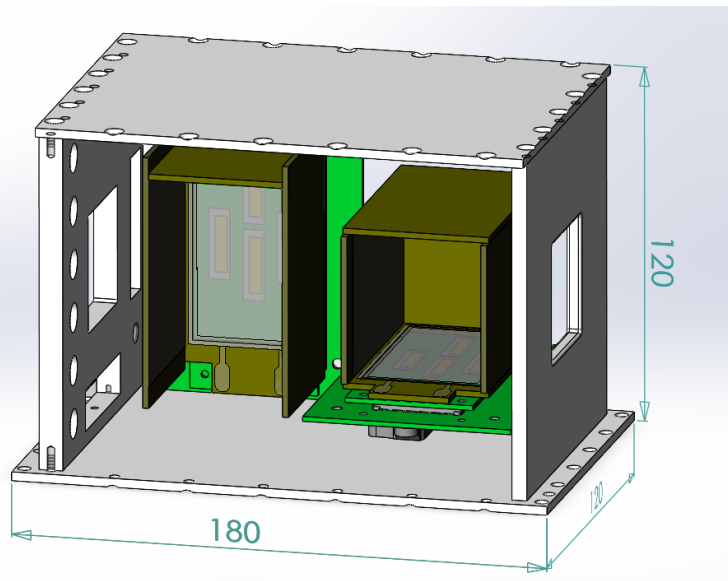
## CSR External-target Experiment

- Study the properties of nuclear matter at high baryonic density
- Fixed target, with heavy-ion (up to U) beam energy:  $\sim 0.4 - 1.1$  GeV/u
- Maximum event rate:  $10^4$  s $^{-1}$
- Start operation in 2025

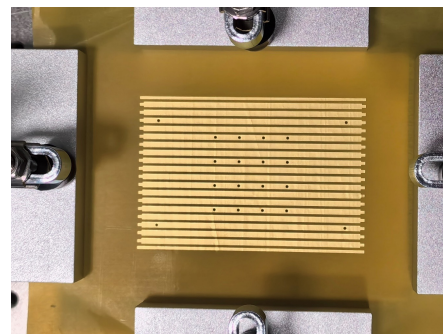
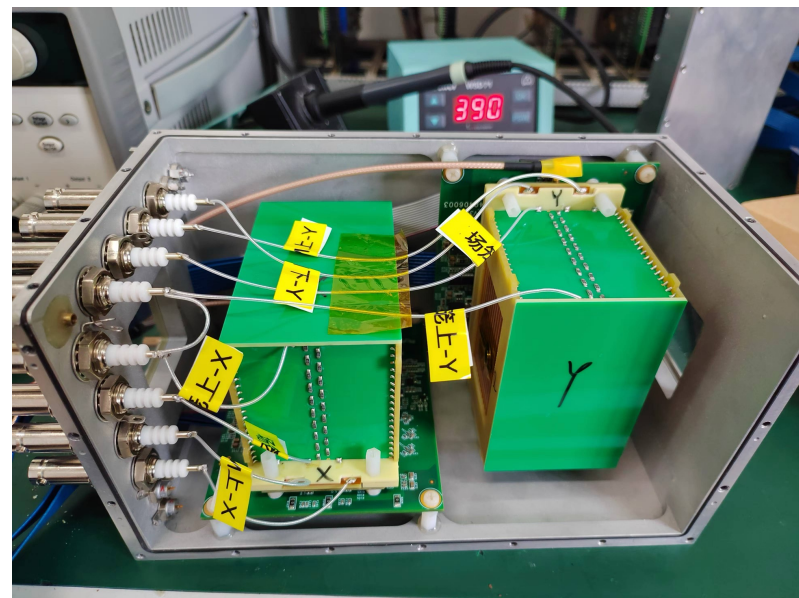
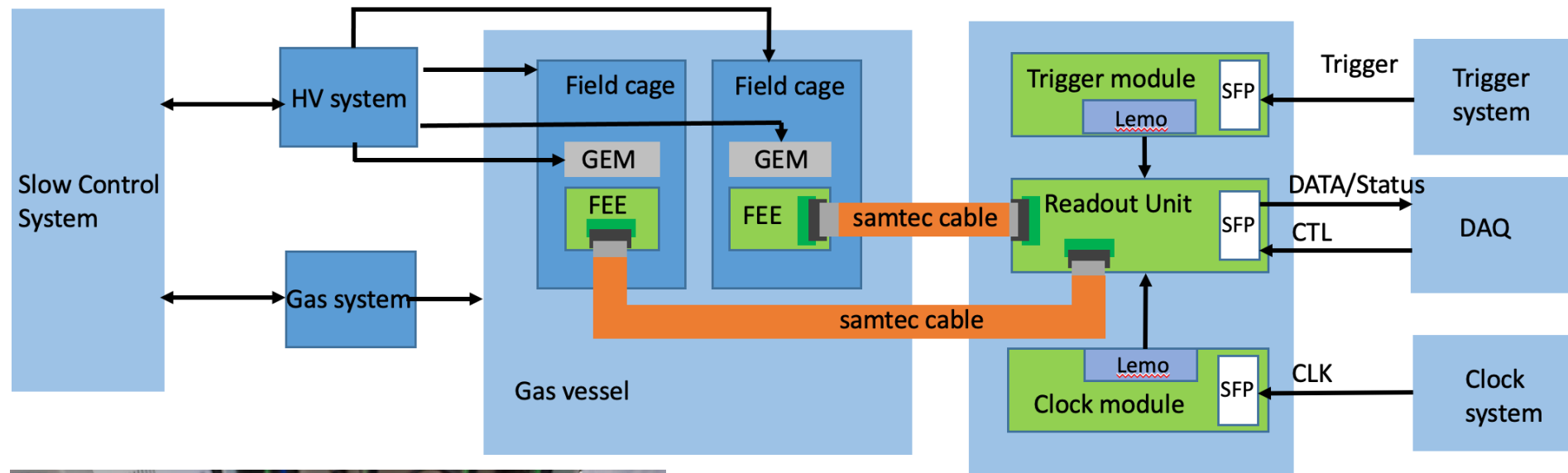


# Beam Monitor of CEE

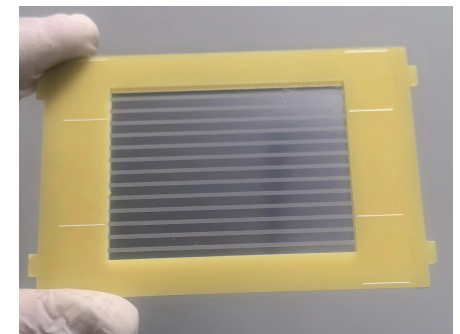
- Placed upstream of the fixed target in a magnetic shield
- Measure the position of each beam particle
- Offline: **vertex reconstruction** (combined with TPC and MWDC)
- Online: monitor the beam status
- Main design parameters:
  - Position resolution :  $50 \mu\text{m}$
  - Time resolution:  $1 \mu\text{s}$
  - Maximum event rate:  $\sim 1 \text{ MHz}$
  - Sensitive area:  $30 \times 30 \text{ mm}^2$
- Two micro-TPCs in a gas vessel, with electric field orthogonal to each other
- Position measured in two readout planes; arrival time used for track matching between two micro-TPCs
- Custom-designed **Topmetal-CEE chip** as anode for charge sensing and readout
- Amplification with **GEM**



# Detector system

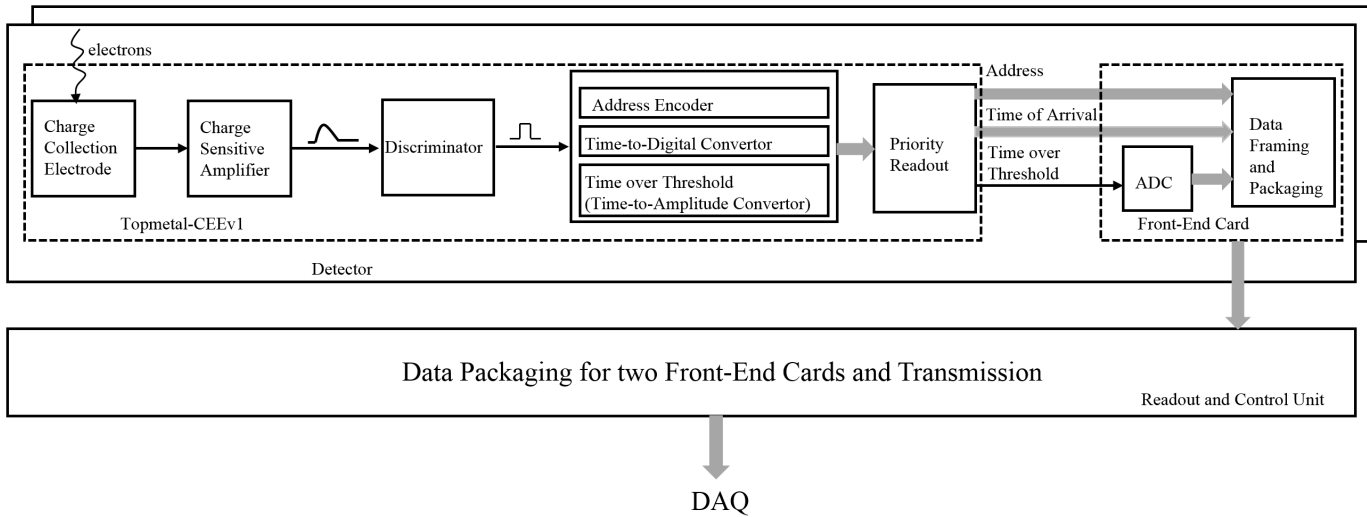


Field cage v1 :  
25  $\mu\text{m}$  Kapton+5  $\mu\text{m}$  Au



Field cage v2 :  
2  $\mu\text{m}$  Mylar+100 nm Al

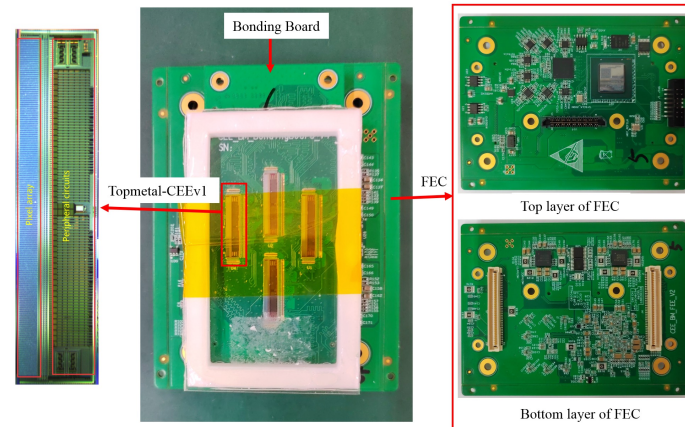
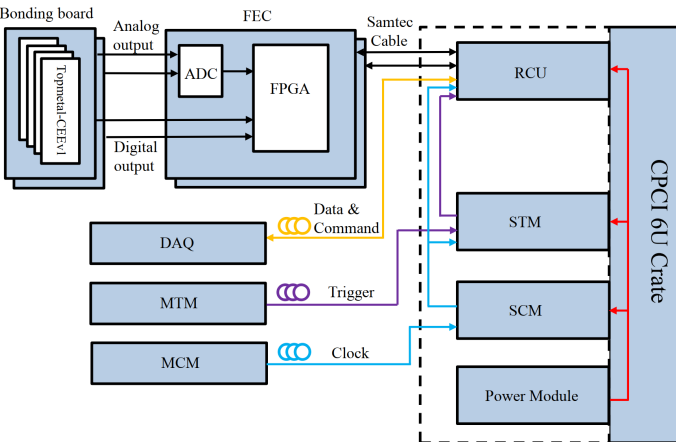
# Electronics



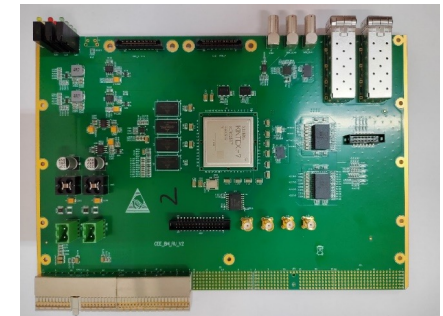
One chip: max. 40 MPixel/s  
 FEE (8 chips) : max. 1.92 Gbps  
 FEE to RCU: max. 3.2 Gbps

Typical data rate ( $10^6$  pps):

- Chip: 10 MPixel/s
- FEE: 0.36 Gbps



Front-end electronics

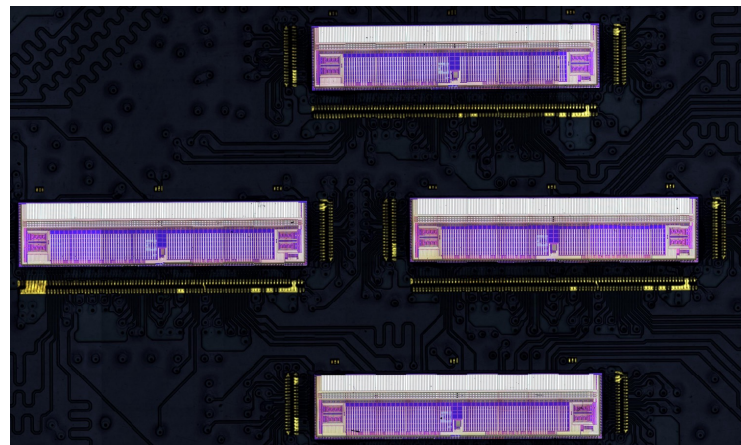
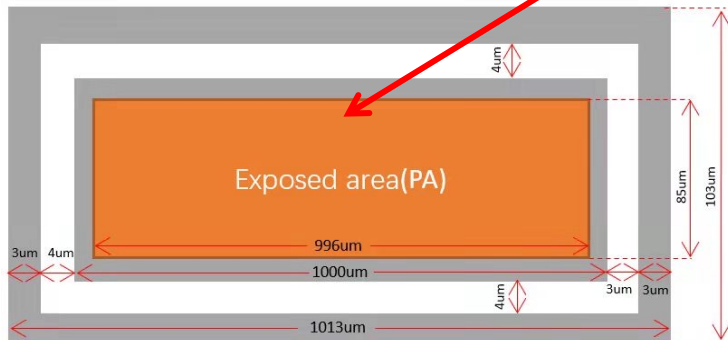
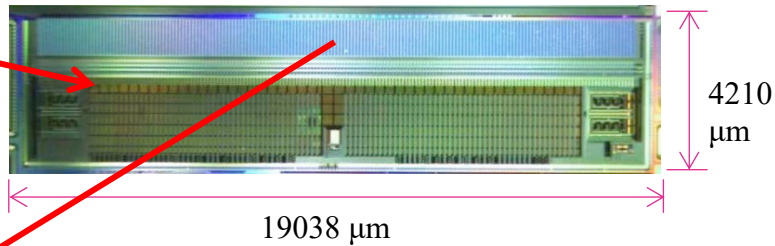
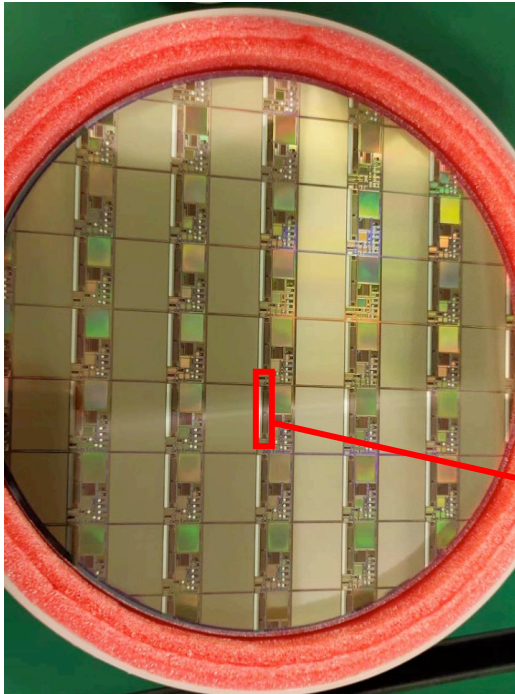


Readout and control unit

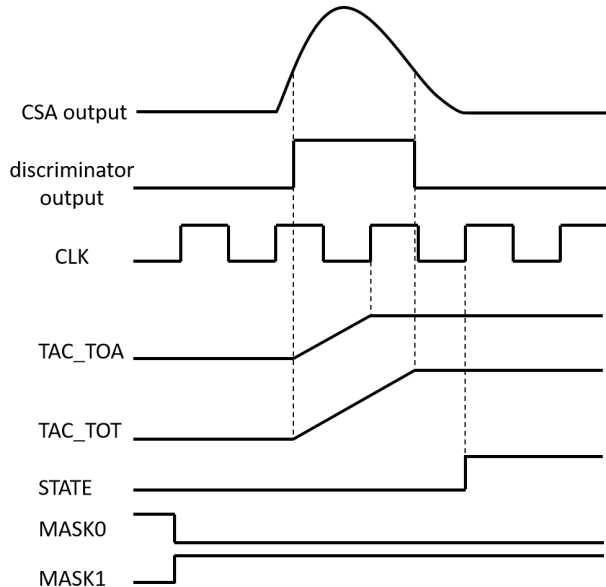
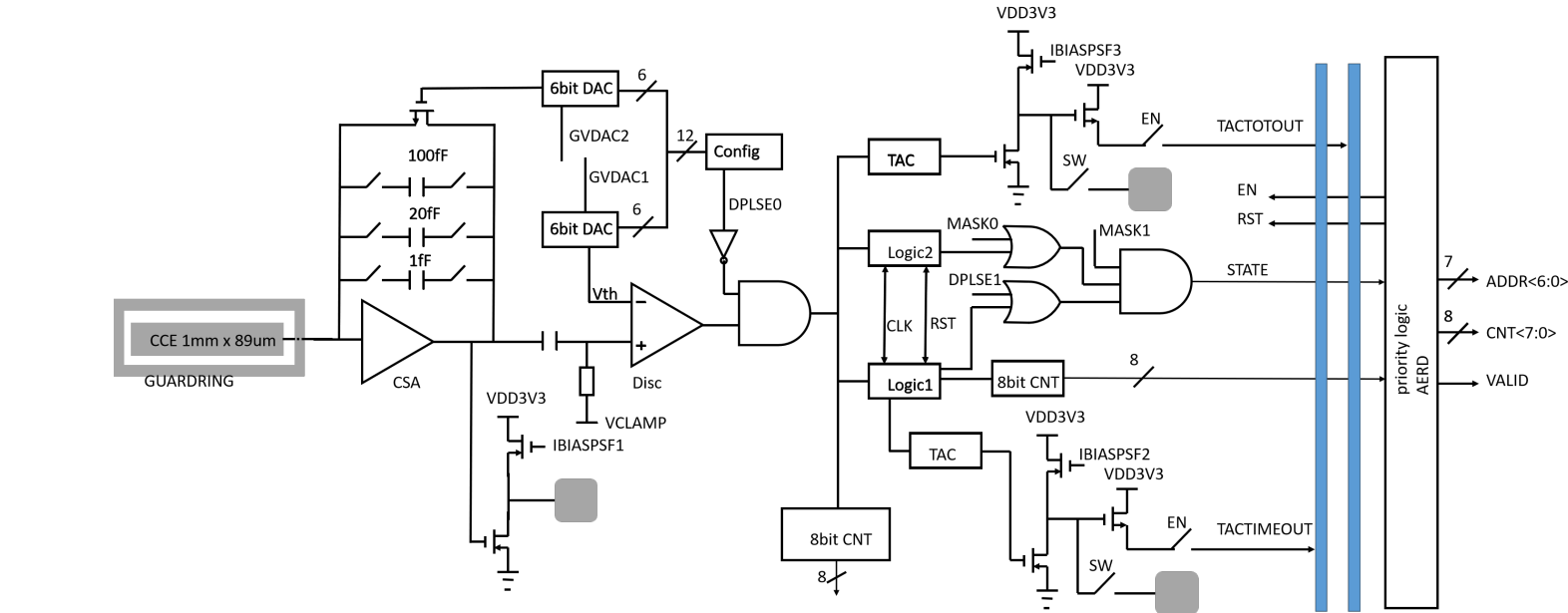
# Topmetal-CEEv1 chip

The main features of the Topmetal-CEEv1 chip.

Feature size	130 nm
Chip area	4.2 mm × 19 mm
Number of pixels	1 × 180
Pixel pitch	100 μm
CCE size	1 mm × 89 μm
Shaping time (tunable)	~ 0.5 μs to 2 ms
Peaking time	~ 100 ns
Readout scheme	Data-driven readout
Readout time	25 ns/pixel
Amplitude measurement	TOT method



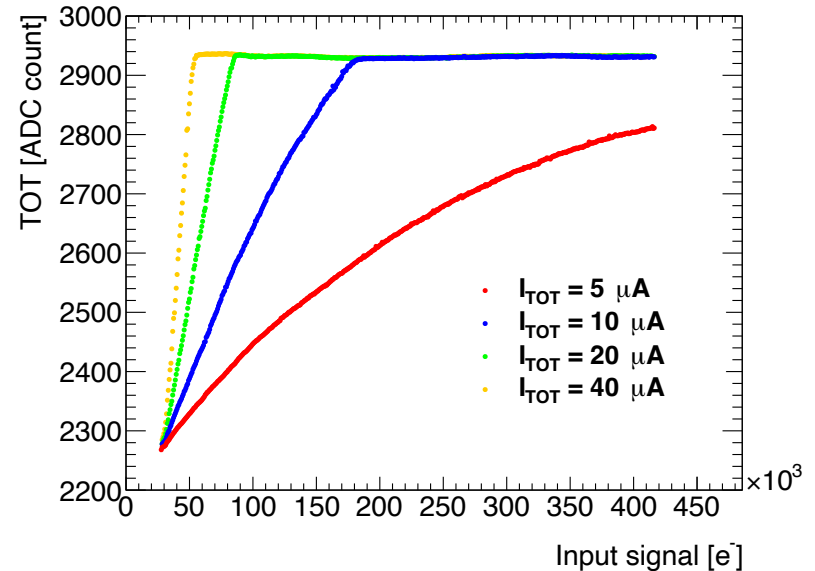
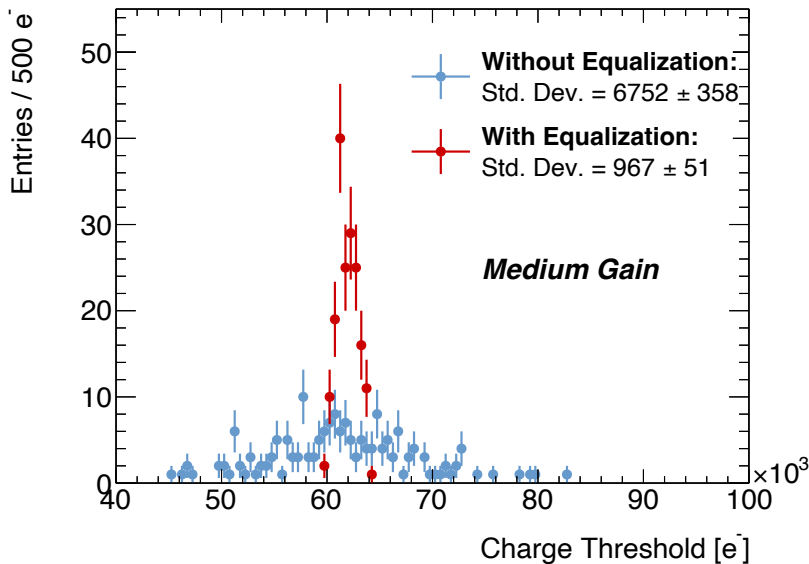
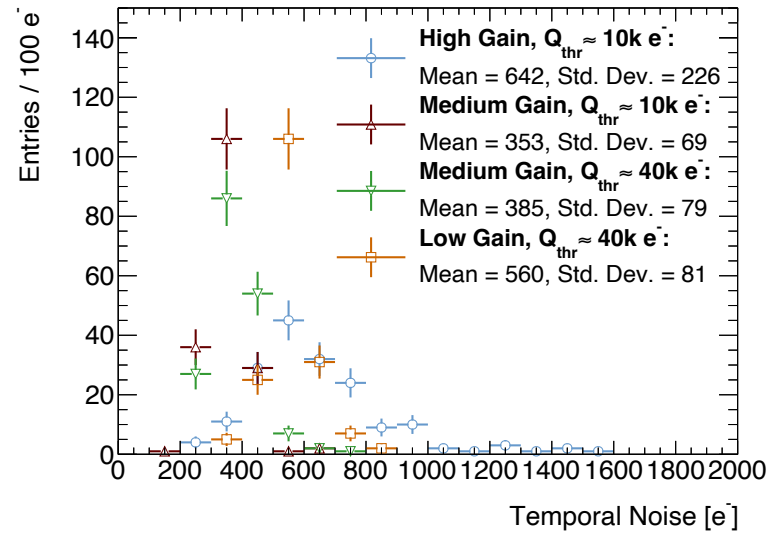
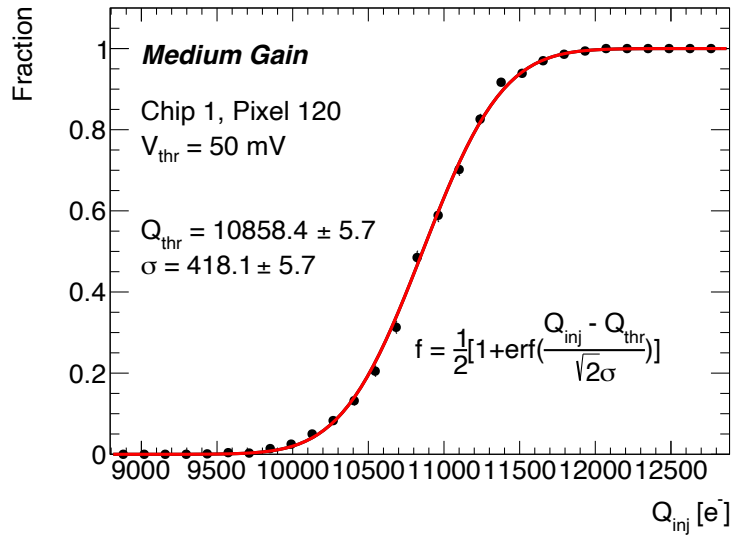
# Topmetal-CEEv1 chip



- Exposed metal (CCE): sense the drifting charge carriers in the gas
- Three feedback capacitors: low to high gains
- Time measurement:
  - Coarse: 8-bit counter with 25 ns precision
  - Fine: TAC for TOA (**not used**)
- Amplitude measurement: TAC for TOT
- Two on-chip ADCs for analog signals of TOA and TOT (**not used**)
- High speed serial readout module (**not used**)

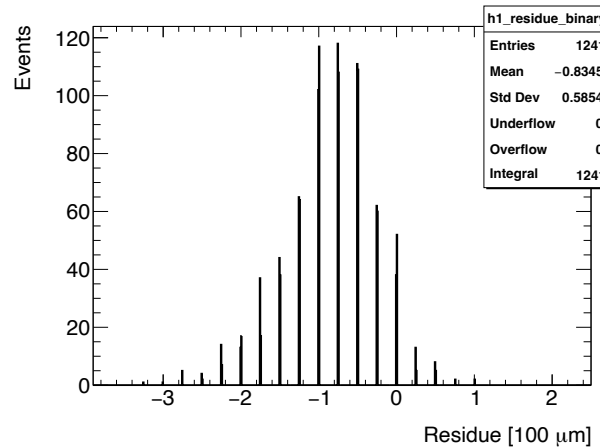
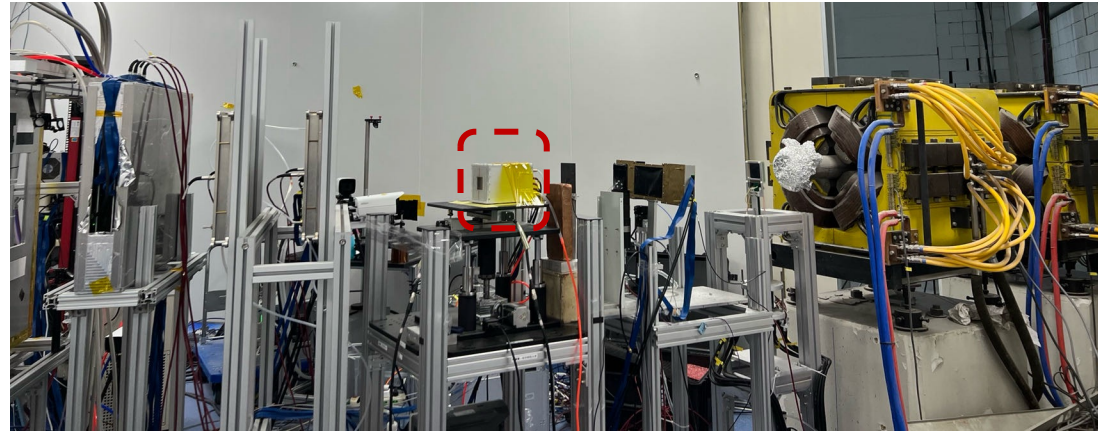
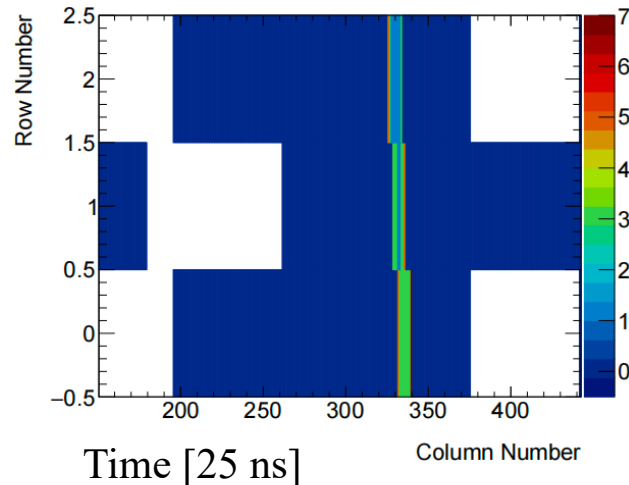
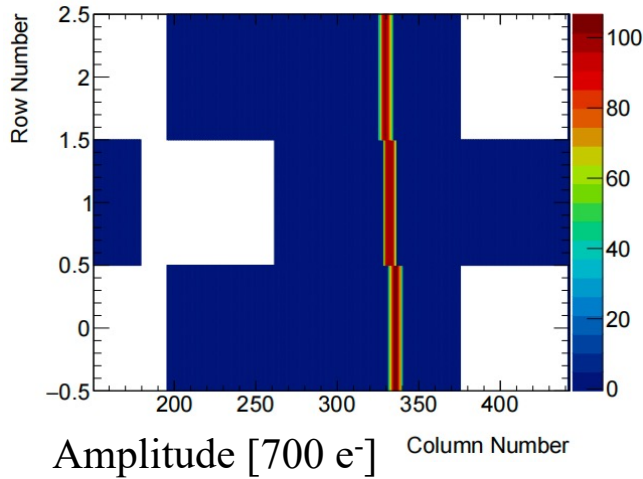


# Topmetal-CEEv1 chip: basic test

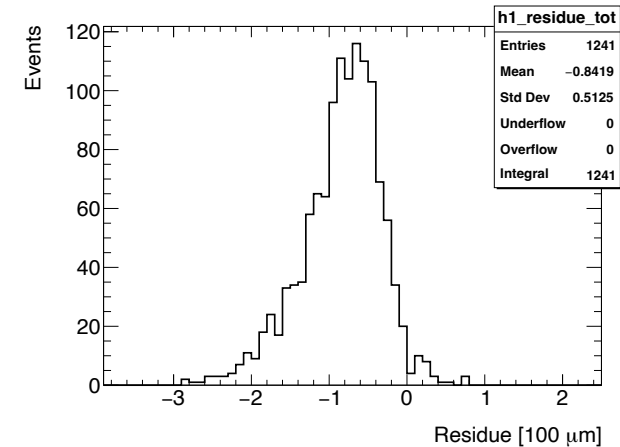


# Topmetal-CEEv1 chip: heavy-ion beam test

- Kr at  $\sim 320$  MeV/u
- Rate:  $\sim 10^4 - 10^6$  s $^{-1}$



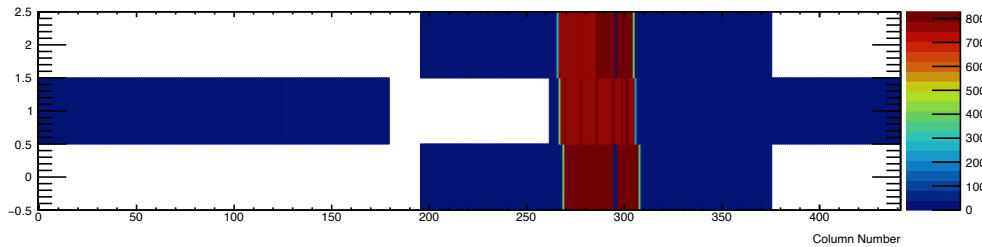
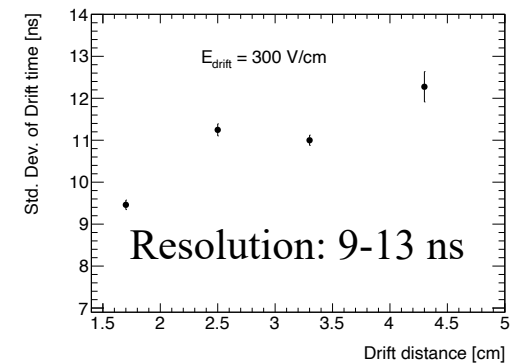
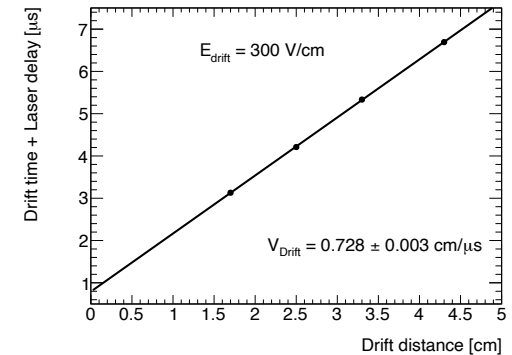
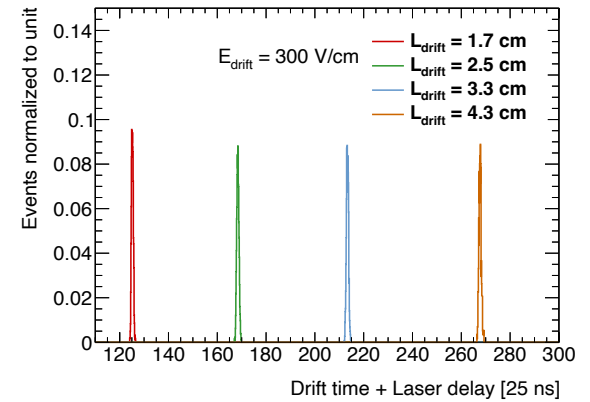
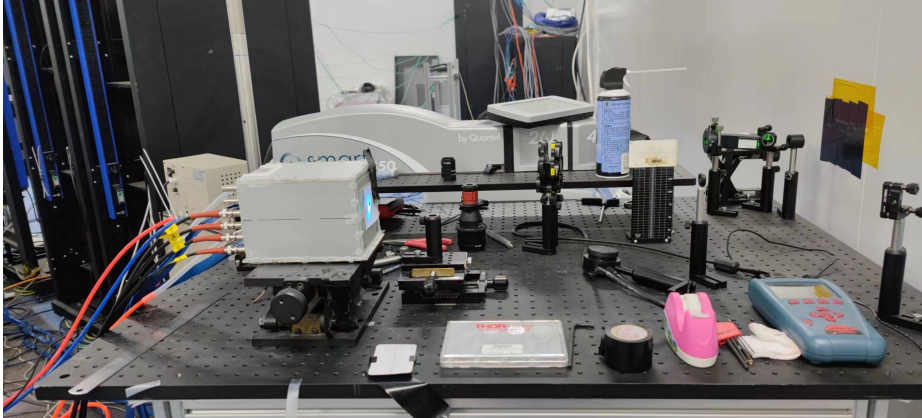
Center of geometry  
Resolution (one row):  
47.80  $\mu$ m



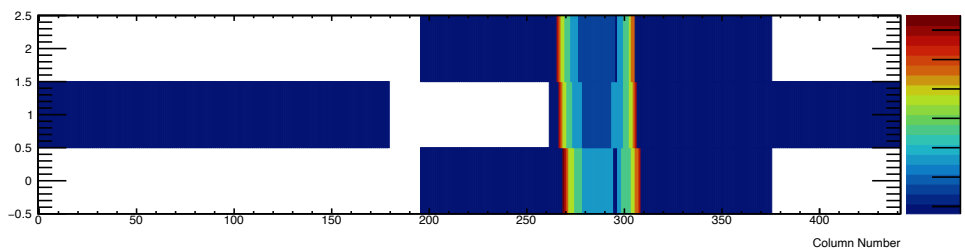
Center of gravity  
Resolution (one row):  
41.85  $\mu$ m

# Topmetal-CEEv1 chip: laser test

- 266 nm pulsed laser



Amplitude [ $700 e^-$ ]



Time [25 ns]

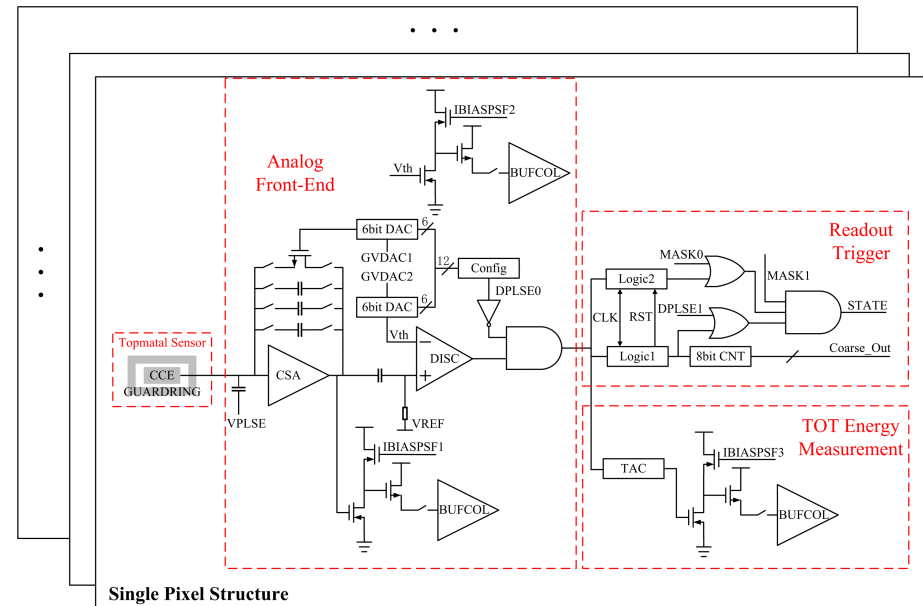
# Topmetal-CEEv2 chip

Main issues in Topmetal-CEEv1 chip:

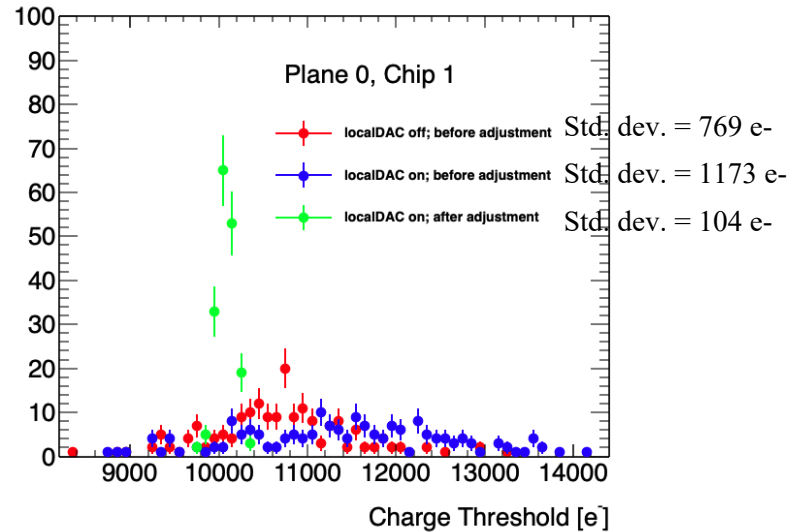
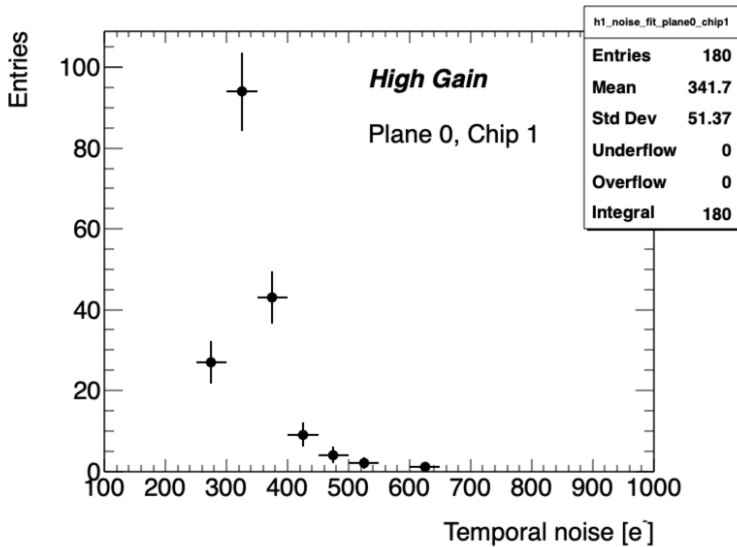
1. Disturbance of digital circuit to the analog circuit : large pixel threshold  $\sim 20 \text{ ke}^-$
2. Large noise for high gain (custom-designed 1 fb feedback capacitor) : use medium gain as default setting: shaping time  $\sim 1 \mu\text{s}$
3. Large fixed-pattern noise without threshold equalization

Changes in Topmetal-CEEv2 chip:

1. Careful isolation of digital and analog circuits; remove pads inside pixels; remove TAC for TOA, on-chip ADCs, and high-speed serial readout module: pixel threshold  $\sim 5 \text{ ke}^-$
2. Use 5 fb capacitor in the foundry device library for high gain : shaping time  $\sim 0.5 \mu\text{s}$
3. Option to disable the local DAC for tuning

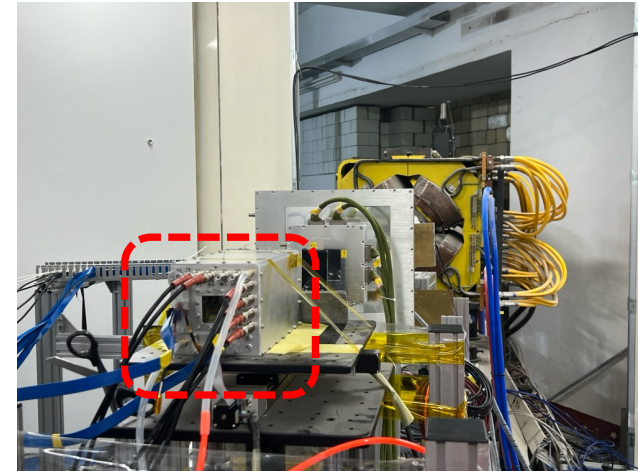


# Topmetal-CEEv2 chip



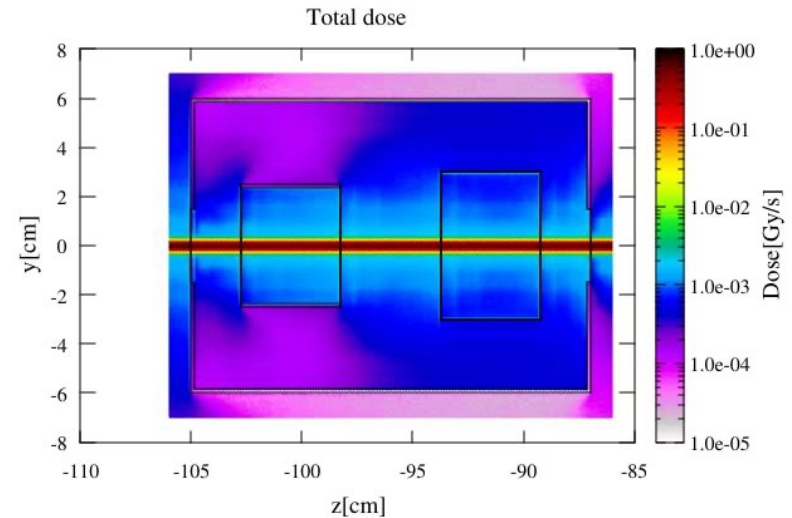
Heavy-ion beam test: Topmetal-CEEv1 VS Topmetal-CEEv2 :

- Pixel threshold:  $\sim 20\text{ke}^- \Rightarrow \sim 5\text{ke}^-$
- GEM voltage: 350V  $\Rightarrow$  230 V
- Maximum particle rate before GEM sparks:  $\sim 10^4 \text{ Hz} \Rightarrow \sim 10^6 \text{ Hz}$
- Position resolution: similar (dominated by detector calibration, electric field uniformity, space charge effect ...)



# Summary and Outlook

- Gaseous beam monitor, part of the CEE experiment, is under development. It features Topmetal-CEE chips for charge sensing and readout in the gas, with GEM for amplification.
- Complete detector system, including the gas detector, front-end electronics, and readout and control electronics, have been developed.
- Preliminary results from heavy-ion beam and laser tests showed a spatial resolution better than 50  $\mu\text{m}$  and a time resolution better than 15 ns.
- Ongoing work on the radiation tolerance study of the chip, detector calibration, track reconstruction and matching with other sub-detectors of CEE.



Thank you