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Impact of the circuit layout on the charge collection in a monolithic pixel sensor

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Monolithic CMOS sensors combine the sensing volume and the processing electronics in the same die, leading to complex shapes of doped regions with various concentrations. As a consequence, the electric field in such sensors cannot be accurately expressed analytically. Considering the importance of the charge propagation process on the signal formation in the pixels, the electric field is usually simulated with Technology Computer Aided Design (TCAD) prior to any further study.
While in most circumstances the sensor can be considered independent of the CMOS electronics thanks to an implant separating the two parts, measurement results of the Hybrid to Monolithic (H2M) chip feature a clearly asymmetric efficiency pattern at high threshold. This pattern was not expected since the sensitive volume is designed symmetric, it is however correlated with the asymmetric layout of the circuitry.
This contribution details the simulation method including TCAD and Monte Carlo deployed to better understand this effect. The simulation procedure highlighting the differences compared to the case where the circuit is not considered will be presented first, before focusing on the results obtained with the TPSCo 65nm technology used by the CERN Experimental Physics R&D and for the H2M.
Simulations qualitatively reproduce the efficiency pattern observed in the H2M only when taking into account the layout of the CMOS part, and allowed to clarify its origin: an interplay between the relatively large pixel pitch of 35um, the fast front end and the specific layout of the circuit. The same simulation flow was used on other prototypes in the same technology, confirming that this effect is marginal for smaller pitch, in agreement with previous measurements.

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