环形正负电子对撞机
Circular Electron Positron Collider

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# Development of monolithic pixel sensor prototypes for the first CEPC vertex detector prototype


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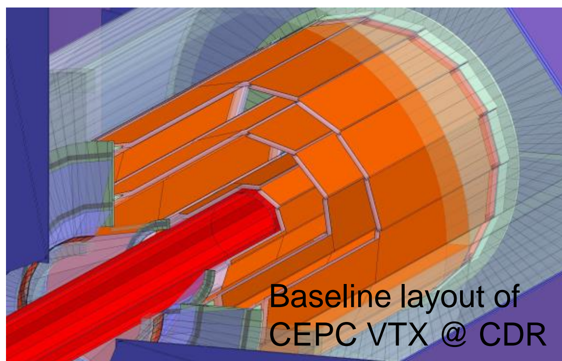
# CEPC Vertex detector requirement

**The Circular Electron Positron Collider (CEPC) is a large international scientific facility proposed by the Chinese particle physics community in 2012.**

- **Efficient tagging of heavy quarks (b/c) and τ leptons**
  - ➔ Excellent impact parameter resolution：

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$




Baseline design parameters for CEPC VTX in CDR

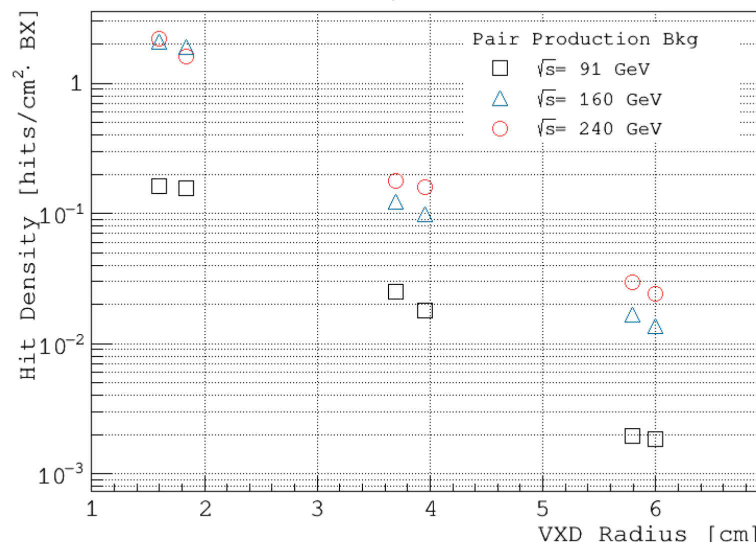
| | $R$ (mm) | $\lvert z \rvert$ (mm) | $\lvert \cos\theta \rvert$ | $\sigma$ (μm) |
|---|---|---|---|---|
| Layer 1 | 16 | 62.5 | 0.97 | 2.8 |
| Layer 2 | 18 | 62.5 | 0.96 | 6 |
| Layer 3 | 37 | 125.0 | 0.96 | 4 |
| Layer 4 | 39 | 125.0 | 0.95 | 4 |
| Layer 5 | 58 | 125.0 | 0.91 | 4 |
| Layer 6 | 60 | 125.0 | 0.90 | 4 |

| Physics driven requirements | Running constraints | Sensor specifications |
|---|---|---|
| $\sigma_{s.p.}$ 2.8 μm | | Small pixel ~16 μm |
| Material budget 0.15% $X_0$/layer | | Thinning to 50 μm |
| | Air cooling | low power 50 mW/cm$^2$ |
| r of Inner most layer 16 mm | beam-related background | fast readout ~1 μs |
| | radiation damage | radiation tolerance ≤ 3.4 Mrad/ year; ≤ 6.2×10$^{12}$ $n_{eq}$/ (cm$^2$ year) |

*Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector*

# Main specifications of the full-scale chip

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm$^2$ for Higgs/W;
    0.2 hits/bunch/cm$^2$ for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18/25 μm
  - Pixel size：25 μm × 25 μm

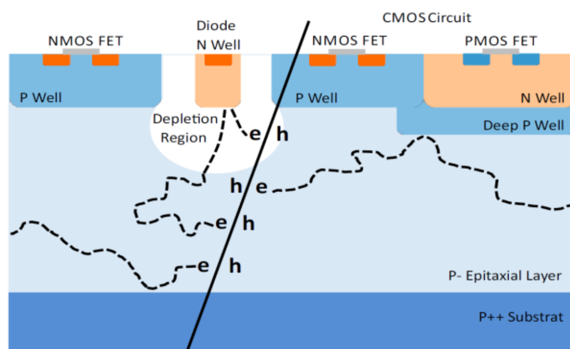



*Ref: CEPC Conceptual Design Report, Volume II*

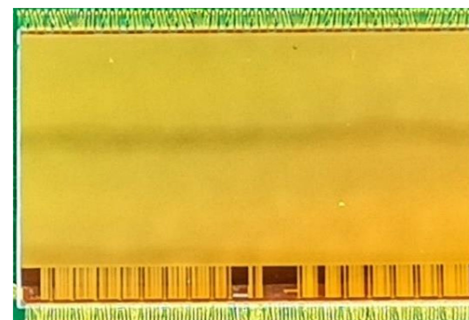
| For Vertex | Specs | For High rate Vertex | Specs. | For Ladder Prototype | Specs. |
|---|---|---|---|---|---|
| Pixel pitch | ≤ 25 μm | Hit rate | 120 MHz/chip | Pixel array | 512 row × 1024 col |
| TID | >1 MRad | Data rate | 3.84 Gbps --triggerless ~110 Mbps --trigger | Power Density | < 200 mW/cm$^2$ (air cooling) |
| | | Dead time | < 500 ns --for 98% efficiency | Chip size | ~1.4 × 2.56 cm$^2$ |

# TaichuPix prototypes overview

- **Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz ) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 rounds of sensor prototyping in a 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm )
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023



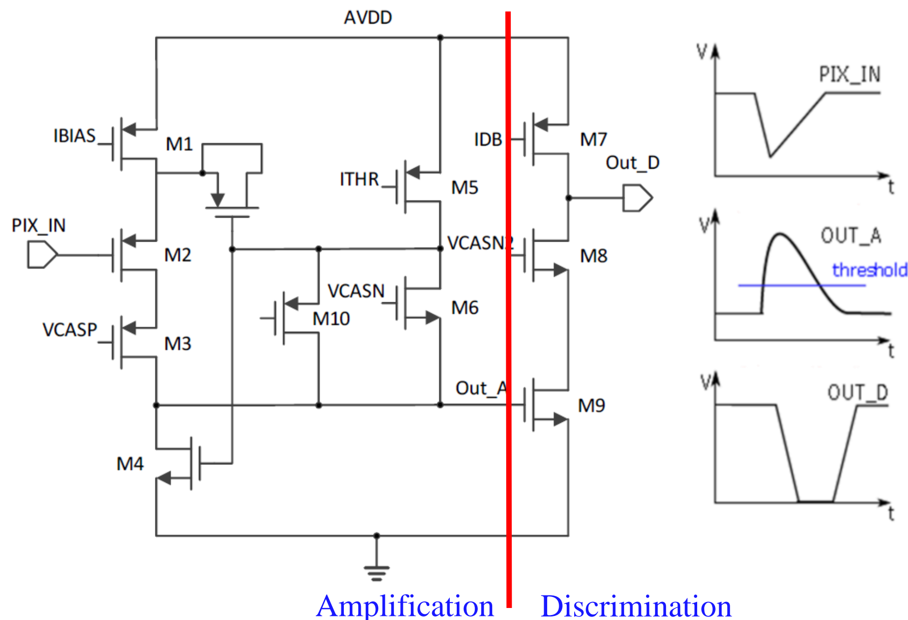

**CMOS monolithic pixel sensor**

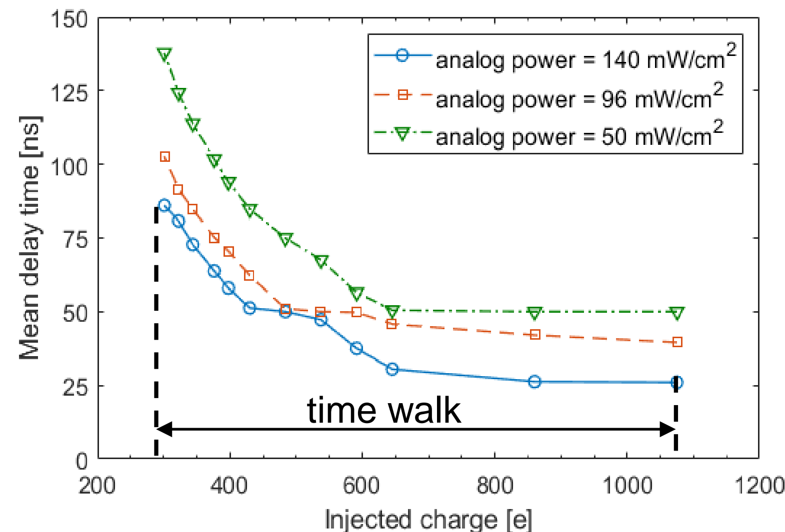


**TaichuPix-3**
(15.9 × 25.7 mm²)

# Pixel architecture – Analog

Ref : D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

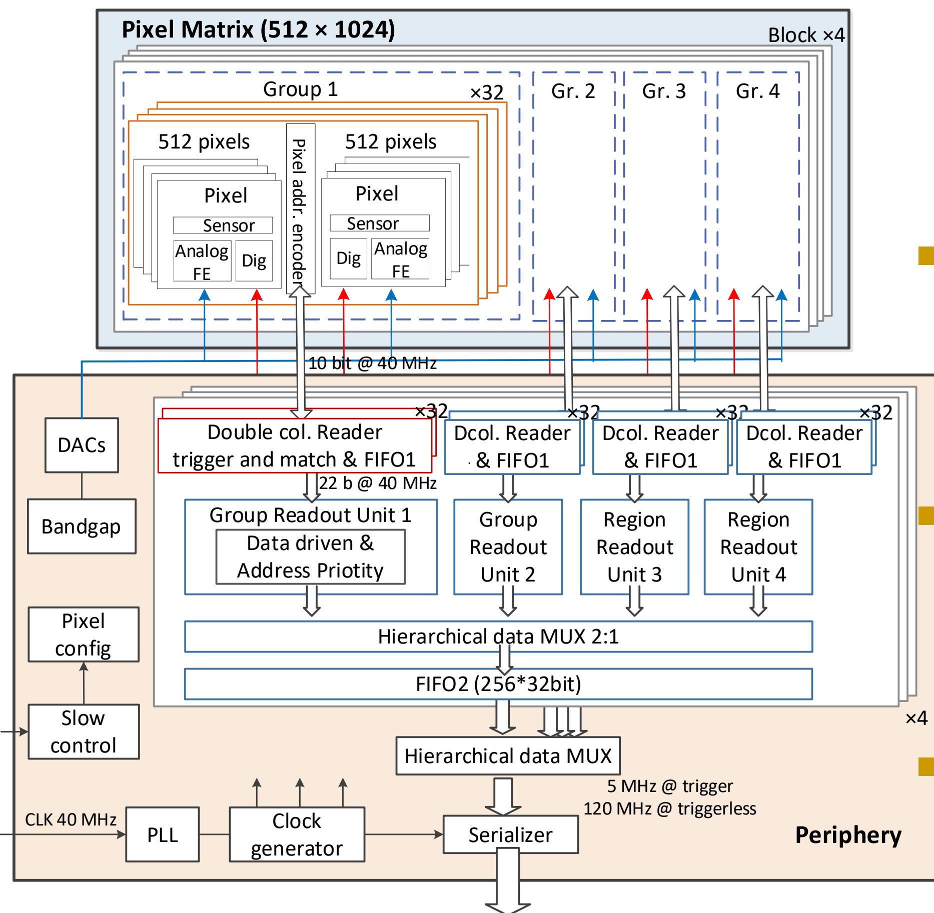



Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp with a step of 25 ns.

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE**
- **Biasing current has to be increased, for a time walk of ~25 ns**
  - for 40 MHz BX @ Z pole
- **Consequence:**
  - Power dissipation increased
  - Fast charge collection needed

# TaichuPix sensor architecture

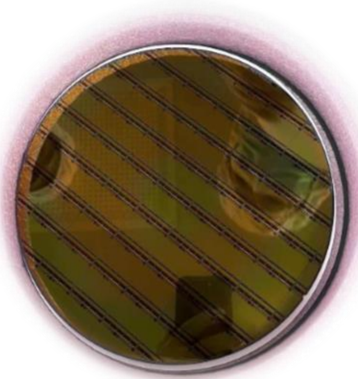



Architecture of the full-scale TaichuPix

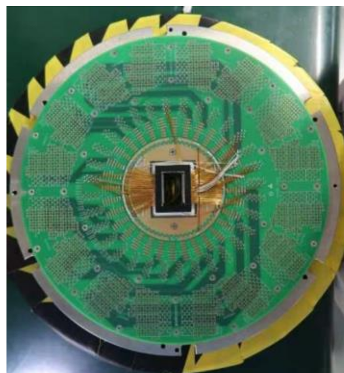
- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

# Full size sensor TaichuPix-3

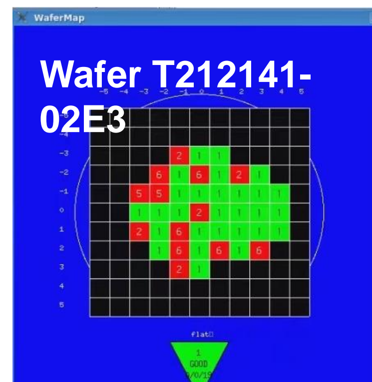
- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers tested on probe-station** → chip selecting & yield evaluation



8-inch wafer

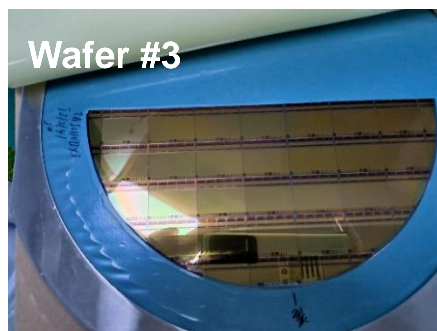


Probe card for wafer test




An example of wafer test result (yield ~67%)

  - **Wafers thinned down to 150 μm and diced**

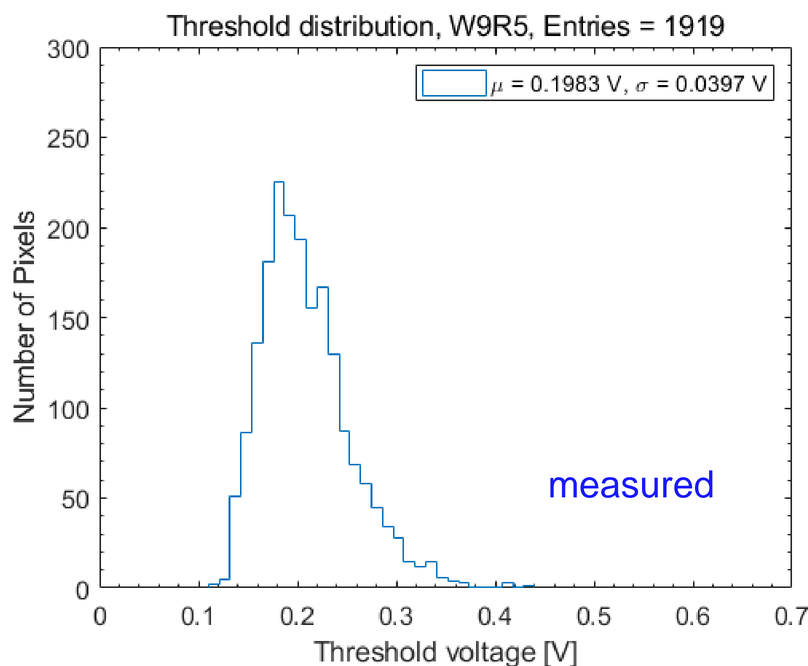


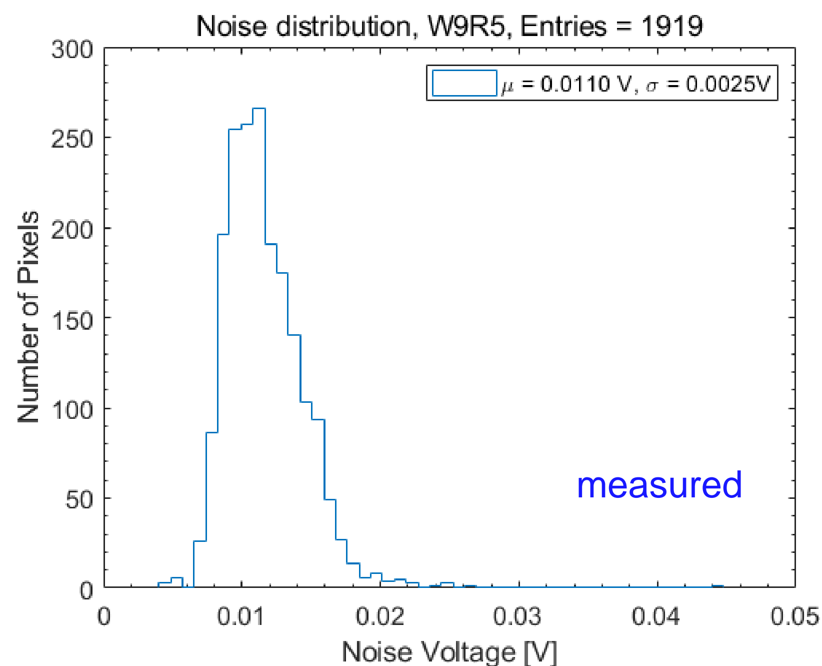

Wafer after thinning and dicing

Thickness after thinning

# Threshold and noise of TaichuPix-3

- **Pixel threshold and noise were measured with selected pixels**
  - S-curve method was used to test and extract the noise and the threshold
  - Average threshold ~215 $e^-$, threshold dispersion ~43 $e^-$, temporal noise ~12 $e^-$ @ nominal bias setting

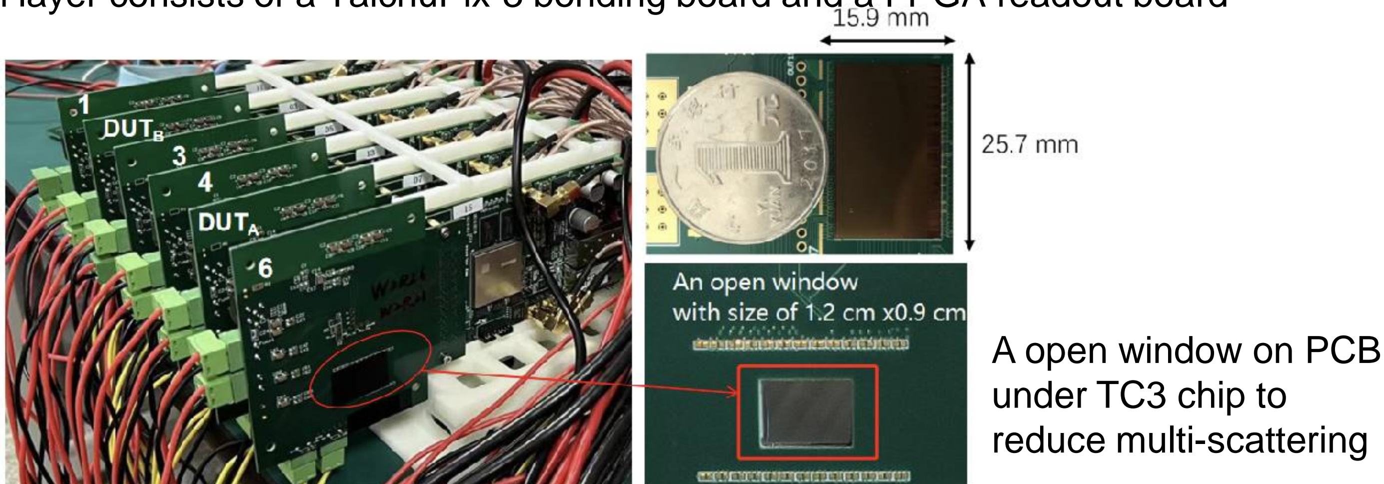



- **Power dissipation of 89 ~ 164 mW/cm² tested @ 40MHz clk with different biasing conditions**

# TaichuPix-3 telescope

- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

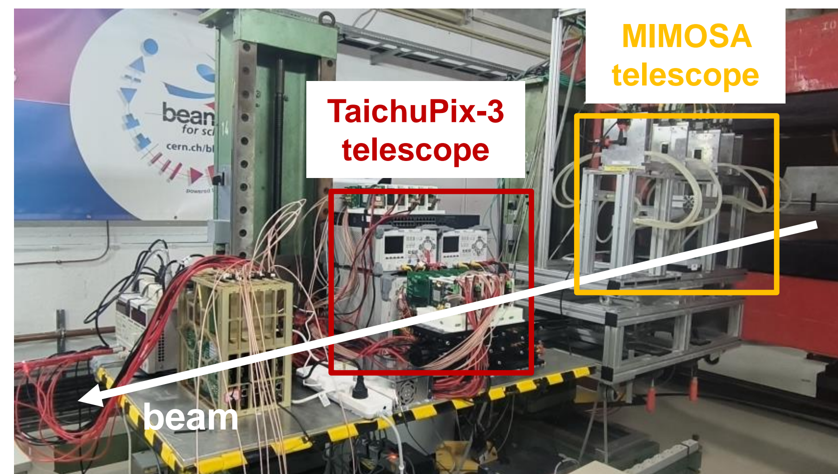



A open window on PCB under TC3 chip to reduce multi-scattering

6-layer TaichuPix-3 telescope

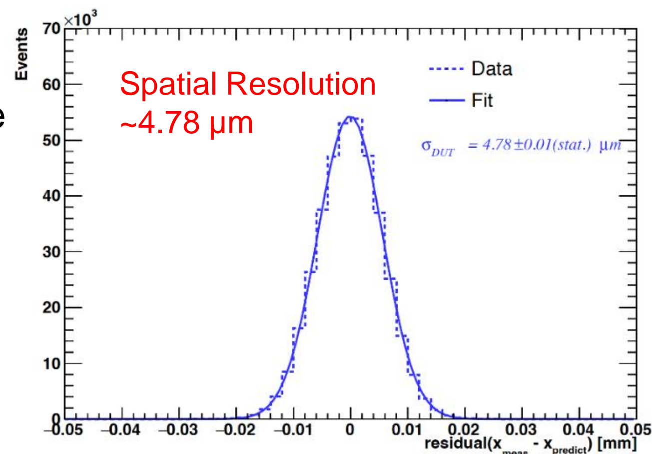
- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT

(Detector Under Test)

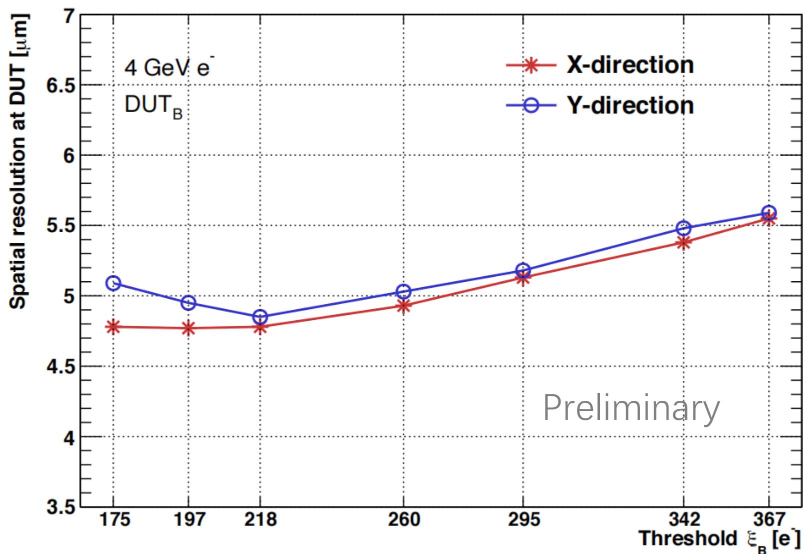


# TaichuPix-3 beam test result

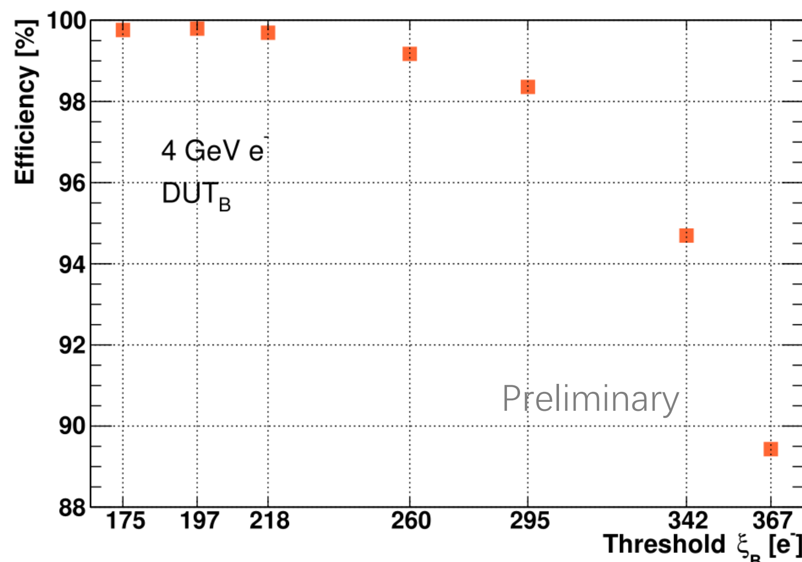
- **Spatial resolution**
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- **Detector efficiency**
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution



Distribution of residual X



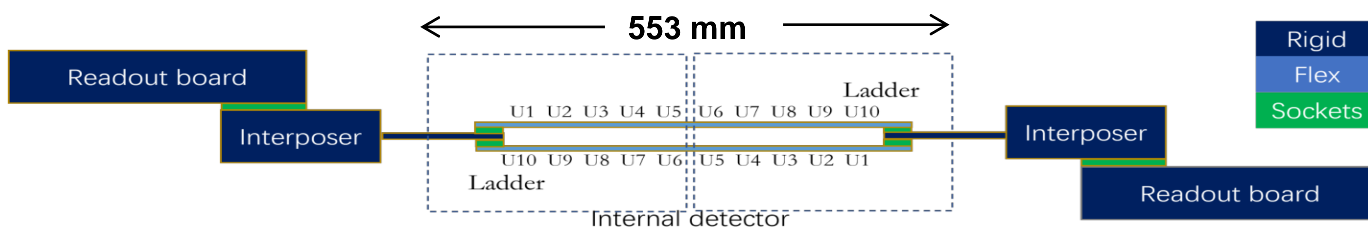
Spatial resolution vs. pixel threshold

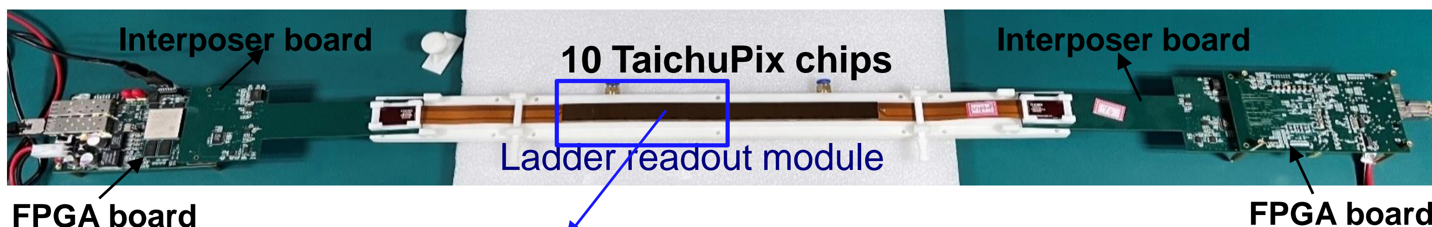


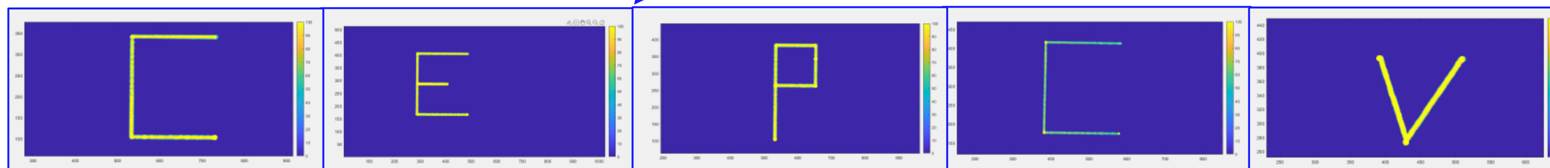
Detection efficiency vs. pixel threshold

# Ladder readout design

- **Detector module (ladder) = 10 sensors + support structure + readout board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Functionality of a full ladder fundamental readout unit was verified**
  - Read out from both ends, with careful design on power placement and low noise
  - Scanning a laser spot on the different chips with a step of 50 μm, clear and correct letter imaging observed → **one ladder readout unit working**



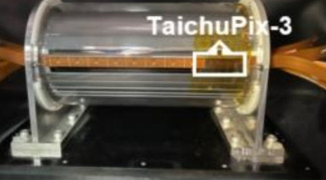



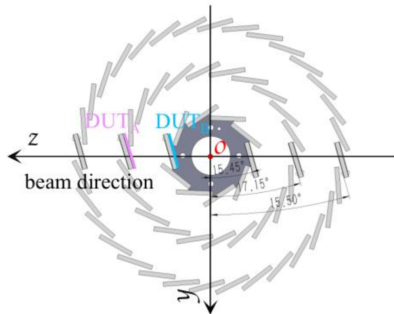



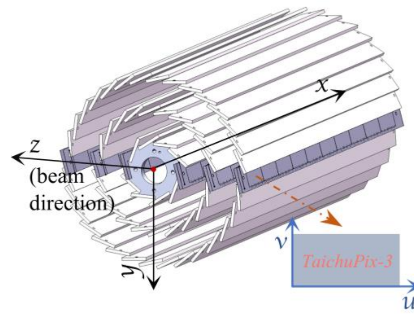
Laser tests on 5 Taichupix chip on a full ladder

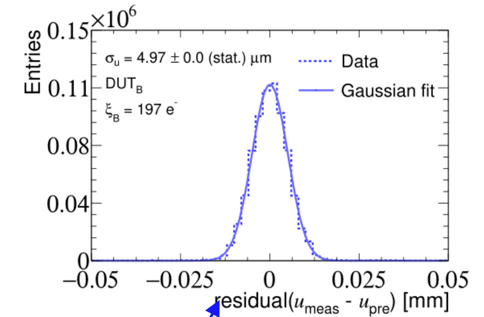
# Detector prototype and beam test

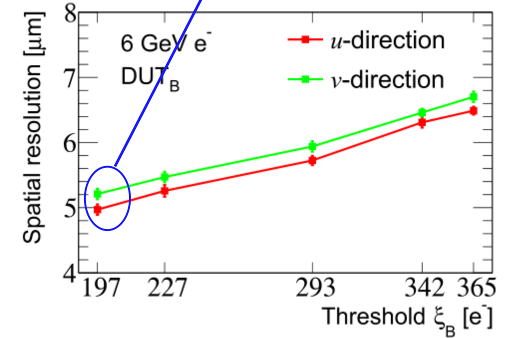
- **6 double-sided layers assembled on detector prototype**
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector
  - Best spatial resolution 4.97 μm @ detection efficiency > 99%

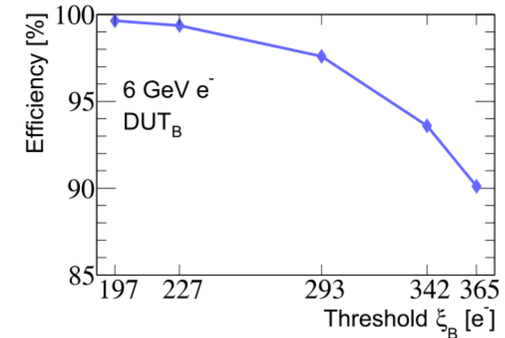




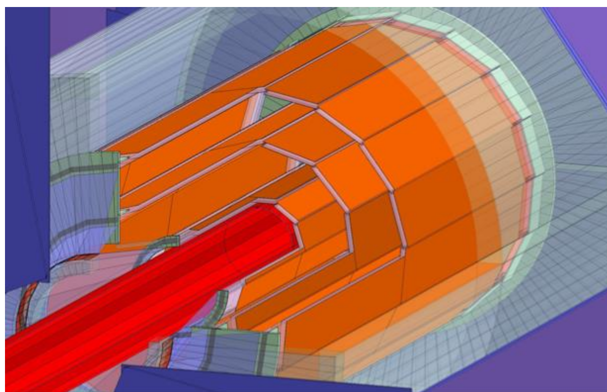



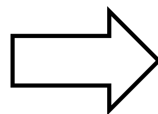

Ref: DOI-10.1109/TNS.2024.3395022

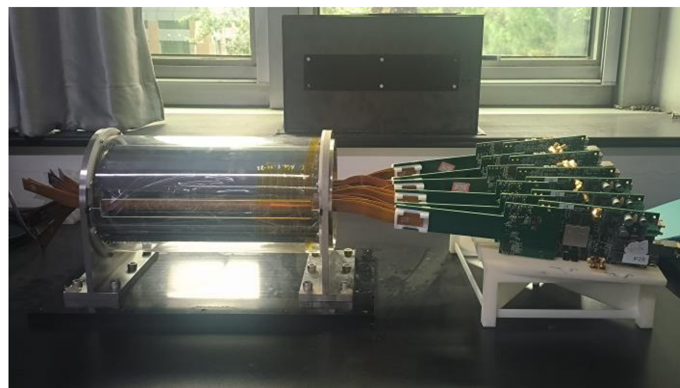
# Summary

- **The full-scale and high granularity pixel prototype, TaichuPix-3, has been designed and tested for CEPC VTX R&D**
  - Spatial resolution of 4.78/4.97 μm measured with 4 GeV electron beam in DESY
  - 
- **Readout electronics for the sensor test and the ladder readout were developed**
  - Performed the sensor characterization in the lab successfully
  - Completed beam tests for the pixel sensor prototype and the vertex detector mechanical prototype



Concept (2016)

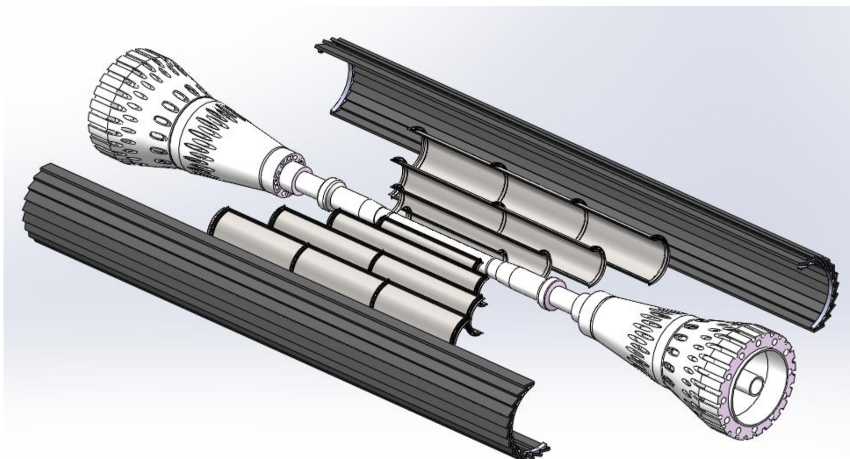




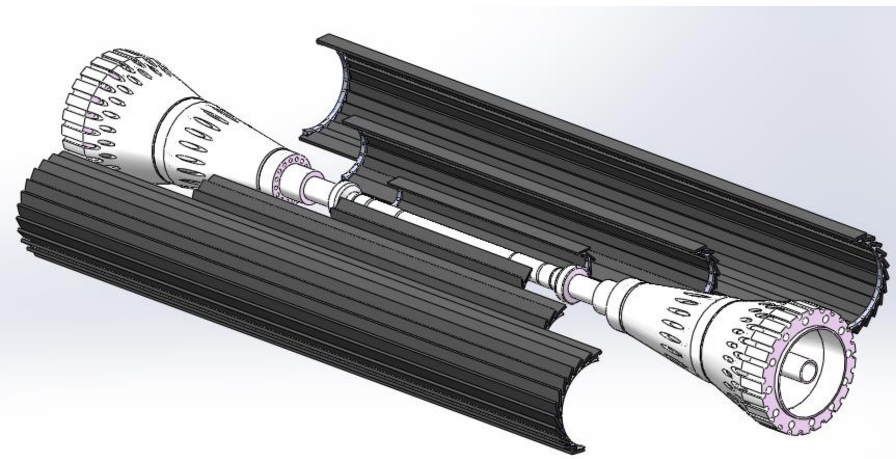
1st Vertex detector prototype (2023)

# Outlook

- **The reference detector TDR under preparation, to be completed by the mid-2025 for the proposal of China's 15th 5-year plan.**
- **The bent MAPS option has been chosen as baseline for the reference detector TDR. Technical challenges:**
  - Inner-most layer radius (11 mm) is smaller compared with ALICE ITS3 (18 mm)
  - Low material budget ( less than 0.15%$X_0$ per layer)
  - Detector Cooling with air cooling (power consumption<= 40 mW/cm$^2$)
  - Spatial Resolution (3-5 μm)



Baseline: Bent MAPS

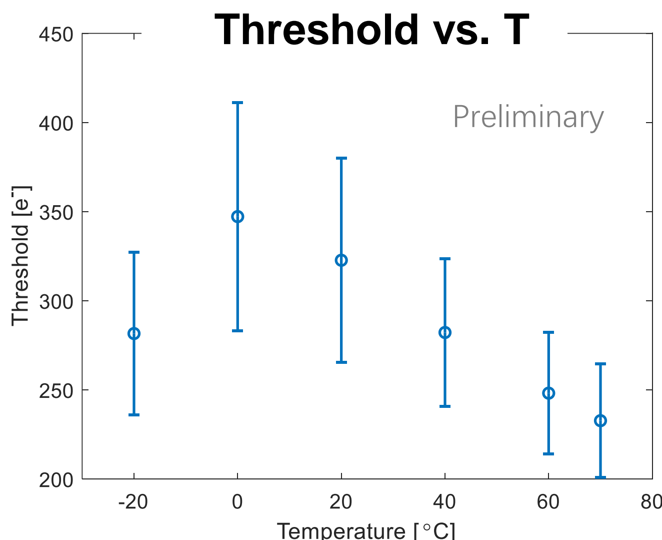


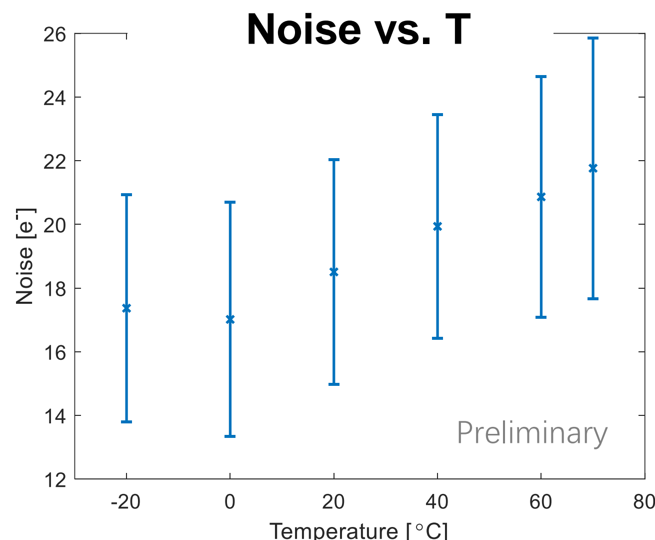
Alternative: ladder based MAPS

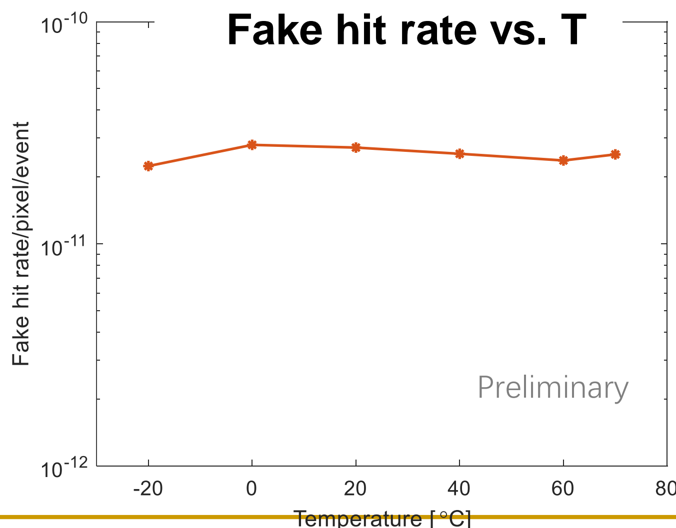
**Thank you very much for your attention !**

# Performance at different temperatures

- Test under a consistent configuration @ different T




- **TC3 shows a normal functionality @ -20 ~ 60 °C**
- **Main performance (i.e. threshold, noise, fake hit rate) can satisfy the requirements @ -20 ~ 60 °C**
- **Threshold and noise fluctuate with T, probably attribute to the fluctuation of pixel biasing**

# Hitmap

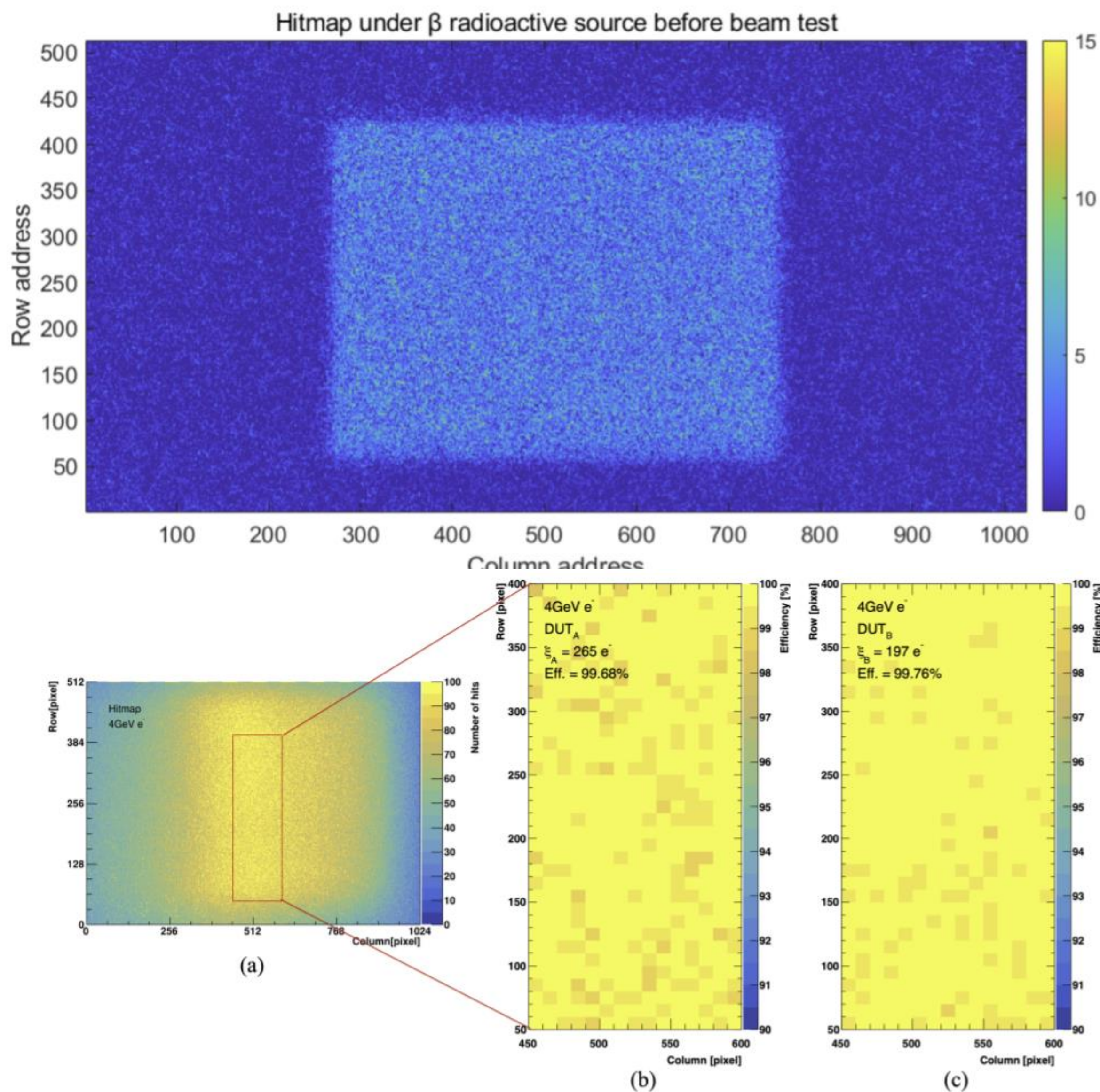
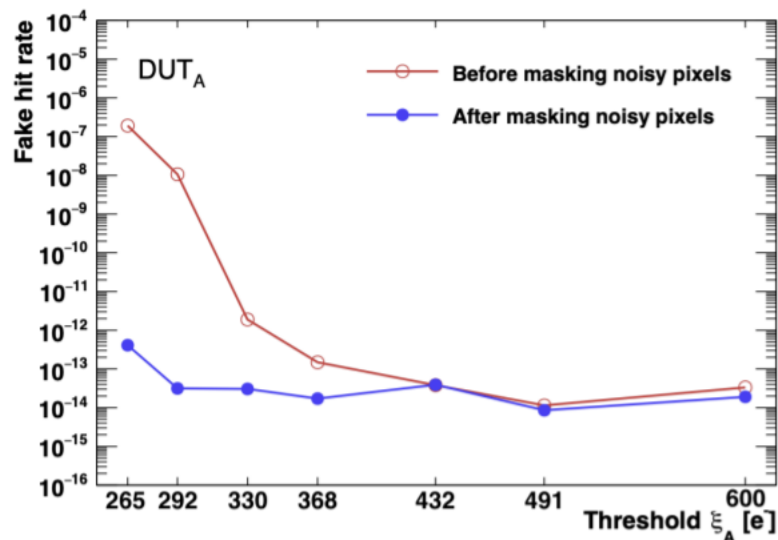
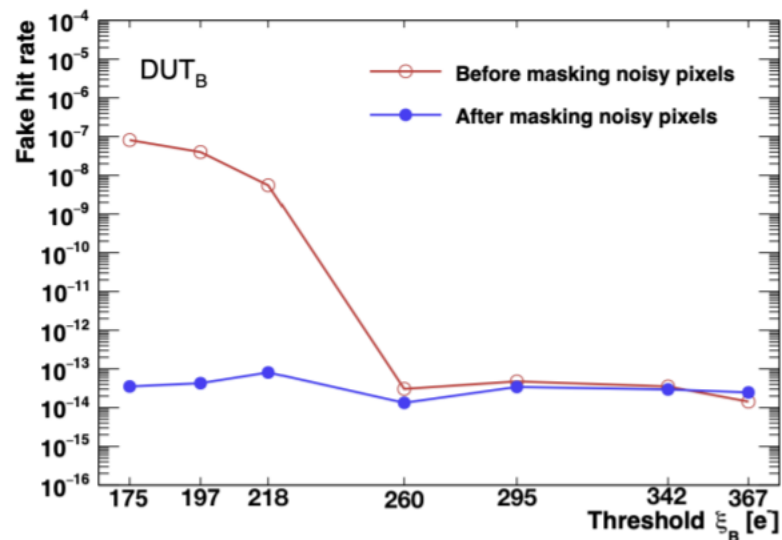



Figure 12: (a) The hitmap of one example DUT under 4 GeV electron beam. The pixels inside the red box are used to calculate the average efficiency of every 10 × 10 pixels. (b) (c) The efficiency map of $DUT_A$ and $DUT_B$ at the minimum threshold.

# Fake hit rate




(a)




(b)

Figure 3: Fake hit rate of $\mathrm{DUT}_A$ (a) and $\mathrm{DUT}_B$(b) as a function of threshold.

# Cluster size

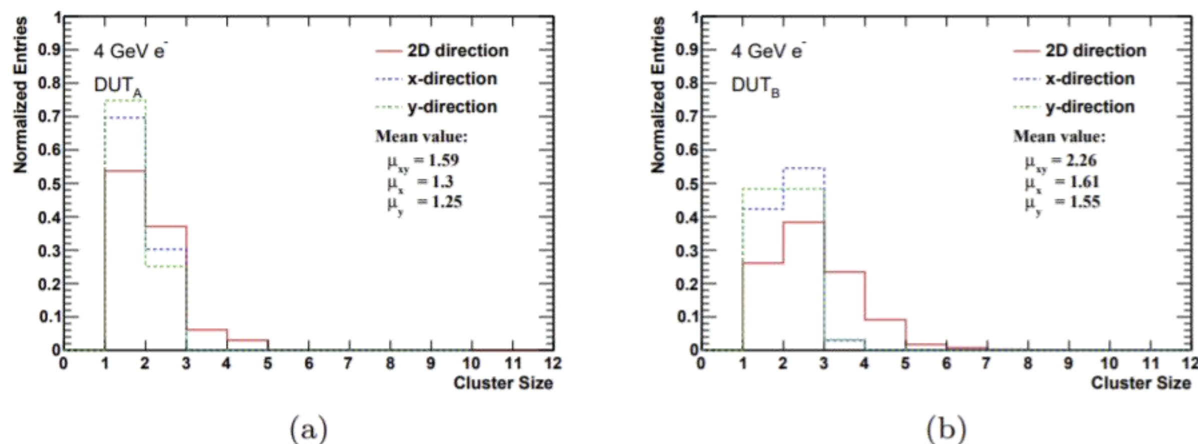



Figure 6: The cluster size distribution for $\text{DUT}_A$ with $\xi_A = 265e^-$ (a) and $\text{DUT}_B$ with $\xi_B = 175e^-$ (b), shown in the 2D detector plane direction and 1D projections along the $x$-direction (row direction of the sensor) and $y$-direction (column direction of the sensor).

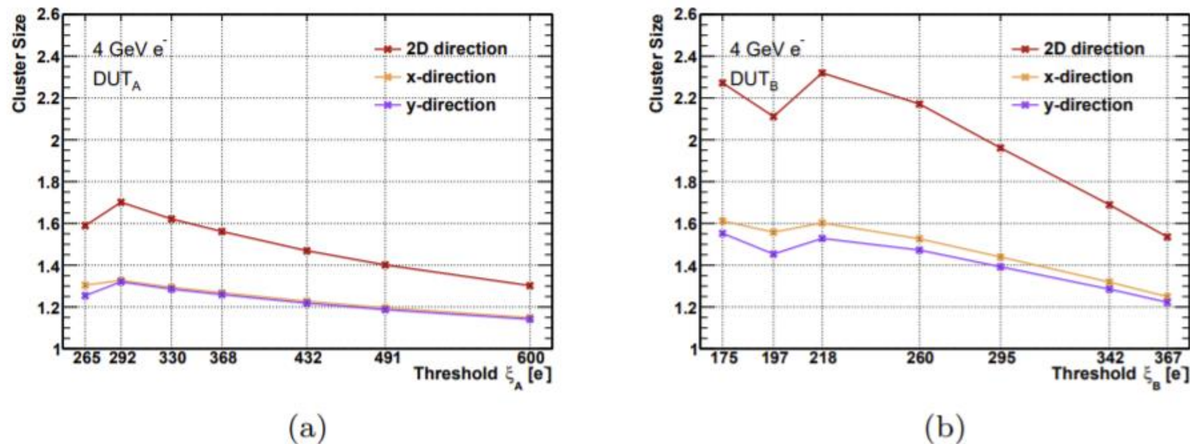



Figure 7: Average cluster size of $\text{DUT}_A$ (a) and $\text{DUT}_B$ (b) as a function of threshold $\xi$, shown in the 2D detector plane and 1D projections along $x$-direction and $y$-direction.