Eleventh International Workshop on Semiconductor Pixel Detectors for Particles and Imaging

ID de Contribution: **56** Type: **Poster**

A small area 11-bit SAR ADC for integrating pixel detectors at high repetition rate XFELs

jeudi 21 novembre 2024 13:30 (3 minutes)

The charge-integrating pixel detector is one of the major enablers of new science at X-ray free electron laser (XFEL) facilities. Such detector must revolve high dynamic range diffraction images resulting from interaction between the sample and ultra intense X-ray pulses with duration in order of femtosecond. Ideally, the frame rate of the detector should match the repetition rate of the laser machine. Some state-of-the-art integrating pixel detectors read out analog signals directly, which usually have limited frame rates of a few kHz. The CSPAD detector designed for LCLS (Linac Coherent Light Source) implements a single-slope ADC (Analog-to-Digital Converter) in each pixel, establishing a digital readout architecture with a frame rate of 120 Hz [1]. One recent work utilizing a similar pixel architecture as CSPAD intends to develop a high frame rate detector system up to 10 kHz with dedicated pixel readout chip design combined with high throughput data acquisition system [2-3]. However, none of the existing pixel detectors can satisfy the needs of future high repletion rate XFELs beyond 100 kHz, necessitating new detector development with the frame rate matching the laser machine. The high data throughput arising from high frame rate requires new digital readout architectures for the pixel readout chip with high speed and high resolution analog-to-digital conversion followed by fast digital signal processing and transmission.

This work proposes a small area and low power 11-bit SAR ADC suitable for massive on-chip integration in a pixel readout chip for high dynamic and high frame rate X-ray imaging at XFELs. The ADC circuit has been designed and implemented in a prototype chip using a 130 nm CMOS process. The area of the SAR ADC is typically dominated by the CDAC (capacitor digital-to-analog converter) array. In order to reduce the total number of unit capacitors, the CDAC employs a bridge capacitor to split the CDAC into an LSB (least significant bit) array and an MSB (most significant bit) array, with the weights of LSB array attenuated by the bridge capacitor. The susceptibility of the bridging CDAC structure to capacitor mismatches and parasitics is mitigated by using a non-binary radix with redundancy, which allows for correction of the missing level errors caused by capacitor mismatches through simple foreground calibration. A small unit capacitor of ~10fF was used for the CDAC and the ADC core circuit occupies an area of only 0.026 mm^2. The ADC design is expected to be implemented within the pixel array and one ADC will be shared by a 4 × 4 pixel group. At an ADC sampling rate of 2 MS/s, the pixel array can be readout with a frame rate of 125 kHz.

First measurement of the prototype chip shows that the ADC can achieve an ENOB of ~10 at 2 MS/s after calibration. Further measurements are ongoing. The design and measurement results of the prototype chip will be presented in the conference.

Auteurs principaux: WANG, Tianyang (Zhangjiang Laboratory); JI, zizhao (Shanghai Institute of Microsystem and Information Technology)

Co-auteurs: GAN, Fuwan (Shanghai Institute of Microsystem and Information Technology); LU, ShiJie (Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS)); SUN, Tao (Shanghai Institute of Microsystem and Information Technology); Dr JU, Xudong (ShanghaiTech University); SHENG, Zhen (Shanghai Institute of Microsystem and Information Technology); LIU, Zhi (ShanghaiTech University)

Orateur: JI, zizhao (Shanghai Institute of Microsystem and Information Technology)

Classification de Session: Posters

Classification de thématique: Electronics