A small area 11-bit SAR ADC for integrating pixel detectors at high repetition rate XFELs

Z. Ji[1,2], S. Lu[1,2], S. Liu[4,5], T. Sun[1], X. Ju[3], S. Zhang[3], Z. Sheng[1], F. Gan[1], Z. Liu[3], T. Wang[4*]

1 Shanghai Institute of Microsystem and Information Technology (SIMIT); 2 University of Chinese Academy of Sciences;

3 ShanghaiTech University; 4 Shanghai Optoelectronics Science and Technology Innovation Center; 5 Fudan University

1. Introduction

- The charge-integrating pixel detector is one of the major enablers of new science at X-ray free electron laser (XFEL) facilities. In order to improve the frame rate of the pixel detector to match the repetition rate of the laser machine, a digital readout architecture is essential[1],which necessitates an ADC with high speed and high resolution to satisfy the requirements of frame rate and dynamic range. As illustrated in Figure 1, there are commonly two ways for on-chip digitization: column-level ADC[2] and superpixel-level ADC[3].
- Since successive approximation register(SAR) ADC is characterised by small area and low power consumption, this work proposes a SAR ADC designed for next generation X-ray pixel detectors, which can be implemented as either a column-level ADC or a superpixel-level ADC.

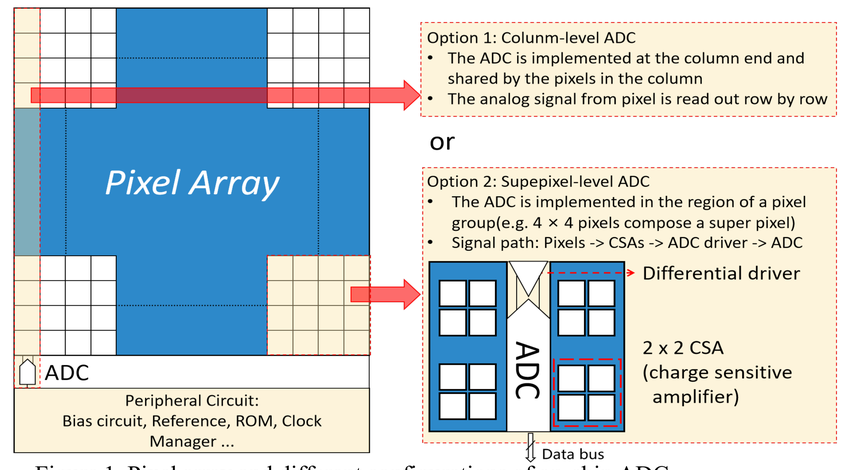

Figure 1. Pixel array and different configurations of on-chip ADC

2. ADC Design

- Resolution: 11-bit
- Architecture: SAR ADC
  - A bridge capacitor splits the CDAC and attenuate the weights of LSB (least significant bit) array, which can reduce the core area significantly
  - The attenuation factor β can be expressed as:

$$\beta = \frac{C_{BX}}{C_X + C_{LSB} + C_{BX}}$$

  - A non-binary radix with redundancy, allowing for correction of the missing level errors

Table 1. CDAC implementation

Bit	11	10	9	8	7	6	5	C_{BX}	4	3	2	1	0	C_X
Number of unit capacitors	37	20	13	7	4	2	1	2	6	4	2	2	1	6
Weight	444	240	156	84	48	24	12	-	6	4	2	2	1	6

  - A custom-made Metal-Oxide-Metal (MOM) unit capacitor of ~ 10 fF
  - A StrongArm latch as the comparator

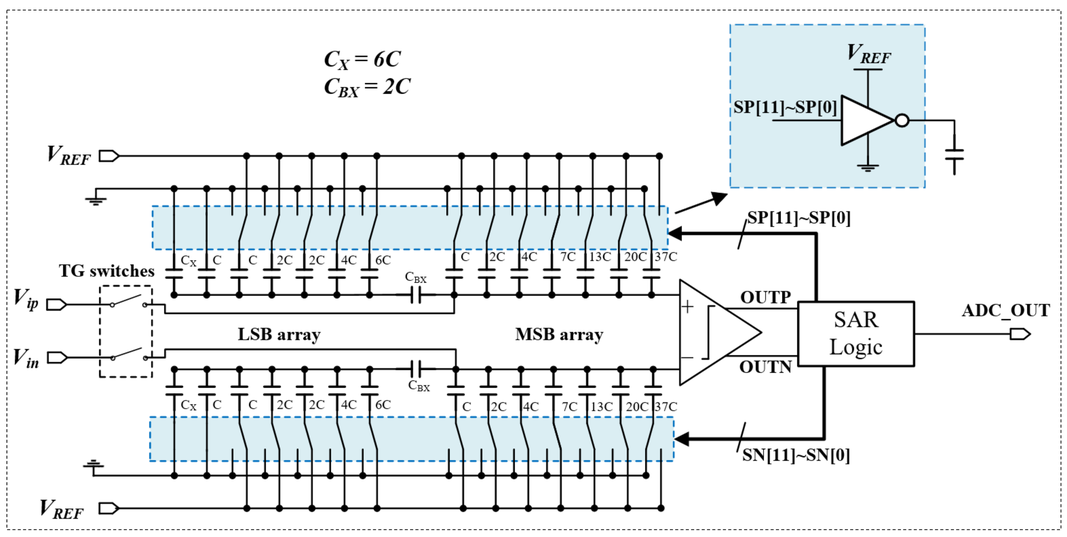

Figure 2. Schematic diagram of the proposed SAR ADC

3. Setup and ADC core

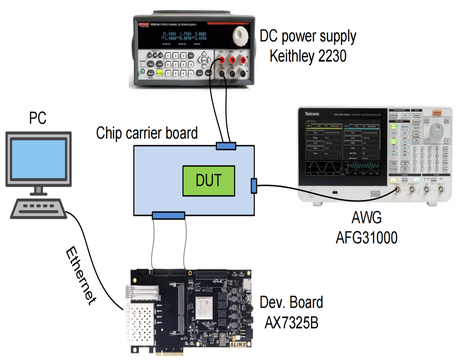

Figure 3. The measurement setup.

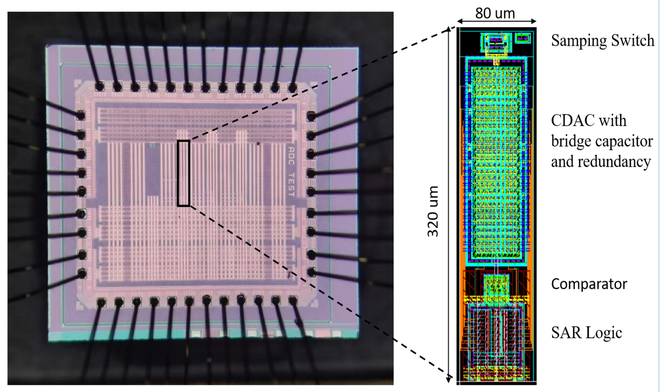

Figure 4. Micrograph of the prototype chip and the ADC layout.

- Core power supply: 1.2 V
- Reference voltage: 1.2 V
- Technology: 130 nm CMOS process
- ADC core dimension: 320 × 80 μm²

4. Results

- The result before calibration:
  - The bridging CDAC structure is sensitive to capacitor mismatches and parasitics
  - The mesured effective number of bit (ENOB) is 8.55-bit
- Use a simple calibration[4] to correct the missing level errors:
  - This calibration is statistically-based and no-additional circuit is needed
  - The ENOB up to 10.36-bit
  - The spurious-free dynamic range(SFDR) up to 77.72 dB

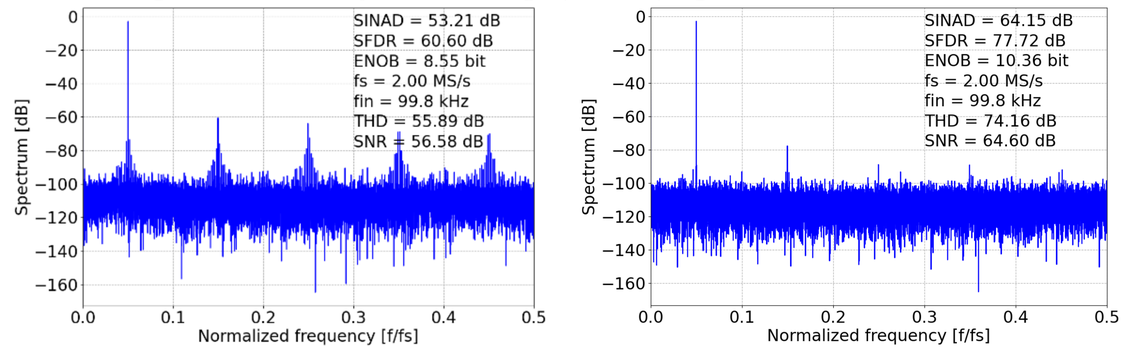

Figure 5. Measured spectra and dynamic performance before (left) and after (right) the calibration.

- Dynamic performance has been measured at sampling rates ranging from 0.5 MS/s to 2 MS/s at an input frequency of ~ 100 kHz
- Core power consumption is estimated to be 53 μW at a sampling rate of 2 MS/s, figure-of-merit (FoM) to be 20.2 fJ/conversion-step

Table 2. Measured dynamic performance after calibration and power consumption versus sampling rate

Characterization / Fs [MS/s]	SINAD [dB]	ENOB [bit]	SFDR [dB]	-THD [dB]	SNR [dB]	Power [uW]
0.5	79.27	10.60	79.27	75.82	66.00	13.36
1.0	78.33	10.41	78.33	74.88	64.85	26.47
2.0	77.72	10.36	77.72	74.16	64.60	52.61

5. Conclusion and Outlook

- The prototype chip has a small area and a high power efficiency, and the ENOB achieves 10.36-bits at a sampling rate of 2 MS/s.
- The calibration requires only a reference input, with no need for additional circuit, making it suitable to correct the ADC in pixel array.
- The chip with a sampling rate of 2MS/s is able to enhance the readout frame rate up to 125 kHz for the superpixel structure(one ADC is shared by a 4 × 4 pixel group).

References

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