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Matterhorn, a high flux detector for 4th generation synchrotrons

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The development of the new fourth-generation storage rings (or diffraction-limited storage rings, DLSR) poses new challenges to detectors in many aspects, the main one being the much-increased photon flux, exceeding the count rate capabilities of many of the actual single photon-counting detectors.
For this reason, the PSD detector group of the Paul Scherrer Institut (PSI, Switzerland) started the development of Matterhorn, a hybrid pixel detector capable of meeting the requirements of DLSRs and in particular of the SLS2. 0, the new storage ring being developed at PSI and which is supposed to be operational in 2025/2026.
The Matterhorn ASIC features a pixel pitch of 75 μm and is designed in UMC 110nm technology. Each pixel contains a charge-sensitive amplifier and a shaper, with selectable polarity, gain and shaping time, connected to four comparators. Each comparator has an independent threshold, gate signal and trim bit set to reduce threshold dispersion. Depending on the mode of operation, the pixel counting logic can trigger one of the four 16-bit counters. The counters state can be saved to a local memory to enable continuous operation.
In high-flux mode, the additional comparator thresholds can be set to values exceeding 100% of the incoming beam energy, thus detecting the pile-up of two or more photons, and effectively extending the count rate capabilities of the pixel to values exceeding 20MHz at 10% counting loss with an ENC<200e-rms.
This contribution will first explain the working principle and functionalities of Matterhorn, and then present the test results of our two prototypes.
Matterhorn 0.1 features a digitally synthesized control periphery, responsible for the chip control and readout, connected to two serial links working at the clock frequency of 1.6 GHz provided by an on-chip PLL.
Matterhorn 0.2 fixes some problems of the first version, and adds to that on-chip DACs for biasing, more debugging capabilities and an improved readout circuitry reaching a data rate of 3.125 Gb/s per data channel.
Finally, the plans for the design and production of the full-scale ASIC, Mattherhorn 1, planned for 2025, will be presented.

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