

Matterhorn, a high flux, single photon counting detector for 4th generation synchrotrons

Roberto Dinapoli, Aldo Mozzanica, Anna Bergamaschi, Bernd Schmitt, Carlos Lopez Cuenca, Christian Rueder, Davide Mezza, Dhanya Thattil, Dominic Greiffenberg, Erik Fröjdh, Filippo Baruffaldi, Jiaguo Zhang, Jonathan Mulvey, Julian Heymes, Khalil Daniel Ferjaoui, Kirsty Paton, Konstantinos Moustakas, Mar Carulla Areste, Martin Brückner, Martin Mueller, Partick Sieberer, Saverio Silletta, Shuqui Li, Simon Ebner, Thomas King, Vadym Kedych, Viktoria Hinger, Viveka Gautam, Xiangyu Xie. 11th PIXEL conference, Strasbourg France, 18-22 November 2024



Increased coherent flux [1]:

- >100x at 10 keV
- Up to 1000x at 20 keV

Increased electron energy (2.4 \rightarrow 2.7 GeV)

• Higher energy photons (80 keV)



[1] SLS 2.0 Storage Ring Technical Design Report PSI Bericht Nr. 21-02 November 2021

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- Faster count rate
- Higher frame rate
- Wider energy range



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- Higher frame rate 20 kHz continuous frame rate
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Charge integration PSI Center for Photon Science





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The "speed challenge": high photon flux





Single photon counting works extremely well if the incoming photon rate is reasonable low

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But as the rate increases we lose efficiency due to pulse pileup

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Pile-up mitigation techniques for SPC:

- Time over threshold
- Retriggering

Pile-up counting with multiple thresholds





100%: Energy of the monochromatic incoming photons

Paralyzable counter: $m = ne^{-\tau n}$

Probablility of two and three events pile-up:

•
$$p_2 = e^{-\tau n} (1 - e^{-\tau n})$$

• $p_3 = e^{-\tau n} (1 - e^{-\tau n})^2$

 $m_s = m + m_2 + m_3$

[1] Glenn F. Knoll, *Radiation Detector and Measurement* 4th Edition, Wiley

[2] M. Andrae The MYTHEN III Detector System - A single photon counting microstrip detector for powder diffraction experiments ETHZ Doctoral Thesis

Multi-thresholding: proof of concept with Mythen3.02(1D)





Settings: standard Energy: 15 keV

90% efficiency at: Single counter : 1.03Mcps

Multi-thresholding: proof of concept with Mythen3.02(1D)





Settings: standard Energy: 15 keV 3 90% efficiency at: Single counter : 1.03Mcps Three counters : 6 Mcps Noise: 175e- RMS

Multi-thresholding: proof of concept with Mythen3.02(1D)





Settings: standard Energy: 15 keV

90% efficiency at: Single counter : 1.03Mcps Three counters : 6 Mcps Noise: 175e- RMS

Settings: Fast [1]

Single counter 3.52 Mcps Three counters 20.87 Mcps Noise:~250e-

PSI Center for Photon Science [1] M Andrä The MYTHEN III Detector System - A single photon-counting microstrip detector for powder diffraction experiments ETHZ PhD Thesis 2021

x6

Matterhorn – a new single photon counter for SLS2.0



	EIGER	MATTERHORN		
Technology	UMC 250 nm	UMC 110 nm		
Pixel size	75 x 75 um ²	75 x 75 um ²		
Thresholds	1	4		
Counter depth	12 bit (3x4)	4x16 bit		
90% efficiency	350k counts/pixel/s*	15-20M counts/pixel/s		
Module size	4x8cm ²	4x8cm ²		
HighZ/LGAD	No	Yes		

*DECTRIS EIGER2 90% efficiency at ~2 Mcps (UMC 110nm)

T. Donath et. al. *EIGER2 hybrid-photon-counting X-ray detectors for advanced synchrotron diffraction experiments* J. Synchrotron Rad. (2023). 30, 723-738







¹⁾ Both e^- and h^+ readout possible

Static power/pixel 9.6µW (4 comparators)





²⁾ One comparator can be connected to two counters (pump-probe)





³⁾ Each comparator can individually be 'masked' (disconnected from the counter)

 \rightarrow reduce switching for noisy channels





⁴⁾ Each comparator can individually be powered-off when noisy or not used

Periphery blocks



> PLL

- Locking range: 930 MHz ÷ 2600 MHz
- Power: 18 mW

Pixel & counter selector

- Pixel/counter addressing logic
- Pixel/counter readout logic (includes 16 or 8 bit mode)
- 8b/10b encoding
- High speed serializers

CML driver

- Main driver and pre-emphasis current tunable (3 bits): 3 mA ÷ 15 mA
- Pre-emphasis delay tunable (2 bits)

All periphery logic synthesized with digital tools for the first time!



Matterhorn prototypes

Matterhorn 0.1, 12.2022



- 2 Pre/shaper variations
- 2 Comparator variations
- 2x 1.6 GHz serializers
- 1.6 GHz CML driver

(with pre-emphasis)

- ASICs: ~5x5 mm² (3.6x3.6 active=48x48=2304 pixels)
- MPW chips bump-bonded to sensor

Matterhorn 0.2, 10.2023



- One pixel version only
- 2x 3.125 GHz serializers
- 3.125 GHz CML driver
- Internal DACs for biasing
- Some "features" fixed

Matterhorn prototypes

Matterhorn 0.1, 12.2022



- 2 Pre/shaper variations
- 2 Comparator variations
- 2x 1.6 GHz serializers
- 1.6 GHz CML driver (with pre-emphasis) PSI Center for Photon Science

- ASICs: ~5x5 mm² (3.6x3.6 active=48x48=2304 pixels)
- MPW chips bump-bonded to sensor
- PLL working
 - Jitter < 5 ps • (limited by measurement setup)
 - HS logic/data transmission working
 - BER< 10⁻¹⁵ •
 - (limited by measurement time)
 - **DACs** working
 - 8 bits

Matterhorn 0.2, 10.2023

PSI



- One pixel version only
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- 3.125 GHz CML driver
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Basic characterization of MH02

- Calibration at: 7, 9, 12, 15 keV
- Threshold scans fitted with analytical model:
- $f(x) = (p_0 + p_1 x) + 0.5 \left(1 + Erf\left(\frac{x-\mu}{\sqrt{2}\cdot\sigma}\right)\right) \left(A + C(x-\mu)\right)$



• Metrologie beamline at SOLEIL with help from: Marie Andrä and Arkadiusz Dawiec



Single pixel data

Four counters scan





Scanned at the same time

Noise performance of MH02





Threshold dispersion at 9 keV



vrf	Untrimmed [eV]	Trimmed [eV]		
200	998	59		
300	905	43		
400	668	33		
500	477	29		
	:16 to	20		

- Small chip (48x48 pixels)
- Non optimized trimming procedure

Single counter rate tests at MS beamline - MH01





Predicted rate capability using analytical model

Single counter rate tests at MS beamline – MH01





Note: slightly over estimated due to kB peak

Single counter rate tests at MS beamline – MH01



Noise vs. rate capability











Note: fitted with simple paralyzable function





- Comparator biased in "low power" mode
- Vrf can be set even lower (100-150)
- Preamp/shaper biases can be further tuned

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	EIGER	MATTERHORN 1		
Technology	250 nm	110 nm		
Chip outputs	32xCMOS, 200 Mb/s	4xCML, 3.125 Gb/s		
Single chip	6.4 Gb/s	12.5 Gb/s		
Module (8 chips)	51.2 Gb/s	100 Gb/s		
Readout channels/module	2x10Gbit/s	1x <mark>100</mark> Gbit/s		
Frame rate	~10 kHz 8bit (burst)	~20 kHz 8bit (continuous)		
Continuous R/W	Yes	Yes		

Timeline



commissioning user op. user operation darktime SD user operation 2022 2023 2024 2025 2026 $\langle 4 \rangle$ \bigcirc $\langle \mathfrak{S} \rangle$ (6) (8) (7) ready for darktime start darktime tunnel closure user operation re-start user op. nom. Beam available start shutdown Second prototype (MPW) Submitted Single module detectors? Full ASIC submission Multi module detectors First prototype First prototype Planned submission submitted (MPW) back! of third prototype Second prototype

back!

Timeline



commissioning user op. user operation darktime SD user operation 2022 2023 2024 2025 2026 10 11 12 01 02 03 04 05 06 07 08 09 10 11 12 01 02 03 04 05 06 07 08 09 10 11 12 01 02 03 04 05 06 07 08 09 10 11 12 01 02 03 04 05 06 07 08 09 10 11 12 01 02 03 04 05 06 07 08 09 10 11 12 $\langle 4 \rangle$ \bigcirc $\langle \rangle$ $\langle \mathfrak{S} \rangle$ (6) ready for darktime start darktime tunnel closure user operation re-start user op. nom. Beam available start shutdown Second prototype (MPW) Submitted Single module detectors? **Full ASIC submission** Multi module First prototype detectors First prototype **Planned submission** submitted (MPW) back! of third prototype Second prototype

Matterhorn 1, the full-size chip

Same pixel as Matterhorn 0.2

	MATTERHORN 1
Technology	110 nm
Chip active area	1.92x1.92 cm ² 256x256 pixels
Pixel size	75 x 75 um ²
Thresholds	4
Counter depth	4x16 bit
Trim bits/compar.	6
Static power/pixel (4 comparators)	9.6µW
HighZ/LGAD	Yes

MH 1.0 ~2 cm MH0.2

New features

- Pixel data transfer:
 - Current mode signal distribution (to pixel periphery)
- New periphery, additional features:
 - Global signals distribution (RES,STO,EN<0:3>)
 - Counter summing mode
 - 4 bit mode
 - 64b/66b encoder for serializers
 - SPI interface for configuration/slow control
- Gating (4 independent EN) <20ns
- No active circuitry on the chip sides (less dead area)

Conclusion and outlook

Matterhorn is a new SPC detector for SLS2.0 targeting:

- 20Mcps count rate with 10% loss of efficiency
- 250 eV 80 keV energy range (with LGADs and HighZ)
- 20kHz frame rate; <20 ns gating

Results from MH01 and MH02:

- Noise down to <~80e- in slow settings
- Demonstrated ~7.5 Mcps at 90% efficiency using multiple thresholds
- Tau of 42ns in single counter mode indicates
 15Mcps should be possible with pileup counting

MH0.

• Tuning ASIC parameters

Submission of full ASIC spring 2025...









Left to right: Jiaguo Zhang, Bechir Braham, Konstantinos Moustakas, Viktoria Hinger, Christian Ruder, Shqipe Hasanaj, Dominic Greiffenberg, Julian Heymes, Anna Bergamaschi, Khalil Ferajoui, Carlos Lopez-Cuenca, Xiangyu Xie, Pawel Kozłowski, Martin Brückner, Roberto Dinapoli, Kirsty A. Paton, Filippo Baruffaldi, Mar Carulla, Bernd Schmitt, Thomas King, Patrick Sieberer

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Backup slides

Pile-up mitigation techniques



- Use charge integration with dynamic gain switching (Jungfrau, Jungfrau 2)
- Time over threshold/retriggering



Operating modes of a single photon "counter"





FIGURE 1. (A,B) Method to compare different strategies for mitigating the pulse pileup: (C) normal counting (reference), (D) time-over-threshold, (E) retriggering, and (F) pileup tracking. The *x*-axis refers to time, while the *y*-axis represents the height of the analog signal.

Pileup tracking

Comparison of pileup mitigation



Figure 2



FIGURE 2. Detected rate as a function of the photon rate for a single-photon counting detector calculated using Eqs 1–4, covering the different solutions described in section 2.2. The rate is expressed as the reciprocal of the shaping time per pixel per second. The gray and the blue secondary axes compare the performance in Mphotons/pixel/s of SPC detectors with τ =150 ns and τ =30 ns, respectively.

[1] A. Bergamaschi et. al. Time-over-threshold readout to enhance the high flux capabilities of single-photon-counting detectors J. Synchrotron Rad. 18, 923-929. 2011

[2] P. Zambon, Dead time model for X-ray photon counting detectors with retrigger capability, NIMA 2021

Pixel testability





⁵⁾ The preamp can be pulsed with a programmable voltage step ⁶ Preamp and shaper outputs of pixel 0,0 can be monitored

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⁶⁾ Each counter can individually be pulsed Comparator and "count" outputs of pixel 0,47 can be monitored

The «energy challenge»: low photon energies



Soft X-ray applications at SwissFEL and SLS (250 eV – 2 keV)





The «energy challenge»: high photon energies



Hard x-ray applications at Synchrotrons, 15-80keV

	Absorption efficiency	Signal stability	Afterglow	Spectral resolution capability	Dark current	Noise	Availability
Silicon	-	++	++	++	+	+	++
CdZnTe High Flux type	++	++	++	+	++	++	+
CdZnTe Spectroscopic type	++	+	+	+	++	++	+
CdTe e ⁻ Schottky type	++		ο	ο	+	+	+
CdTe Ohmic tye	++			-	-		+
GaAs:Cr	+	0	0	+		-	+

- CdZnTe is the material of choice above 15 keV
- 4×4 cm² sensor commercially available
- Dynamic behavior (signal stability, afterglow) close to silicon sensors
- → Higher photon energies need to be studied
- Crystal defects influence sensor uniformity
- Fluorescence photons with long absorption range

- **GaAs:Cr** is **promising**, but doesn't perform as well as CdZnTe
- Two European suppliers, 8×4 cm² sensors available
- > Afterglow acceptable up to photon fluxes
 - \rightarrow Continuous: <10⁽⁸⁻⁹⁾ ph/mm²·s
 - → Pulsed: $<10^{(6-7)}$ ph/mm² ·pulse
- Some signal loss at photon fluxes above > 3×10^{10} ph/mm²·s
- Crystal defects influence sensor uniformity, variation of effective pixel size + Short hole lifetime → Craters
- High dark current → For long exposure times: ideally SPC

Timeline



¹ Move to new building



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MatterHorn 0.2 Efficiency Simulation

