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Thermomechanical design validation for quad pixel modules for the ITk

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The current programme of upgrades to the ATLAS detector to take advantage of the opportunities presented by the HL-LHC will include a complete replacement of the tracking system. This upgrade will install an all-silicon tracker called the ITk, the innermost five layers will be made up of Si Pixel detectors.
The majority of the installed Si detectors are Quad Pixel detectors. These are ~4x4 cm2 assemblies consisting of a Si sensor tile which is attached using a flip chip bonding process to four Front End readout ASICs (ITkPix) to make a bare Quad module. Each of the Quad modules has over 600,000 50x50 m pixels, ~150,000 pixels per FE. A flexible PCB is mounted on the bare module and connected to the FE-ASICs and the sensor tile by means of wedge wire bonding and provides connectivity for power, DCS and data. After assembly the modules are coated in parylene for HV isolation. Once the module is completed it is attached to a support structure made from materials with a low coefficient of thermal expansion (CTE) and a high thermal conductivity, which hold the module in position and supply cooling and route power and data services to the module.
Quad modules will operate in extremely challenging radiation environments. The total radiation doses ranging from 1.7 MGy for the outer barrel, 3.5 MGy for the outer endcap and 7.3 MGy for the inner system with fluences of 2.3 × 1015cm21MeV neq to 9.2 × 1015cm21MeV neq. To ensure long term survival while operating in this very high radiation environment the modules are operated cold, the minimum coolant temperature will be -45oC and the upper operating temperature is controlled by an interlock system to +40oC. However, because the quad module is made from a range of materials with widely varying CTE's and is attached to the local supports using a high CTE adhesive they needed to be carefully designed to ensure bump disconnections are not caused by thermal stresses.
FEA was used to model the stresses within a module, particularly on the solder bumps, during temperature cycling of a quad module attached to the local supports material. The design space covers several parameters including the thickness of the copper traces in the PCB and the thickness and stiffness of the adhesives to ensure that the stresses induced by the CTE mismatch of the components do not cause catastrophic failure of the module. Design was validated with prototype modules. The design validation utilised 100 cycles over an extended temperature range of 55 to +60oC to ensure that the modules are robust enough to cope with the various temperature regimes it will be exposed to over 10yrs of operation and pre-installation transportation. Here we present the FEA carried out to guide the design of the flex PCB and the module testing regimes, and compare the results from design validation of prototype modules.

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