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H2M: Porting a hybrid readout architecture into a monolithic 65 nm CIS

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The high energy physics community recently gained access to a 65 nm CMOS imaging process, which enables a higher density of in-pixel logic in monolithic active pixel sensors (MAPS). To explore this novel technology, the H2M (Hybrid-to-Monolithic) test chip has been designed and manufactured. The design followed a digital-on-top design workflow and ports a hybrid pixel-detector architecture, with digital pulse processing in each pixel, into a monolithic chip. The chip matrix consists of 64×16 square pixels with a size of 35x35 µm2, and a total active area of 1.25 µm2. The charge collection in the sensitive layer is improved by employing process modifications and layout optimizations.

This contribution introduces the H2M chip, its in-pixel analog and digital front-end, the four acquisition modes (time-of-arrival, time over-threshold, hit-counting, and triggered), and its integration into the Caribou readout system. It will also cover parameter optimization through laboratory measurements, threshold equalization, and noise characterization. Furthermore, laser measurements and test beam results from the SPS and DESY-II show a non-uniform charge collection pattern across the pixel cell. The origin and impact of this pattern on efficiency, timing, and spatial resolution will be discussed. This effect is less visible at lower thresholds, where a hit detection efficiency above 99% has been achieved in triggered mode.

Auteurs principaux: SIMANCAS, Adriana; DORDA, Ana; VELYKA, Anastasiia; RECKLEBEN, Christian; LEMOINE, Corentin; DANNHEIM, Dominik; BUSCHMANN, Eric; FEINDT, Finn; VIGNOLA, Gianpiero; WENNLÖF, Håkan; GREGOR, Ingrid-Maria; KREMASTIOTIS, Iraklis; SCHLAADT, Judith; HANSEN, Karsten; MENDES, Larissa; HUTH, Lennart; DEL RIO VIERA, Manuel Alejandro; CAMPBELL, Michael; GADOW, Philipp; BALLABRIGA, Rafael (CERN); CASANOVA MOHR, Raimon; RUIZ DAZA, Sara (DESY); RETTIE, Sebastien; SPANNAGEL, Simon; MAFFESSANTI, Stefano; VANAT, Tomas; SNOEYS, Walter; HE, Yajun; OTARID, Younes (CERN)

Orateur: RUIZ DAZA, Sara (DESY)

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