ID de Contribution: **37** Type: **15mOral**

The LHCb VELO Upgrade II: design and development of the readout electronics

mardi 19 novembre 2024 09:44 (20 minutes)

The LHCb Upgrade-I detector is currently operating at the Large Hadron Collider at CERN and it is expected to collect about 50 fb−1 by the end of Run 4 (2032), when many sub-systems of the detector will reach their end of lifetime. In order to fully exploit the High-Luminosity LHC potential in flavour physics, the LHCb collaboration proposes a Phase-II Upgrade of the detector, to be installed during the LHC Long Shutdown 4 (2032-2034). This Upgrade will consist of a re-designed system with the capability of operating at an instantaneous luminosity of 2×10^{34} $cm^{-2}s^{-1}$, i.e. a factor 10 larger than that of the Phase-I Upgrade detector and will allow the experiment to accumulate an integrated luminosity of about 300 fb−1.
Operating in the HL-LHC environment poses significant challenges to the design of the upgraded detector, and in particular to its tracking system. The primary and secondary vertices reconstruction will become more difficult due to the increase, by a factor 8, of the average number of interactions per bunch crossing (pile-up). Similarly, the track reconstruction will become more challenging, as well as time-consuming, because of the large increase in the track multiplicity. Finally, the much harsher radiation environment will make the design of the sub-systems quite challenging, with the radiation damage expected to be more severe for most detectors. In particular, the performance of the VErtex LOcator (VELO), which is the tracking detector surrounding the interaction region, is essential to the success of this Phase-II Upgrade. With the expected higher particle flux, the VELO Upgrade-II detector will have to tolerate a dramatically increased data rate: assuming the same hybrid pixel design and detector geometry, the front-end electronics (ASICs) of the VELO Upgrade-II will have to cope with rates as high as 8 Ghits/s, with the hottest pixels reaching up to 500 khits/s. With this input rate, the data output from the VELO will exceed 30 Tbit/s, with potentially a further increase if more information is added to the read-out.

The VELO collaboration is currently exploring new sensor technologies, and the benefits that would derive from adding a time stamp to the track reconstruction, such that interactions in the same bunch crossing can be more effectively disentangled. The VELO case is extremely challenging, as the high granularity required for the spatial measurement severely limits the area in each pixel of the ASIC where the time-stamping circuitry can be implemented. With a 50 ps hit resolution, each VELO track would have multiple time measurements from the traversed pixels and thus a precise estimation of the production time of charged particles. The most recent advances in this field, and the potential candidates that can meet the VELO Upgrade-II requirements, will be presented. In particular, the current state-of-the-art prototypes in the development of ASICs with TDC-per-pixel architecture, the PicoPix ASIC (which is an evolution of the Timepix4 design) and the TIMESPOT ASIC, will be discussed.

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Classification de Session: Electronics

Classification de thématique: Electronics