Readout for the LHCb HL-LHC VELO

19.11.2024

Dan Johnson, on behalf of the LHCb collaboration

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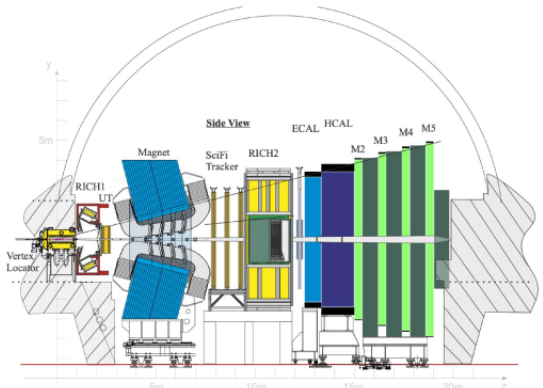
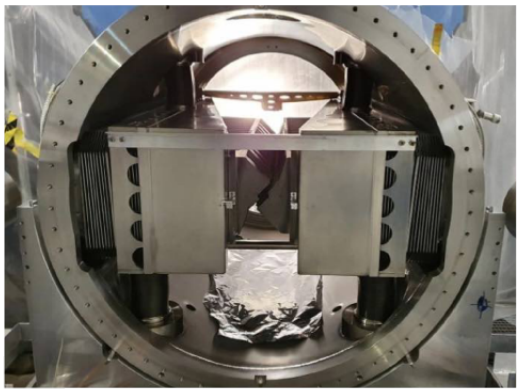
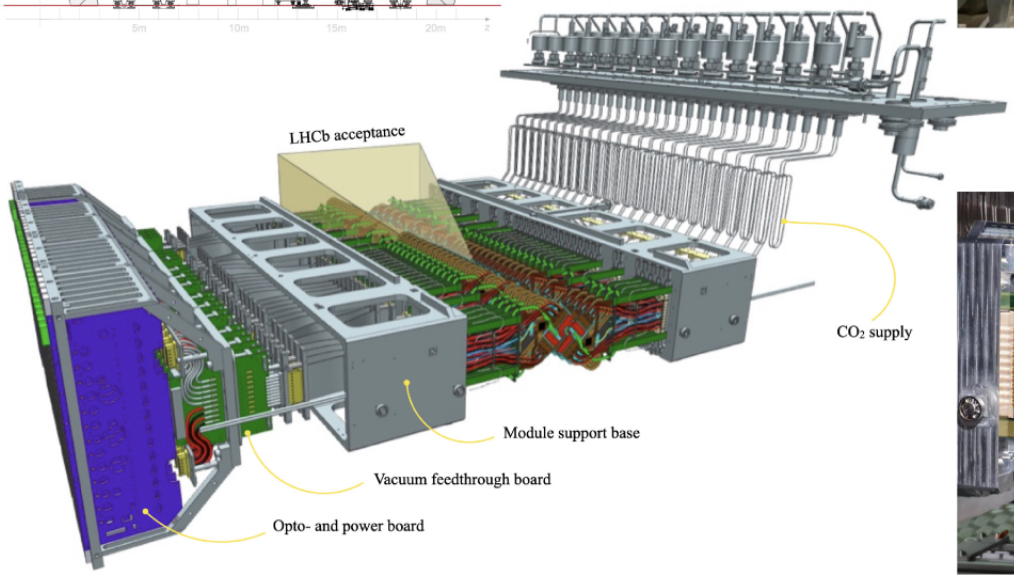
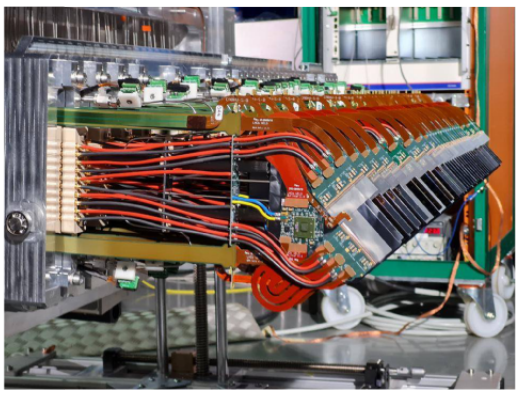
The present LHCb VELO





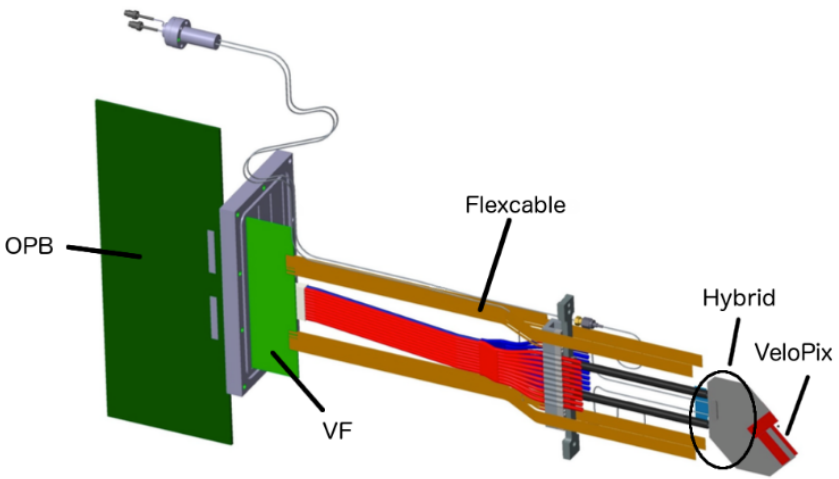


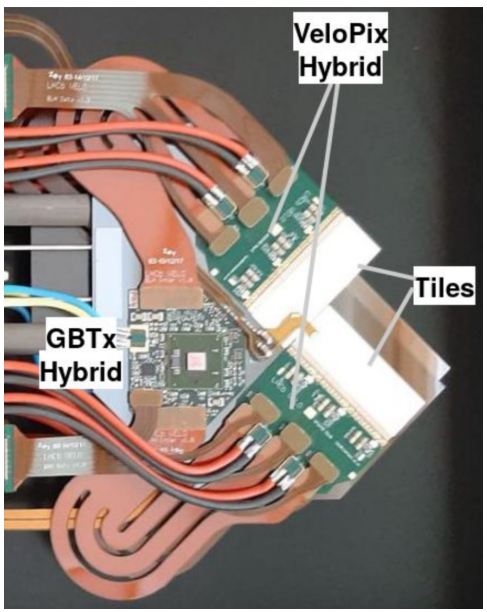


- Upgrade from strips ⟶ pixels in 2022
- Approaches beam at 5.1 mm
- Instantaneous luminosity of $2 \times 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- 41M 55μm × 55μm pixels across 208 hybrid sensors
- VELO sep. from LHC vacuum by 250μm RF foil
- Readout every bunch crossing (40 MHz)

The present readout: front-end

- Ten 5.12 Gbps links per 6 ASICs direct to backend (and control signals via GBTx)
  - 50 cm flexible PCB cables absorb VELO motion
  - Vacuum feedthrough board
  - Optical and power board - OPB (& monitoring, LV distribution)





- Down-links used to distribute control signals and LHC clock

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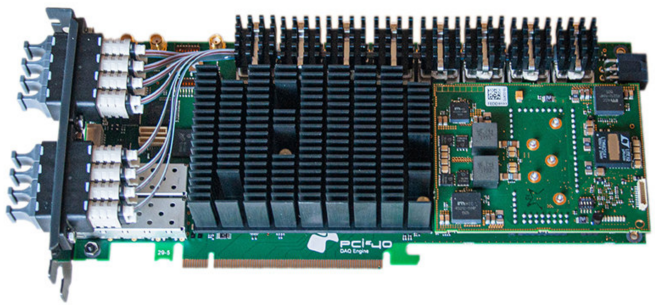
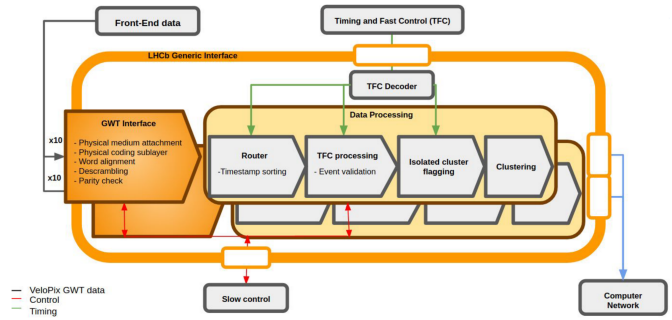
The present readout: back-end

3 Tbps from VELO distributed to 52 LHCb-common PCIe40 boards, based on Intel Arria10 FPGA

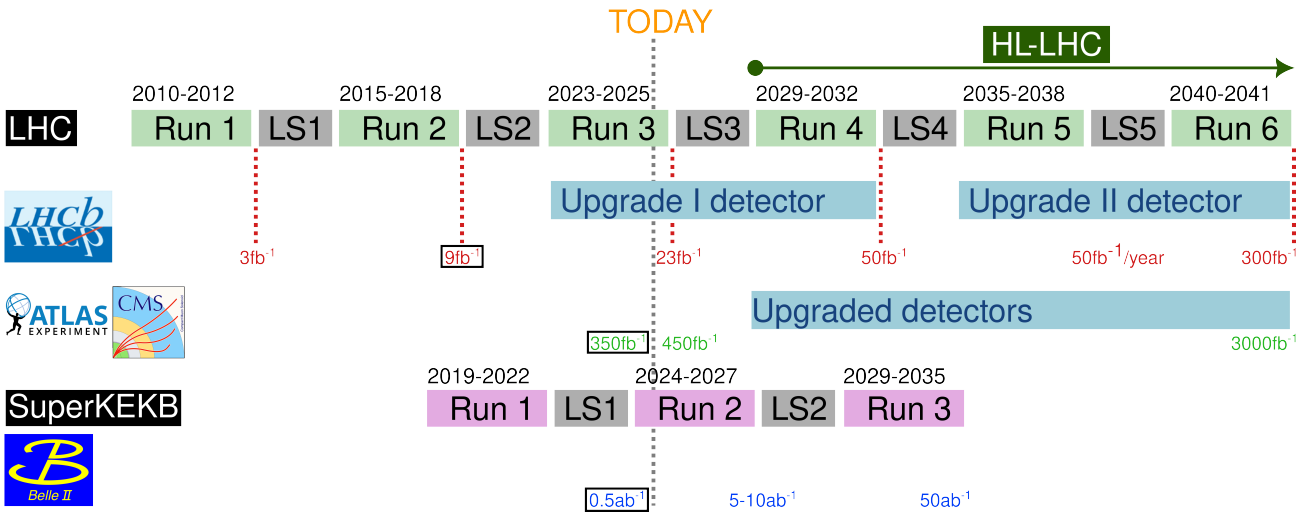




Custom firmware:

- Low-power (4 x 5.12 Gbps; 30 mW each) GWT serializer/protocol: GWT interface
- Data unordered by bunch crossing ID: router sorts data from 10 input links by timestamp
- Align the data: TFC processing
- Clustering: could be delegated to another FPGA board

Conditions for the HL-LHC VELO



- Instant. lumi. from 2 → 15 × $10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (cf 5 × $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at ATLAS/CMS)
- Machine optimisation → longer 'luminosity levelling' times. Accumulate 50 fb^{-1} per year through Run 5 and 6
- Saturate machine limits at LHC point 8 after 6 years at 300 fb^{-1}

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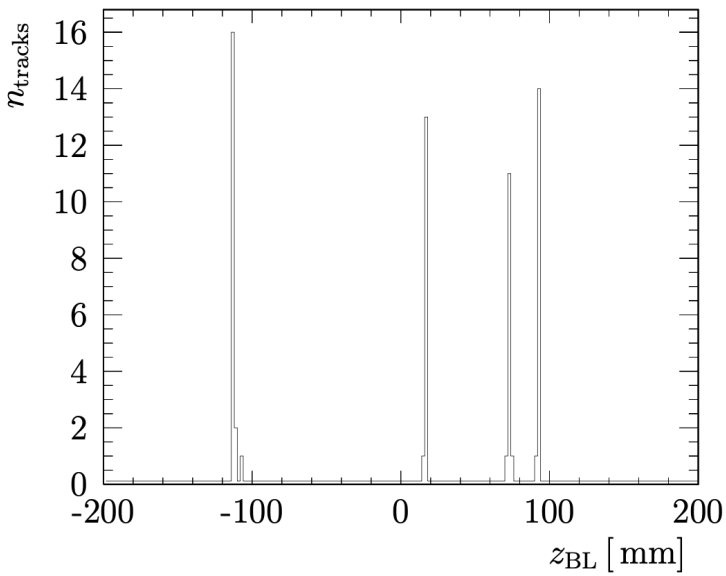
Challenges for the HL-LHC VELO

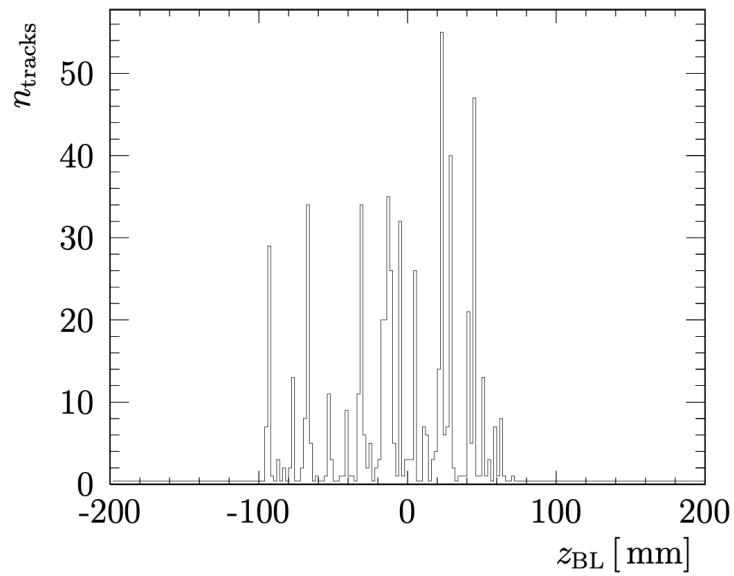
7.5 x higher $\mathscr{L}$ a challenge: focus on event reconstruction

PVs overlap: the centrality of a high-precision timestamp ($\sim 20\,\mathrm{ps}$ per track)

Today



HL-LHC



- 'minIP wrt any PV' falls down
- much more combinatorial background
- nearby PVs can fake displaced vertices

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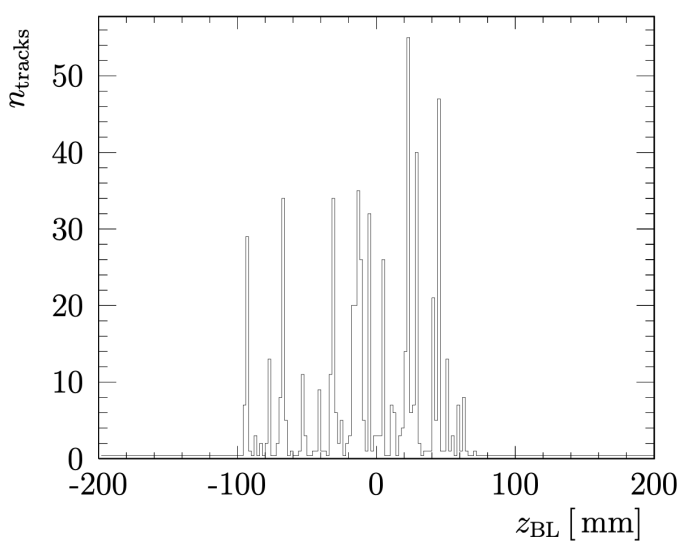
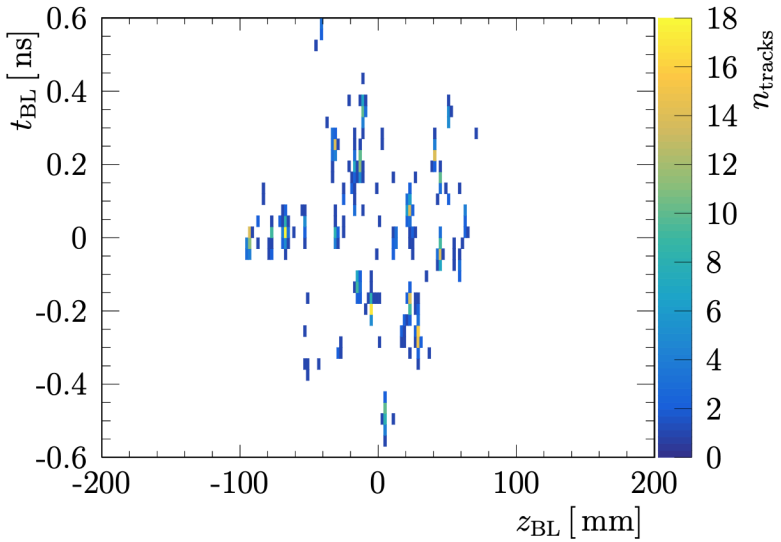
Challenges for the HL-LHC VELO: reconstruction

Extrapolate time of track to point of closest approach to beam-line





Associate tracks to closest local maximum and then 4D fit to the vertices iteratively adding tracks

Recover present reconstruction environment with timing; **physics programme depends on maintaining performance benchmarks in HL-LHC operation**

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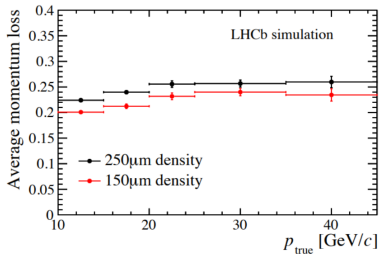
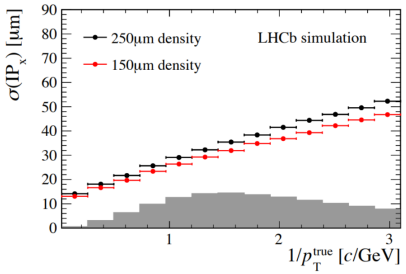
Challenges for the HL-LHC VELO: material

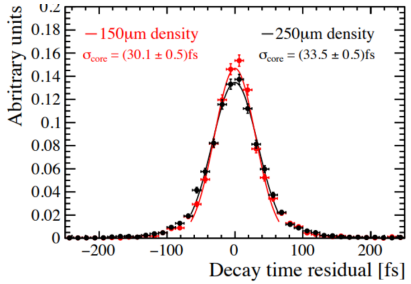
- Need low material budget:



Comparison of energy loss of electrons between the 250 μm and 150 μm foils.(1)

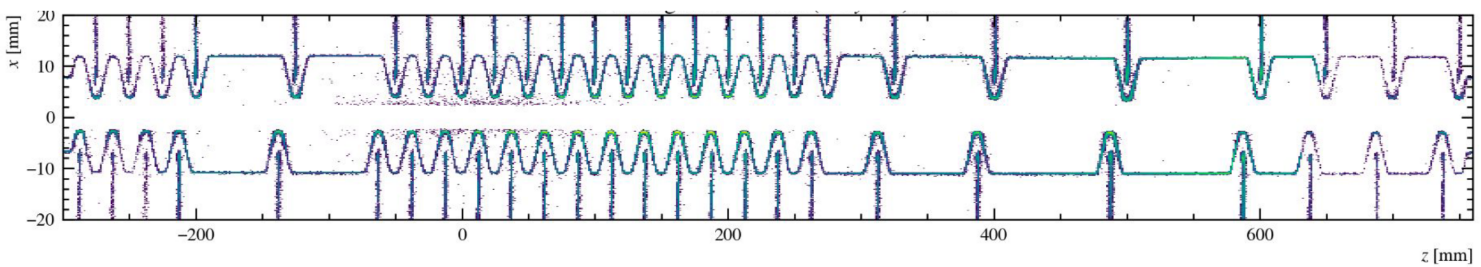


IP resolution simulated for different foil thicknesses.(2)



Proper time resolution for Bs->Dspi simulated events (2)

- New designs for LHC RF continuity may place U2 VELO in primary LHC vacuum
  - Constraints for outgassing of elements (glue securing fibers)
  - Emphasis on volume and nature of vacuum feed-through



Imaging the VELO modules and RF foil in 2024 with hadronic interactions

Challenges for the HL-LHC VELO: module

- Maintaining today's performance:
  - Today's sensors reach 5.1 mm from LHC beam with $\sim$ 50μm pitch
  - TID at that distance increases by $\mathcal{O}(10)$ to $5 \times 10^{16} n_{eq}\,\mathrm{cm}^{-2}$
  - VELO location less readily accessible than today
- whilst adding $\mathcal{O}(10)\,\mathrm{ps}$/track time resolution
  - 3D sensor technology
  - First HEP ASIC in 28nm process
- Pseudorapidity coverage likely largely similar to current VELO, but
  - are backgrounds tolerable at very small angles?
  - is a rectangular sensor geometry desirable to maintain?

Proposed readout technology requires significant flexibility to design changes

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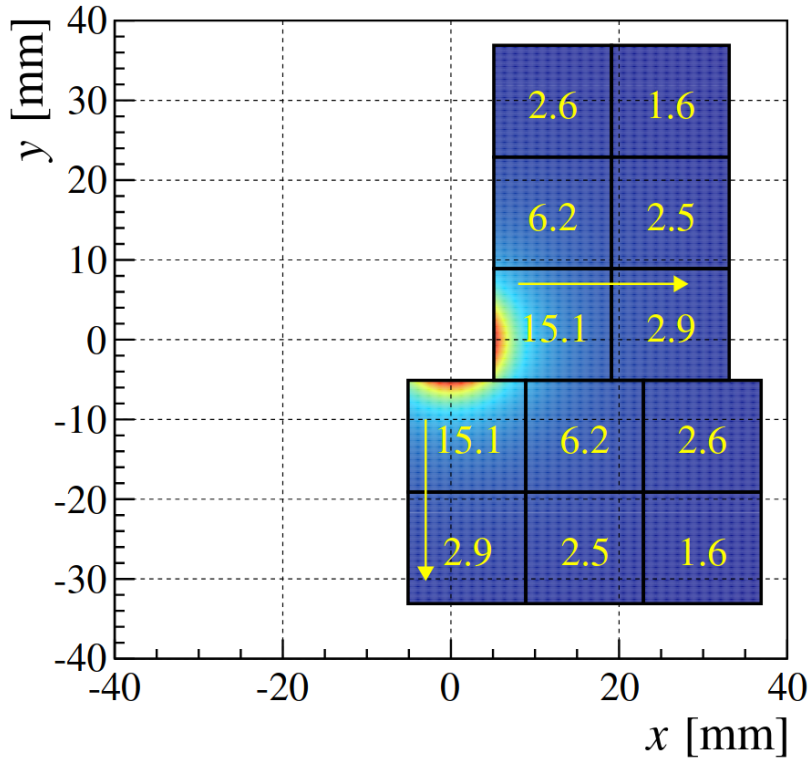
Effect on data volume

- Hottest module (today) 90 hits/event
  - Cluster typically 2.2 pixels
- ASIC data rate peaks at 15 Gbps
- Highly non-uniform across sensors
- Total VELO data rate of 3 Tbps



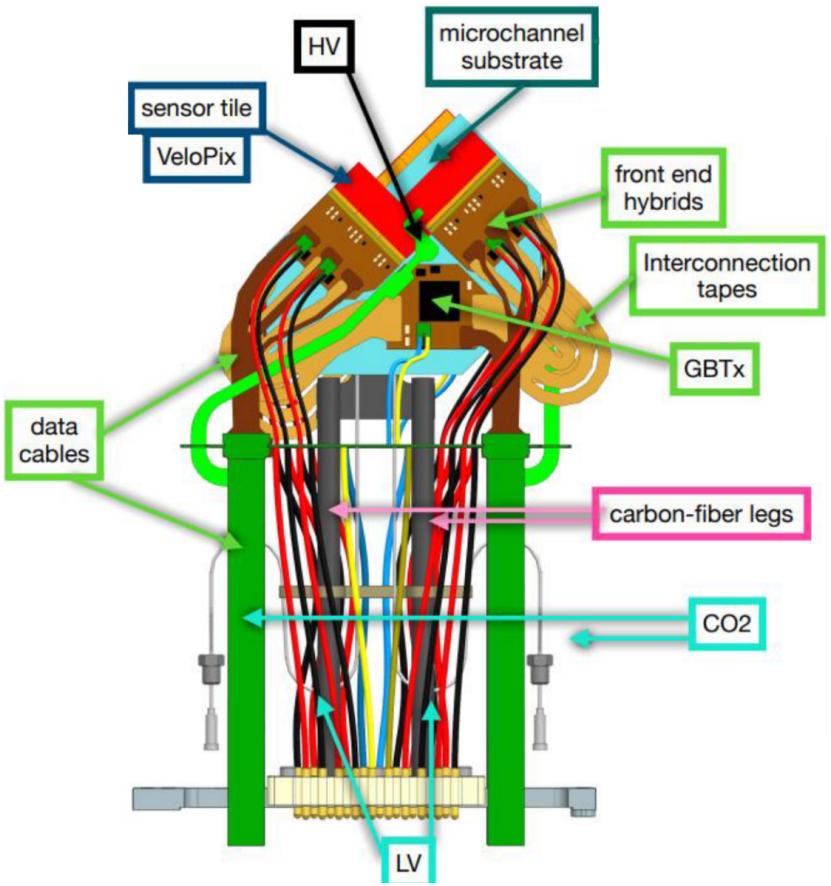
For upgrade II:

- Assume hit rate increases by 7.5
- Addition of cluster timestamp increases data packet
- Consider on-ASIC clustering

Reasonable to plan for $\mathcal{O}(100)$Gbps hottest ASIC

Module development

- Today's ASIC power budget: 3W/module
  - Roughly 30 mW devoted to each high-speed serializer
- Finite cooling budget: evaporative CO_2 cooling; 500μm wafer
- Consequences for volume of LV-copper entering downstream acceptance
  - Resolution impact of multiple scattering
  - Downstream occupancy impact of secondary production
- More details here



Multivariate problem: material budget, ASIC power, and readout lanes

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Candidate technology: copper readout

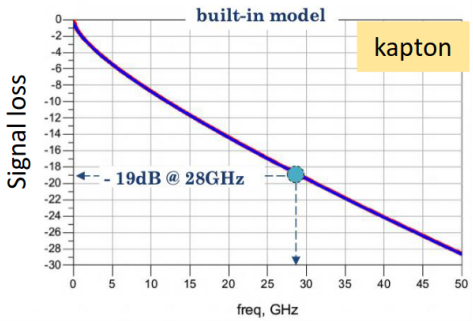
At the edge of the ASIC:

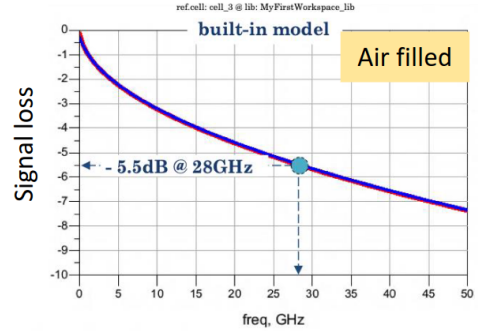
- Timepix4: 16 10Gbps serializers per chip; 24mW each
- VeloPix2: 28Gbps serializers at periphery

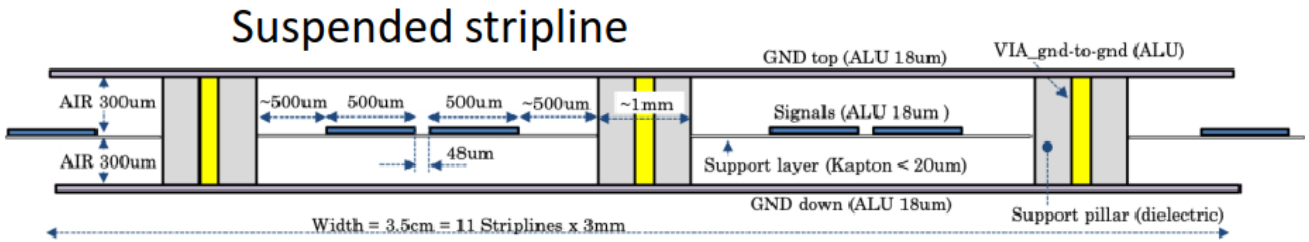
Traversing the vacuum:

- Roughly 70cm to the electro-optic converters
- U1 5Gbps links; losses tolerable
- U2 28Gbps! Repeaters? New transmission line?

Attenuation in 1 m stripline
(courtesy V. Gromov)







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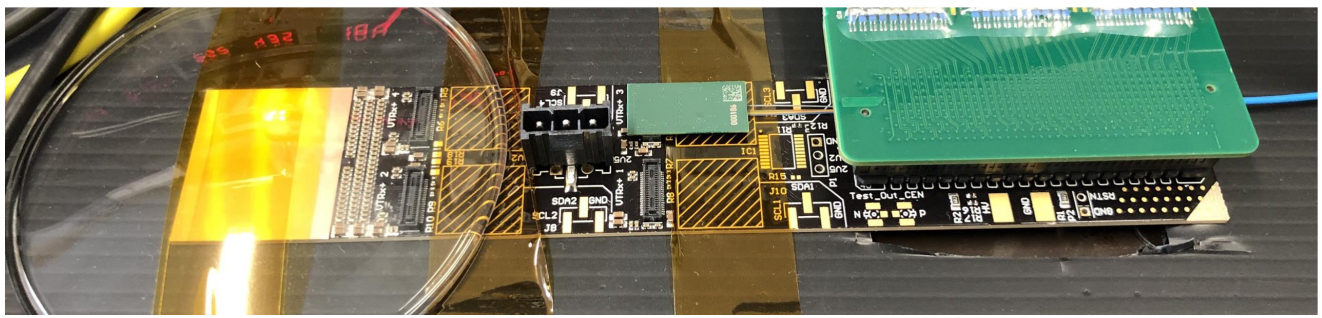
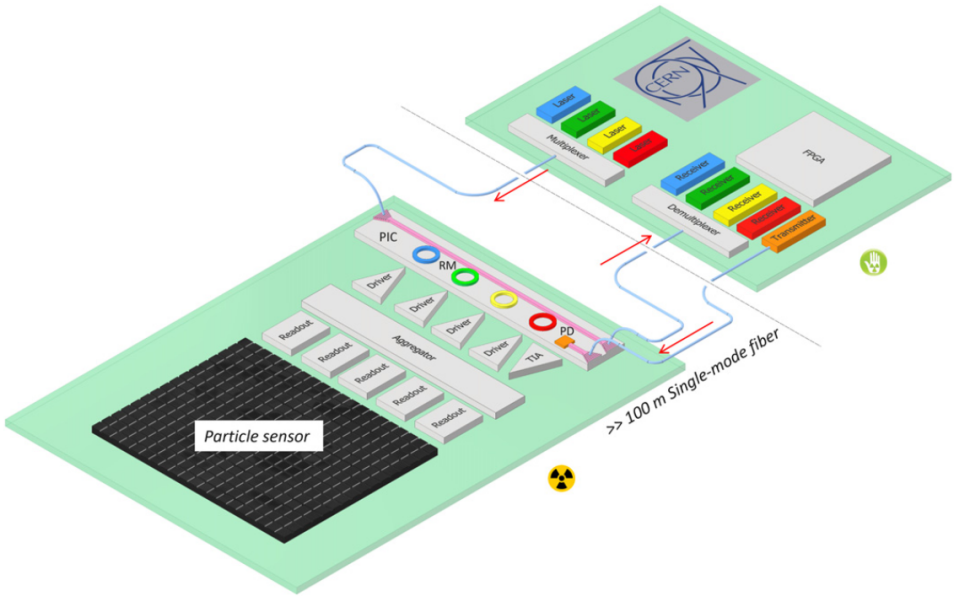
Candidate technology: copper readout

- Next generation of LHC links: Versatile Link+
  - 10.24 Gbps radiation-tolerant links (can approach beam within few cm; few 100 MRad)
  - Recent opto-demonstrator module shown last month



- Some scenarios require > 10 links per ASIC
  - Large number of feed-throughs and glued fibres
  - Challenge to integrate with hottest ASIC periphery
- Standard backend

Candidate technology: silicon photonics



- Optical transmission, with optical source in low-radiation zone
- Custom low-power, small-footprint, radiation-hard front-end
  - Ring-modulators imprint signal on four WDM 25Gbps links
  - 100Gbps per PIC/fiber
  - Co-packaged optics in development in DRD WP 7.1a
- Commercial, off-the-shelf back-end

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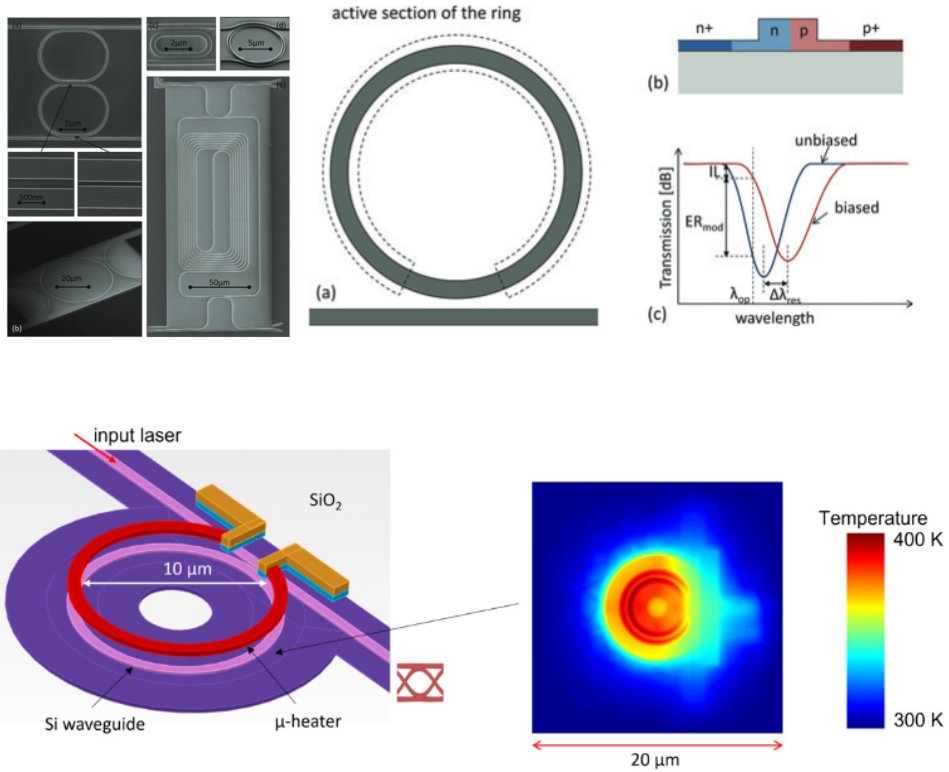
Candidate technology: silicon photonics



- Biasing junction shifts optical length and shifts ring resonance
- Operate ring on the edge of resonance
- Micro-heater (well-insulated by SiO_2) fine-tunes resonance
- Excellent tolerance to TID up to 1 Grad

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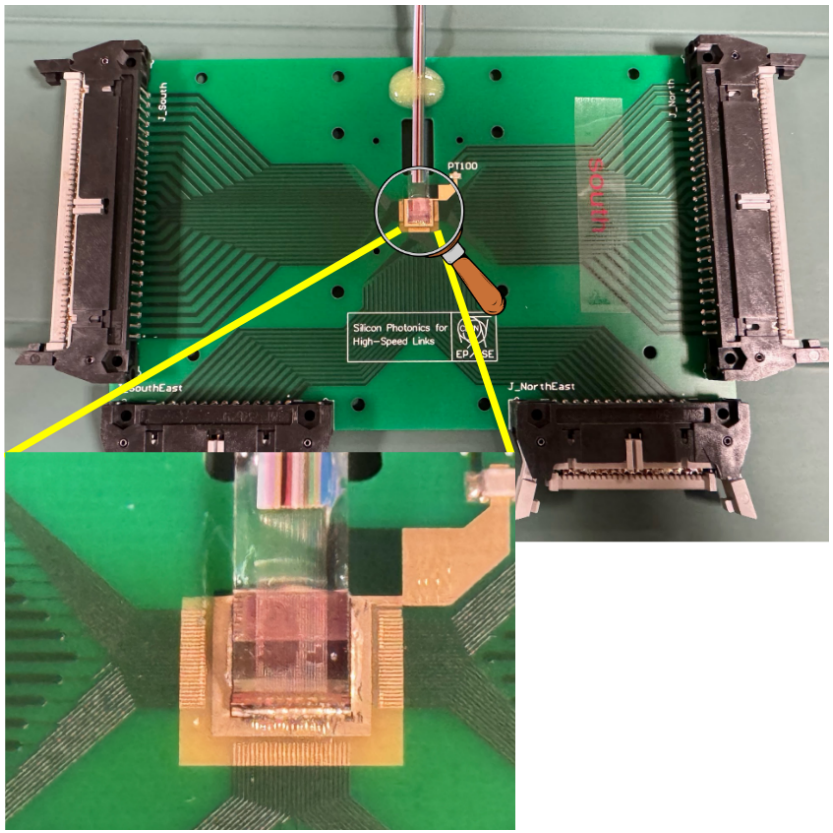
Candidate technology: silicon photonics

- Ring modulators require very low power
- Bandwidth (100 Gbps): some headroom for even hottest VELO ASIC
- Very short copper element then low-material fiber
- Challenge to develop vacuum feed-through for 624 fibers
- Must demonstrate high-speed 25 Gbps serializer stabilty



Candidate technology: silicon photonics

- Link depends upon external laser driver
- Optical Internetworking Forum multi-source agreement
- Development underway: EL**SFP** module with 8 × 100mW light source at 1310nm
- First prototypes demonstrated at ECOC 2024 two months ago
- One module drives ∼ 4 ASICs
- $\mathcal{O}(100)$ required for LHCb

OIF

White Paper: Management of External Light Sources and Co-Packaged Optical Engines

OIF-MGT–Co-Packaging–ELSFP-01.0

November 1st, 2022

Conclusions

- Increase in luminosity and addition of timing pose a major data-challenge for the LHCb VELO
- Mitigate with on-detector processing, within power budget
- Two options to readout the residual high data rate
  - Copper variant: LHC standard, but large number of links
  - Optical-at-periphery: Larger headroom, but non-standard backend
- LHCb@HL-LHC in review by LHC experiments committee
- VELO upgrade II technical design report for submission in 2026