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Survey of sub-electron noise CMOS image sensors

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Low-light imaging applications, such as astronomy or microscopy, require low-noise image sensors. Noise levels far below 1 e_{rms}^- are pursued. Single-photon detection is considered the holy grail of image sensing.

Existing imaging technologies capable of detecting and resolving individual photons like Photomultiplier Tubes (PMT), Single Photon Avalanche Diodes (SPAD), and Electron Multiplication Charge-Coupled Devices (EMCCD) employ internal multiplication of the primary electron. Although these have sub-fractional e_{rms}^- noise, these methods suffer from two performance-limiting properties: dark counts and excess noise.

This paper surveys solutions for photo charge integrating active pixel sensors (APS) and classic CMOS image sensor (CIS) technology. For integrating image sensor pixels to have quantum-limited photon detection, the readout noise at the pixel front needs to be substantially less than 0.3 e_{rms}^- [1].

APS pixel separates the photo charge sensing and the charge to voltage conversion node. This results in a high in-pixel conversion gain and the cancellation of the kTC noise with correlated double sampling (CDS). The pinned photodiode in APS has benefits regarding dark current and rivals the charge-coupled devices (CCD) performance. Continuous improvement of CIS over the last two decades has led to the replacement of CCD by CIS.

In this survey, we review the publications that report a noise figure close to 0.3 e_{rms}^- or lower. Based on the device and circuit techniques used and breakthroughs reached, we classify the publications into the following categories:

1. Pixel circuit topologies
   - CCD-based skipper in CMOS [2][5],
   - Classic PPD-based pixel with source follower readout,
   - In-pixel capacitive trans-impedance amplifier (CTIA) [8], etc.
2. Circuit operation techniques
   - Non-destructive readout [2][5],
   - In-pixel amplification [6],
   - Oversampling methods [2][4][8], etc.
3. Device optimizations
   - Floating gate skipper in CMOS [2],
   - Reduction in floating diffusion (FD) capacitance [4][7][9],
   - Reset gateless pixel [4][7], etc.
4. Transistor selection
   - Buried channel transistors [9],
   - Thin oxide transistors [4],
   - Standard transistors, etc.

At the conference, we will give an outlook on recent developments at Caeleste.

References

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[7] M. Seo *et al.*, IEEE Electron Device Letters, 2015

[8] Q. Yao *et al.*, Proceedings of the International Image Sensor Workshop, 2015

[9] S. Wakashima *et al.*, Symposium on VLSI Circuits, 2015

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Classification de Session: Astrophysics applications

Classification de thématique: Astrophysics applications