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Survey of sub-electron noise CMOS image sensors

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Outline

- Motivation: why ultra-low noise?
- Ultra-low noise non-{CMOS image sensors}
- Introduction to CMOS image sensors
- Read noise to reach photon counting performance
- What optimizations are needed?
- Low noise readout techniques
- Literature survey
- Floating Transfer Gate (FTG) pixel
- Overview table
- References

Motivation: why ultra-low noise?

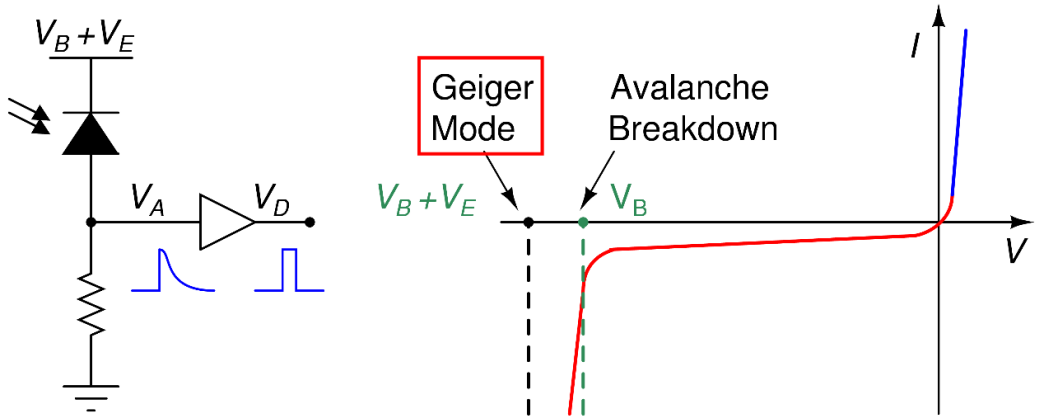
- **Astronomy**
  - Observation of distant faint planets and stars in dark background.
  - Ground-based spectroscopy of distant bodies, exoplanets.

- **Medical and Life science**
  - Study cells, genes and micro-organisms with fluorescence microscopy.
  - Analysis of chemical compounds with Raman spectroscopy.

- **Quantum sensors**
  - Measurement of spatial correlation in-between photons.

Ultra low noise *non*-{CMOS image sensors}

SPAD (Single Photon Avalanche Diode)

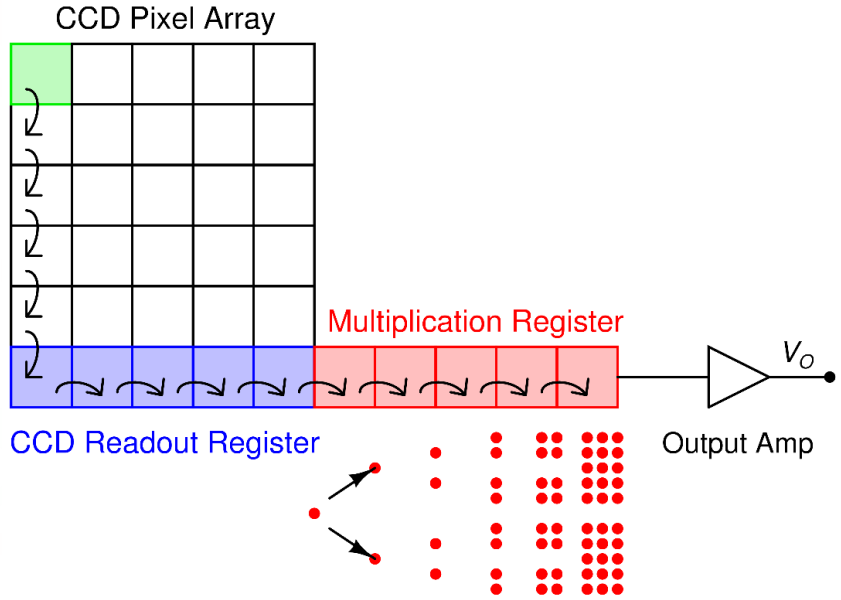


SPAD frontend circuit and I-V curve

- **Pros:**
- Single photon detection
- Very high timing resolution (pico-sec)

- **Cons:**
- Dark counting and after-pulsing
- Dead time of a few nsec to 100 nsec
- High voltage is needed for operation (20-25 V)
- Large pixel and low fill factor

EMCCD (Electron Multiplication Charge Coupled Devices)

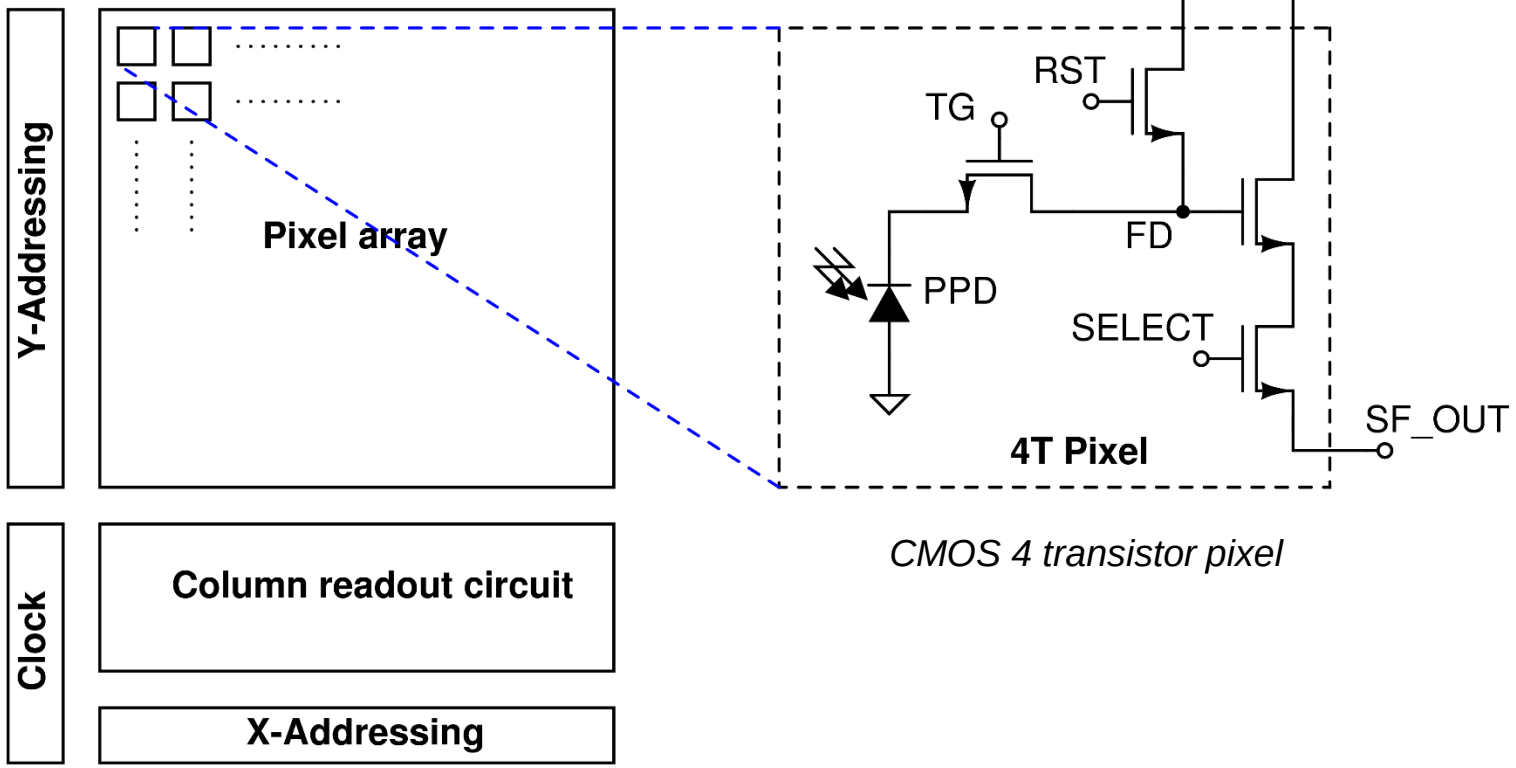


EMCCD block diagram

- **Pros:**
- High gain before Q-V conversion (usually up to 1000x)

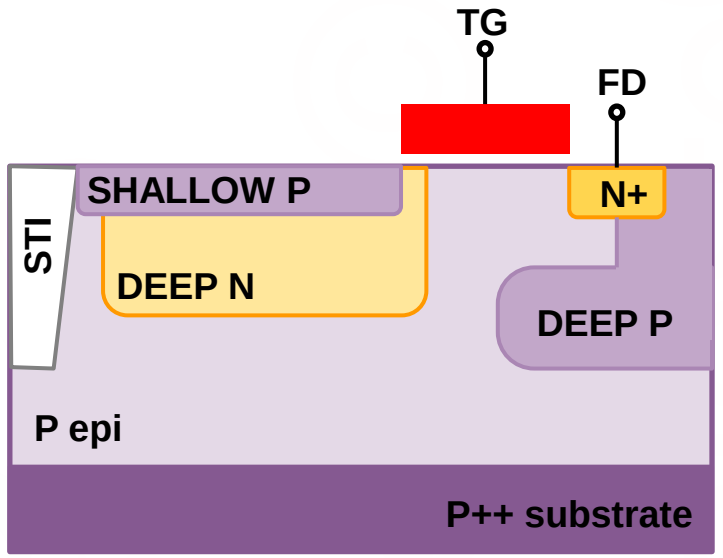
- **Cons:**
- Excess noise due to the stochastic multiplication process
- Multiplication gain aging
- High voltage is needed for electron multiplication (50 V)
- Extra cooling to reduce the dark current

CMOS image sensors



CMOS image sensor block diagram

CMOS 4 transistor pixel



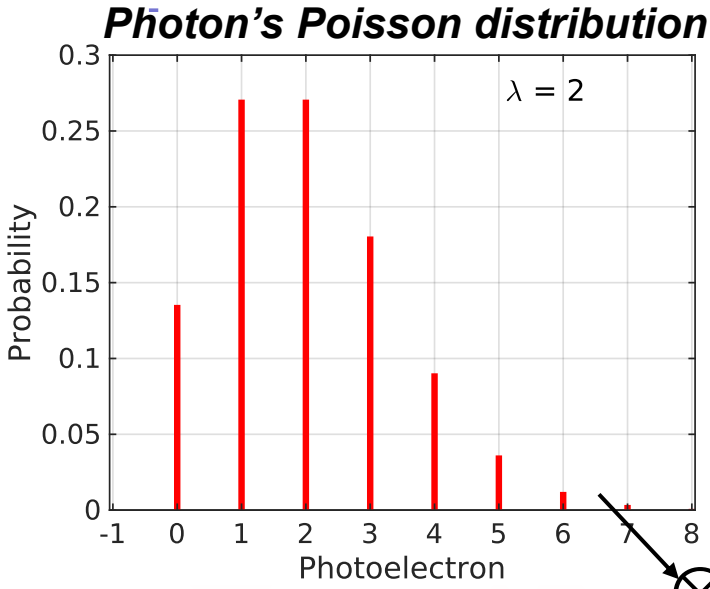
Pinned photo-diode device structure

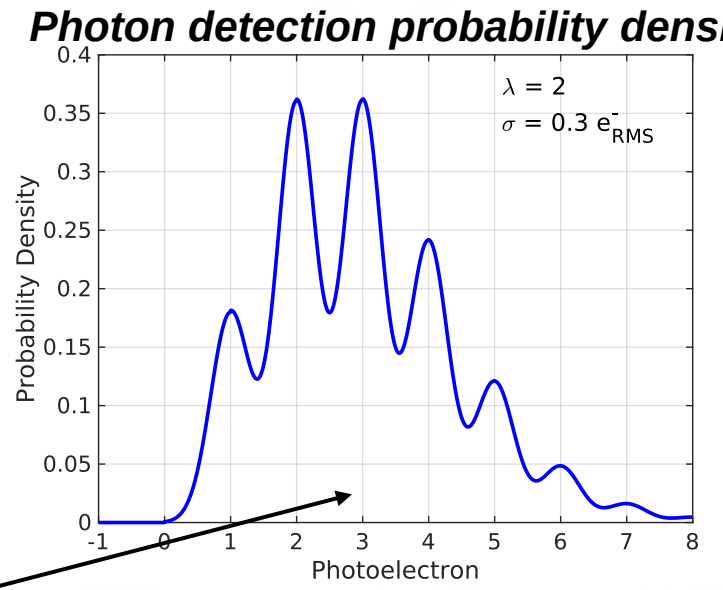
Typical measures to reduce noise:

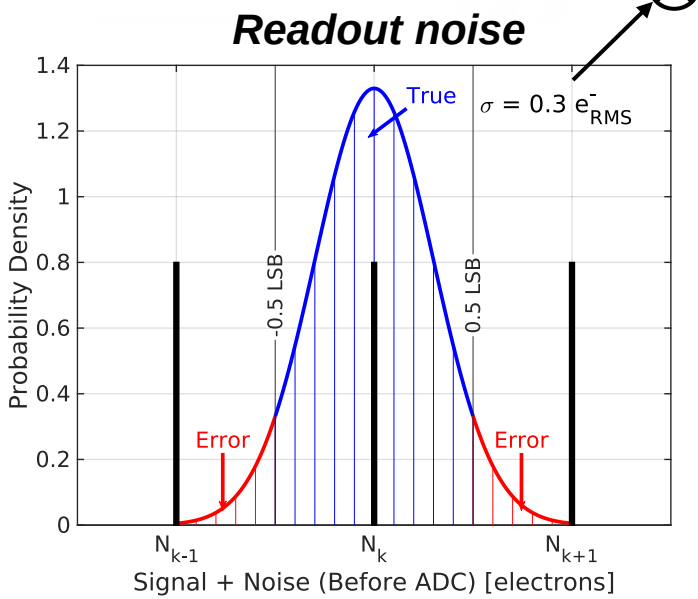
1. Low dark current for low Dark Current Shot Noise (DCSN)
2. Correlated Double Sampling (CDS) for reset noise cancellation
3. High Charge to Voltage conversion Factor (CVF)

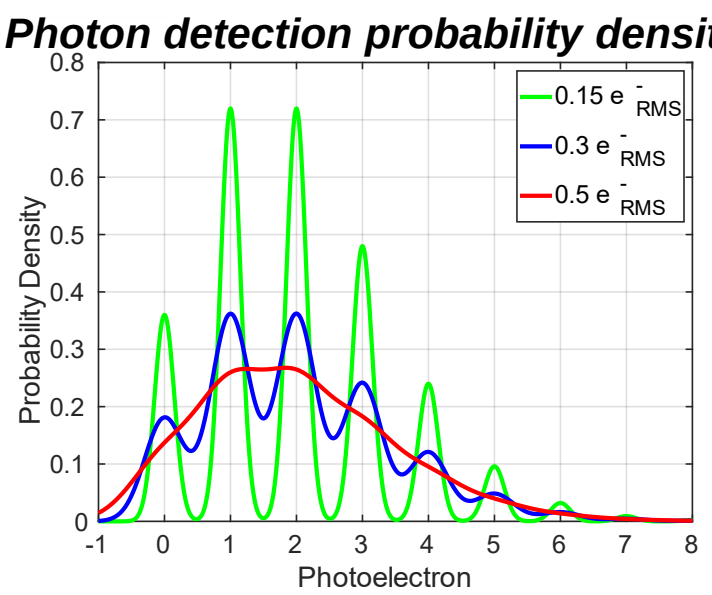
PPD - Pinned Photodiode
TG - Transfer Gate
RST - Reset
FD - Floating Diffusion
SF - Source Follower
4T - 4 Transistor pixel
STI - Shallow Trench Isolation

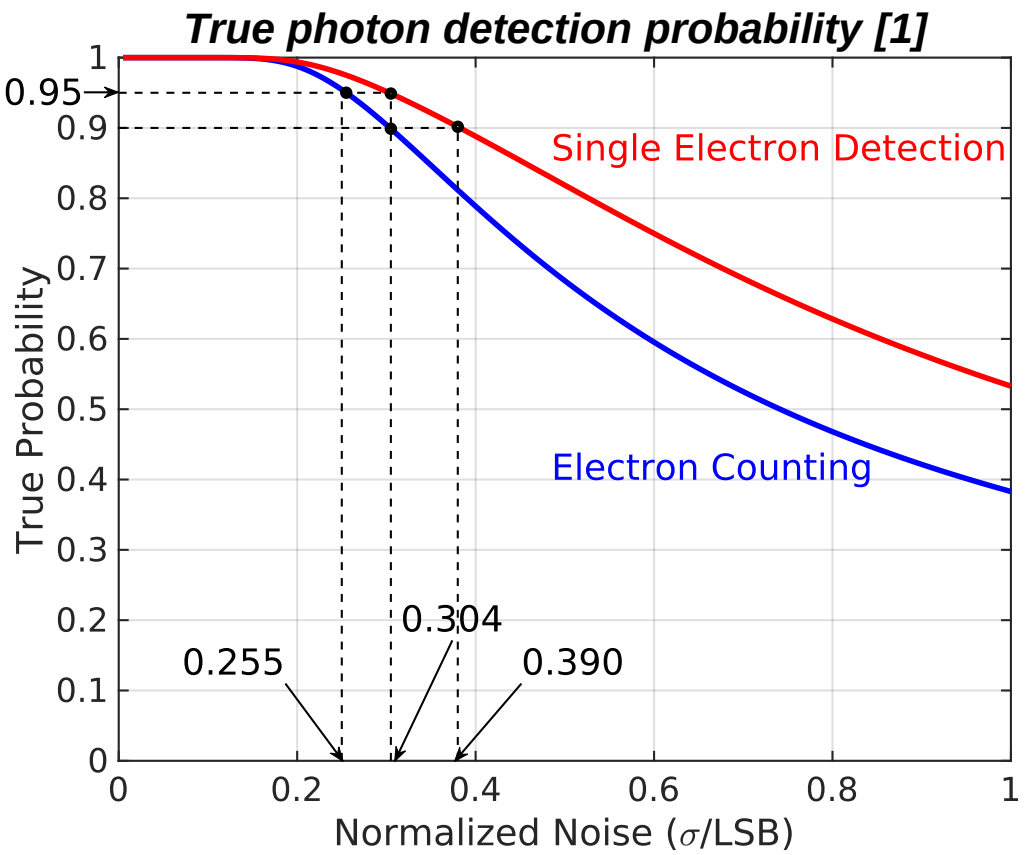
Read noise to reach photon counting performance







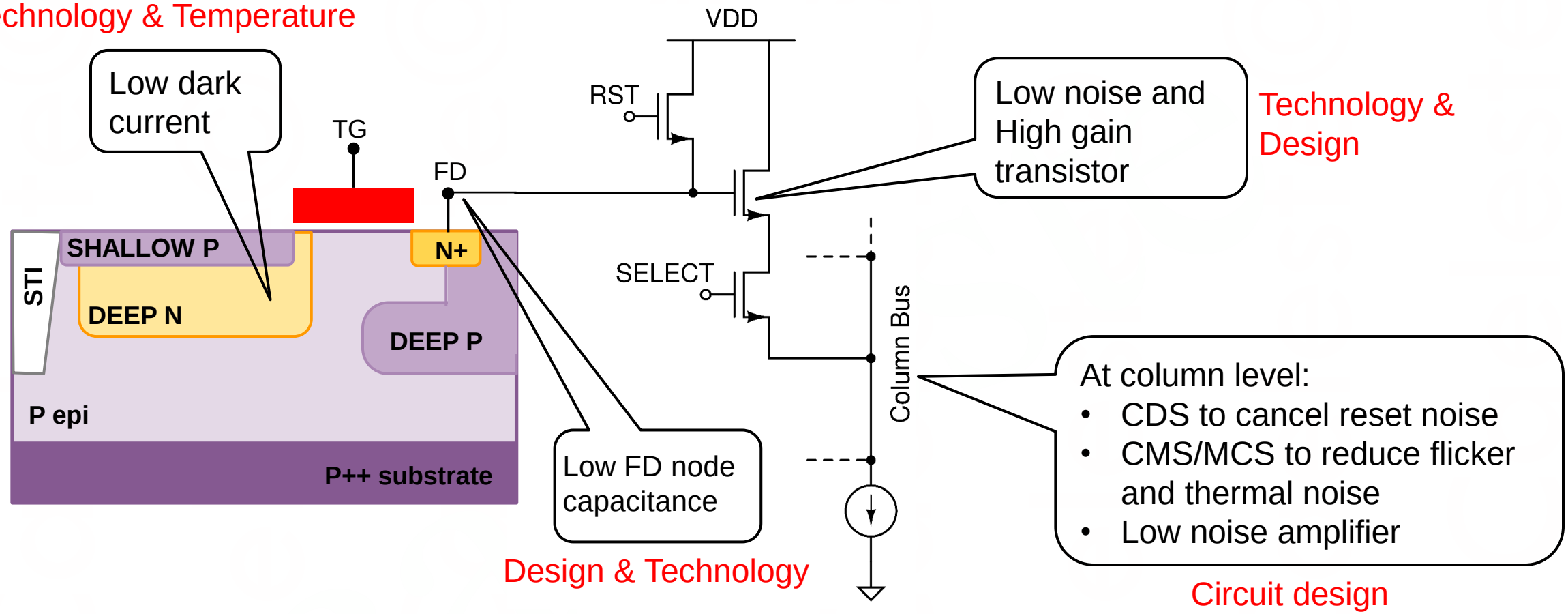




λ – average no. of incoming photons
σ – readout noise standard deviation in e^-_{RMS}

Which optimizations are needed?

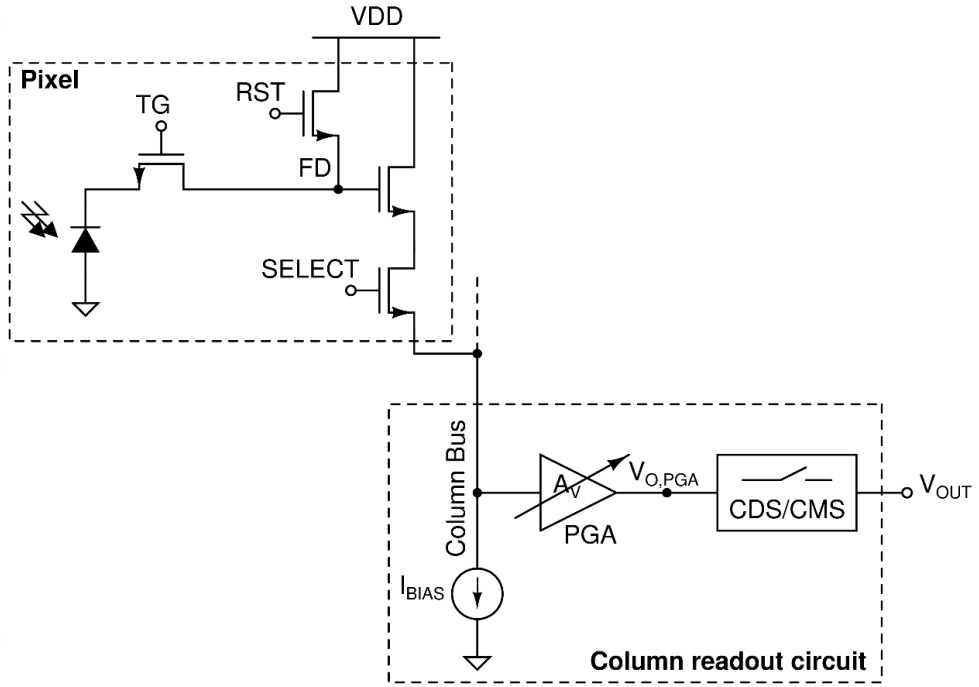
Technology & Temperature



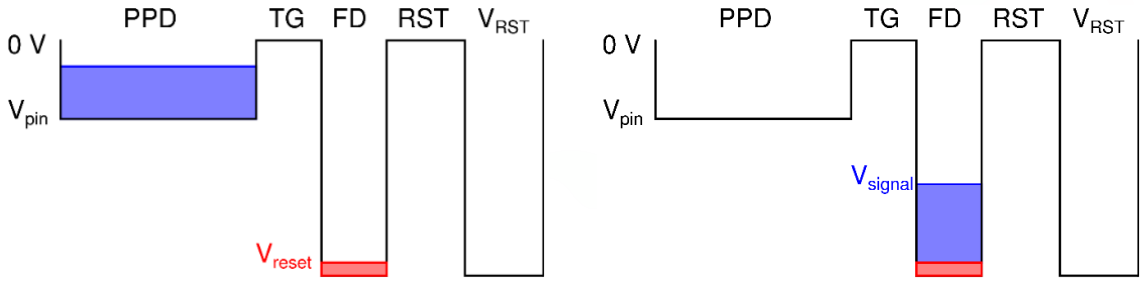
CMOS 4T pixel frontend readout circuitry

CDS – Correlated Double Sampling
CMS – Correlated Multiple Sampling
MCS – Multiple Correlated Sampling
FD – Floating Diffusion

Correlated Double Sampling (CDS)

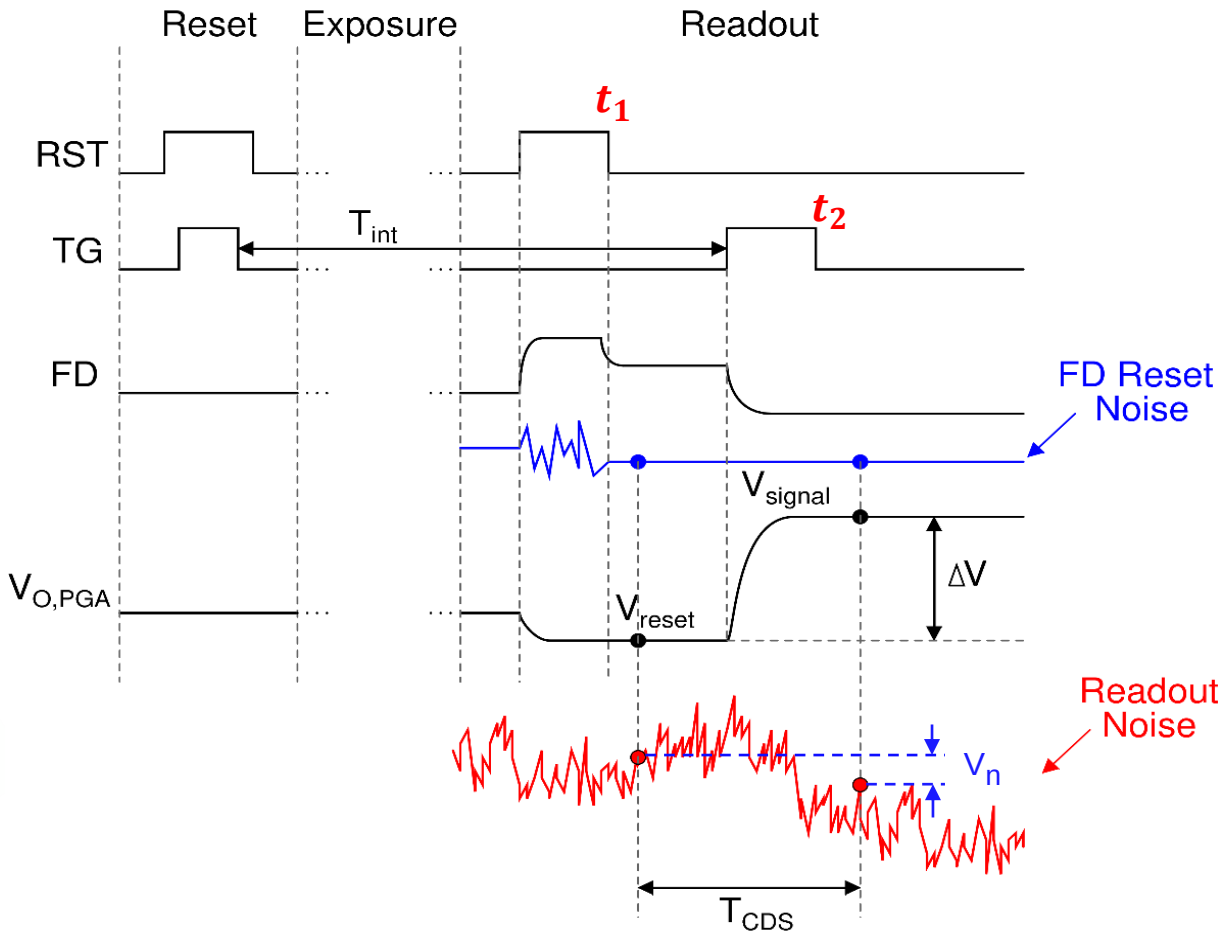


Conventional CMOS pixel and readout architecture



(a) Integration and FD node reset (t_1) *(b) Photocharge transfer (t_2)*

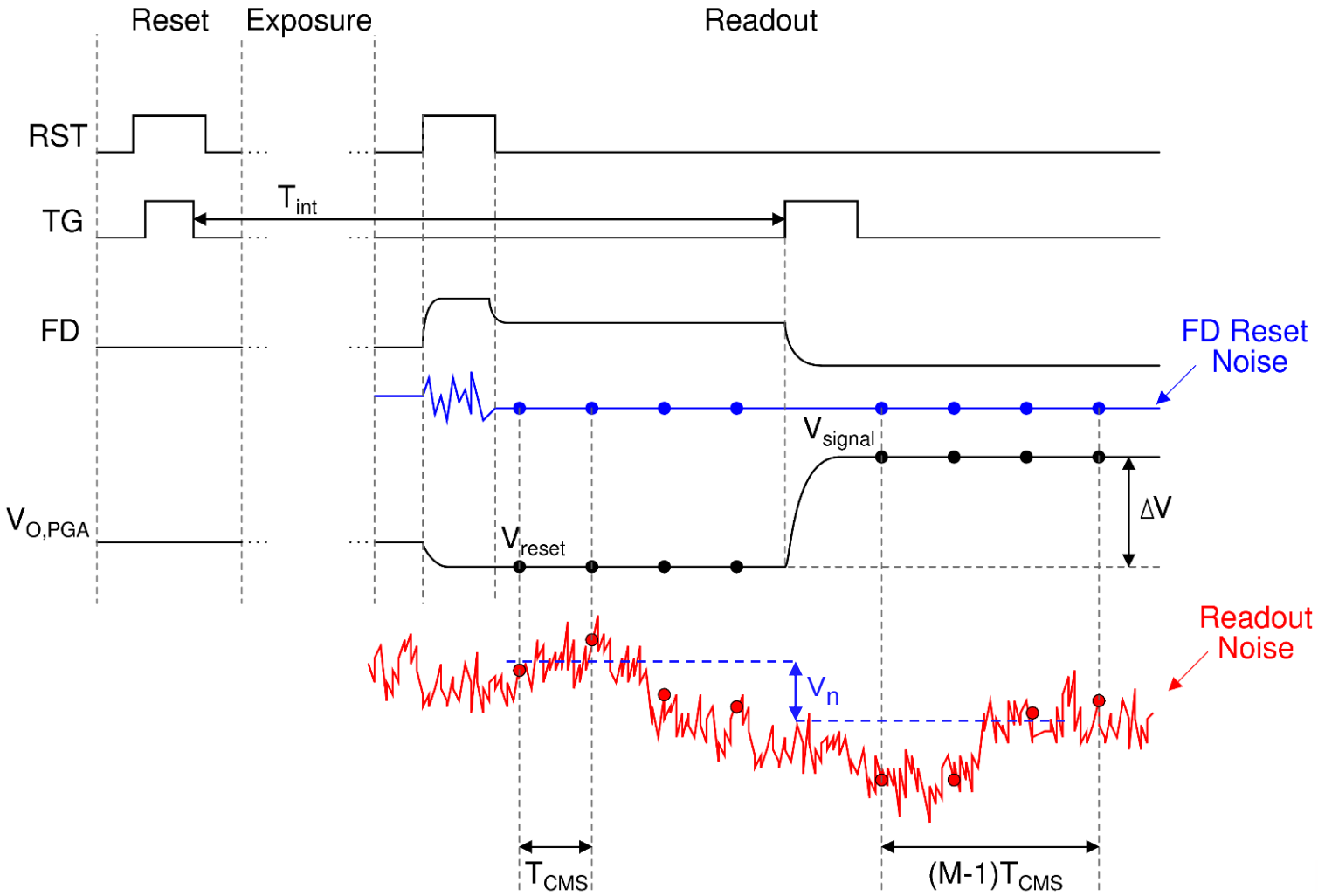
Potential diagram during CMOS pixel photo-charge readout



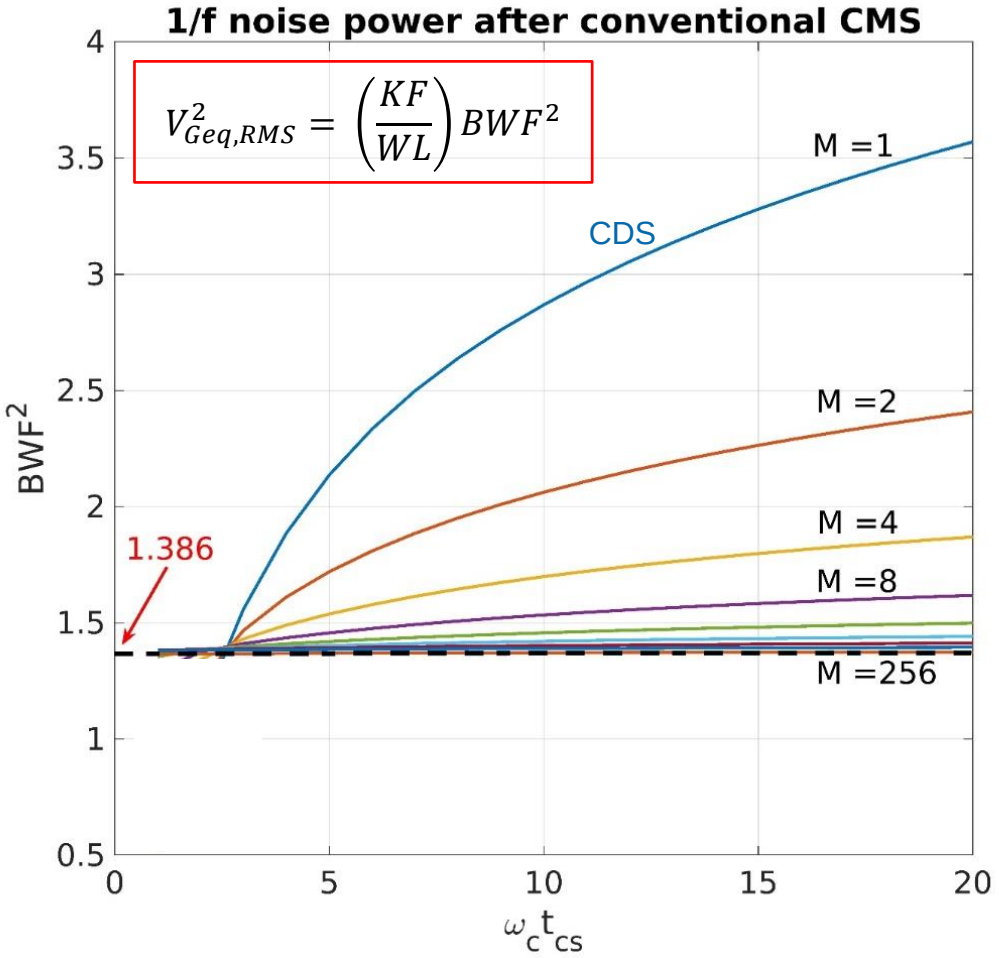
Timing diagram for CMOS pixel CDS readout [11]

FD – Floating Diffusion
PGA – Programmable Gain Amplifier
CDS – Correlated Double Sampling
CMS – Correlated Multiple Sampling

Correlated Multiple Sampling (CMS)



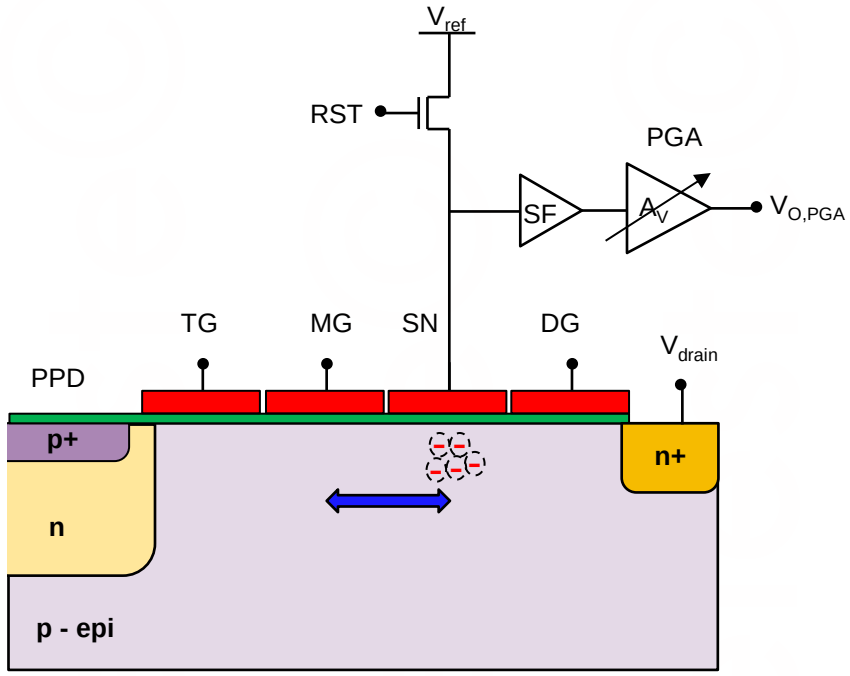
Timing diagram for CMOS pixel CMS readout [11]



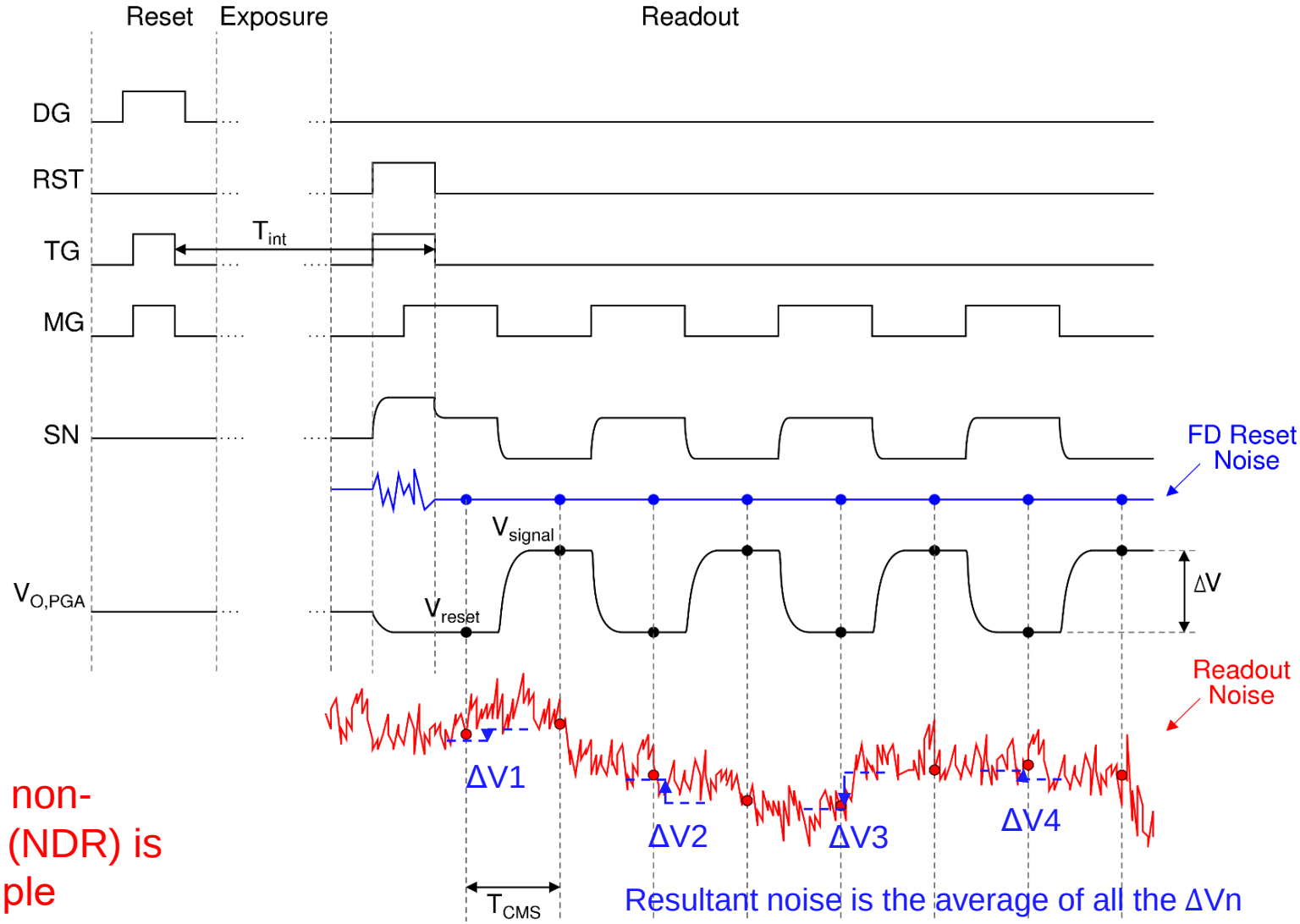
Normalized flicker noise power after CMS [12]

BWF – Bandwidth Factor
ω_c – Cutoff frequency
t_{cs} – Sampling time period (T_{CMS})

Non-Destructive Readout / Multiple Correlated Sampling



CCD inspired CMOS skipper pixel [8]



Timing diagram for CMOS skipper pixel non-destructive readout

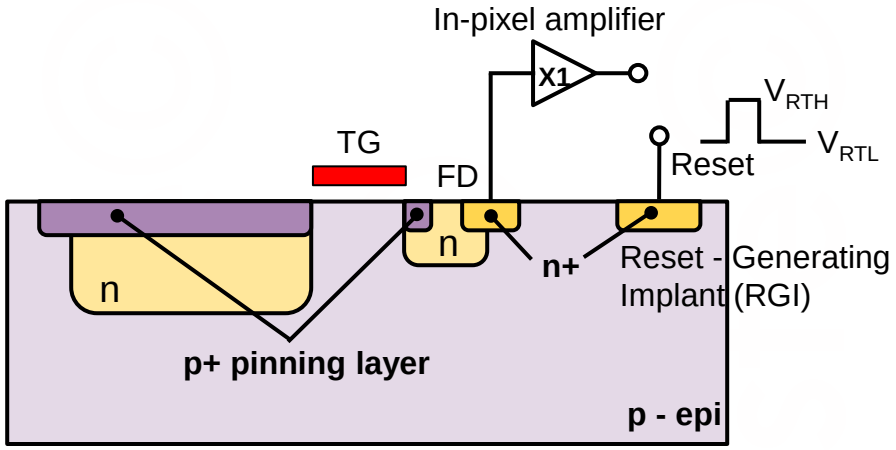
PPD – Pinned Photo Diode
CCD – Charge Coupled Device
TG – Transfer Gate
MG – Modulation Gate
SN – Sense Node
DG – Drain Gate
RST – Reset Gate
SF – Source Follower
PGA – Programmable Gain Amplifier

NOTE: This form of non-destructive readout (NDR) is referred to as “Multiple Correlated Sampling” (MCS) in further slides

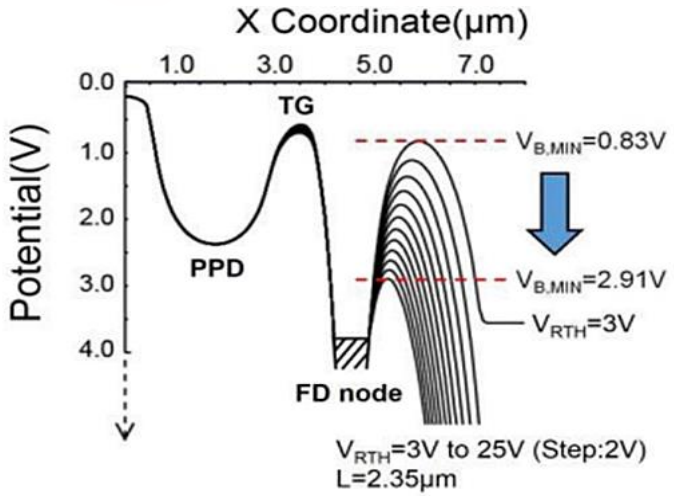
Literature Survey

Reset Gate less CIS (0.27 e^-_{RMS})

Shizuoka University, Japan, 2015



Pixel device structure [2]



Potential profile during punch-through reset [2]

Optimization area	Technique used	Impact
Technology	110 nm CIS with PPD	
C_{FD} reduction	Reset generating implant	CVF: 220 μV/e^-
Temperature	-10 °C	Low I_{dark}
Transistor selection	N.A.	
Column readout circuit	CMS	Low read noise

Pros:

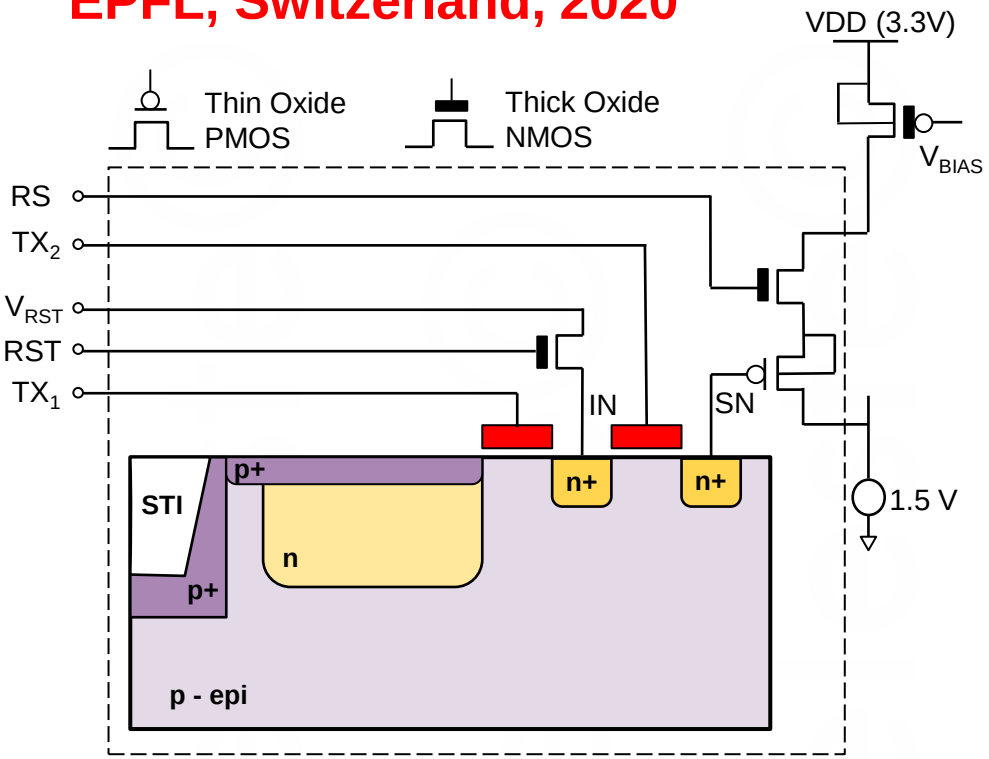
- Reduced coupling capacitance at FD node (High CVF)

Cons:

- High voltage (25 V) required for reset
- Possibility of image lag due to p+ implant near to FD n implant
- Slow reset operation
- Low pixel fill factor

5T adjustable gain CIS (0.32 e^-_{RMS})

EPFL, Switzerland, 2020



Pixel device structure and schematic [3]

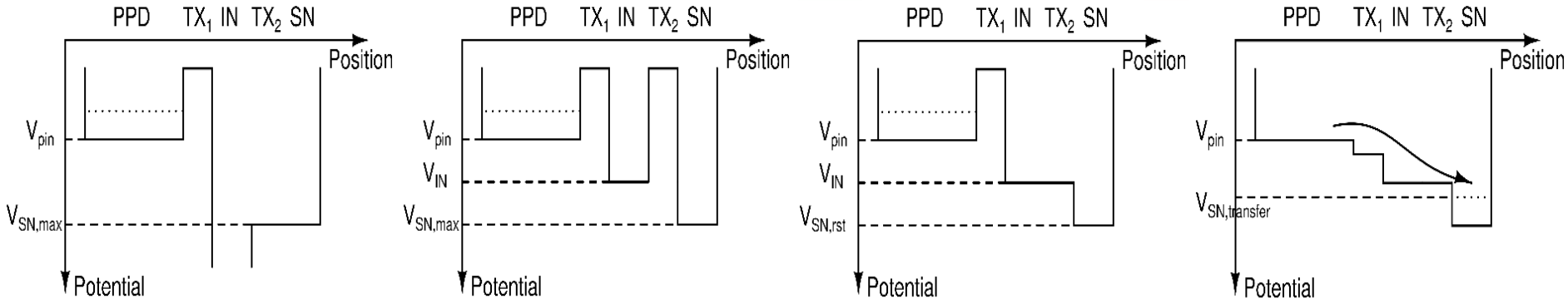
Optimization area	Technique used	Impact
Technology	180 nm CIS with PPD	
C_{FD} reduction	Reset with additional TX_2	CVF: 250 µV/e^-
Temperature	27 °C	
Transistor selection	Thin oxide PMOS as SF	Cap: 0.4 fF
Column readout circuit	CMS (Digital,4)	Low read noise

Pros:

- Reduced coupling capacitance at FD node (High CVF)

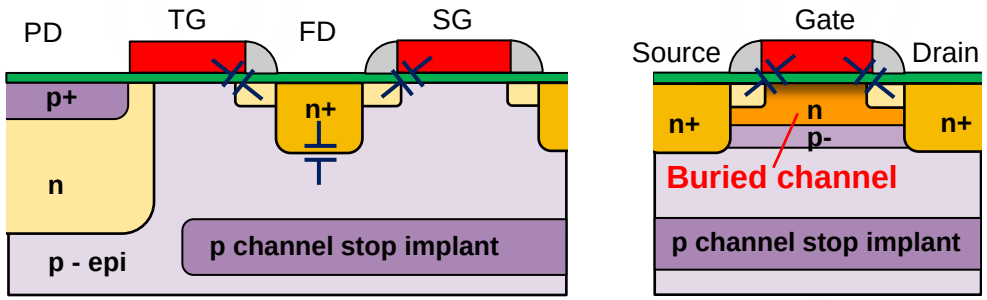
Cons:

- Prone to image lag due to intermediate potentials
- Low fill factor (PMOS inside pixel)

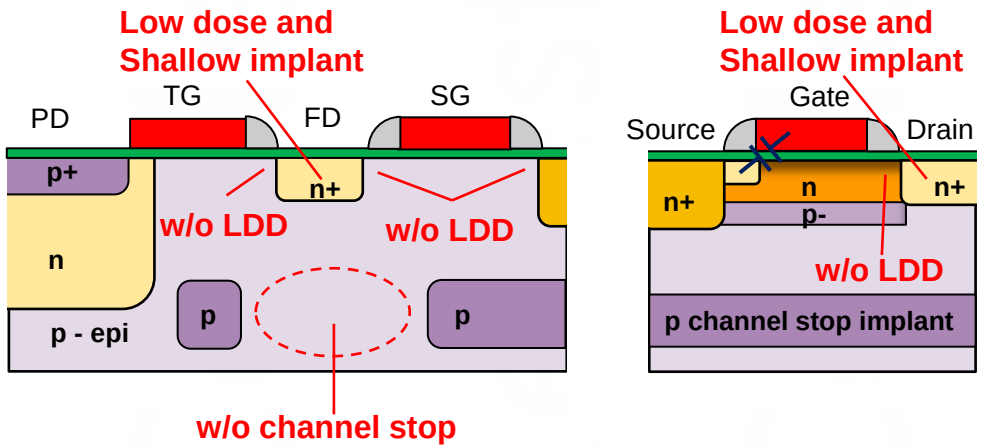


Potential profile during charge transfer [3]

A linear response CIS (0.46 e^-_{rms})
Tohoku University, Japan, 2015



Conventional PPD and SF cross-section [4]



Optimized PPD and SF cross-section [4]

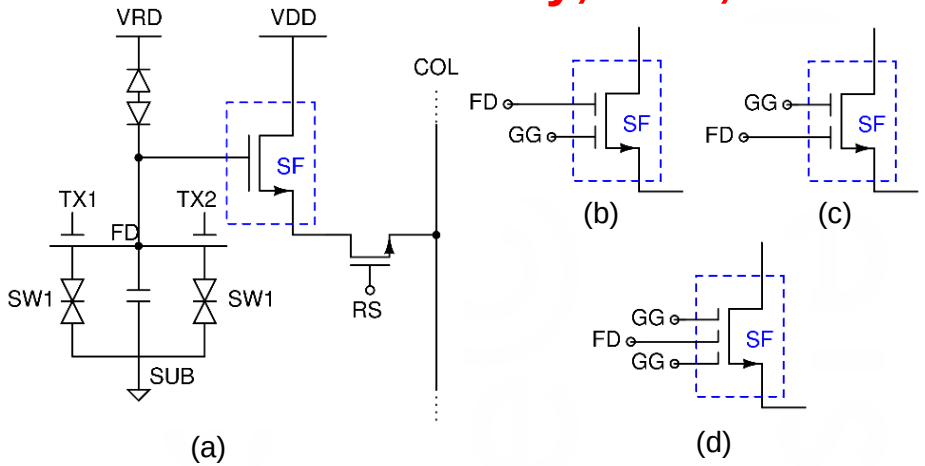
Optimization area	Technique used	Impact
Technology	180 nm CIS with PPD	
C_{FD} reduction	Low implant dose & shallow FD w/o LDD	CVF: 232 µV/e^-
Temperature	27 °C	
Transistor selection	Buried channel NMOS as SF	Low 1/f noise
Column readout circuit	Floating capacitor load	Low read noise

Pros:
- Overall reduction in FD node capacitance
- Lower flicker noise due to buried channel NMOS as SF
- Low noise due to switched capacitor load at SF output

Cons:
- Possibility of image lag due to removed LDD
- Prone to FD leakage due to removed channel stop beneath
- Settling error due to sampling time jitter

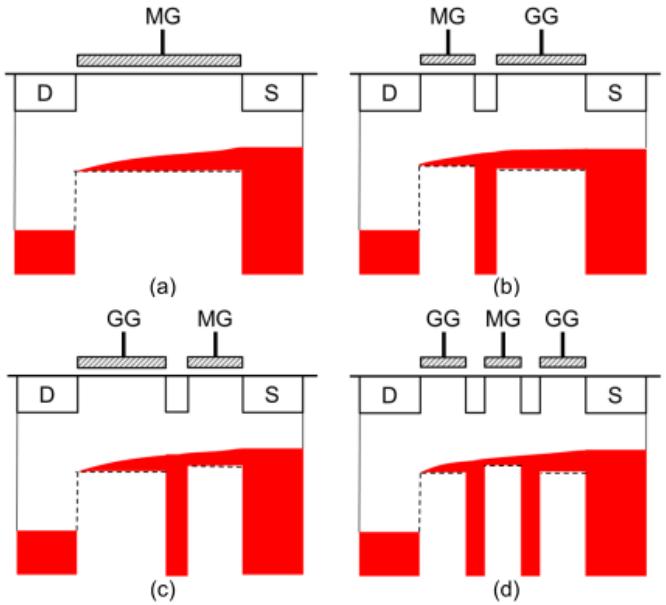
Multi-Gate Source Follower QIS (0.17 e^-_{rms})

Dartmouth University, USA, 2022



Pixel schematic and multi-gate nmos SF variants [6]

Optimization area	Technique used	Impact
Technology	45/65 nm stacked BSI CIS	
C_{FD} reduction	Small Modulation Gate (MG)	CVF: 700 µV/e^-
Temperature	-	
Transistor selection	Buried channel devices	Low 1/f noise
Column readout circuit	CDS + Amplification	Low read noise

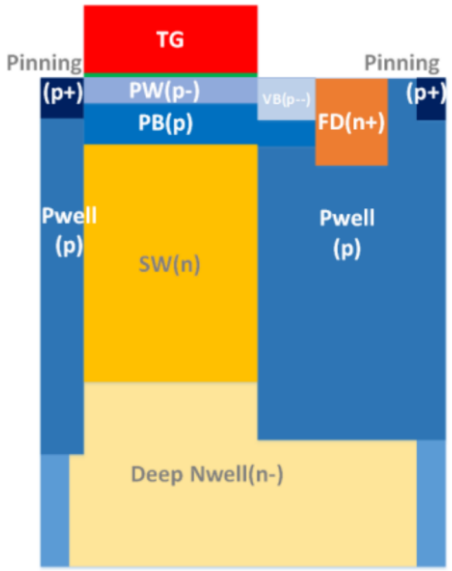


SF operational potential diagram [6]

High CVF
Lower C_{FD}
Lower W*L

vs

Low 1/f noise
High W*L



Jot device structure [13]

Results based on TCAD simulations and spectrum analyzer data.

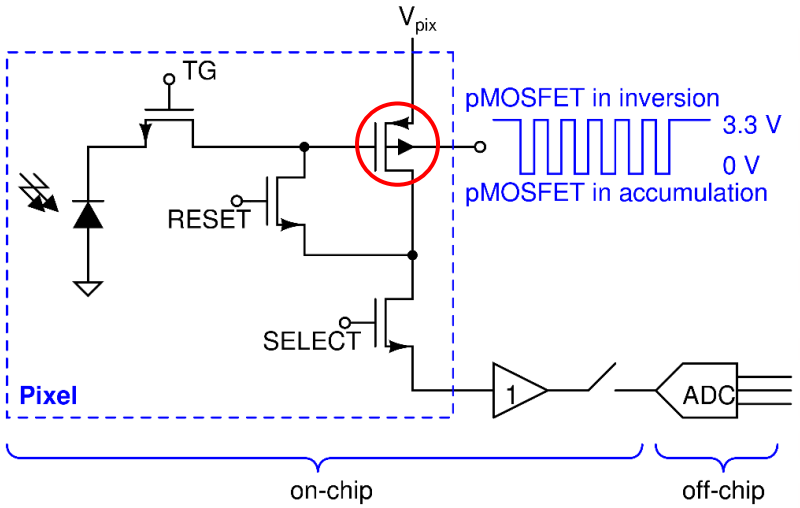
Pixel characterization is needed !

Research Questions:

1. Physics behind obtained results?
2. Optimum integrate gap size?
3. Optimum value of GG bias?

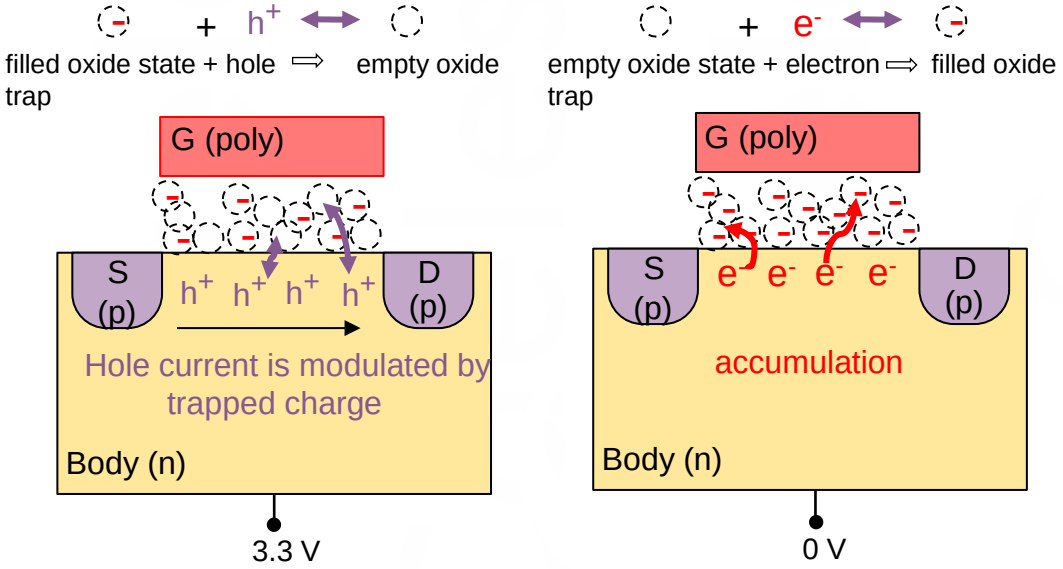
Inversion-Accumulation cycling CIS (0.34 e^-_{RMS})

Caeleste, Belgium, 2015



Pixel schematic [7]

Optimization area	Technique used	Impact
Technology	180 nm CIS with PPD	
C_{FD} reduction	-	
Temperature	- 40 °C	Low I_{dark}
Transistor selection	PMOS as CS amplifier	Low 1/f noise
Readout circuit	CTIA while modulating inversion-accumulation	CVF: 400 µV/e^-



Inversion-Accumulation cycling [7]

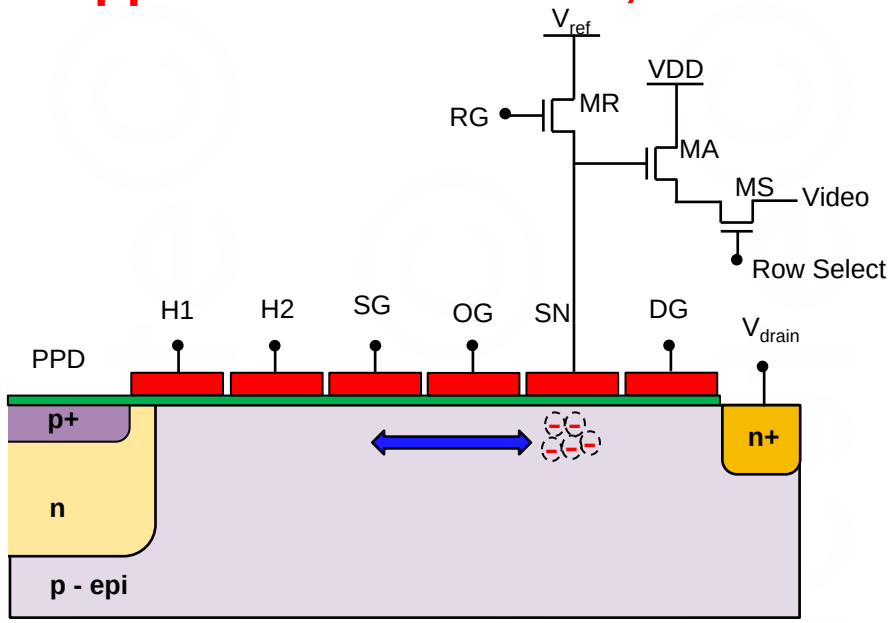
Pros:

- Flicker noise reduction with inversion-accumulation cycling
- High CVF due to CTIA gain

Cons:

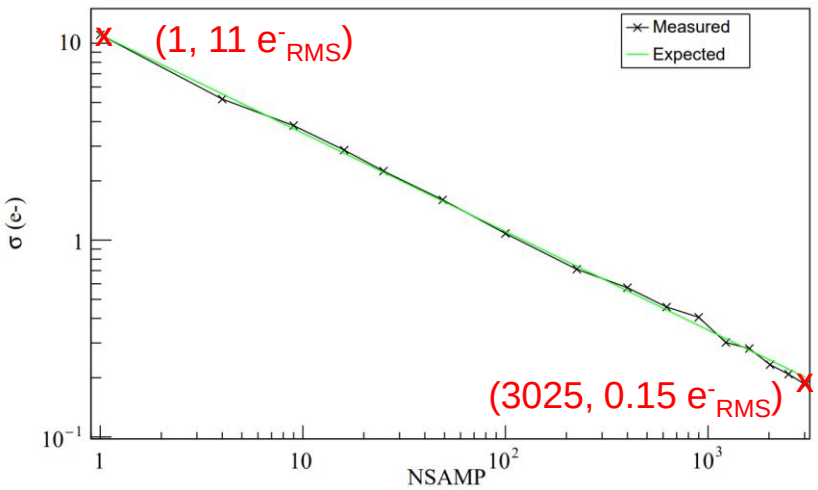
- Very high number of samples required (Low FPS)
- Cooling is needed to lower the dark current
- Low pixel fill factor (PMOS inside pixel)

Skipper in CCD - CMOS CEI, Open University, UK 2020
Skipper in CCD - CMOS ,NU South CONICET, Argentina, 2024



Pixel device structure and schematic [8]

Optimization area	Technique used	Impact
Technology	CIS with CCD	Skipper CCD
C_{FD} reduction	-	
Temperature	-155 °C	Low I_{dark}
Transistor selection	NMOS	High SF Gain
Column readout circuit	NDR + MCS	Low noise

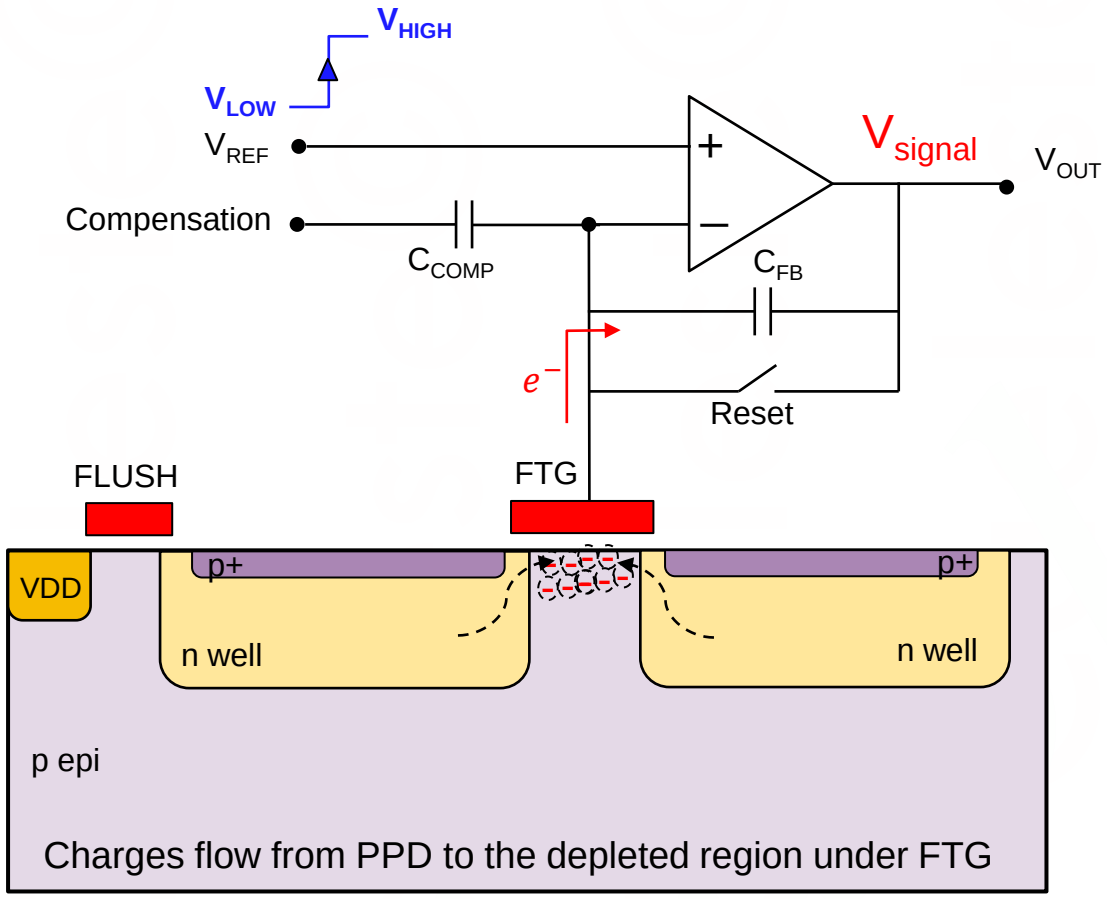


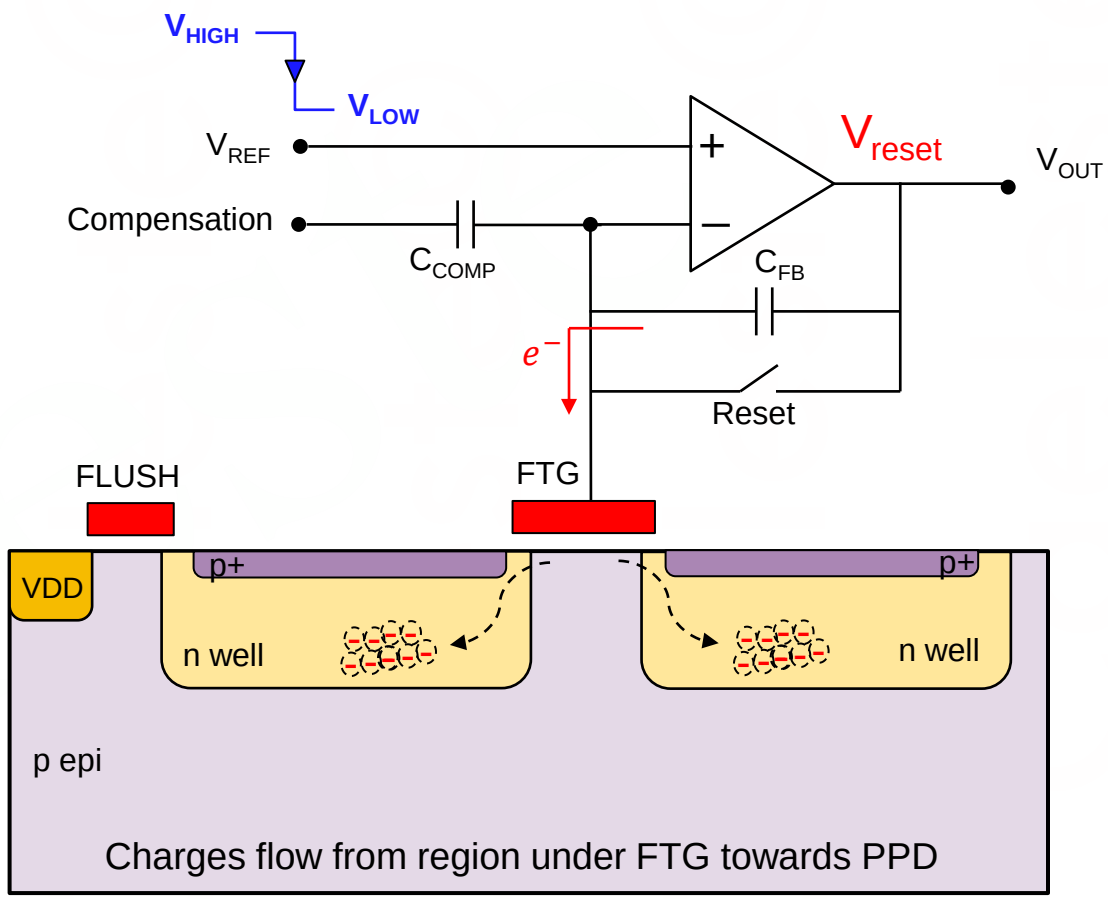
Pros:
- CCD originating non-destructive readout in CMOS
- Readout noise can be reduced to very low levels with multiple correlated samples

Cons:
- Low fill factor due to multiple poly-silicon gates
- Very high number of samples to reach desired noise level (Low FPS)
- Cooling is required to lower the dark current

Floating Transfer Gate CIS
Caeleste, Belgium, 2024

Patent pending





- Compensation capacitor and voltage is required to compensate the crosstalk of CTIA output and reference input during modulation

Overview table

Reference	[2] Shizuoka	[4] Tohoku	[7] Caeleste	[3] EPFL	[5] CEI	[6] Dartmouth	[8] CONICET	[Ongoing work] Caeleste
Year of publication	**2015**	**2015**	**2015**	**2020**	**2020**	**2022**	**2024**	**2024**
Noise (e^-_{rms})	0.27	0.46	0.34	0.32	NA	0.17	0.15	Not available yet
Pixel circuit topology	Reset gateless pixel with SF readout	SF readout	CTIA with modulated bulk	5T pixel with SF readout	CCD skipper with SF readout	Pixel shared FD with SF readout	CCD skipper with SF readout	Floating Transfer Gate (FTG) pixel
Circuit operation technique	High CG pixel	High CG pixel	Switched bulk biasing of in-pixel amplifier	High CG pixel	NDR (MCS)	Multi-gate SF with high CG pixel	NDR (MCS)	NDR (MSC)
Device / technology optimizations	Reduction in C_{FD} capacitance	Low doping, Shallow FD junction	Standard CIS	Additional TX gate for the reset	CCD skipper in CMOS	Low FD Capacitance, and SF modification	CCD skipper in CMOS	Floating TG island in PPD
technology	Low V_{th} NMOS	Buried channel NMOS	PMOS as CS amplifier	Thin oxide PMOS	CCD-CMOS	Buried channel NMOS	CCD-CMOS	4T CIS
Oversampling	N.A.	N.A.	1600 (CMS)	4 (CMS)	34 (MCS)	N.A.	3025 (MCS)	MCS

References

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[3] A. Boukhayma, A. Caizzone and C. Enz, "A CMOS Image Sensor Pixel Combining Deep Sub-Electron Noise with Wide Dynamic Range," IEEE Electron Device Letters, June 2020, vol. 41, no. 6, pp. 880-883, doi: 10.1109/LED.2020.2988378

[4] S. Wakashima, F. Kusuhara, R. Kuroda, and S. Sugawa, "A linear response single exposure CMOS image sensor with 0.5 e- readout noise and 76 ke- full well capacity," Symposium on VLSI Circuits (VLSI Circuits), 2015, Kyoto, Japan, pp. C88-C89, doi: 10.1109/VLSIC.2015.7231334.

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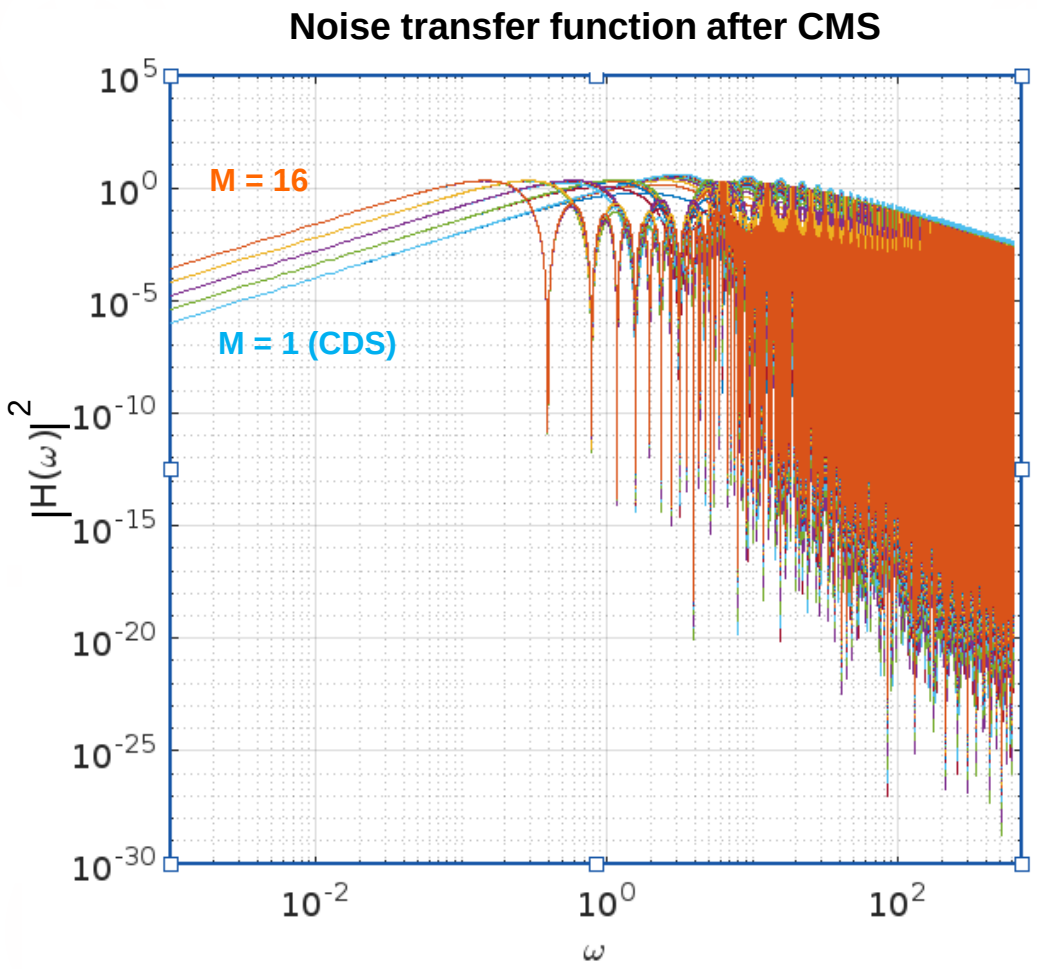
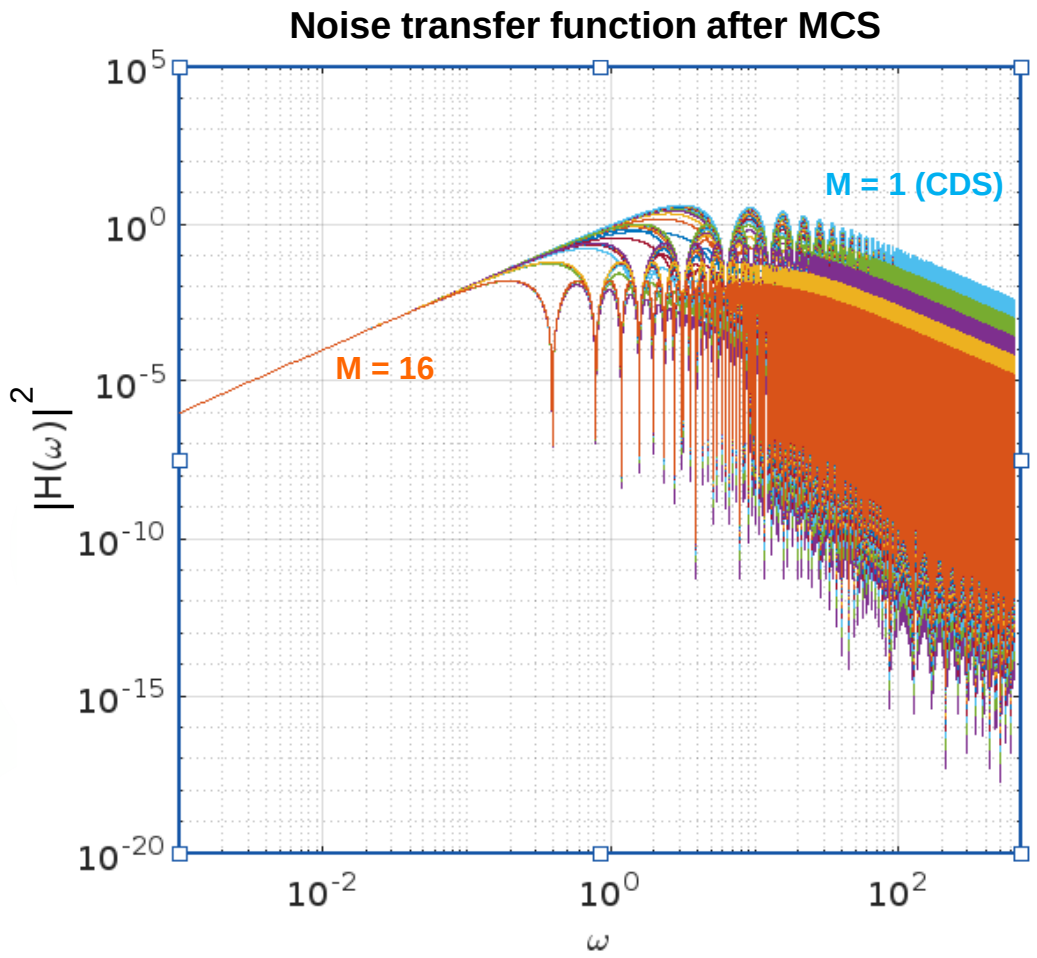
caeleste

Thank you for your attention !

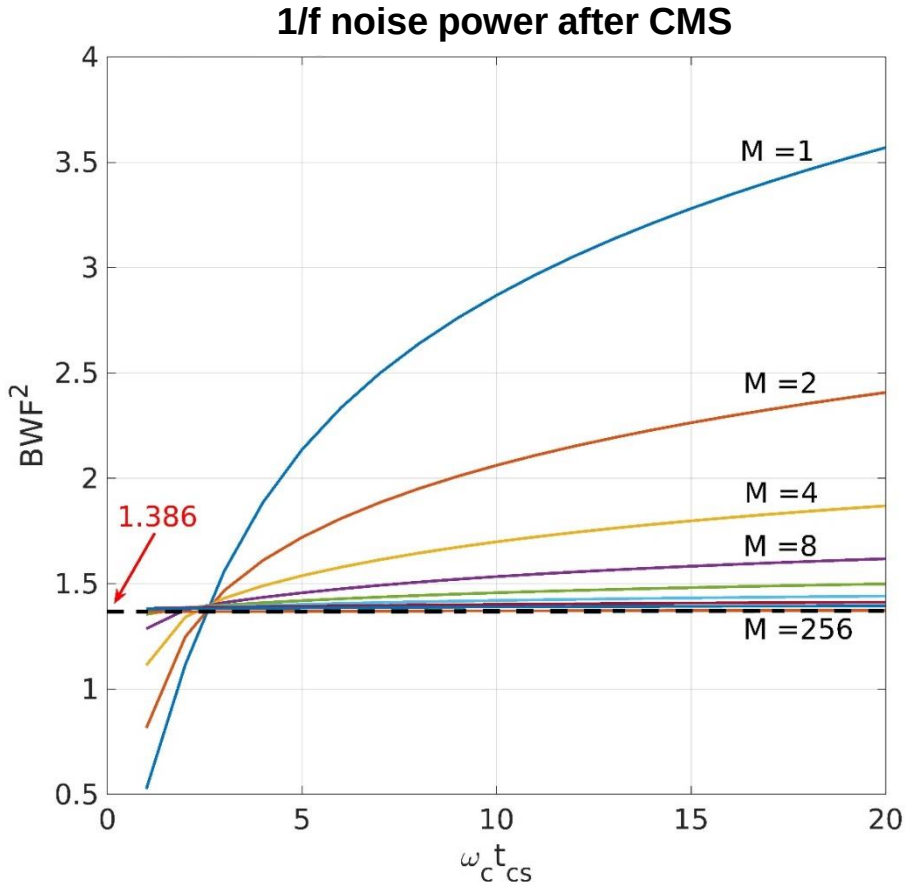
Comparison of NTF after CMS and MCS

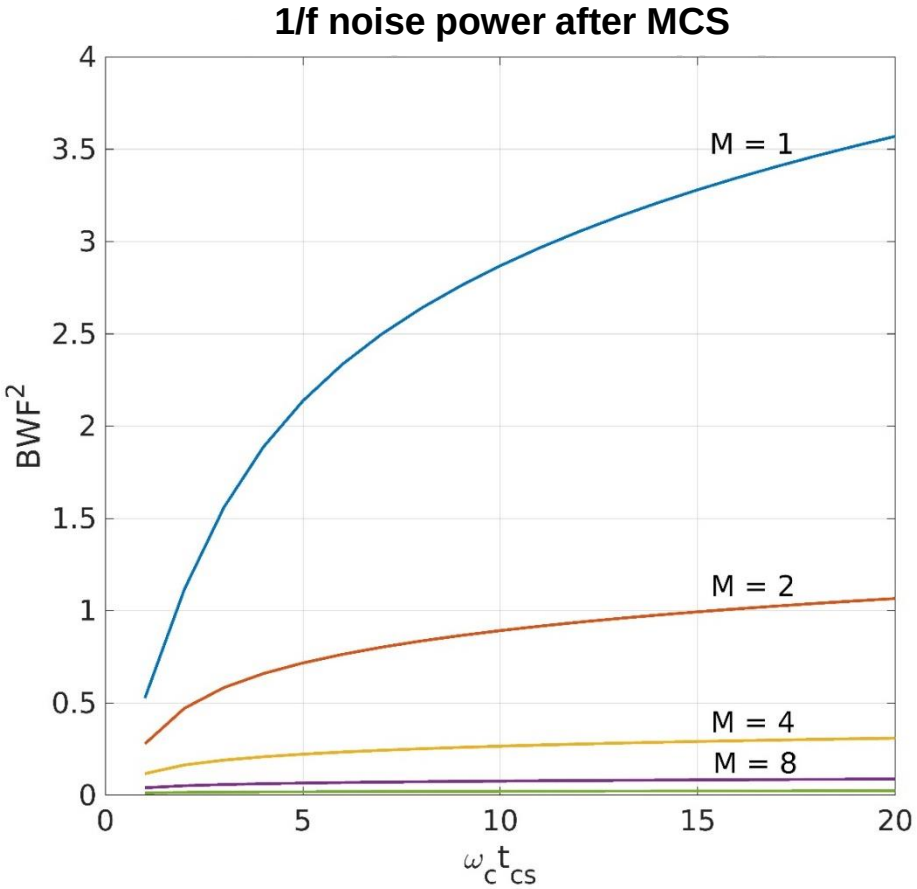




- With increase in number of samples, in CMS, correlation between reset and signal samples reduces as time gap increases, and hence flicker noise doesn't reduce further and saturates at a level.

Comparison of flicker noise power after CMS and MCS





- For settling of voltage signal with accuracy of 99%, $\omega_c t_{cs}$ must be higher than 4.6.
- Two samples in MCS are more effective than infinite samples in CMS.