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A prototype pixel readout chip with column-level ADC for high frame rate XFEL applications

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X-ray free electron laser (XFEL) facilities can delivery femtosecond X-ray pulses with ultra-high peak brightness, which in turn calls for high performance integrating type pixel detectors. State-of-the-art pixel read chips for detectors commissioning at XFEL facilities usually employ amplifiers with multi-gain stages within the pixel to reach high dynamic range, typically from 1 to 10^4 photons per pixel per X-ray pulse. However, the pixel readout chips of these detectors mostly adopt direct analog signal readout, limiting their frame rate to 100 −1kHz [1,2]. Such performance is no longer in line with the evolvement of XFELs towards high repetition rate beyond 10kHz. This work proposes a pixel readout ASIC (Application Specific Integrated Circuit) chip with digital readout architecture for applications at next generation high repetition rate XFELs. Instead of multiplexing the analog signals from the pixel matrix to a few output ports like conventional XFEL detectors, the proposed chip incorporates a low power, small area ADC (analog-to-digital converter) at each column end to digitize the pixel analog signal transmitted sequentially from the column. Further on-chip data processing in the digital domain can be more robust and versatile than in the analog domain. Modern high speed serial interface can be used to transmit the digital stream off chip with high throughput, enabling a significant increase in frame rate as compared to the analog readout scheme.

A small-scale prototype chip with a pixel array of 16 × 16 was designed and fabricated in a 130 nm CMOS process. The goal is to demonstrate the proposed chip architecture for high dynamic and high frame rate X-ray imaging at XFELs. The pixel size is 150 μm × 150 μm. The dynamic-gain-switching amplifier like the AGIPD and JUNGFRAU pixel readout ASIC chips is implemented to achieve a high dynamic range required by XFEL applications. The pixel array is read out row by row. Each column is terminated by an 11-bit SAR ADC working at the nominal speed of 2MS/s. The digital signals are further readout by a serial chip interface. First tests show full chip functionality and the analog front-end can accommodate an equivalent input signal up to 10^4 12keV photons. The measurement of individual ADC channels and calibration of the full readout chain are ongoing. In the conference, the design and measurement results of the prototype chip will be presented.

[1] A. Allahgholi, et al., The Adaptive Gain Integrating Pixel Detector at the European XFEL, Journal of Synchrotron Radiation 26 (2019) 74
[2] A. Mozzanica, et al., JUNGFRAU Detector for Applications at Synchrotron Light Sources and XFELs, Synchrotron Radiation News 31 (2018) 16

Auteurs principaux: M. LU, Shijie (Shanghai Institute of Microsystem and Information Technology); WANG, Tianyang (Zhangjiang Laboratory)

Co-auteurs: Dr GAN, Fuwan (Shanghai Institute of Microsystem and Information Technology); M. SUN, Tao (Shanghai Institute of Microsystem and Information Technology); Dr SHENG, Zhen (Shanghai Institute of Microsystem and Information Technology); Prof. LIU, Zhi (ShanghaiTech University); M. JI, Zizhao (Shanghai Institute of Microsystem and Information Technology)

Orateur: M. LU, Shijie (Shanghai Institute of Microsystem and Information Technology)

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