A prototype pixel readout chip with column-level ADC for high frame rate XFEL applications

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Introduction

As compared to the previous generation of synchrotron light sources, the new generation of X-ray free electron laser (XFEL) facilities can delivery femtosecond X-ray pulses with ultra-high peak brightness, which in turn calls for high performance integrating type pixel detectors with high dynamic range, high frame rate, low noise.

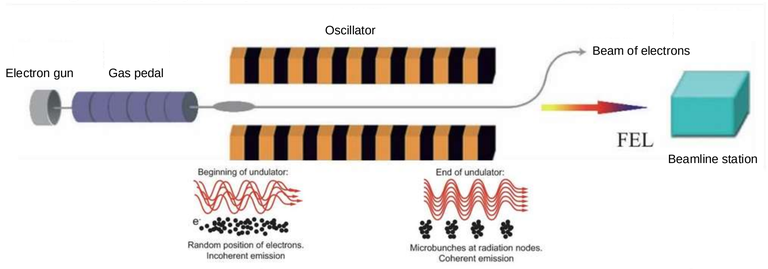

Figure 1 XFEL structure

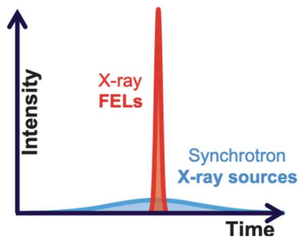

Figure 2 Energy intensity of XFEL and synchrotron radiation

This work presents a high dynamic and high frame rate pixel readout ASIC (Application Specific Integrated Circuit) prototype chip of 16 × 16 pixel array with digital readout architecture working at 10kHz frame rate for applications at next generation XFELs. This chip was designed and fabricated in a 130 nm CMOS process to validate the functionality. The pixel size is 150 μm × 150 μm.

Chip overview

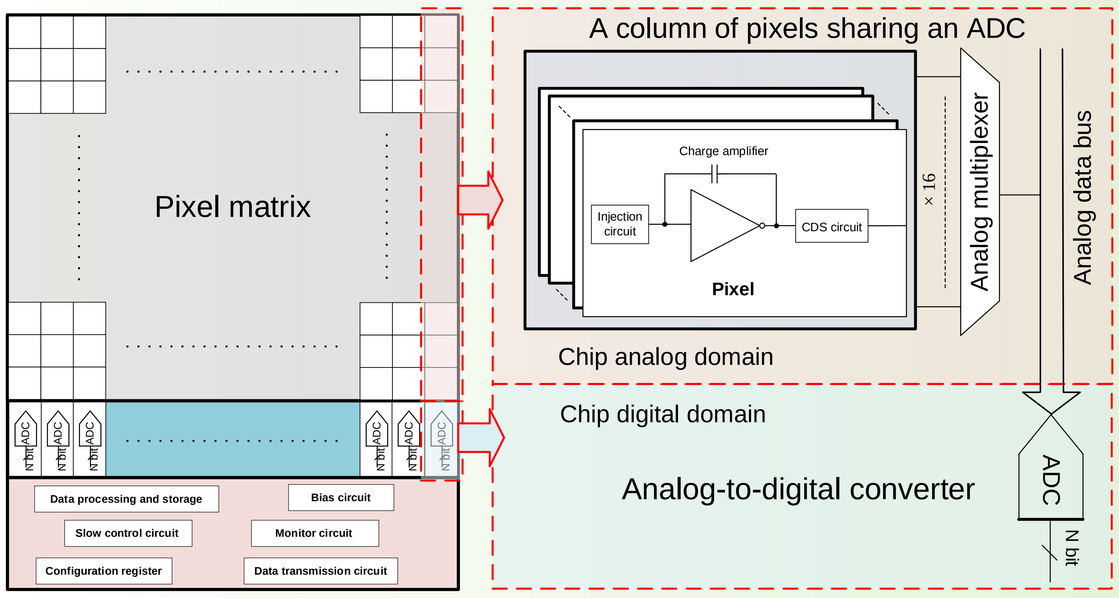

Figure 3 small-scale prototype chip structure

Instead of multiplexing the analog signals from the pixel matrix to a few output ports like conventional XFEL detectors[1,2], the presented chip incorporates a low power, small area 11-bit SAR-ADC (analog-to-digital converter) at each column end to digitize the pixel analog signal transmitted sequentially from the column. These ADCs operate at the speed of 1MSps, each sampling and digitizing a column of 16 pixels row by row.

Design details

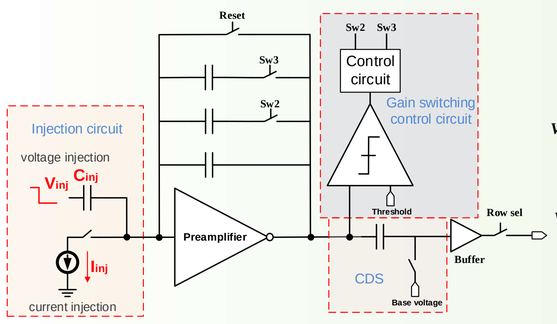

Figure 4 readout circuit of each pixel

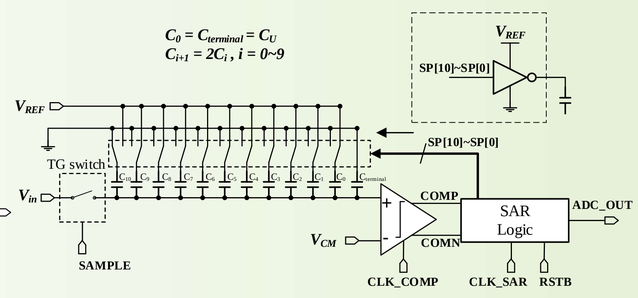

Figure 5 Column level SAR-ADC circuit[3]

- The charge sensitive amplifier (CSA) with dynamic-gain-switching [1,2] is implemented in each pixel to achieve a high dynamic range
- Correlated double sampling (CDS) after CSA to reduce the reset noise and low frequency noise at the first gain stage
- The 11-bit SAR-ADC at the end of each pixel column is designed to ensure sufficient resolution over the entire dynamic range [3]
- Each pixel is equipped with two injection circuits that can generate electrical stimulus to emulate the photon signals(See Figure 4)
  - Voltage injection: Inject an adjustable voltage step through a capacitor into the pixel input node, generating a total amount of charge equal to $V_{inj} \times C_{inj}$. The maximum injection voltage is equal to the supply voltage of 1.2 V, which is equivalent to ~ 243 photons @12keV
  - Current injection: Use a controlled current source to inject current pulses into the pixel input node, generating a total amount of charge equal to $I_{inj} \times T_{inj}$, which can cover the full dynamic range of the pixel

Measurement Object & Operating Timeline

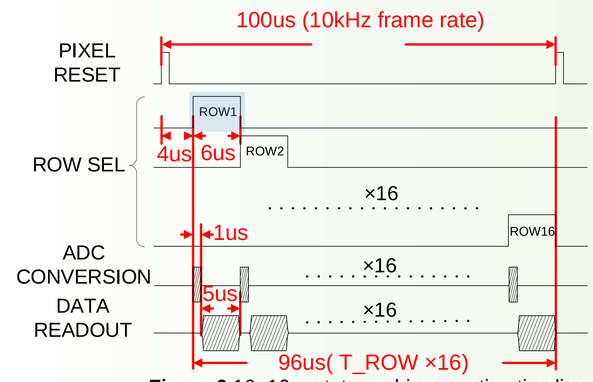

Figure 6 16×16 prototype chip operating timeline

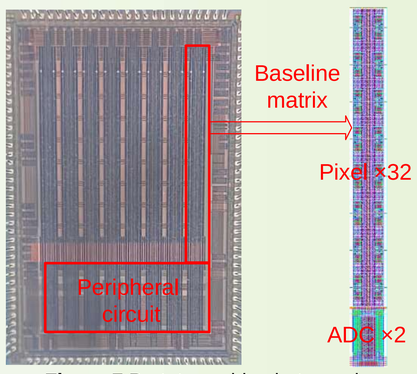

Figure 7 Prototype chip photograph

- This prototype chip has 8 different pixel designs
- The baseline pixel design as shown in Figure 4 is discussed in this poster, which occupies the last two column of the matrix (see Figure 7)

Test results : Transfer Curve of an example pixel

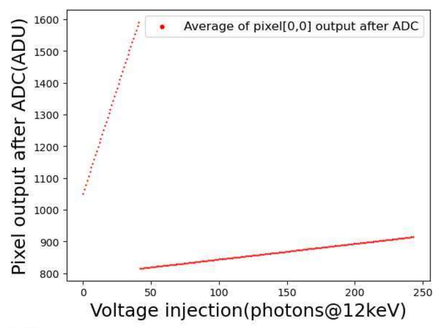

Figure 8 Transfer curve of photons and pixel output after ADC

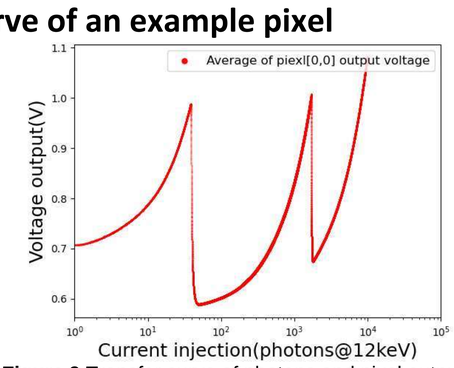

Figure 9 Transfer curve of photons and pixel output voltage

- Both voltage (Figure 8) and current injection (Figure 9) were used to test the pixels
- Full dynamic range of ~10^4 photons @12keV verified by the current injection

Test results : Noise of an example pixel

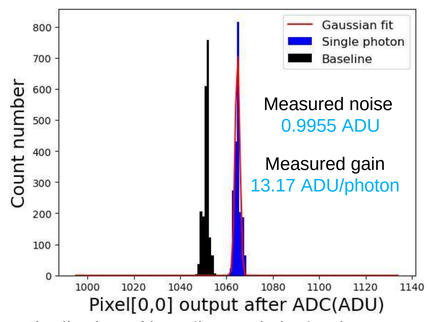

Figure 10 Distribution of baseline and single photon response

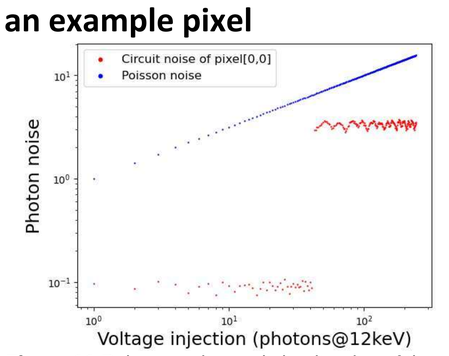

Figure 11 Poisson noise and circuit noise of the pixel

- Well separated single photon signal from the baseline (SNR >10)
- The circuit noise is below the Poisson noise

Test results : Gain & Noise Distribution of the baseline matrix

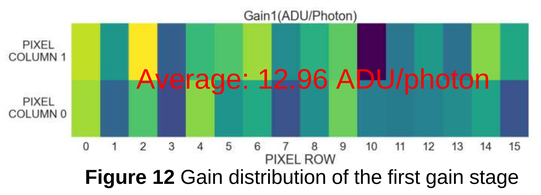

Figure 12 Gain distribution of the first gain stage

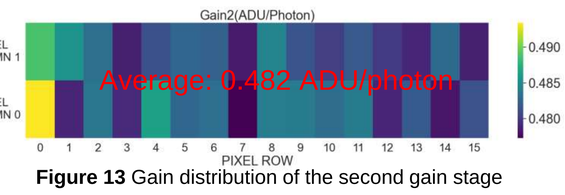

Figure 13 Gain distribution of the second gain stage

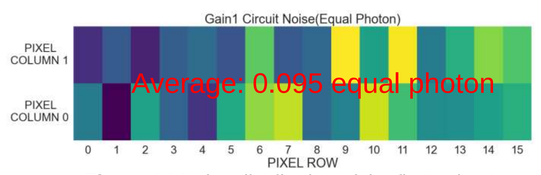

Figure 14 Noise distribution of the first gain stage

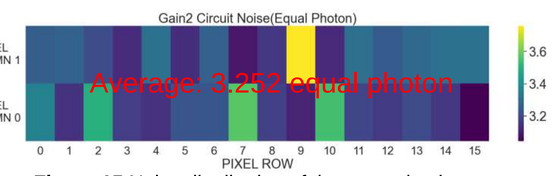

Figure 15 Noise distribution of the second gain stage

- Uniform performance over the measured sub-matrix
- The pixels in each column are sequentially read out row by row. In the first gain stage, the later a pixel is read out, the higher its noise level

Conclusion

- A small-scale prototype chip designed to verify a digital readout architecture with column level ADCs for X-ray detectors at future XFELs
- The baseline pixel design aims at detection of 12keV photons
  - Good single-photon resolution achieved @ 12keV with SNR > 10
  - Full dynamic range ~ 10^4 photons @12keV
- The envisaged full-size ASIC chips will extend the pixel array to 96 × 96 pixels
  - With the current ADC design working at 1MSps, a frame rate of > 10kHz can be achieved

References

[1] A. Allahgholi, et al., The Adaptive Gain Integrating Pixel Detector at the European XFEL, Journal of Syn chrotron Radiation 26 (2019) 74
[2] A. Mozzanica, et al., JUNGFRAU Detector for Applications at Synchrotron Light Sources and XFELs, Syn chrotron Radiation News 31 (2018) 16
[3] Z. Ji, et al., An 11-bit SAR ADC for high frame rate and high-dynamic X-ray imaging at future XFELs, Journal of Instrumentation 19 (2024) 07