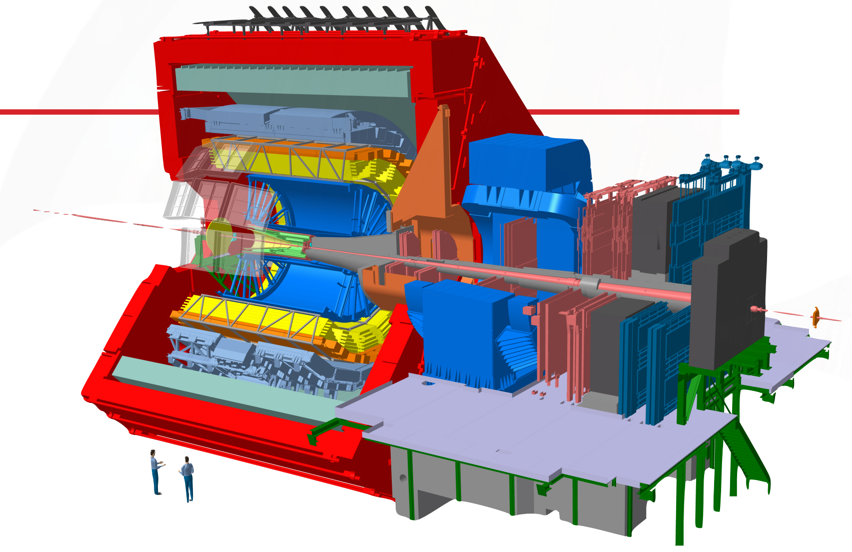
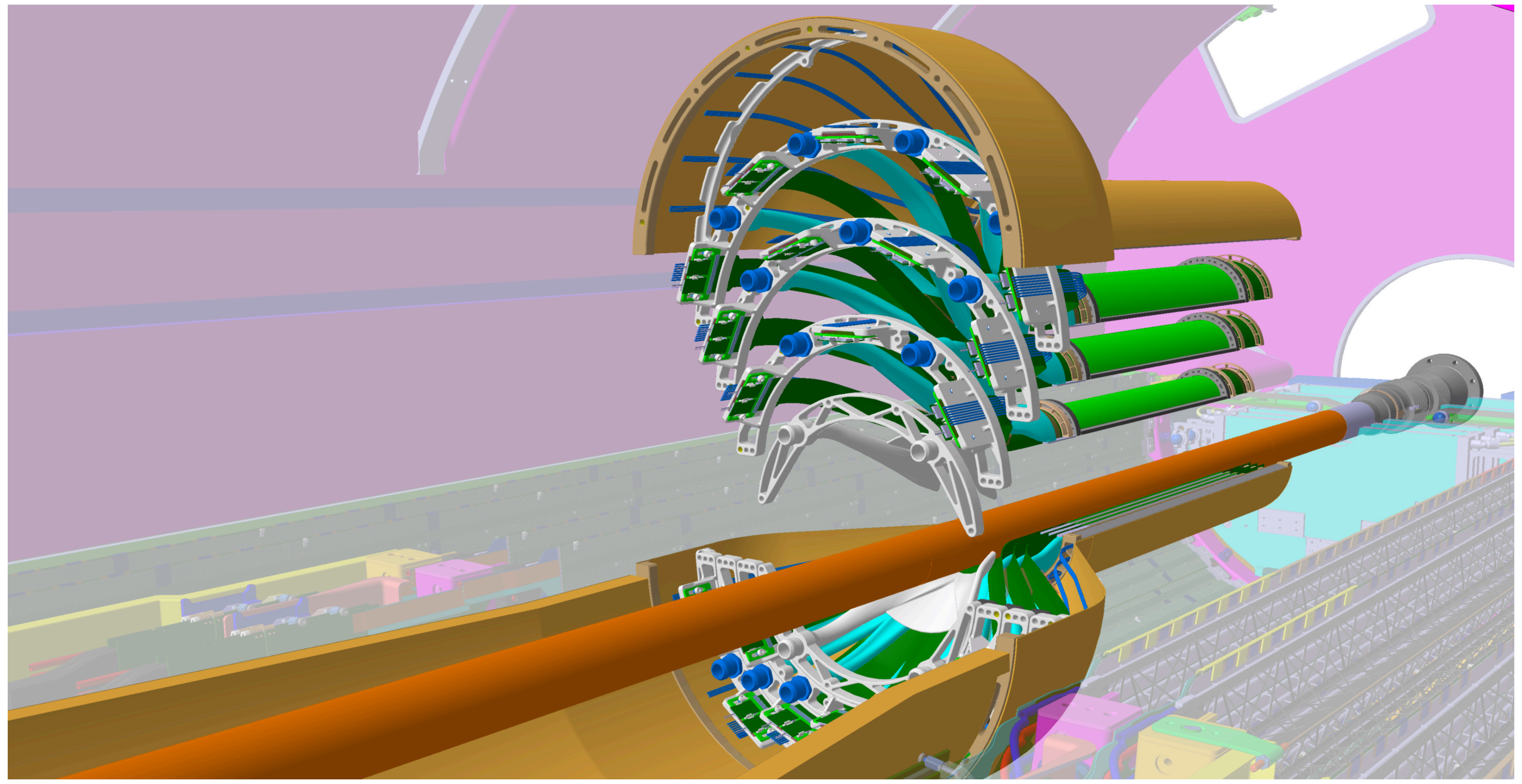
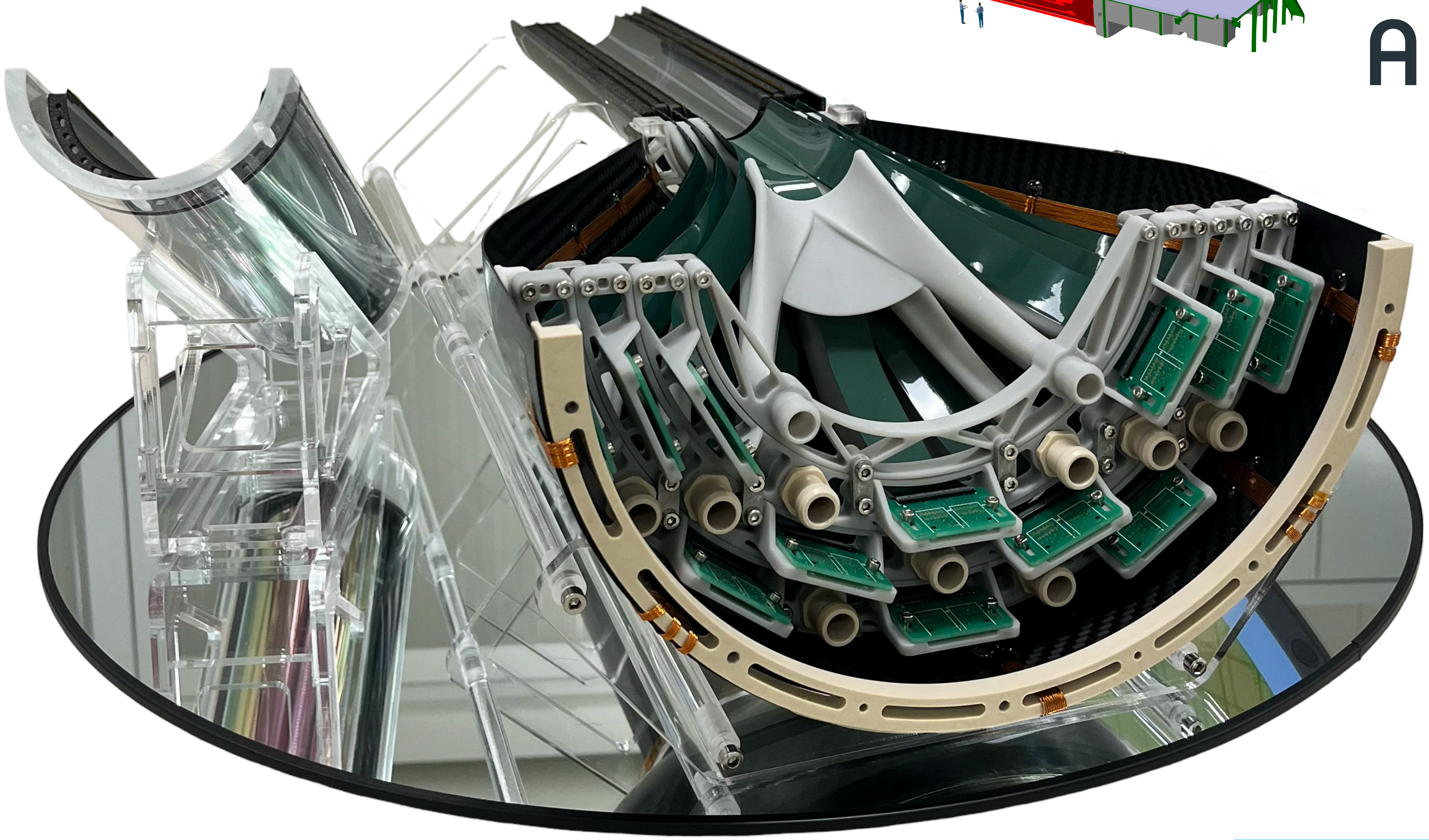


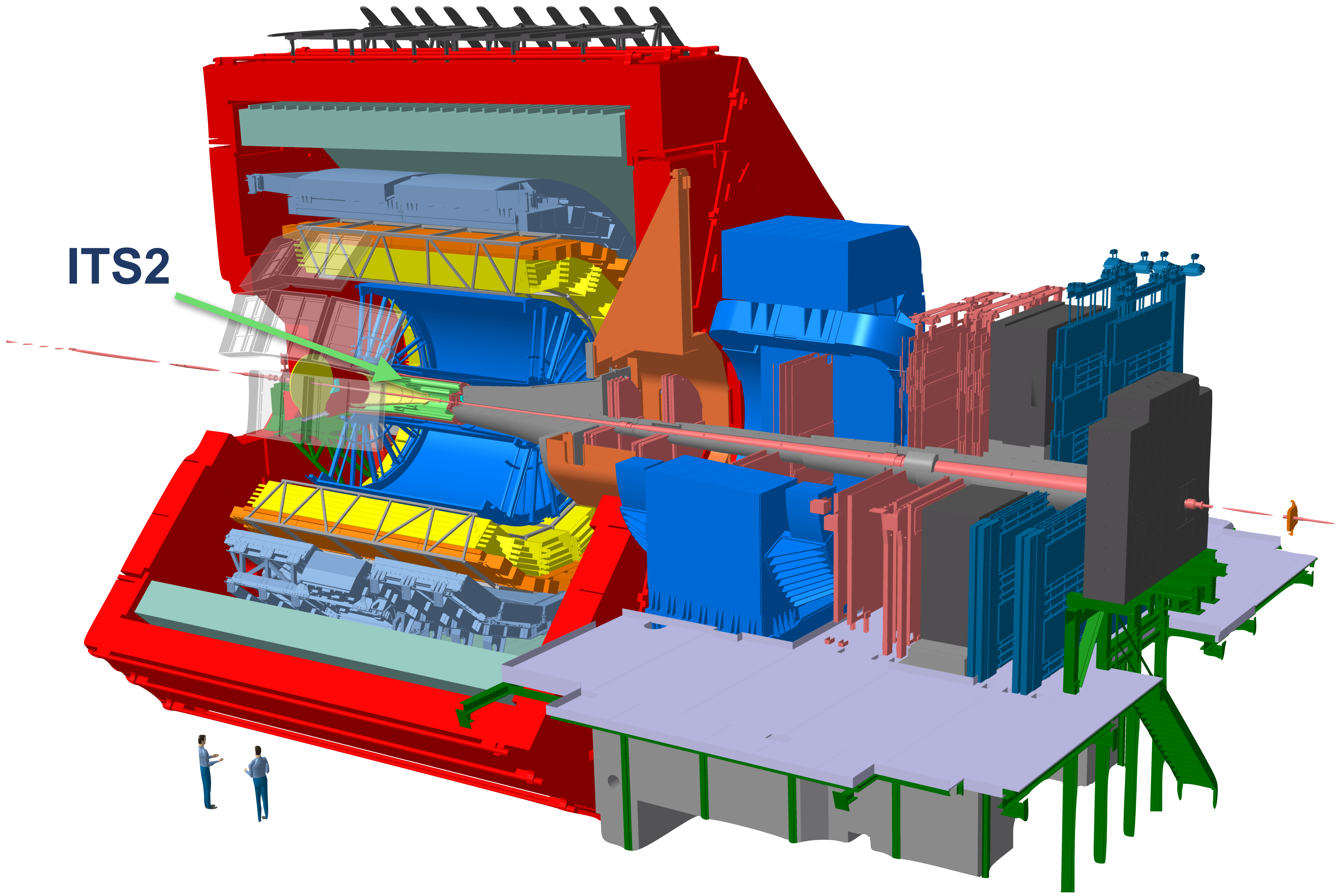


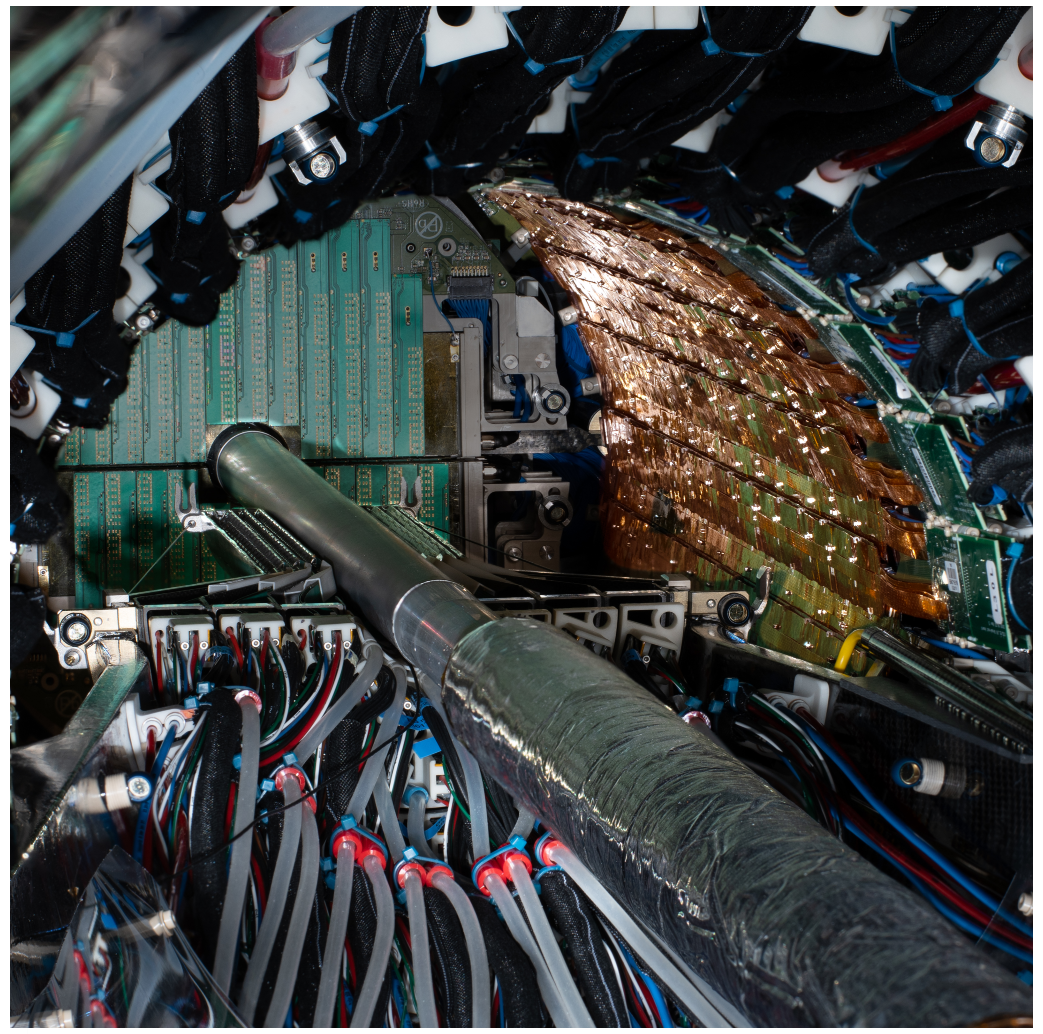


ALICE Inner Tracking System 3 Overview

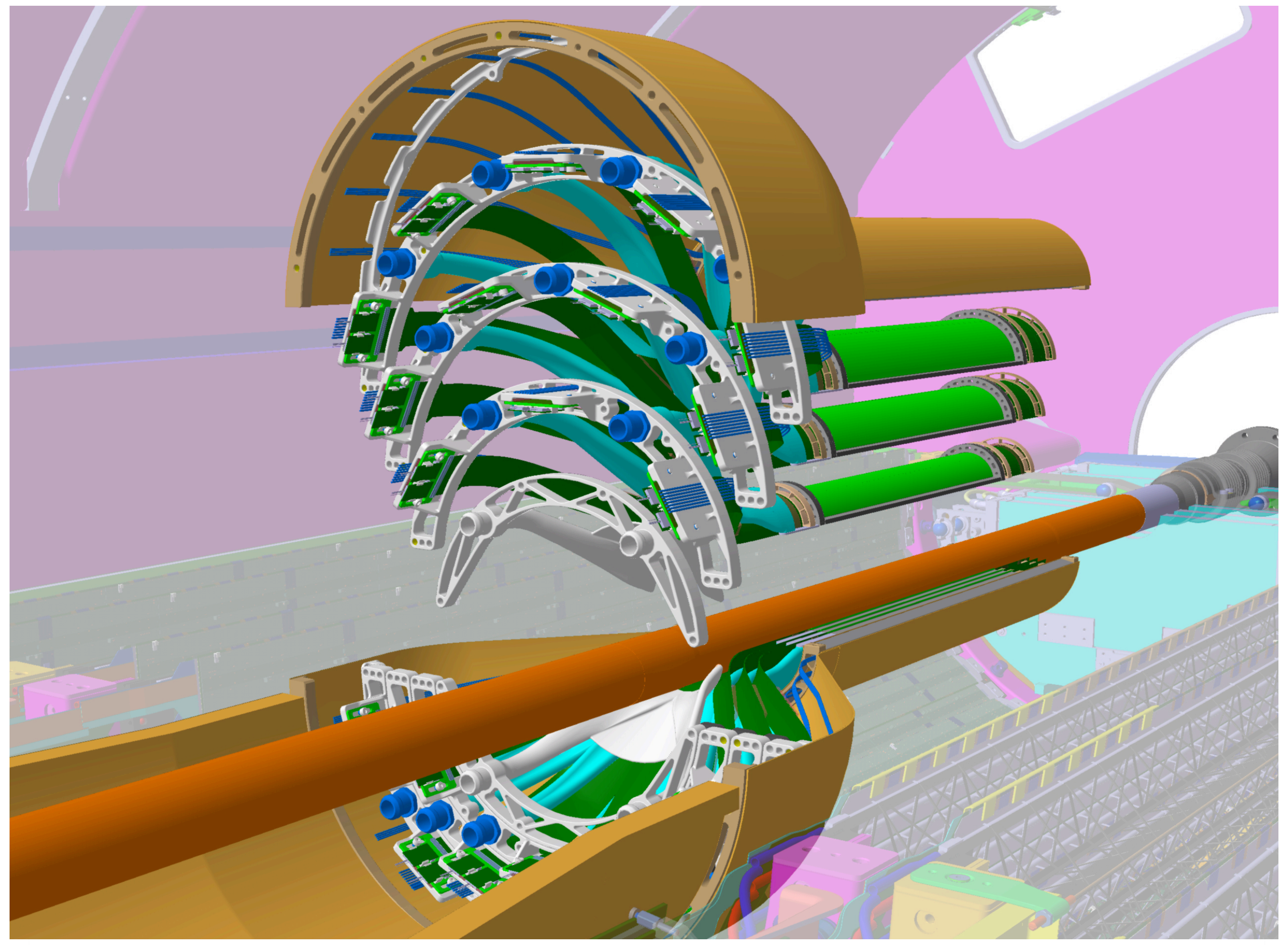
Felix Reidt (CERN) on behalf of the ALICE Collaboration

ALICE

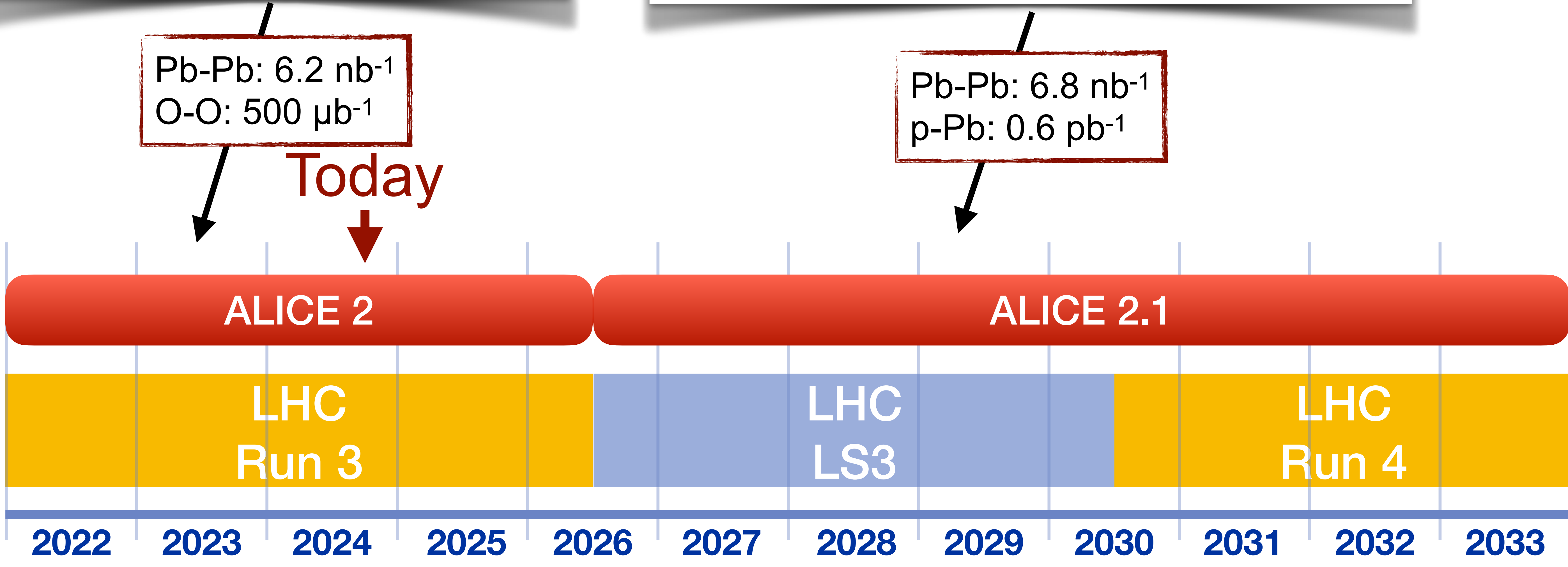




Inner Tracking System 2 (ITS2)

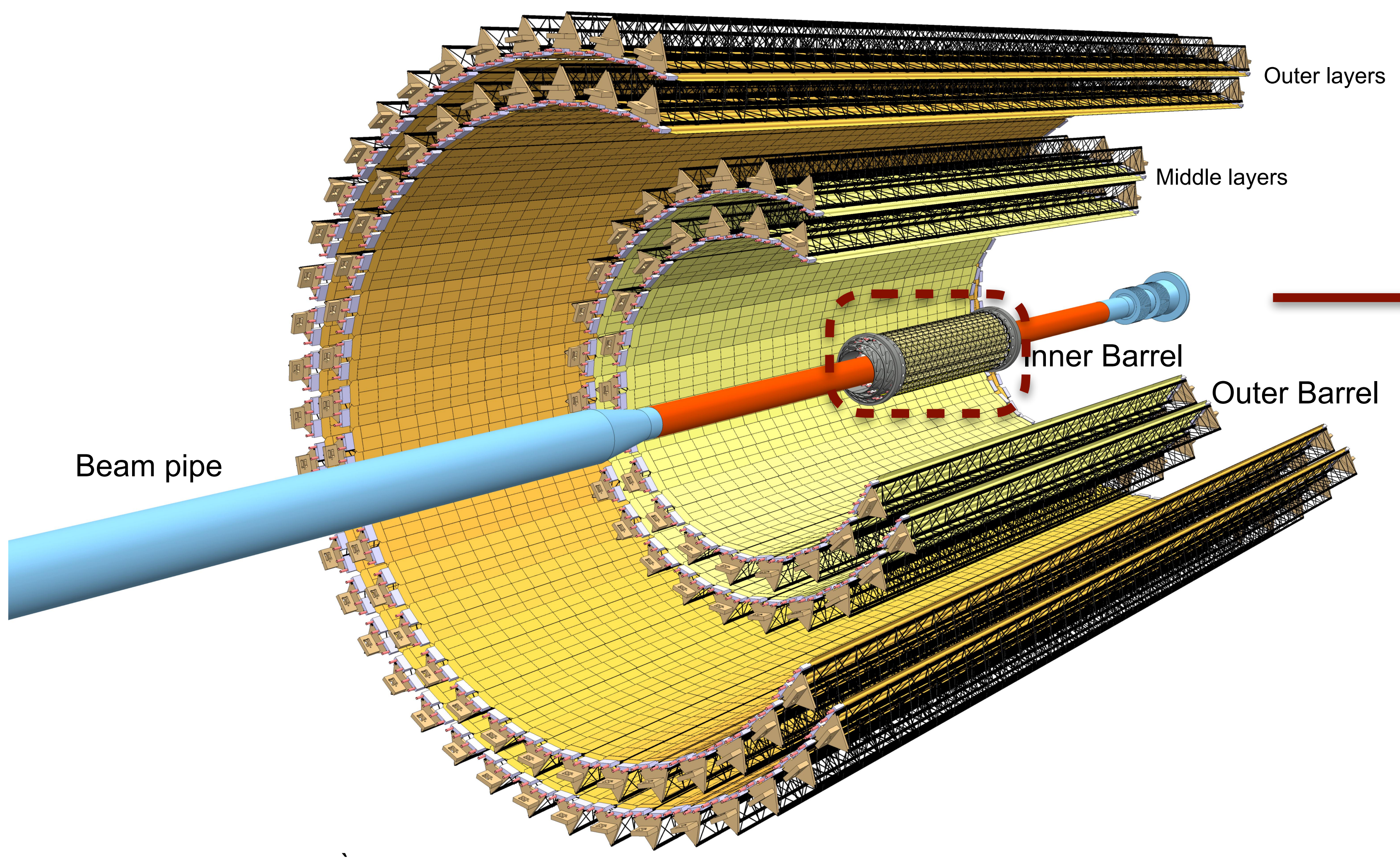


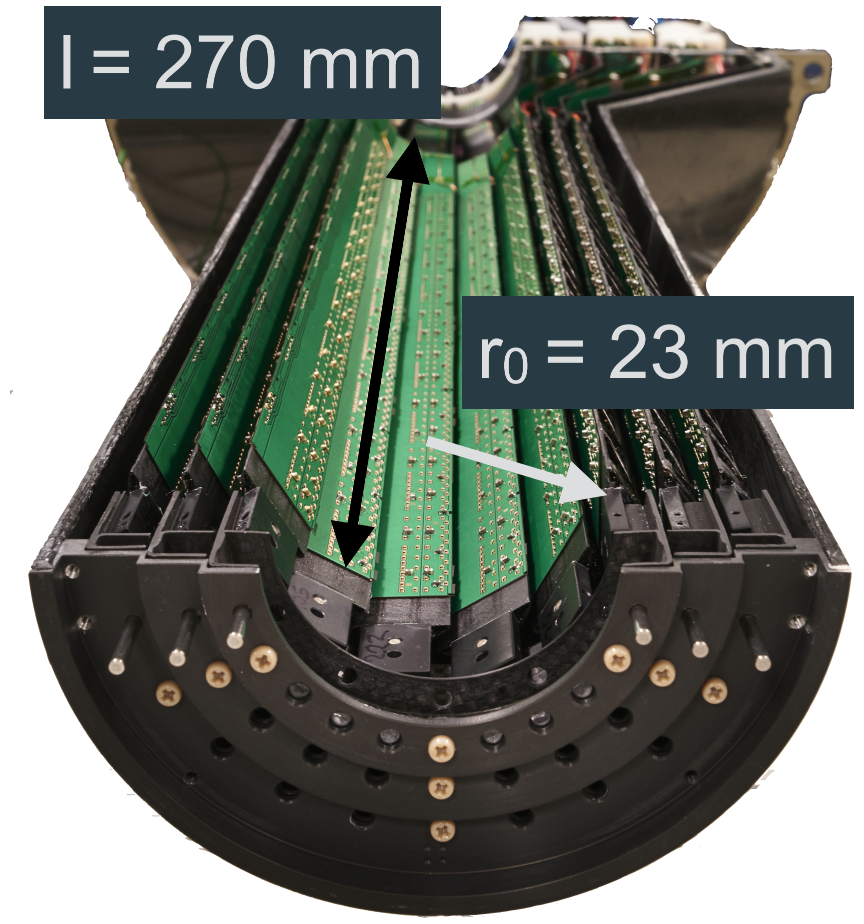
Inner Tracking System 3 (ITS3)



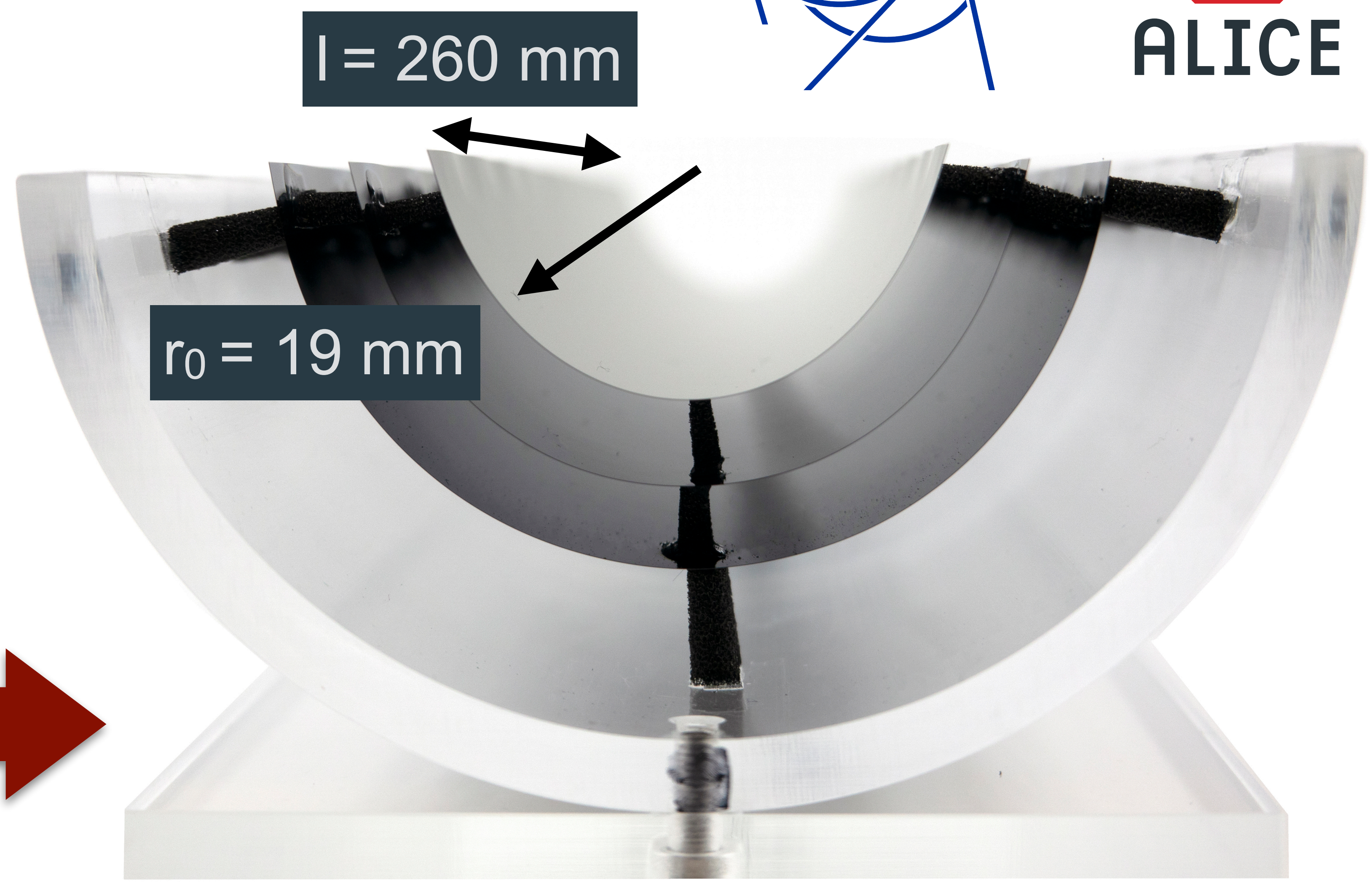
- ALICE is the heavy-ion focussed experiment at the LHC
  - Low p_T heavy flavour hadrons
  - Low-mass dielectrons
  - ➡ Profits significantly high impact parameter resolution
  - ➡ High resolution, low material Inner Tracking System

The Inner Tracking System 3 (ITS3)



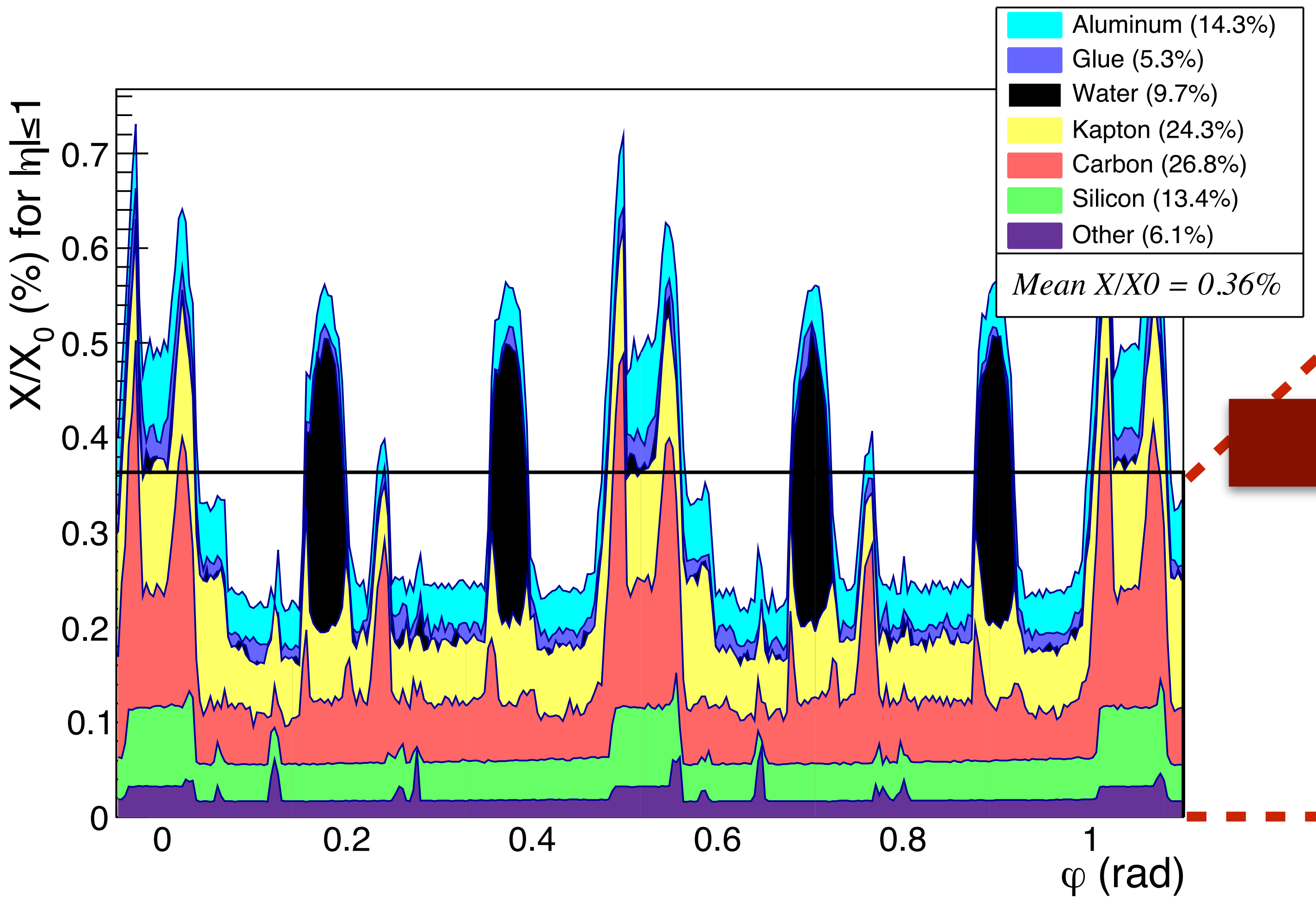


ITS2 Inner Barrel

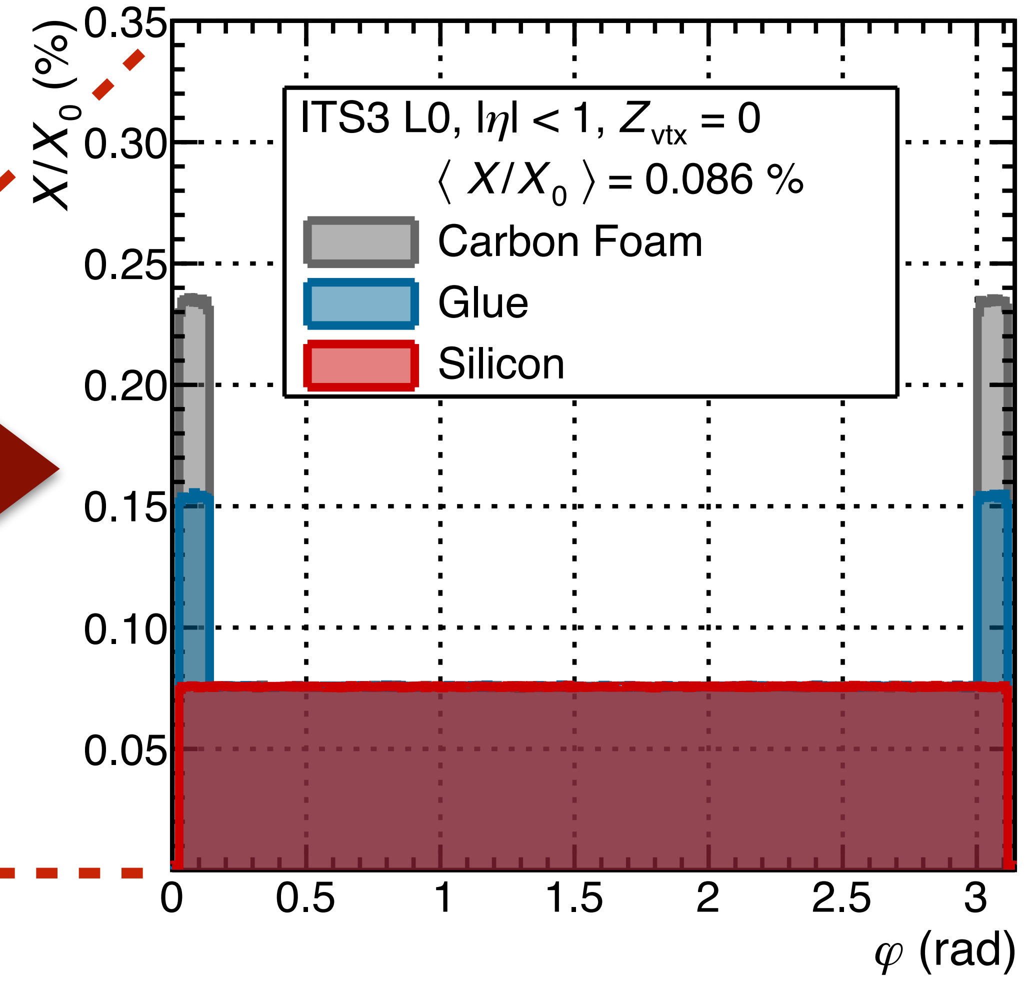


ITS3 Engineering Model 1

- Replacement of ITS2 Inner Barrel with 3 layers of curved, 50 µm thick, wafer-scale MAPS
- Air cooling & ultra-light mechanical supports
- Reduced material budget of on average **0.09% X_0** instead of **0.36% X_0** per layer
- Smaller radius of the innermost layer: **19 mm** instead of **23 mm**



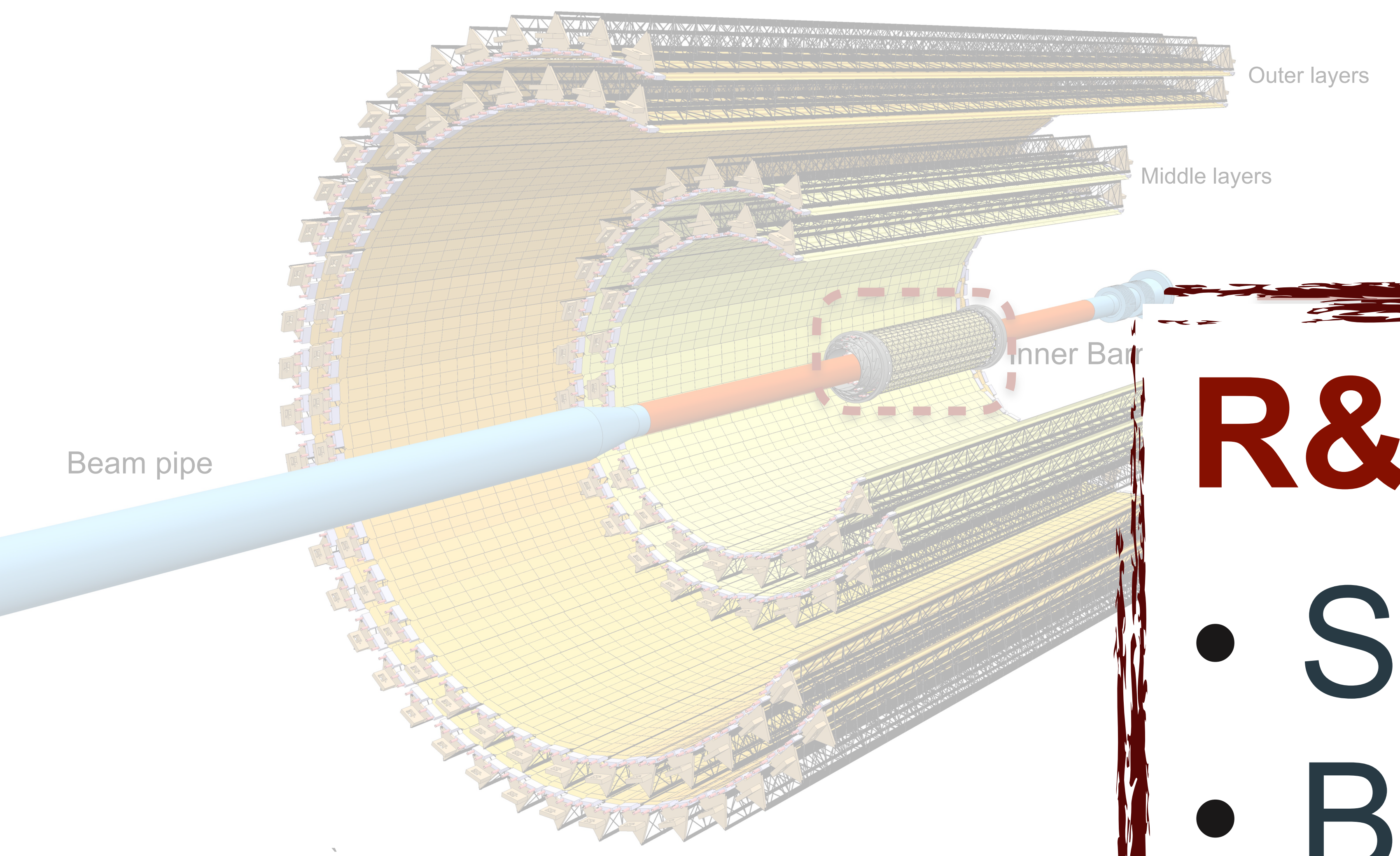
ITS2 Layer 0

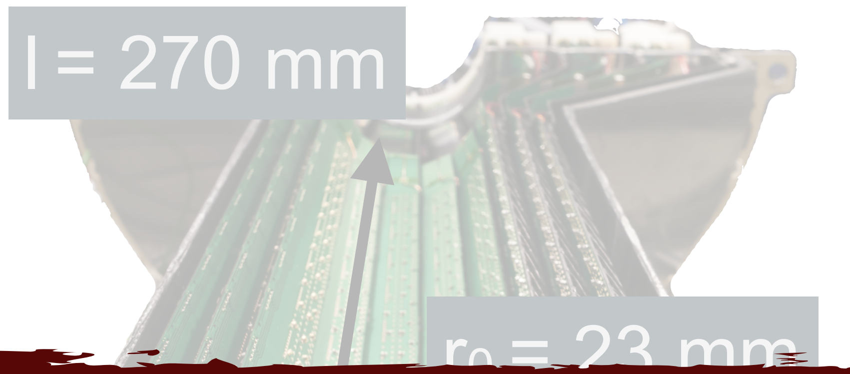


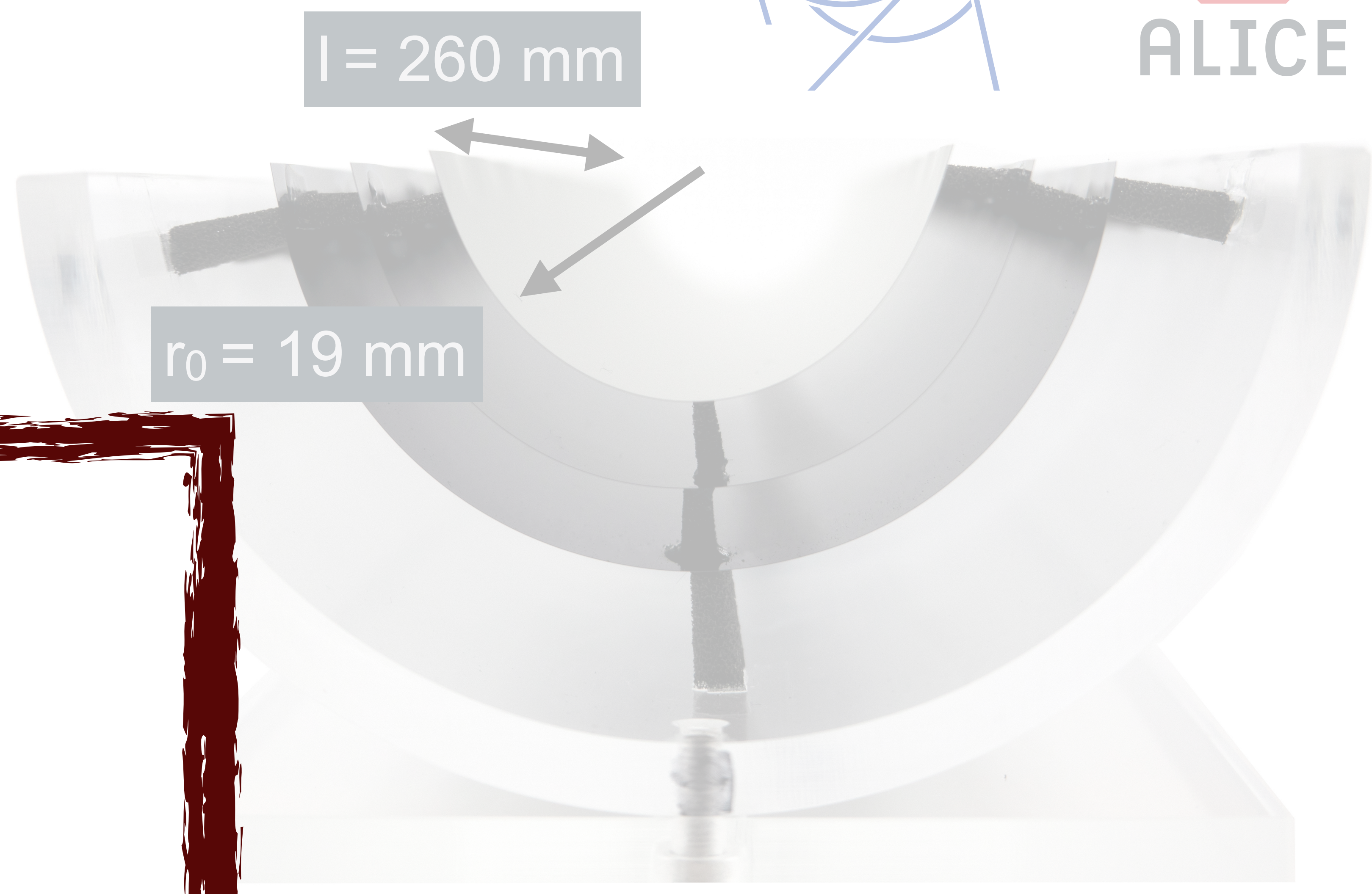
ITS3 Layer 0

ITS3 TDR — CERN-LHCC-2024-003

The Inner Tracking System 3 (ITS3)





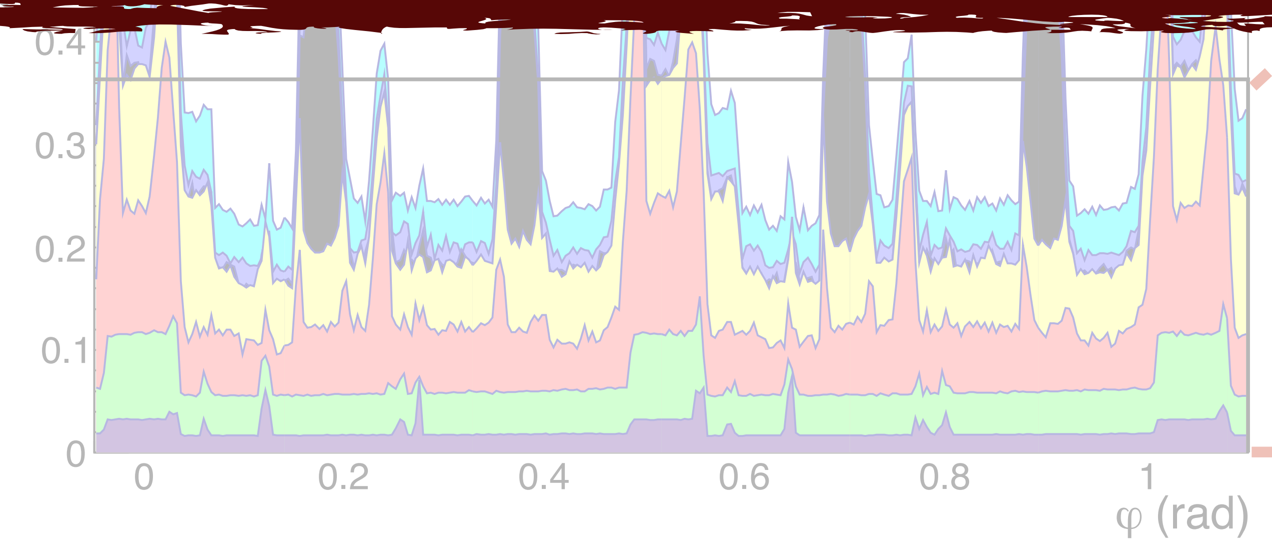


ITS3 Engineering Model 1

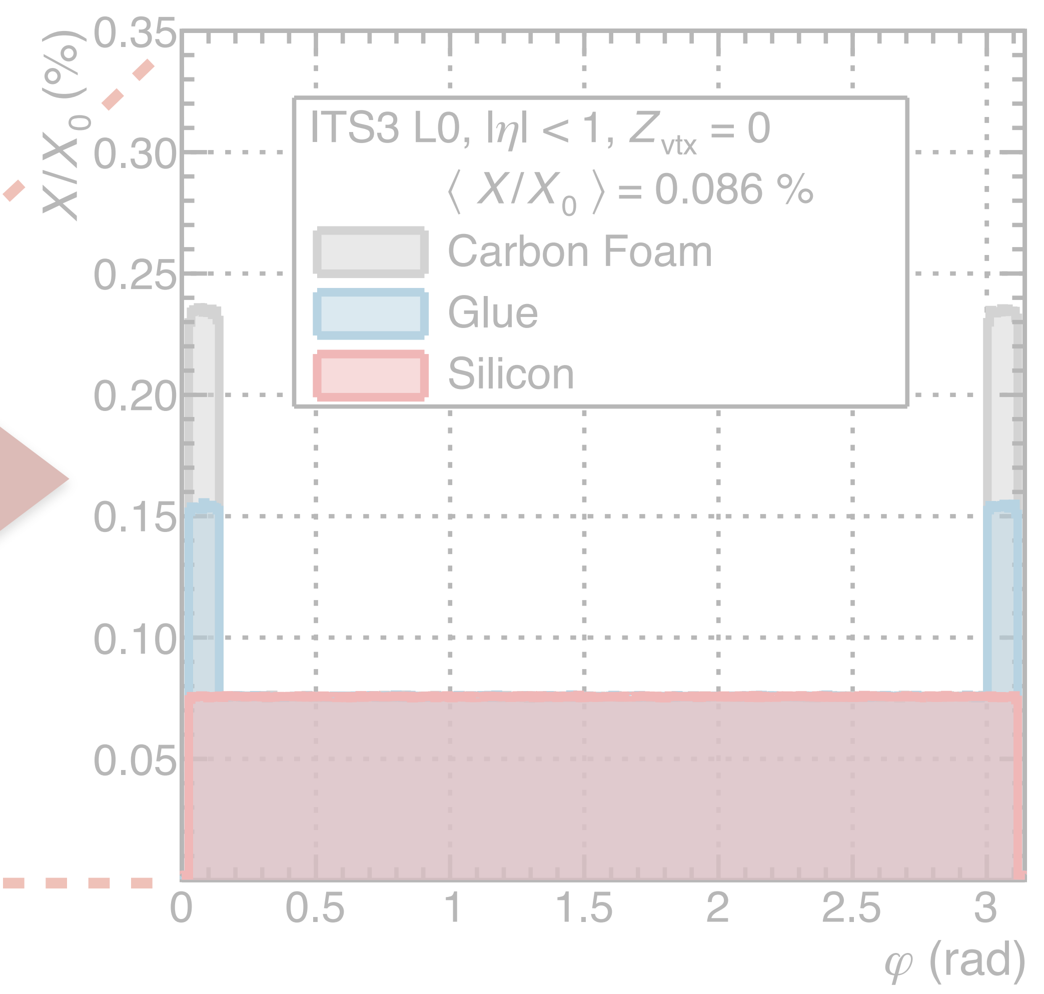
R&D items

- Stitching
- Bending of silicon wafers
- Air cooling
- No electrical substrate

- Replacement of ITS2 Inne… with 3 layers of curved, 50… wafer-scale MAPS
- Air cooling & ultra-light me…
- Reduced material budget of on average **0.09%** X_0 instead of **0.36%** X_0 per layer
- Smaller radius of the innermost layer: **19 mm** instead of **23 mm**



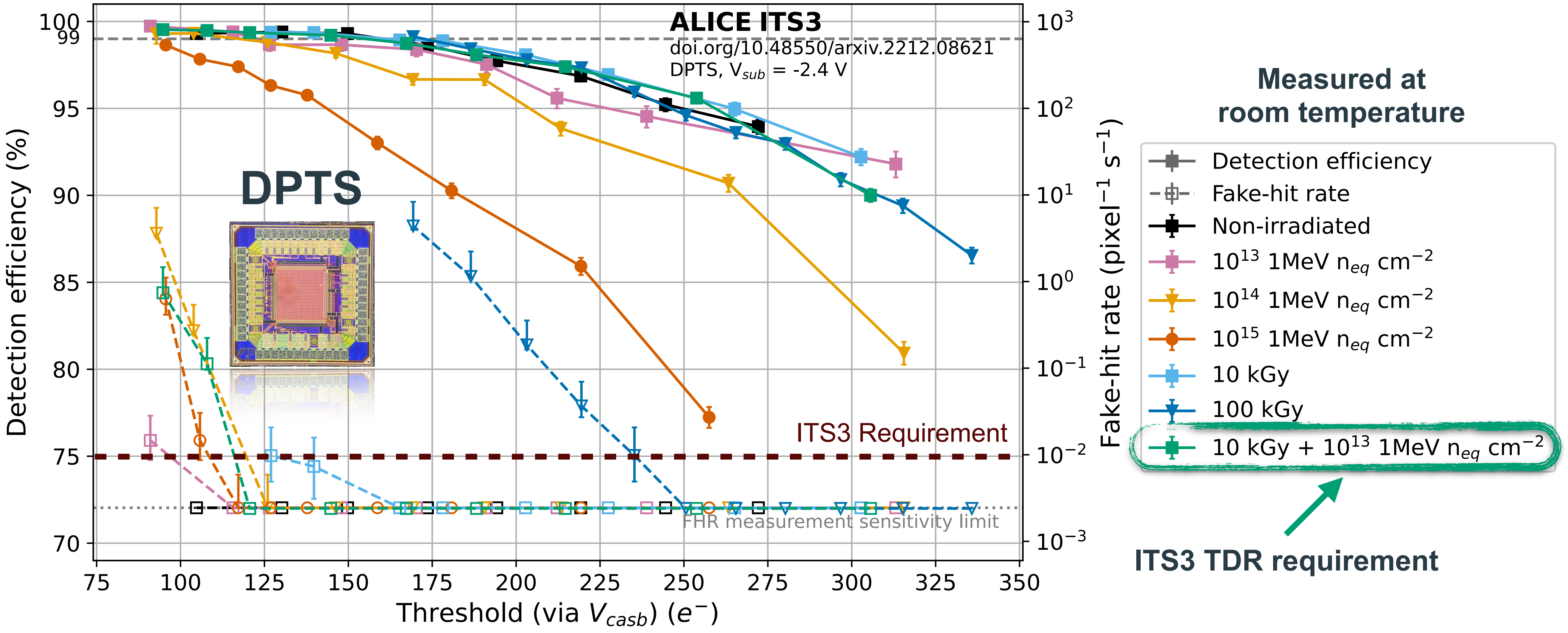
ITS2 Layer 0

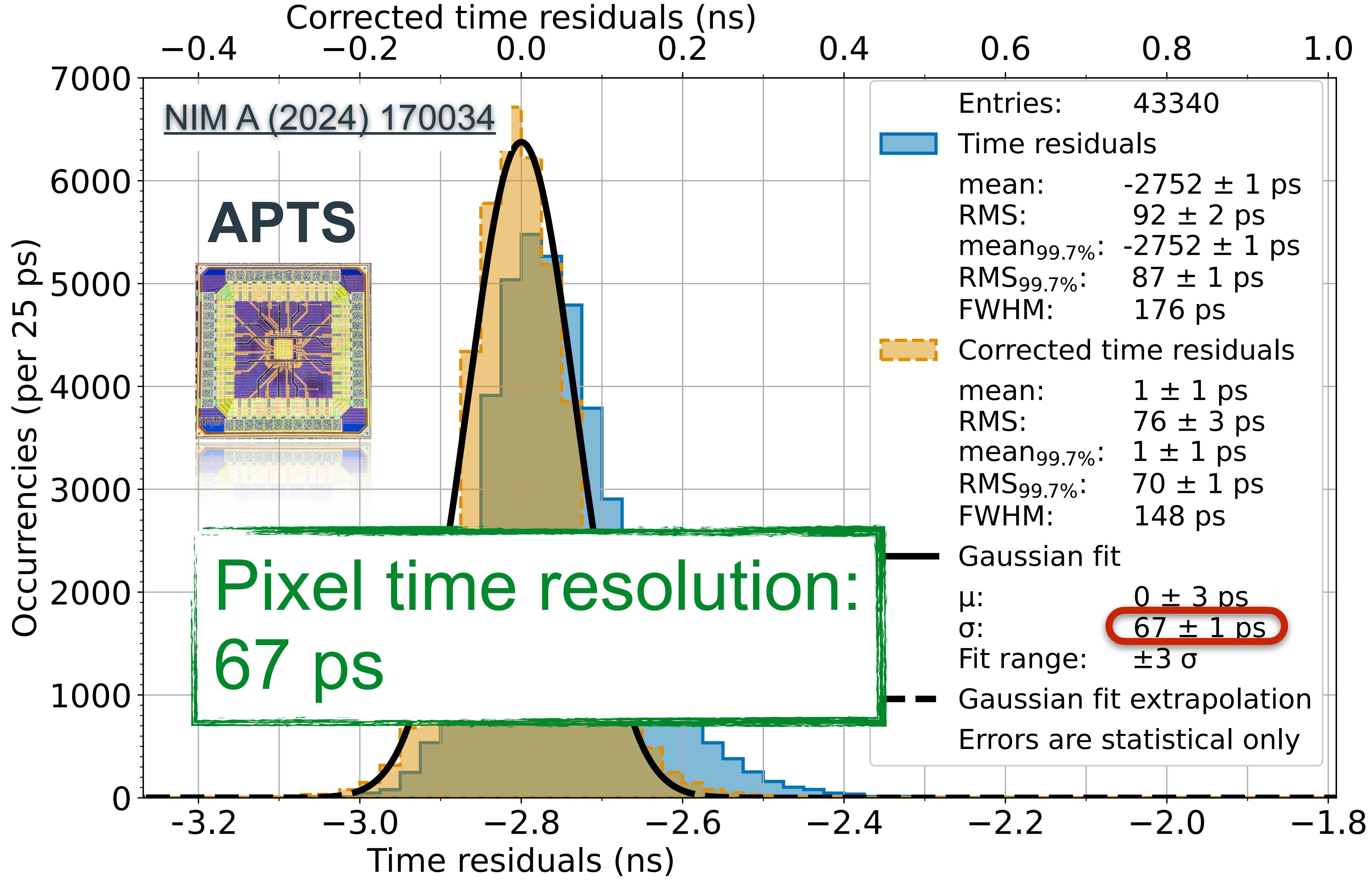


ITS3 Layer 0

ITS3 TDR — CERN-LHCC-2024-003

TPSCo 65 nm technology qualification — pixel prototype chips (selection)

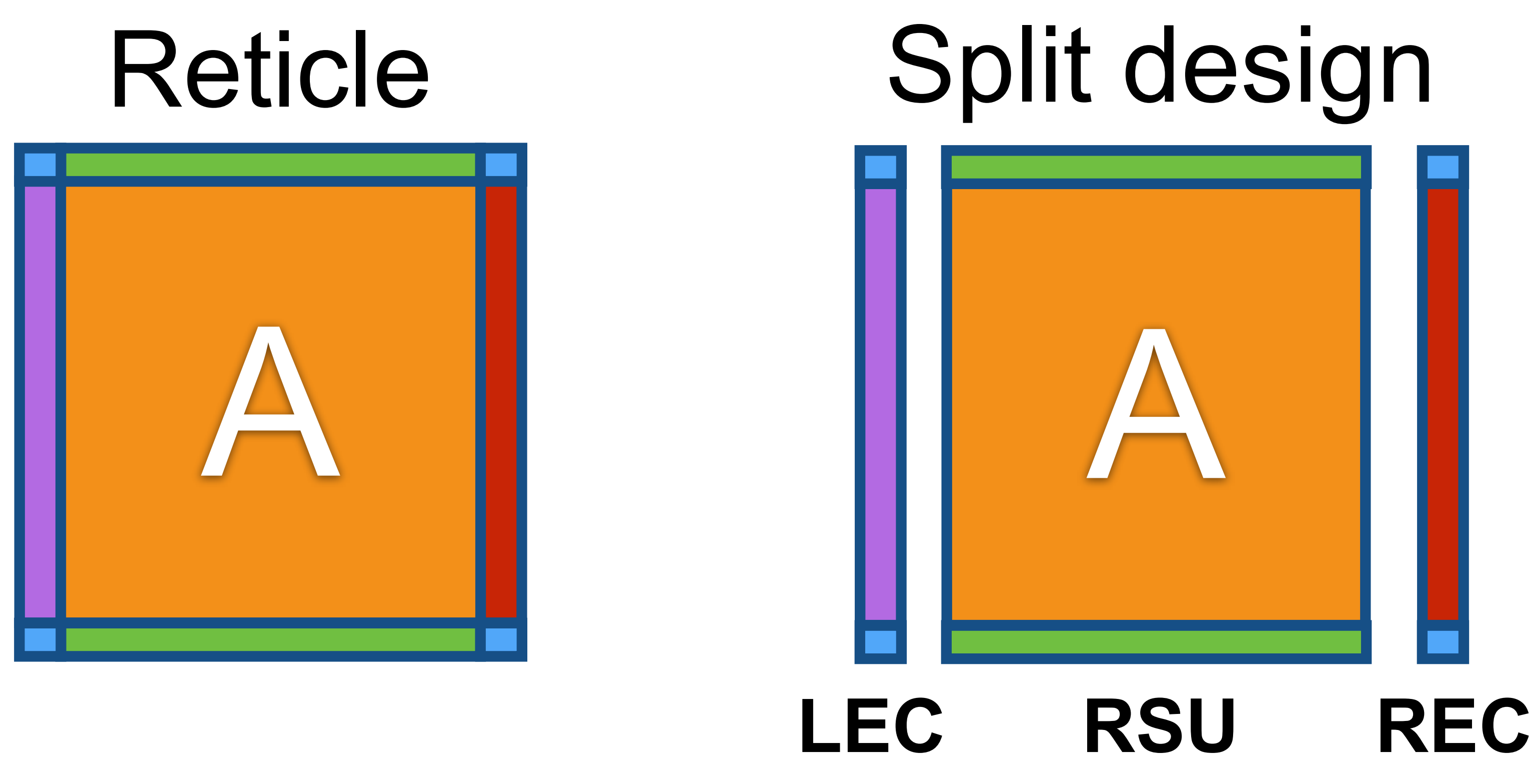




- **Multi-Layer Reticle 1 (MLR-1):** common effort by ALICE ITS3 and CERN EP R&D
- Various small scale prototypes with pixel matrices and ancillary circuitry
- Technology explored far beyond the requirements of ITS3 in terms of radiation hardness and time resolution
  ⇒ Promising also for future applications like ALICE 3 Vertex Detector and FCC-ee

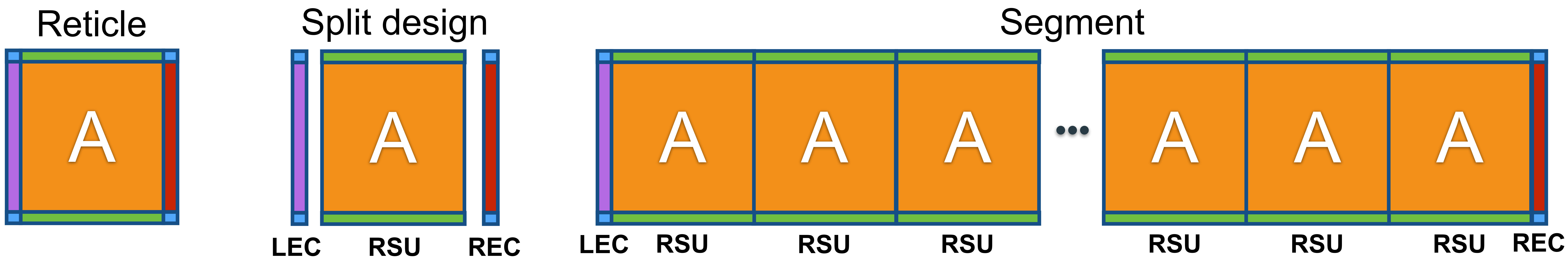
A. Sturniolo - Testing small devices for ALICE ITS3 upgrade [Poster]
A. Lorenzetti - Performance studies of the CE-65v2 MAPS prototype structure [Poster]
I. Sanna - TCAD and charge transport simulations of MAPS in 65nm for the ALICE ITS3 [Poster]
G. Borghello - Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations [Poster]

Stitching



- Reticle design split into:
  - Left End Cap (LEC)
  - Repeated Sensor Unit (RSU)
    “A” denotes active area
  - Right End Cap (REC)

Stitching



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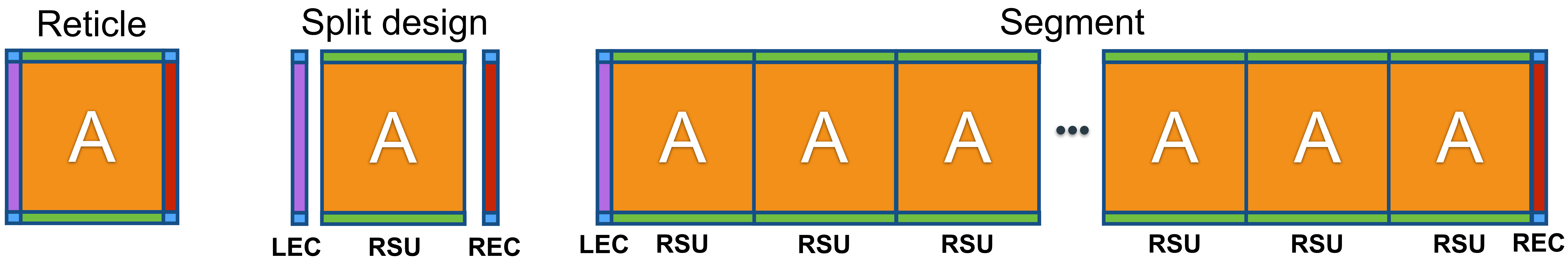
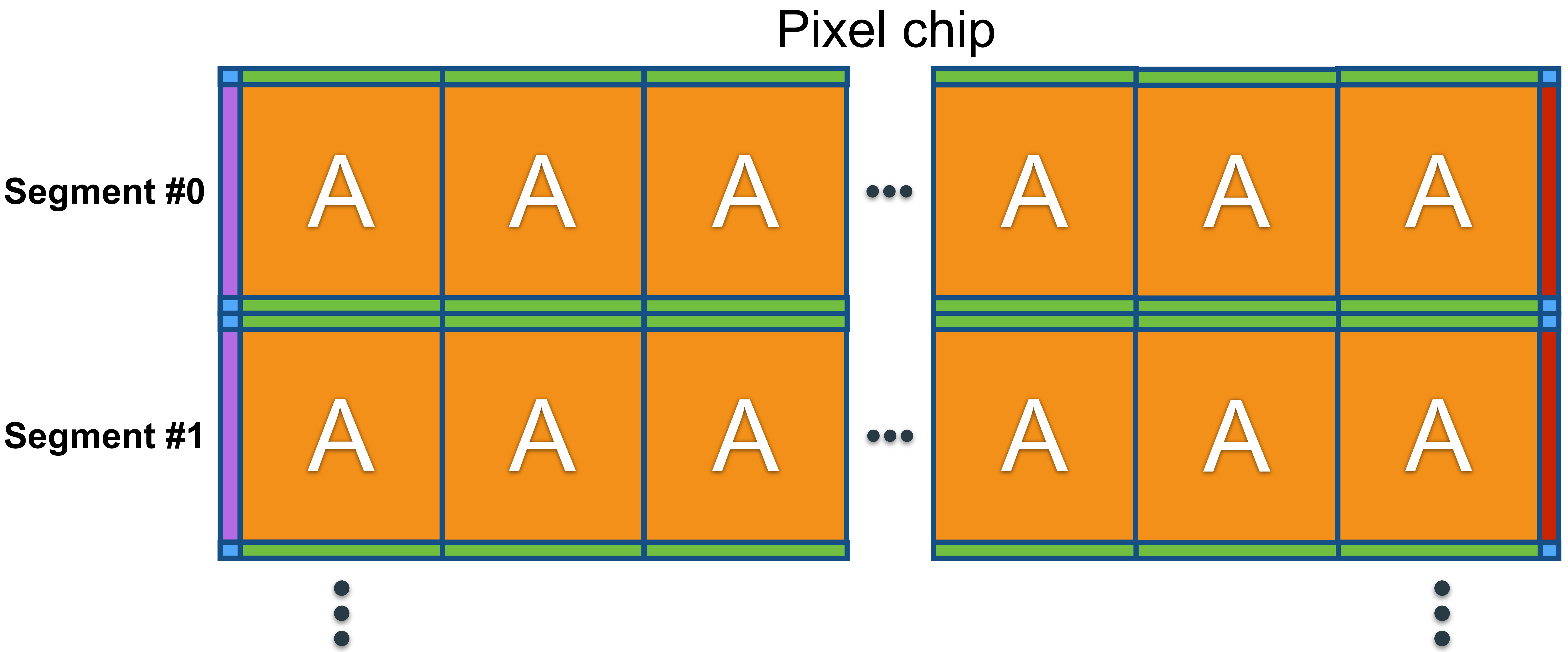
  LEC, multiple RSUs, REC

Stitching



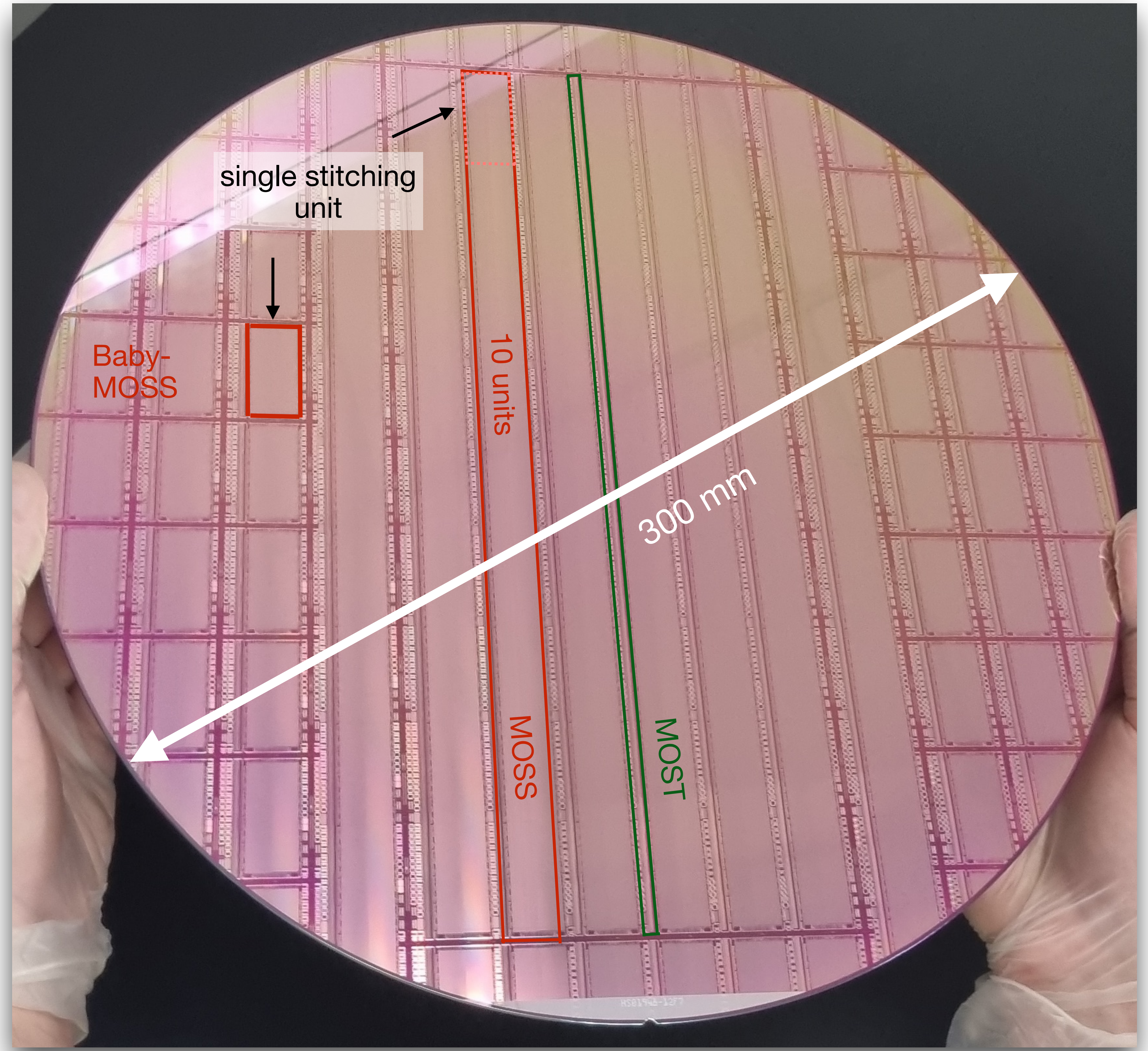
- Reticle design split into:
  - Left End Cap (LEC)
  - Repeated Sensor Unit (RSU)
    “A” denotes active area
  - Right End Cap (REC)
- Segment:
  LEC, multiple RSUs, REC
- Pixel chip:
  - Multiple, independent segments
  - Interfacing only via LEC, REC



Stitched wafer-scale MAPS — Engineering Run 1 (ER-1)

Engineering Run 1 (ER-1)

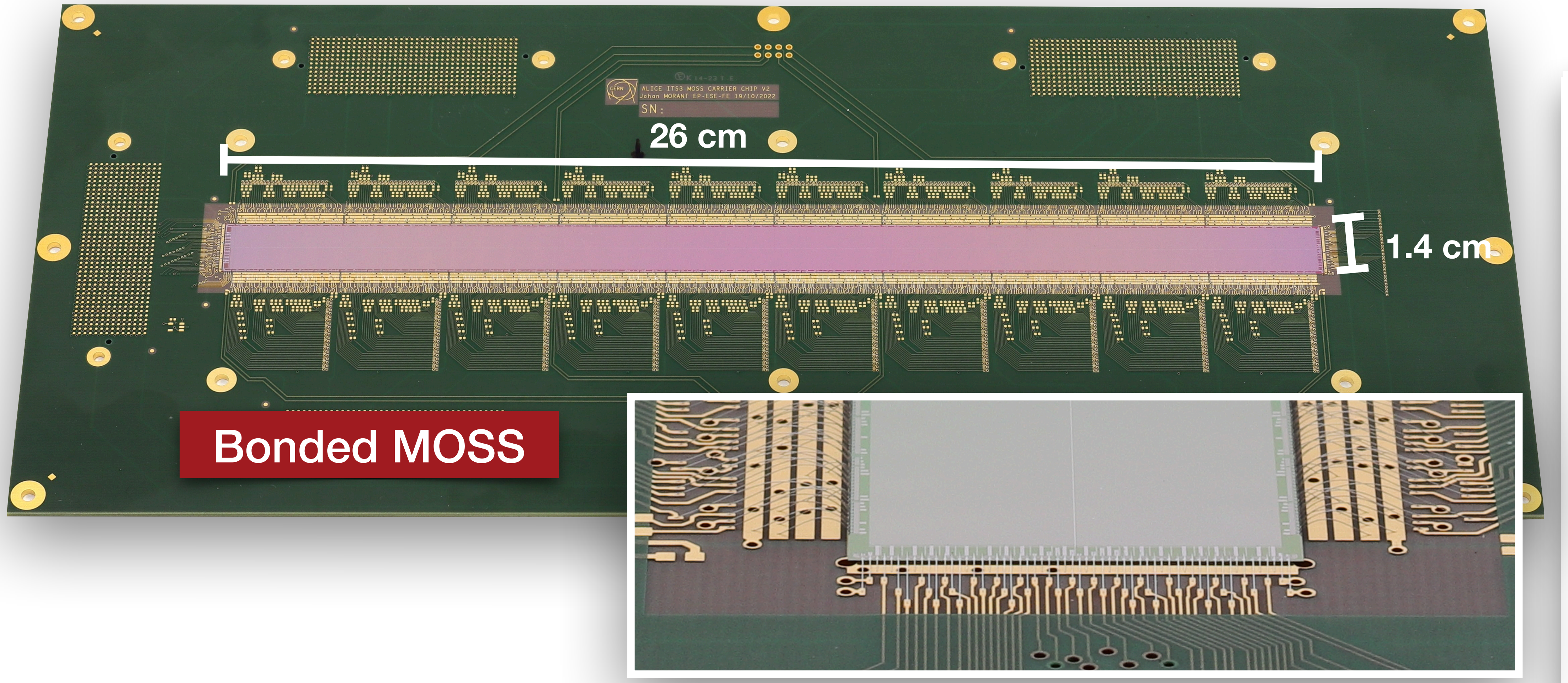
- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips
  - based on TPSCo 65 nm
- "**MOSS**": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²)
  - conservative design (increased feature spacing), different pitches
- "MOST": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²)
  - more dense design, different approach to deal with defects
- Baby-MOSS (single stitch → ~ reticle-sized)
- Plenty of small chips (like MLR-1)

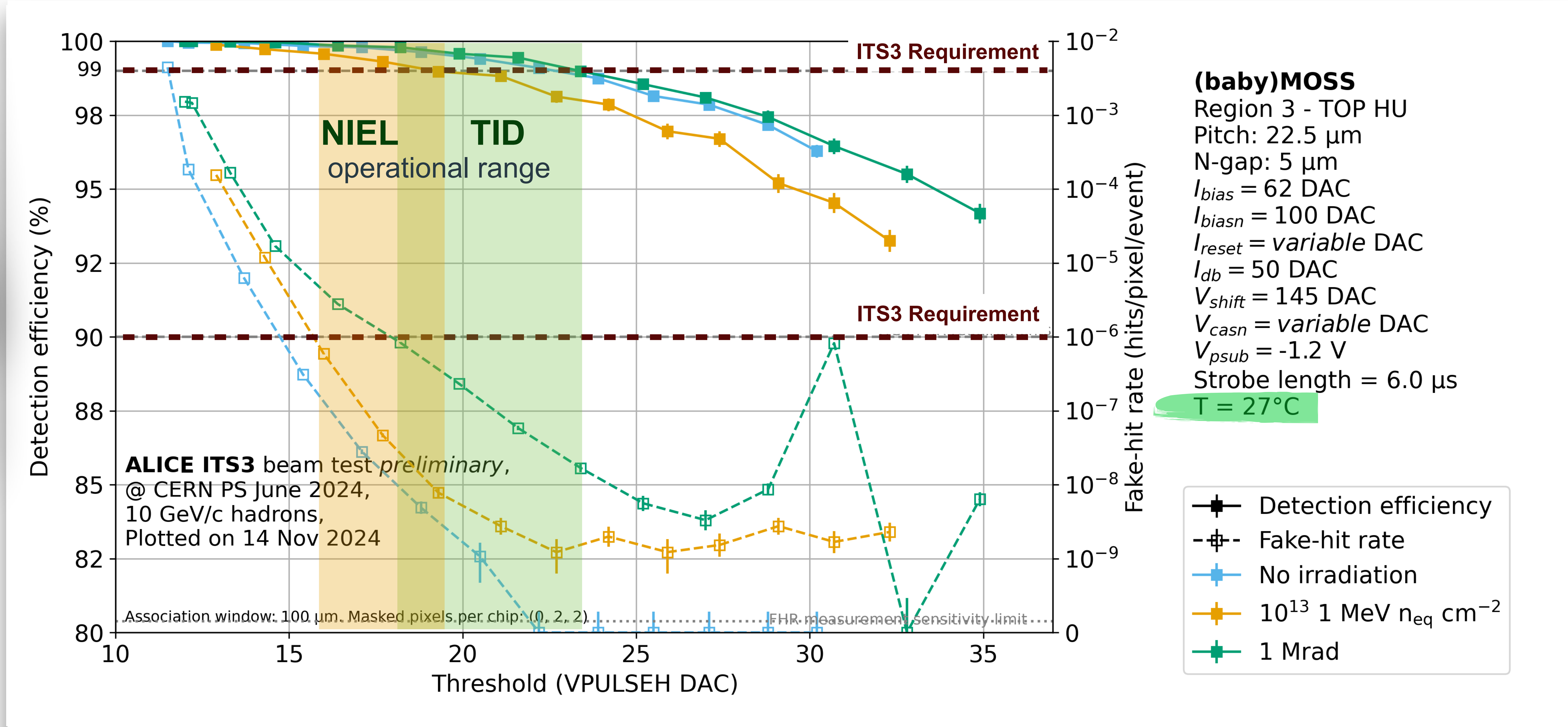


Engineering Run 1 wafer with various dies

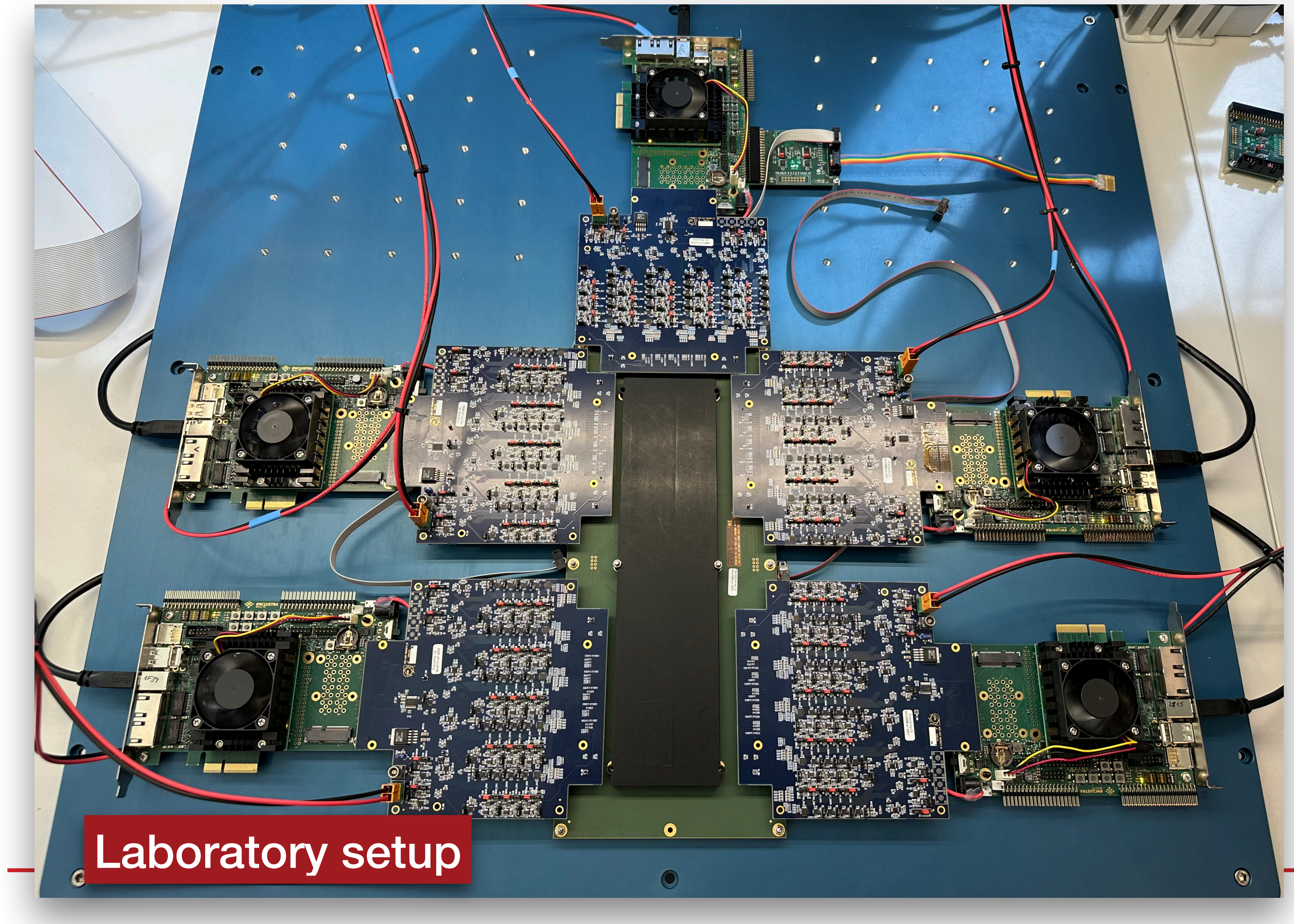
L. Terlizzi - Characterization of MOSS for the ALICE ITS3 for the LHC Run 4 [Nov 21st, 16:40]
M. Selina - Exploring ALICE ITS3 MOST [Nov 21st, 16:57]

Stitched wafer-scale MAPS — MOSS — current results



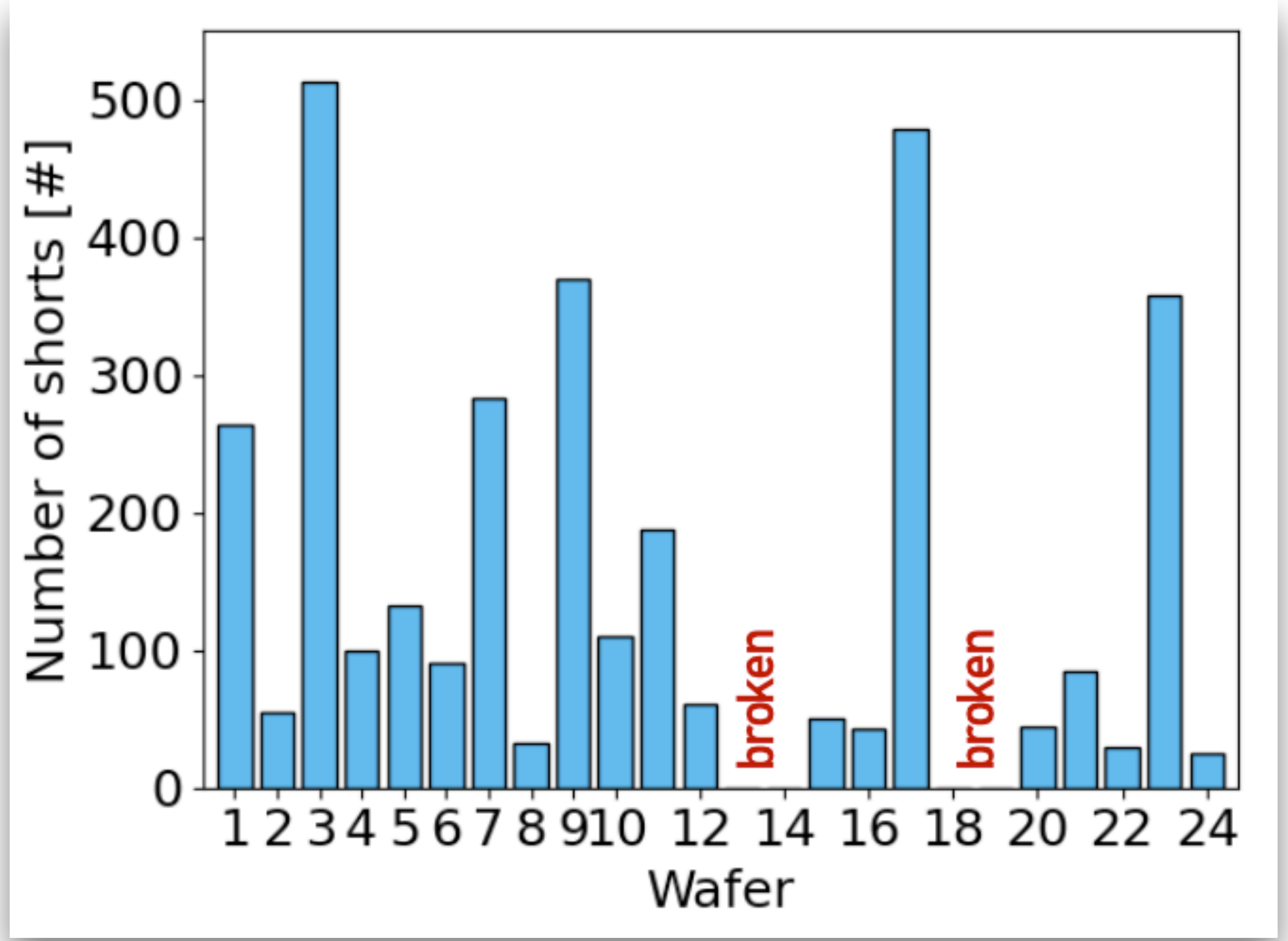


MOSS Detection efficiency and fake-hit rate



- Chip is **operational**
- Detailed characterisation at the laboratory and at test beam
- **Full efficiency** reached at **acceptable fake hit rate,** chip-by-chip variations and calibration being studied

Stitched wafer-scale MAPS — MOSS — production yield



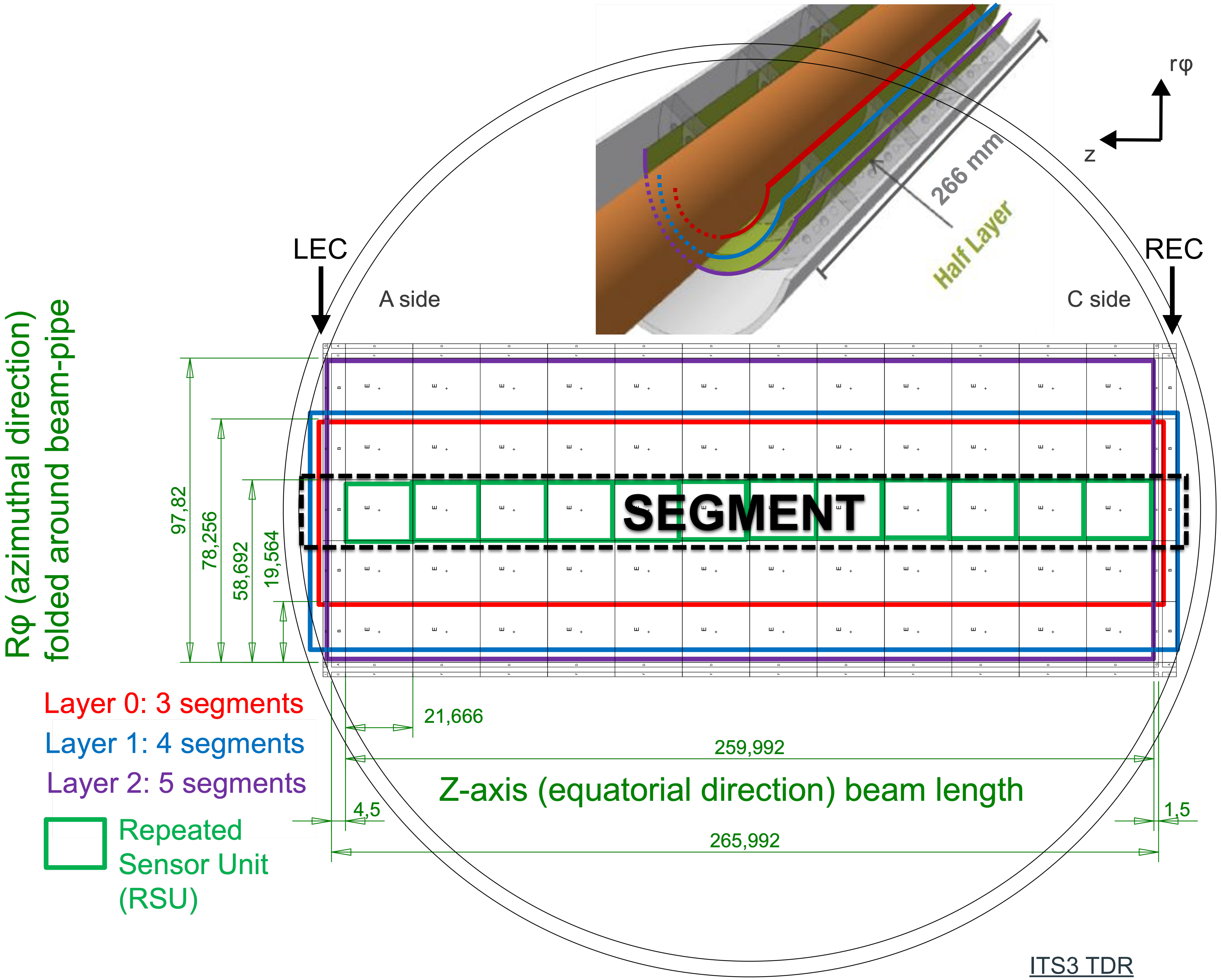
Shorts detected in (Baby-)MOSS

SEM cross section of the top two metal layers

- Rather large number of shorts are observed
- Reason identified (shorts *between metal layers*)
- Metal stack change foreseen to facilitate power distribution ➡ expected to mitigate this issue
- Functional yields for 'powerable' chips: being studied in detail, small losses

Stitched Wafer-Scale MAPS — MOSAIX

- Final **full size**, **full functionality sensor**
  - Modular design:
    - Sensor divided into 5 segments (allowing to use 3, 4 or 5 segments for layers 0, 1 and 2, respectively)
    - 12 Repeated Sensor Units (RSUs) / segment
    - 12 tiles / RSU (independent powering, control and readout) → 144 tiles corresponding to 0.7% modularity
  - Fractional sensitive area: 93%
  - Interfacing:
    - Powering LEC and REC sides
    - Control and readout from the LEC only



ITS3 TDR

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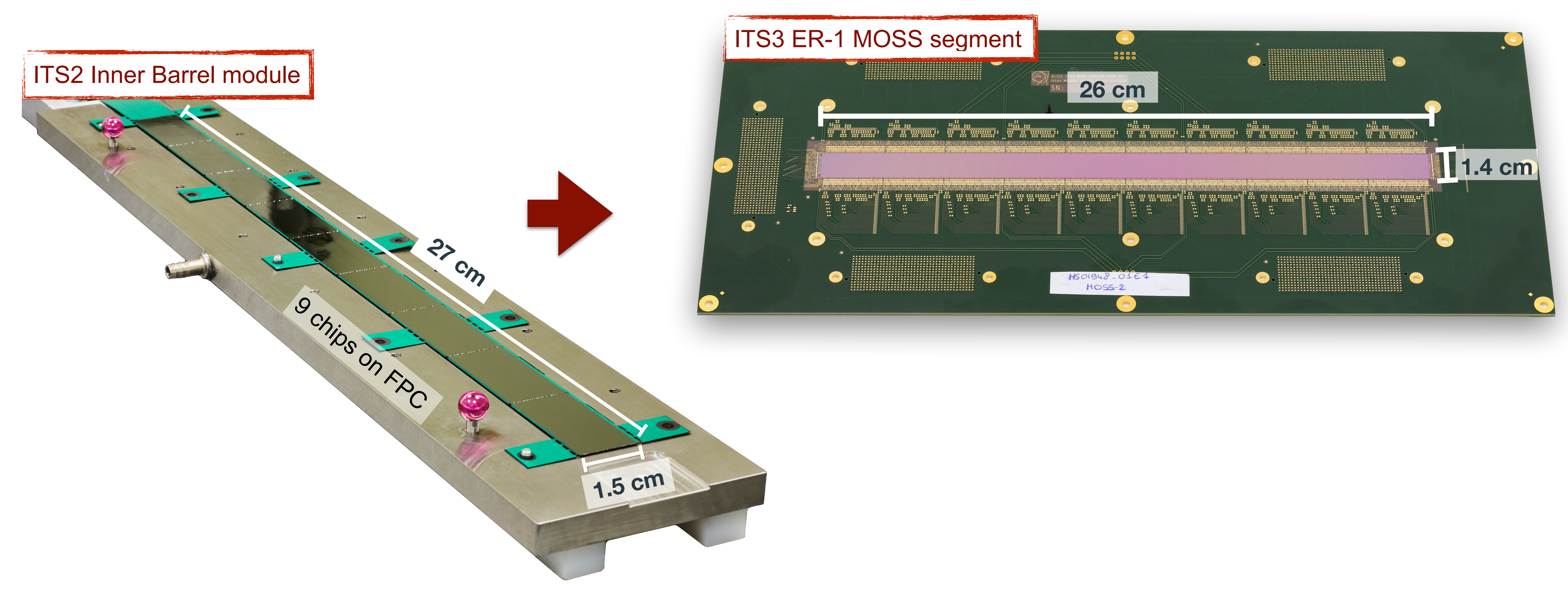
  - Fractional sensitive area: 93%
  - Interfacing:
    - Powering LEC and REC sides
    - Control and readout from the LEC only
  - Pixel:
    - Size: 20.8 x 22.8 μm^2
    - Detection efficiency: > 99%
    - Fake-hit rate: 10^{-6} / pixel / event
  - Hit load and readout:
    - 5.75 MHz / cm^2 particle hit rate (Pb-Pb, safety factor 2)
    - Minimum integration window: 2 μs
    - Off-chip data transmission: 30.72 Gb/s
      - Multiple 5.12 / 10.24 Gb/s links
  - Radiation load*:
    - Non-Ionising Energy Loss (NIEL): ~ 4 x 10^{12} 1 MeV n_{eq} cm^{-2}
    - Total Ionising Dose (TID): ~ 4 kGy / 400 krad

      ** recent estimates, based on radiation dose absorbed by ITS2*
  - Power dissipation (active area): < 40 mW / cm^2
  - Submission to foundry planned for early 2025

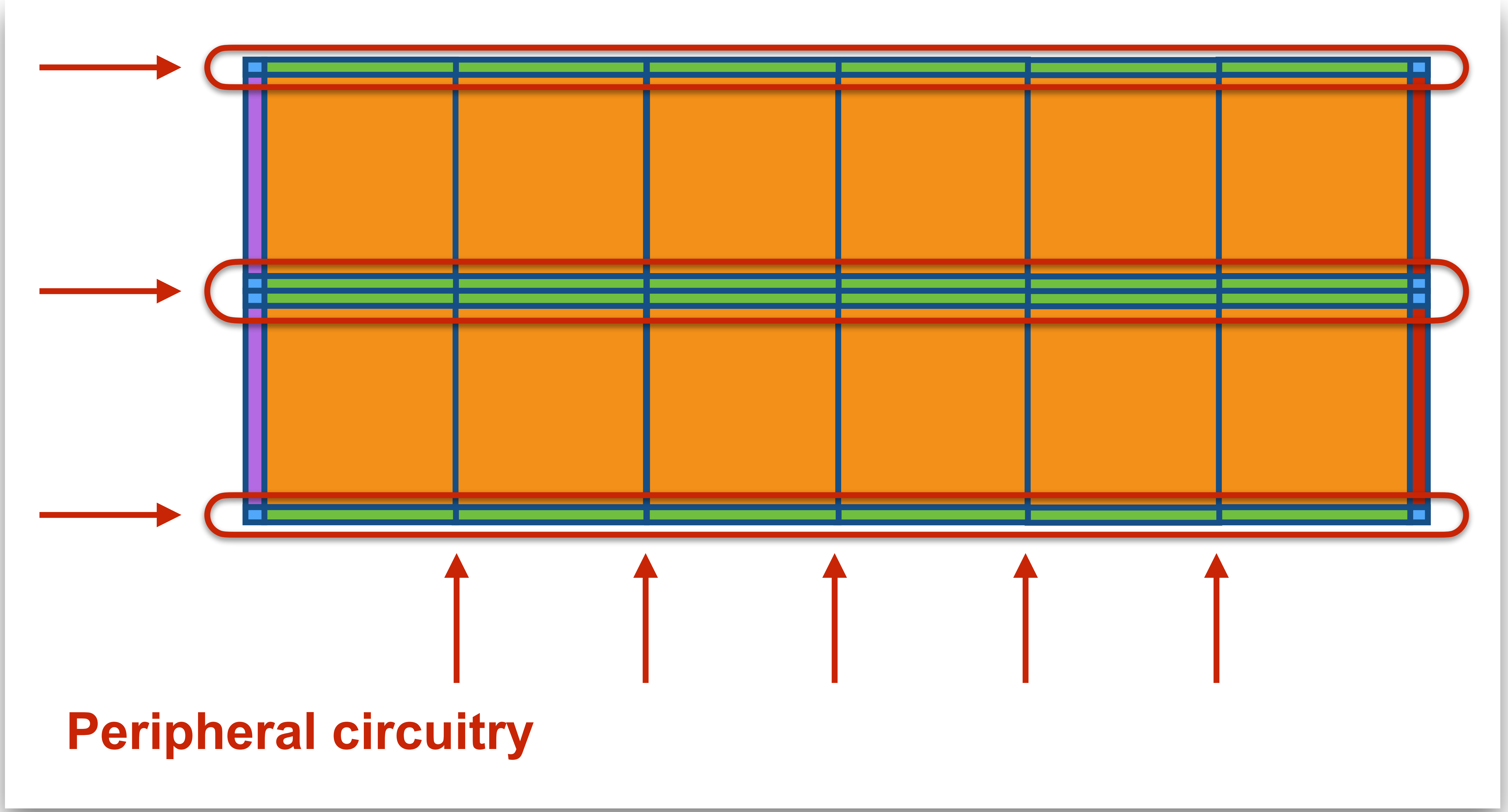
Stitched Wafer-Scale MAPS — MOSAIX — challenges

- Interdependencies and integration: ‘module on a chip’



Stitched Wafer-Scale MAPS — MOSAIX — challenges

- Interdependencies and integration: ‘module on a chip’
- Fractional sensitive area of 93%
  - No overlap zones (like in ‘conventional’ detectors)
  - Readout and biasing need peripheral circuits



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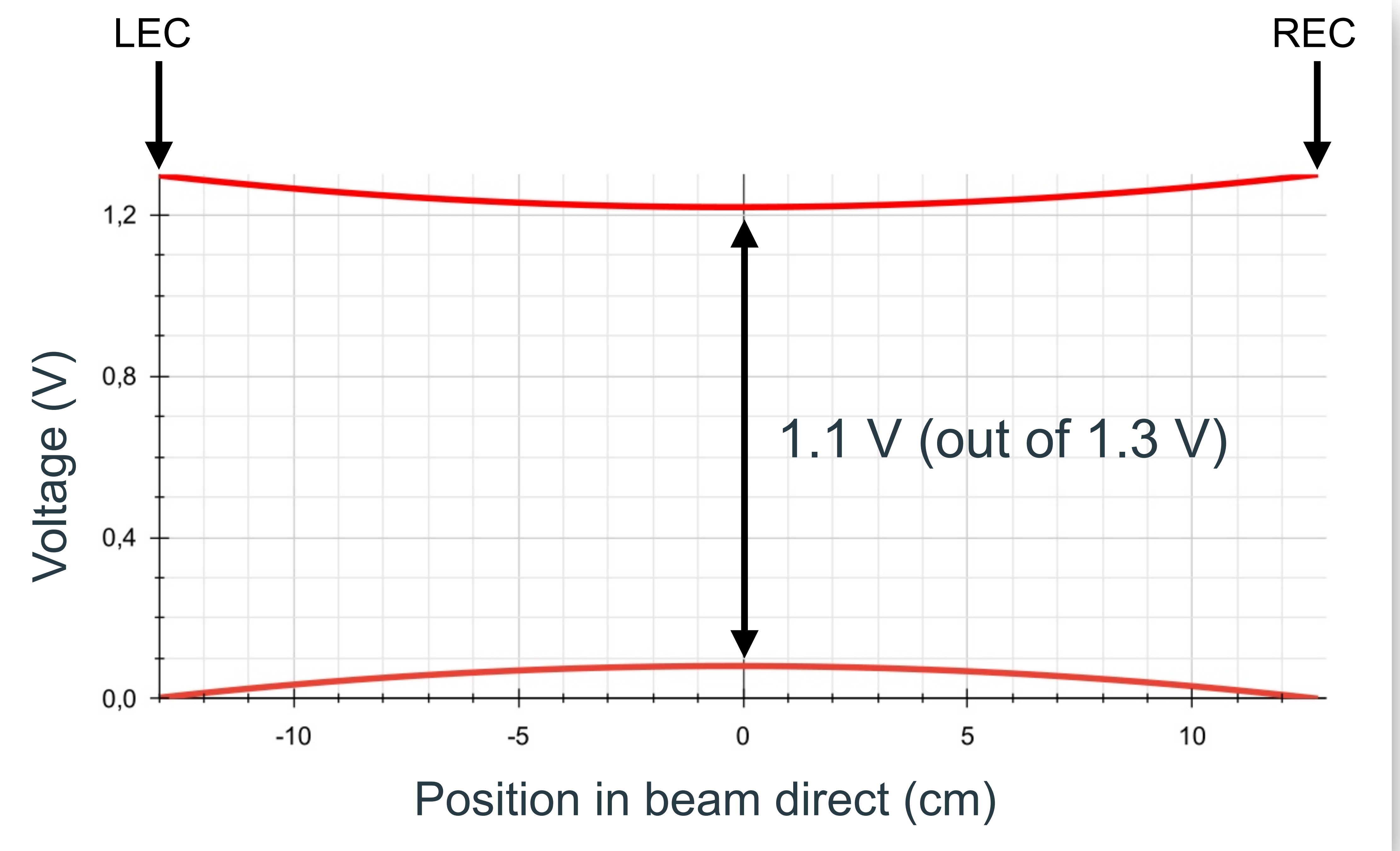
  - Voltage drops on the on-chip metals of the CMOS stack significant
  - Complex segmentation in many independent domains (tiles)
  - Switches and cross-domain signalling and protections



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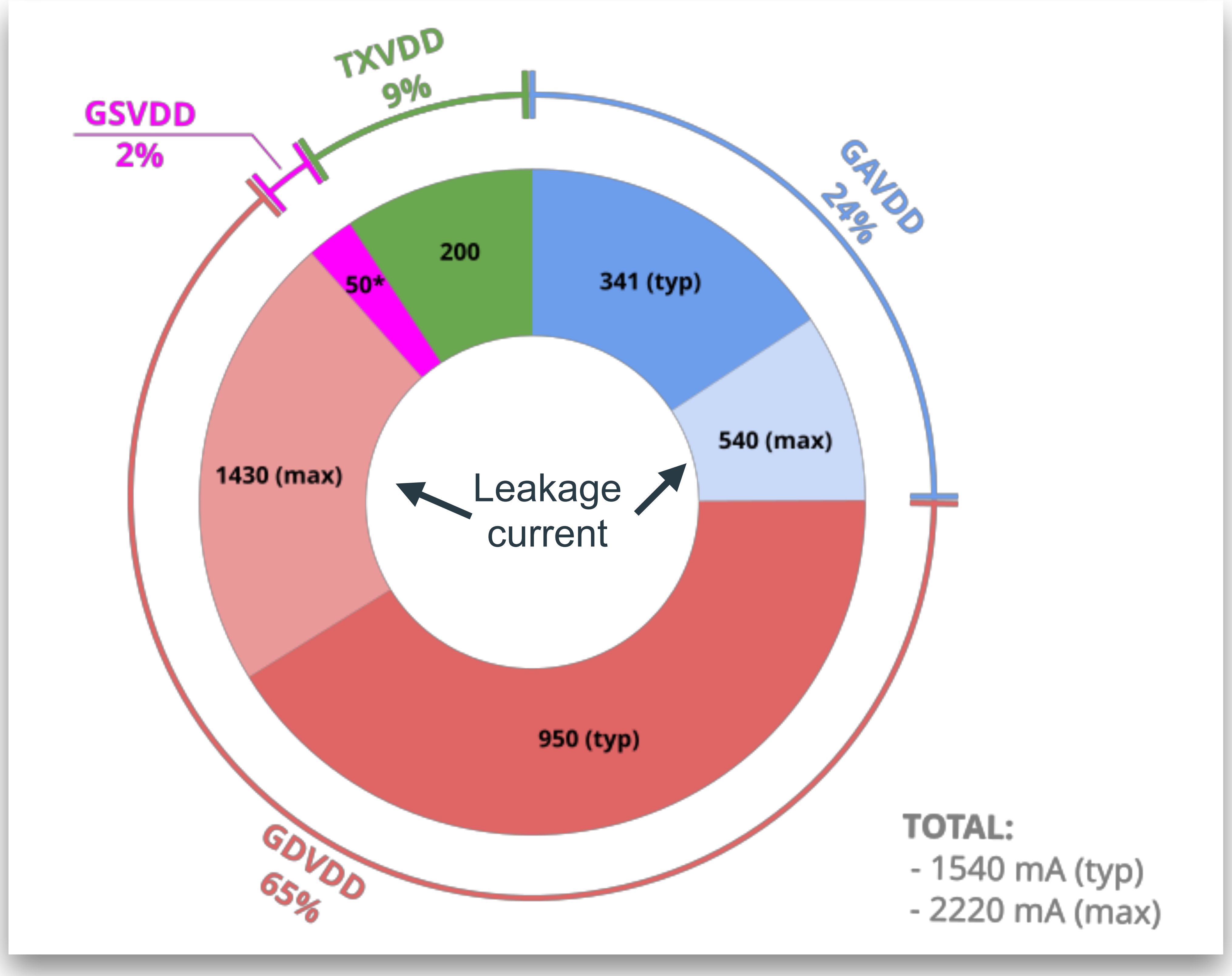
- Significant leakage
  - Large variations with process and temperature
  - Mitigation e.g. w/ custom low-leakage standard cell library



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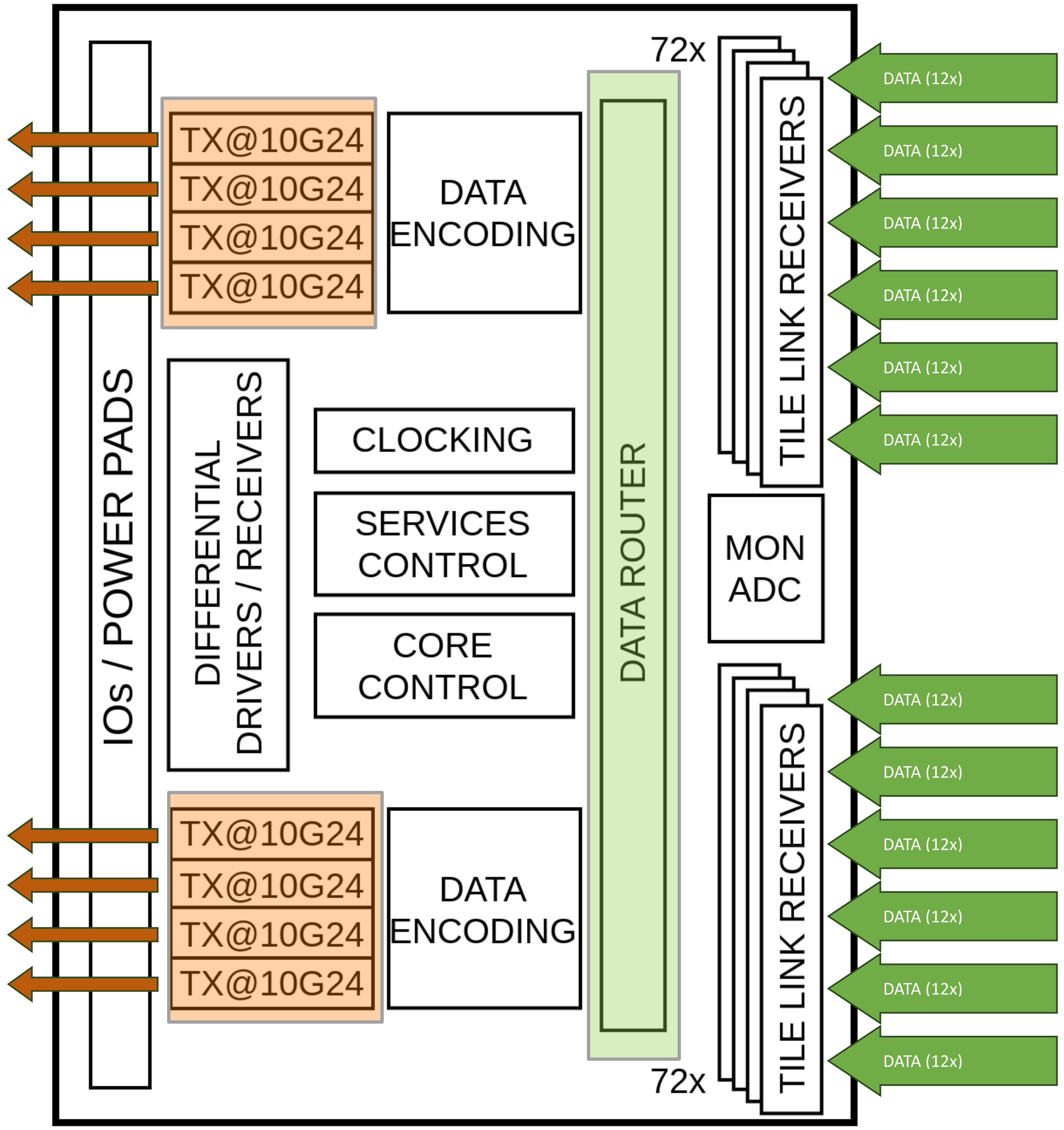
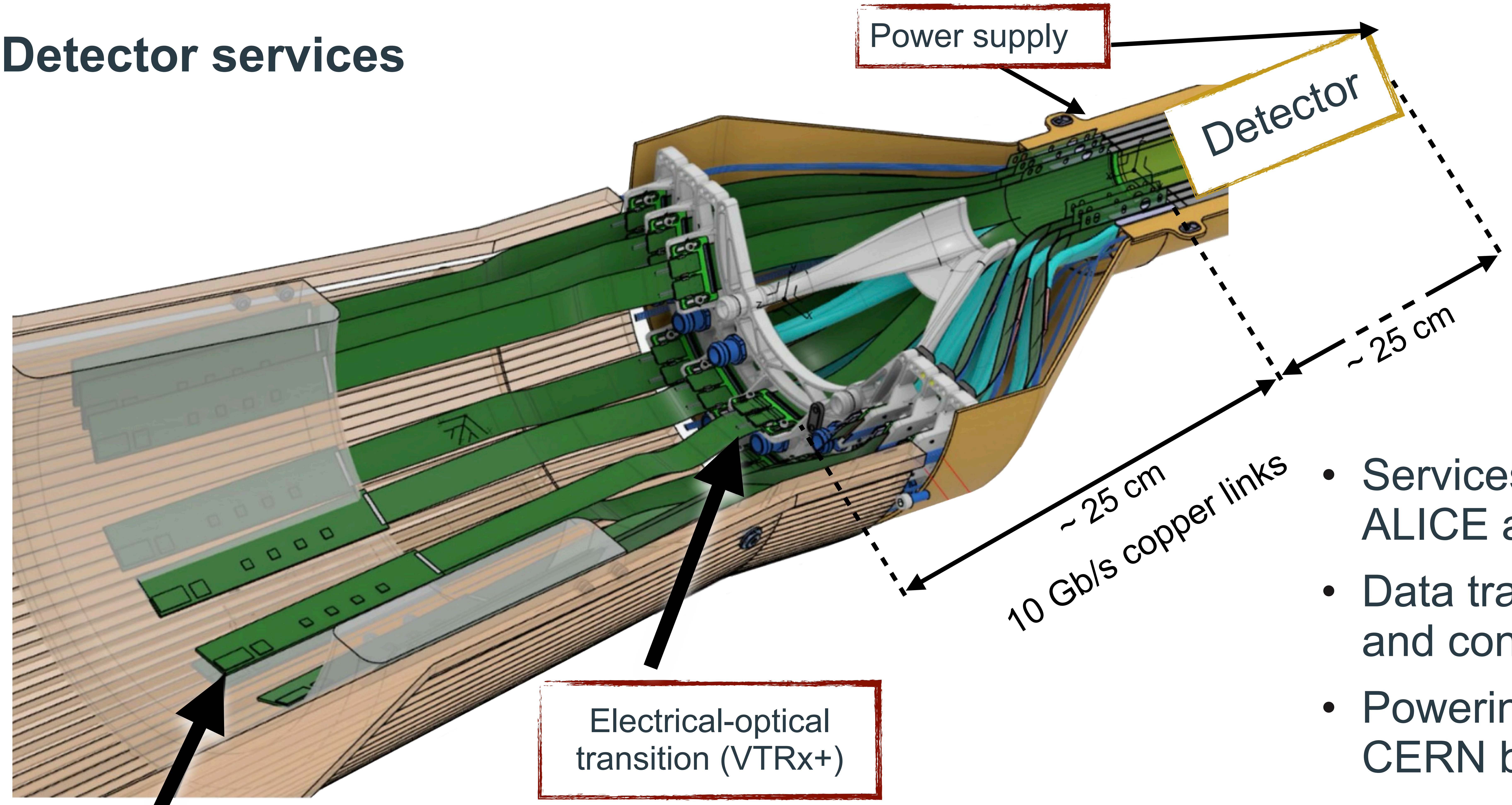
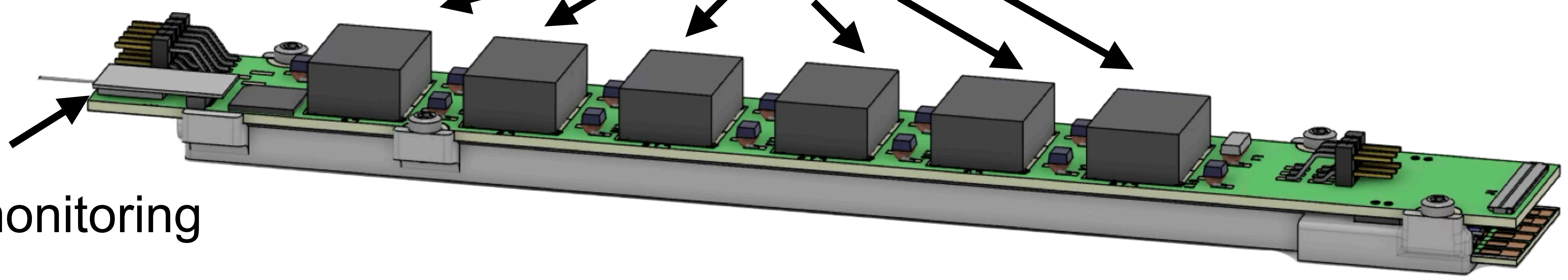
  - Complex segmentation in many independent domains (tiles)
  - Switches and cross-domain signalling and protections
- Significant leakage
  - Large variations with process and temperature
  - Mitigation e.g. w/ custom low-leakage standard cell library
- Data transmission
  - Integrate 144 on-chip transmission lines of 25 cm working at 160 Mb/s
  - High speed (10.24 Gb/s) wireline drivers for off-chip transmission



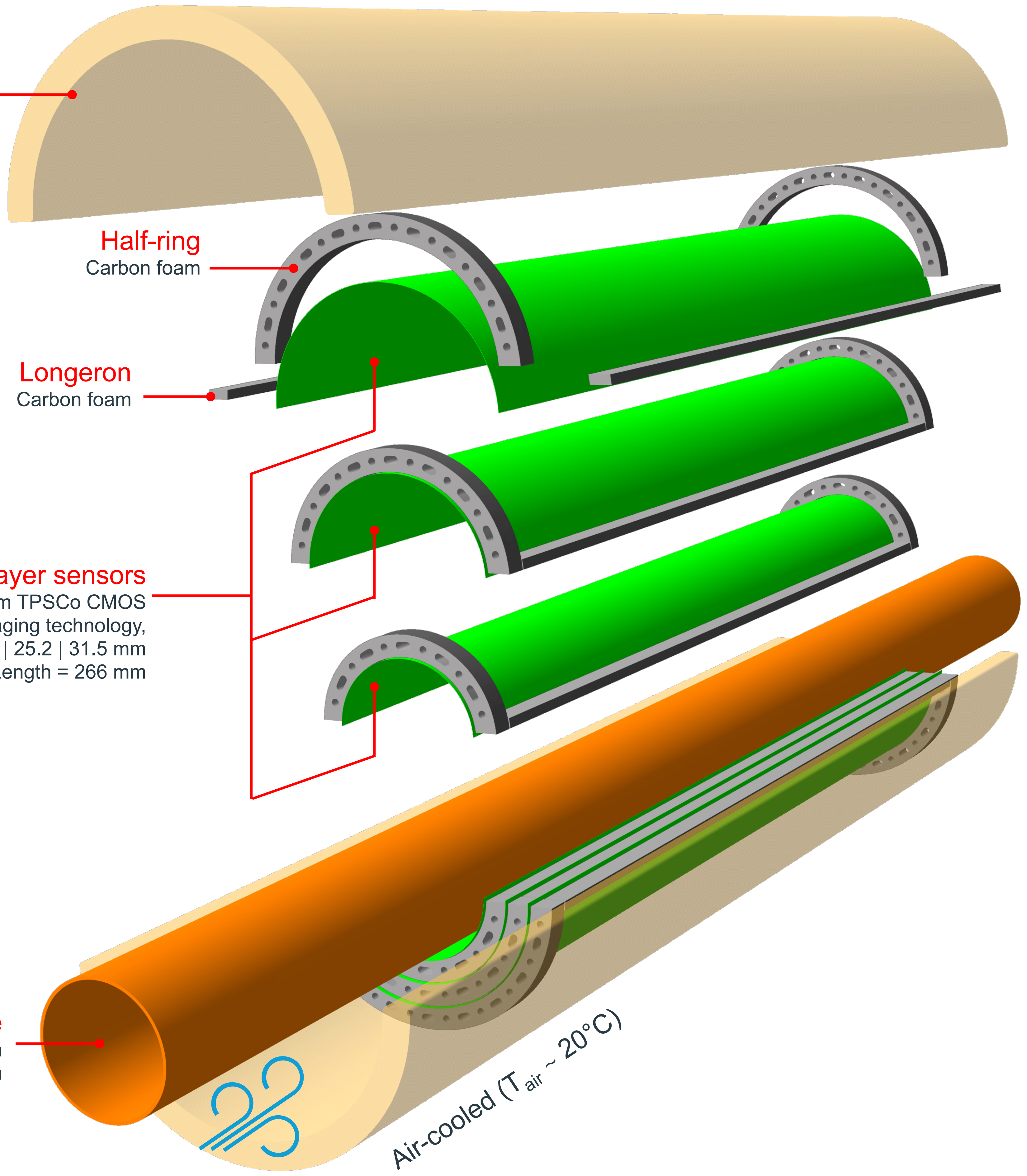
Detector services



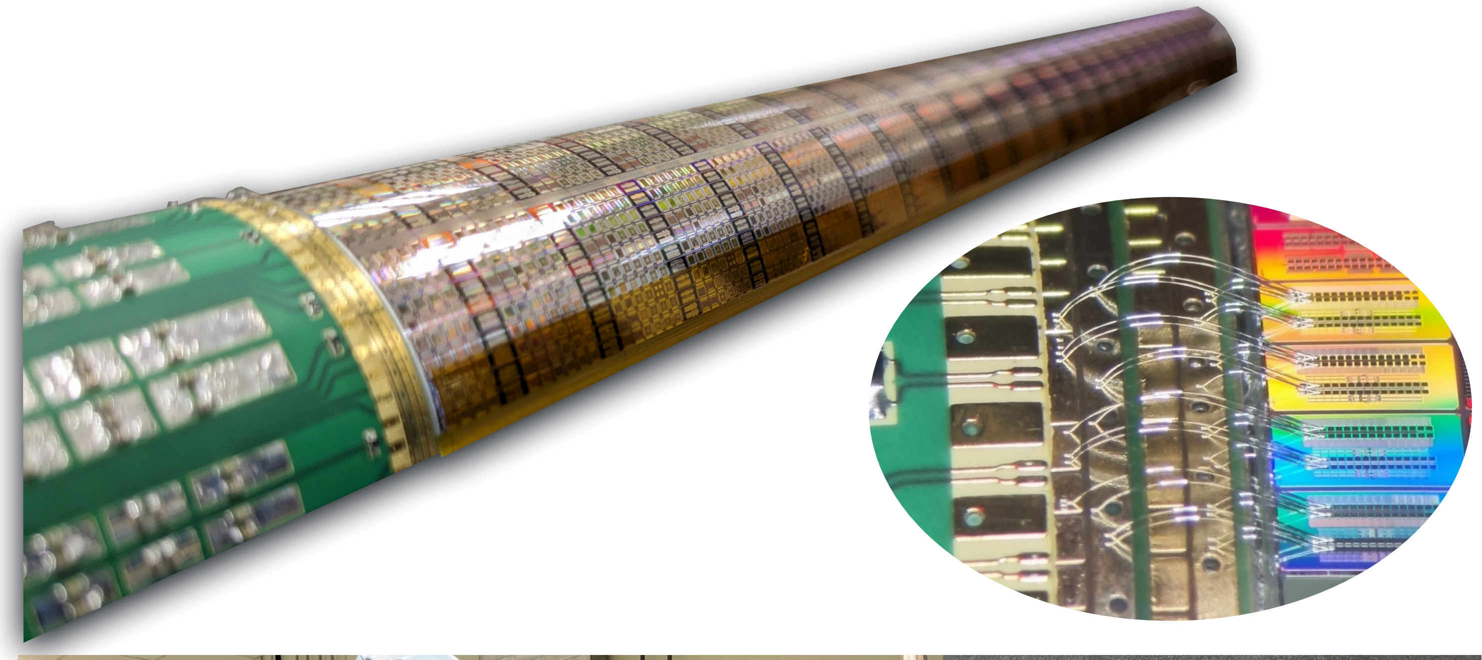
- Services located outside the ALICE acceptance
- Data transmission, monitoring and control: Versatile Link+
- Powering: cascaded CERN bPOL DC-DC converters

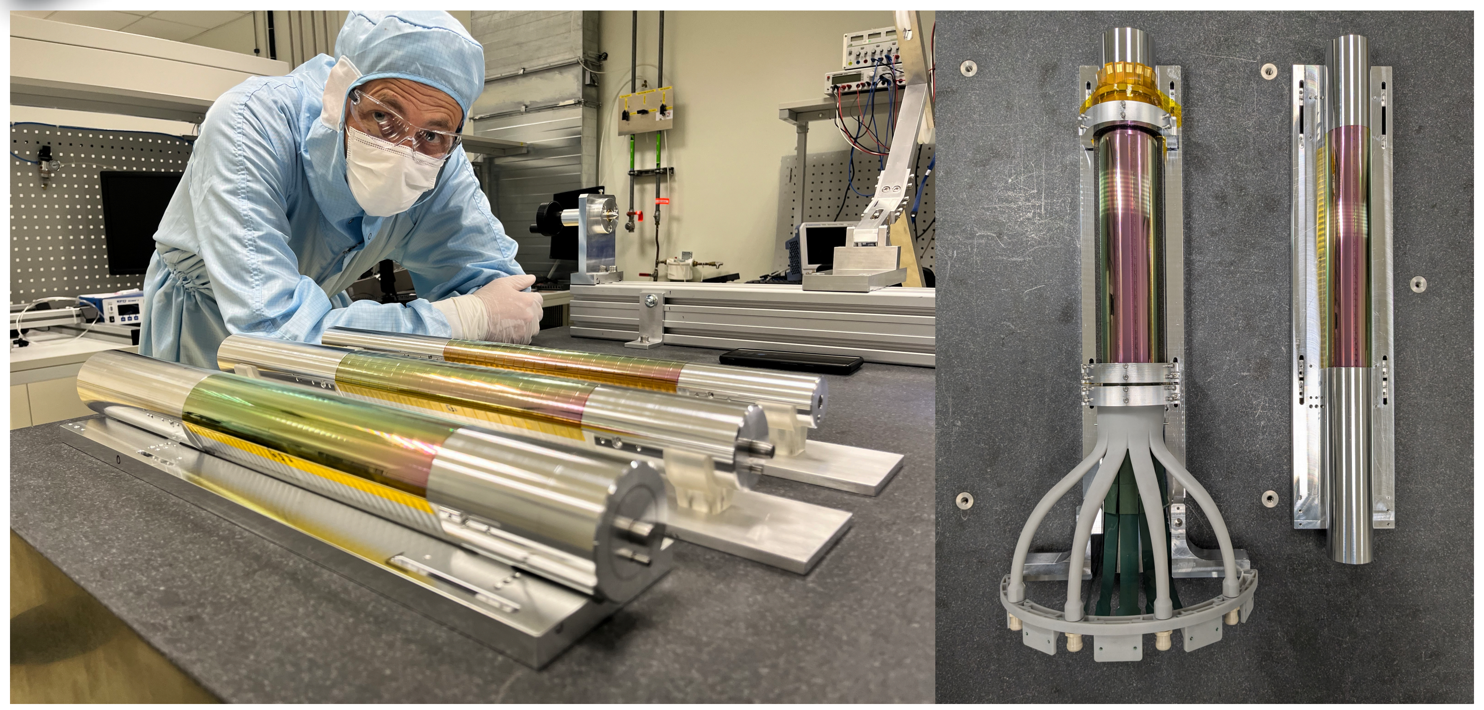


Mechanics and assembly

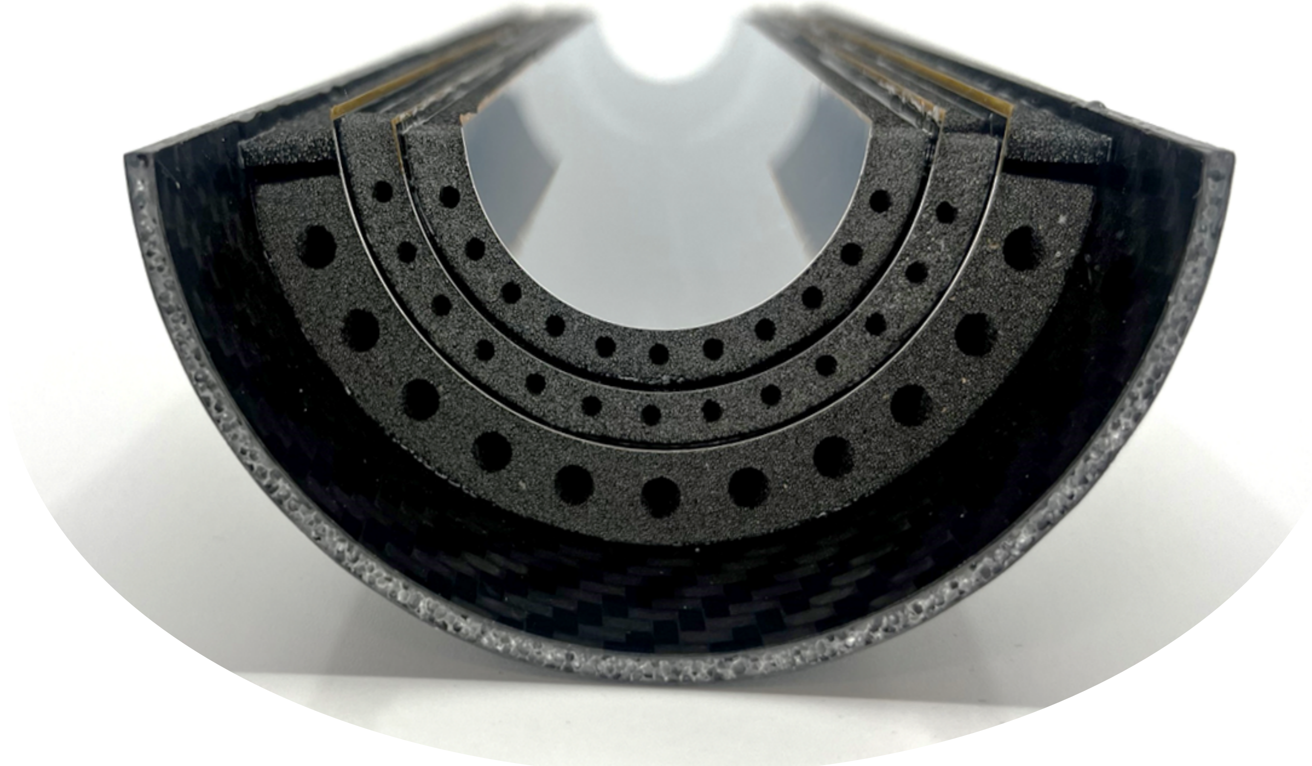


Simplified drawing schematic of the ALICE ITS3





Models based on MLR-1 wafers including FPCs and wire boding

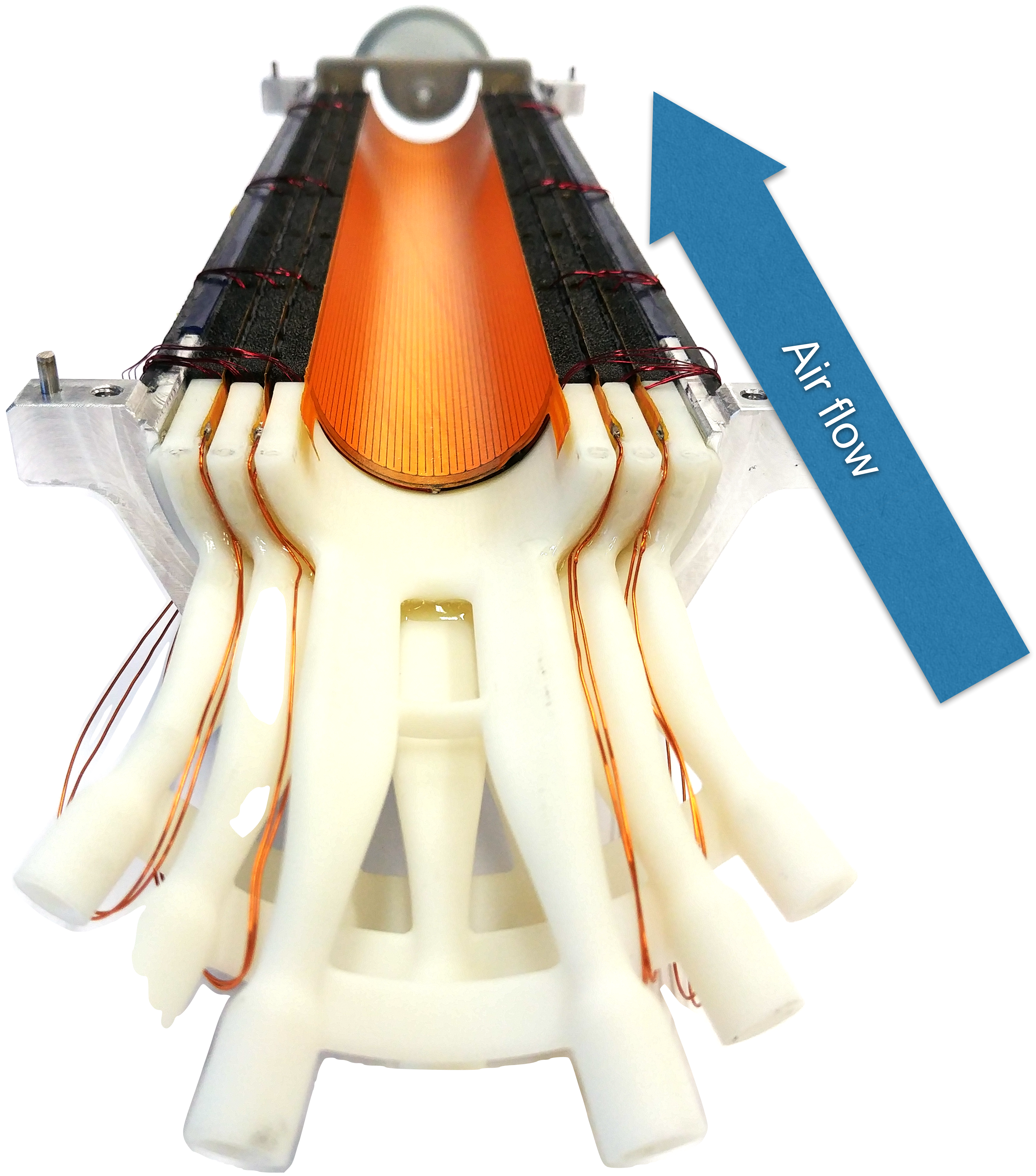


Model for thermal and thermoelastic testing

- Mechanics prototyped and studied with various models
- Next **model based** based on ER-2 pixel sensors and final design

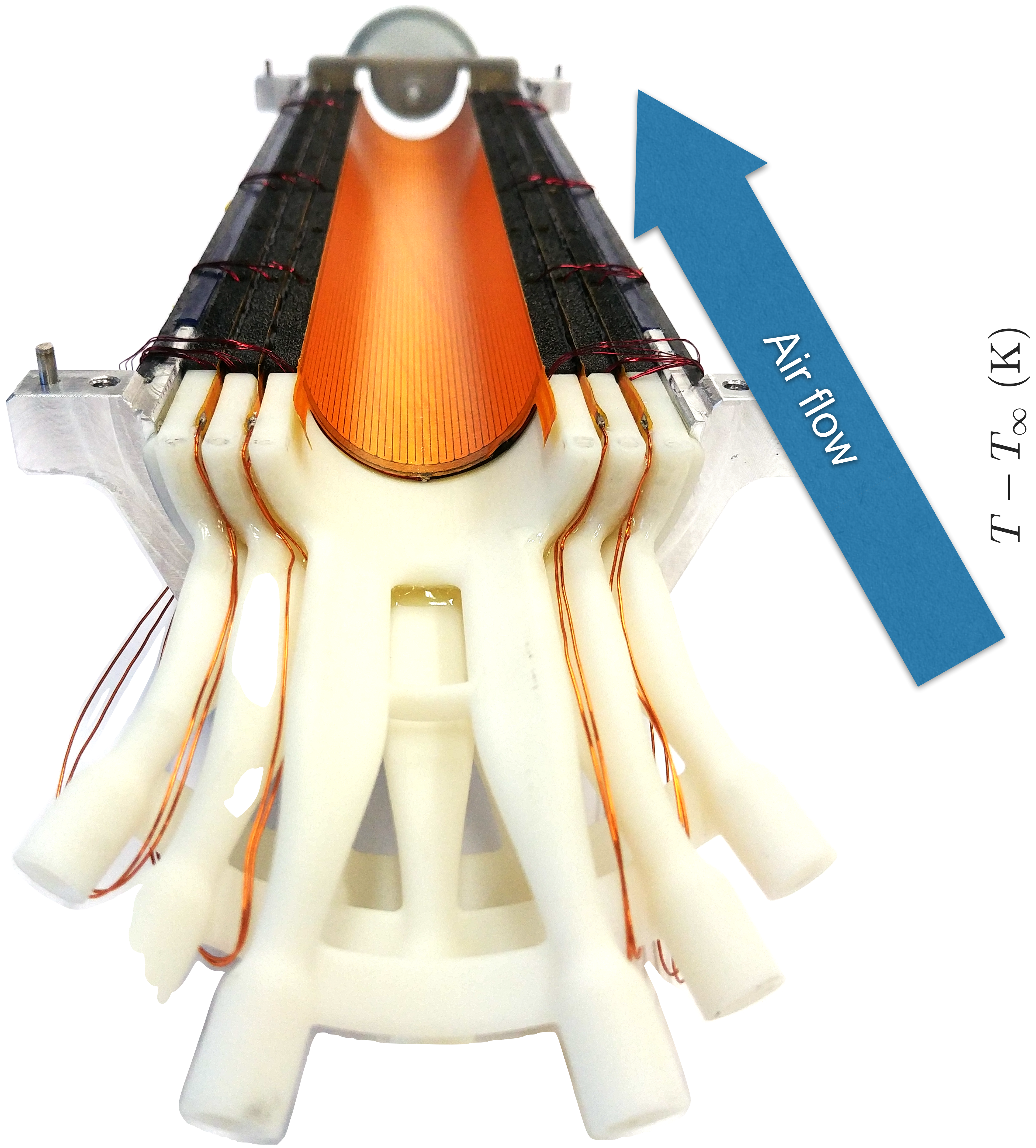
➡Validation of **layout**, **assembly jigs** and **procedure** as well as **installation minimum clearances**

Mechanics and assembly — air cooling



Model for thermal studies with temperature sensors and heaters

Mechanics and assembly — air cooling



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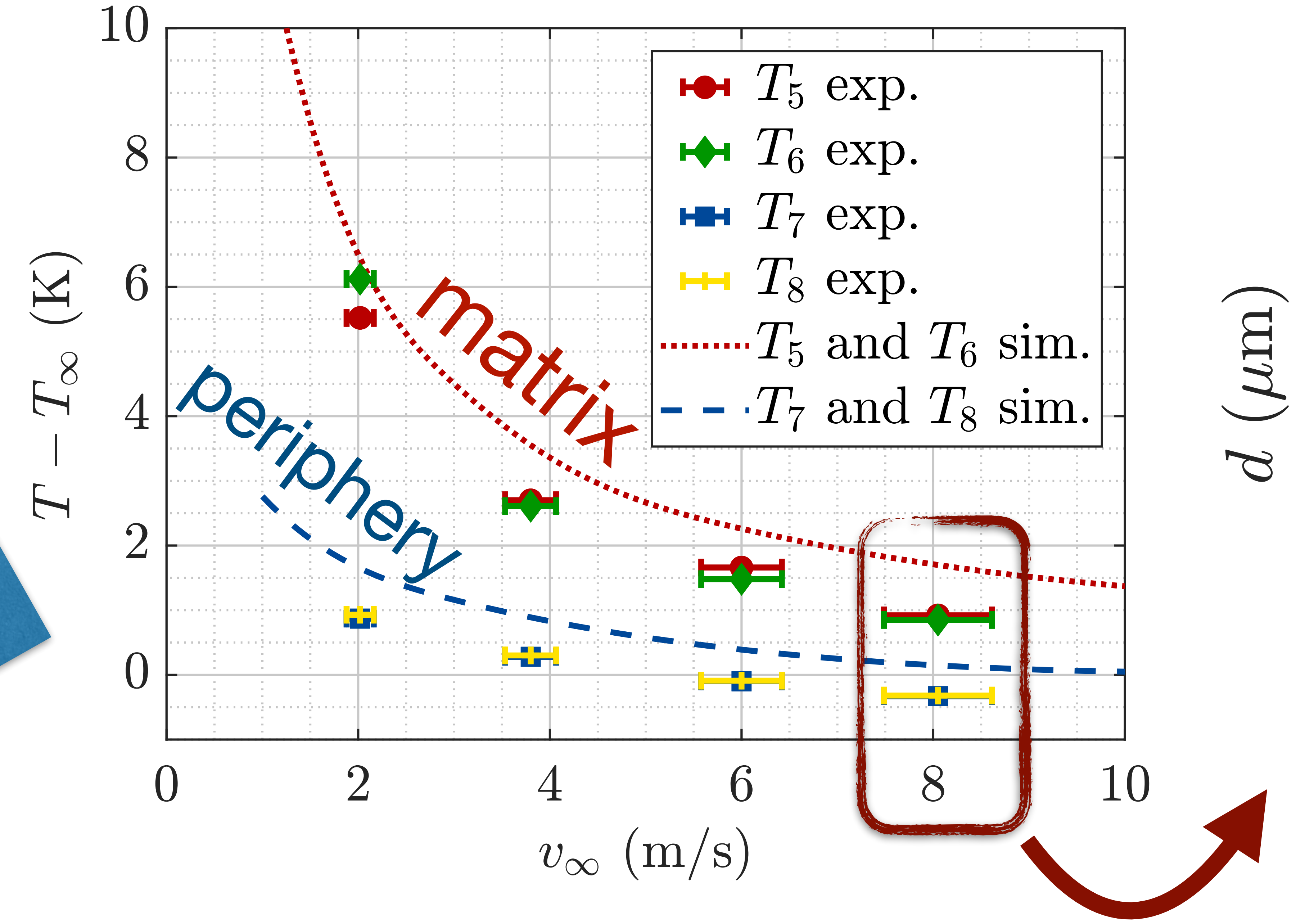
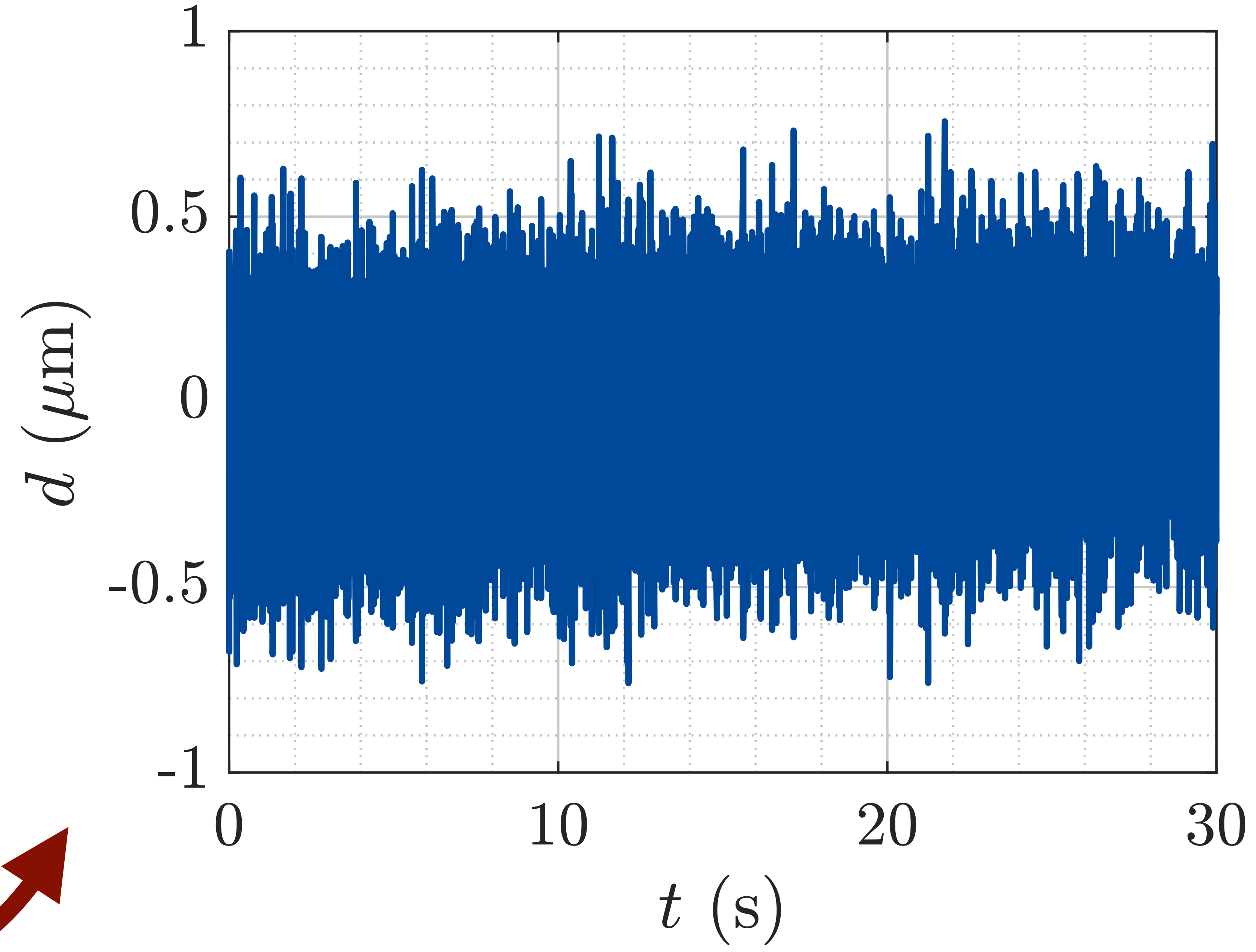


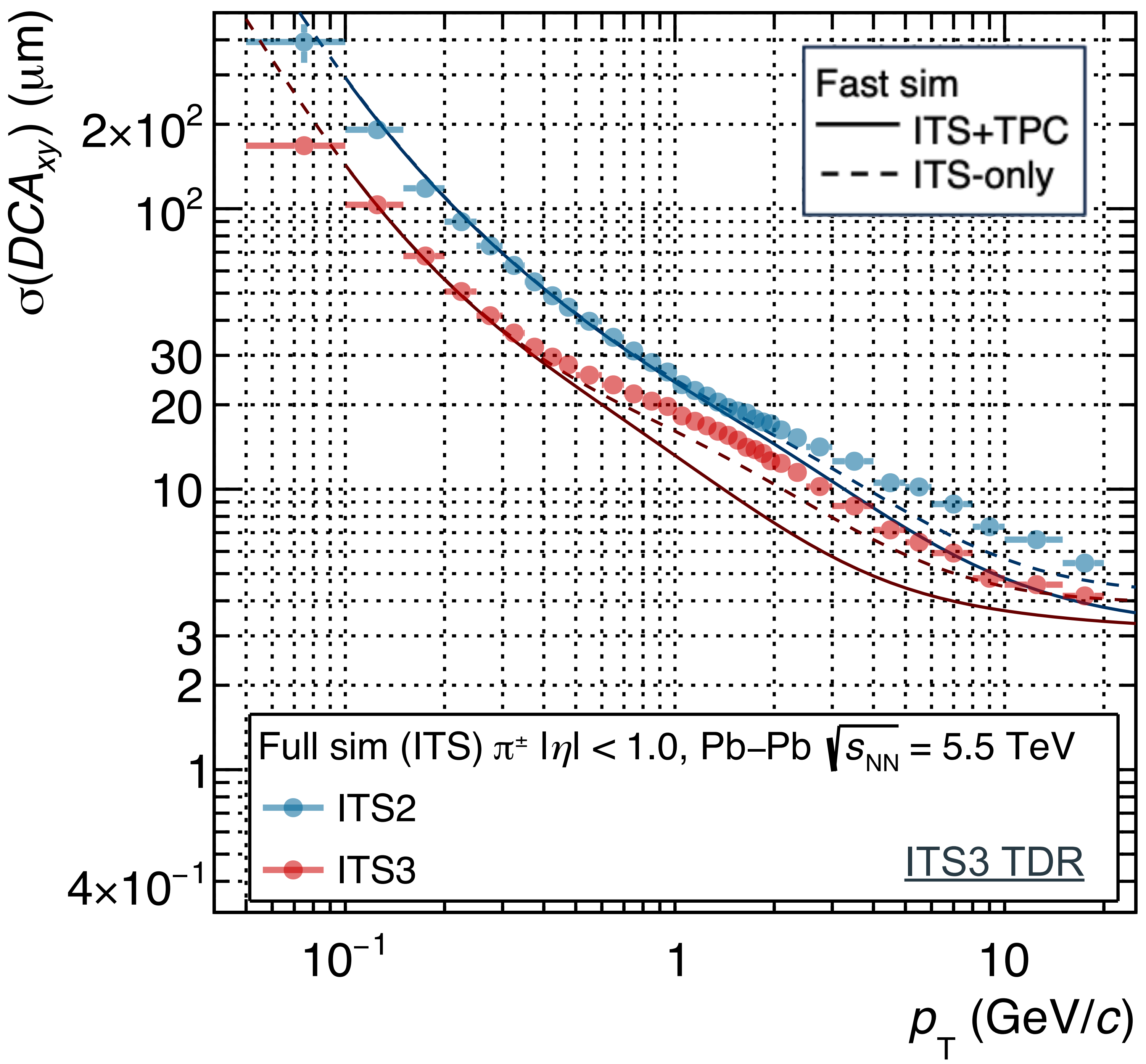
Temperature increase



Vibrations, layer center at 8 m/s

Very good results with quite some margin!

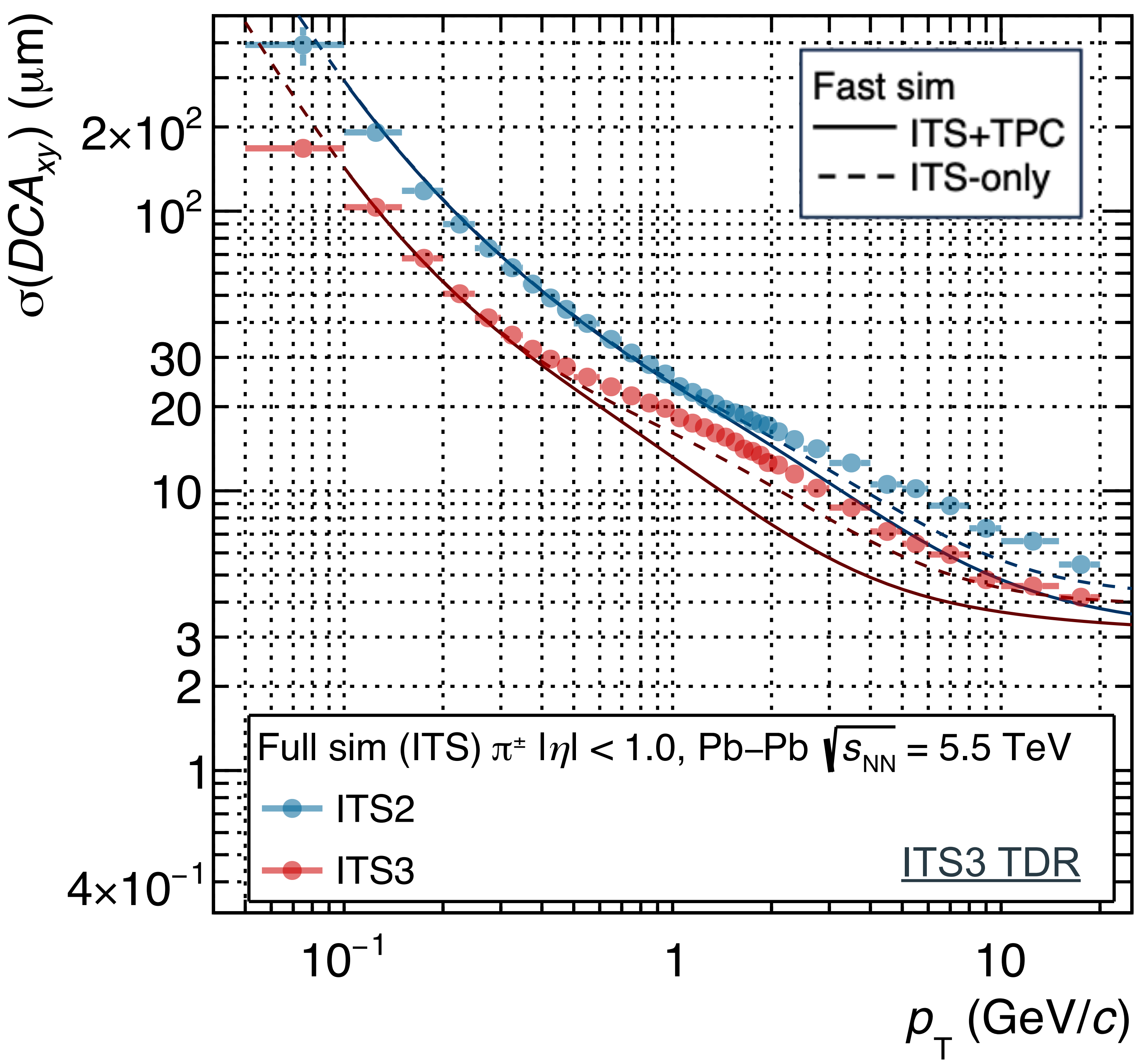
Physics impact



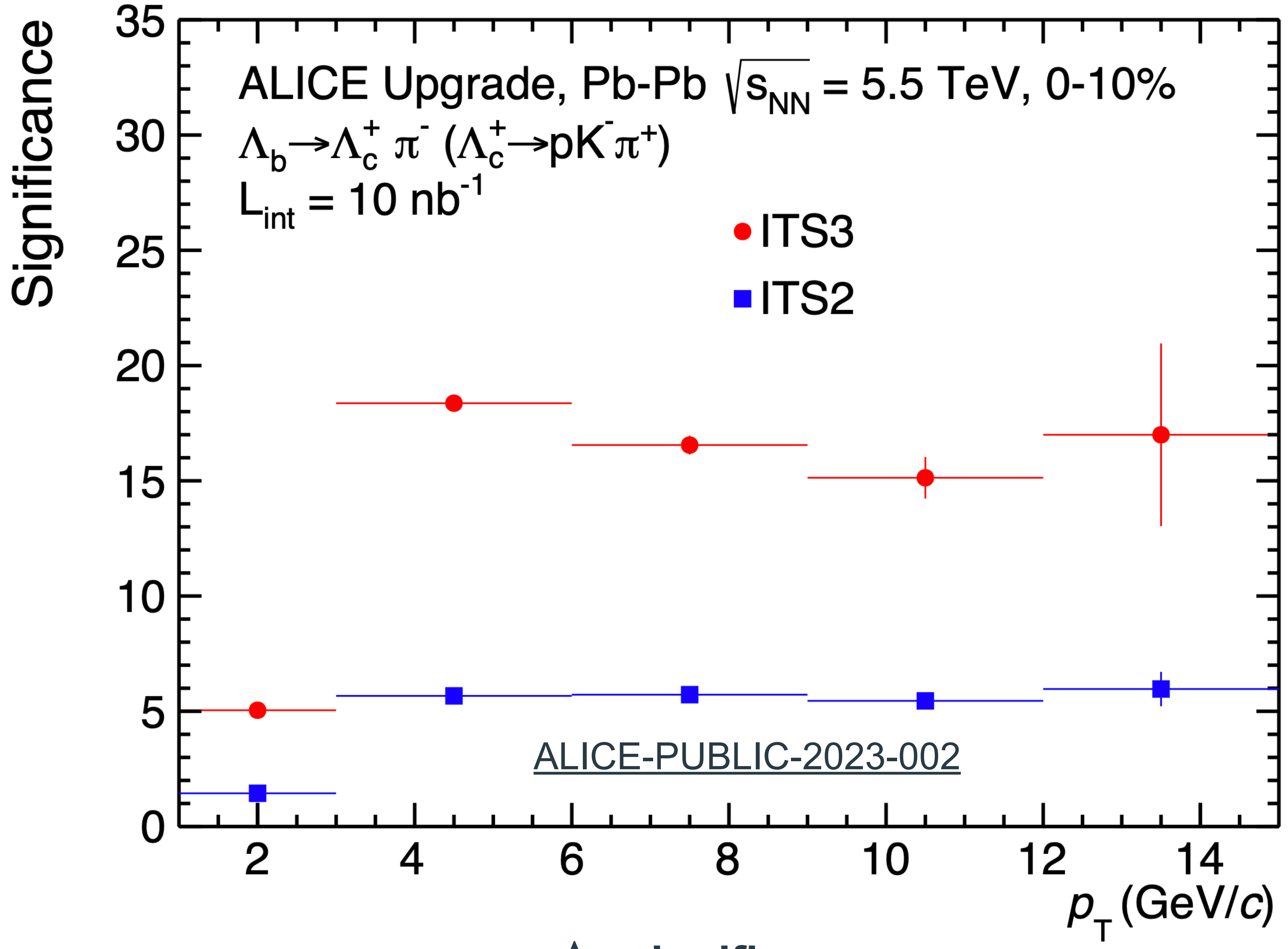
Impact parameter resolution

- DCA resolution improved by a about a factor of 2 → improved separation of secondary vertices

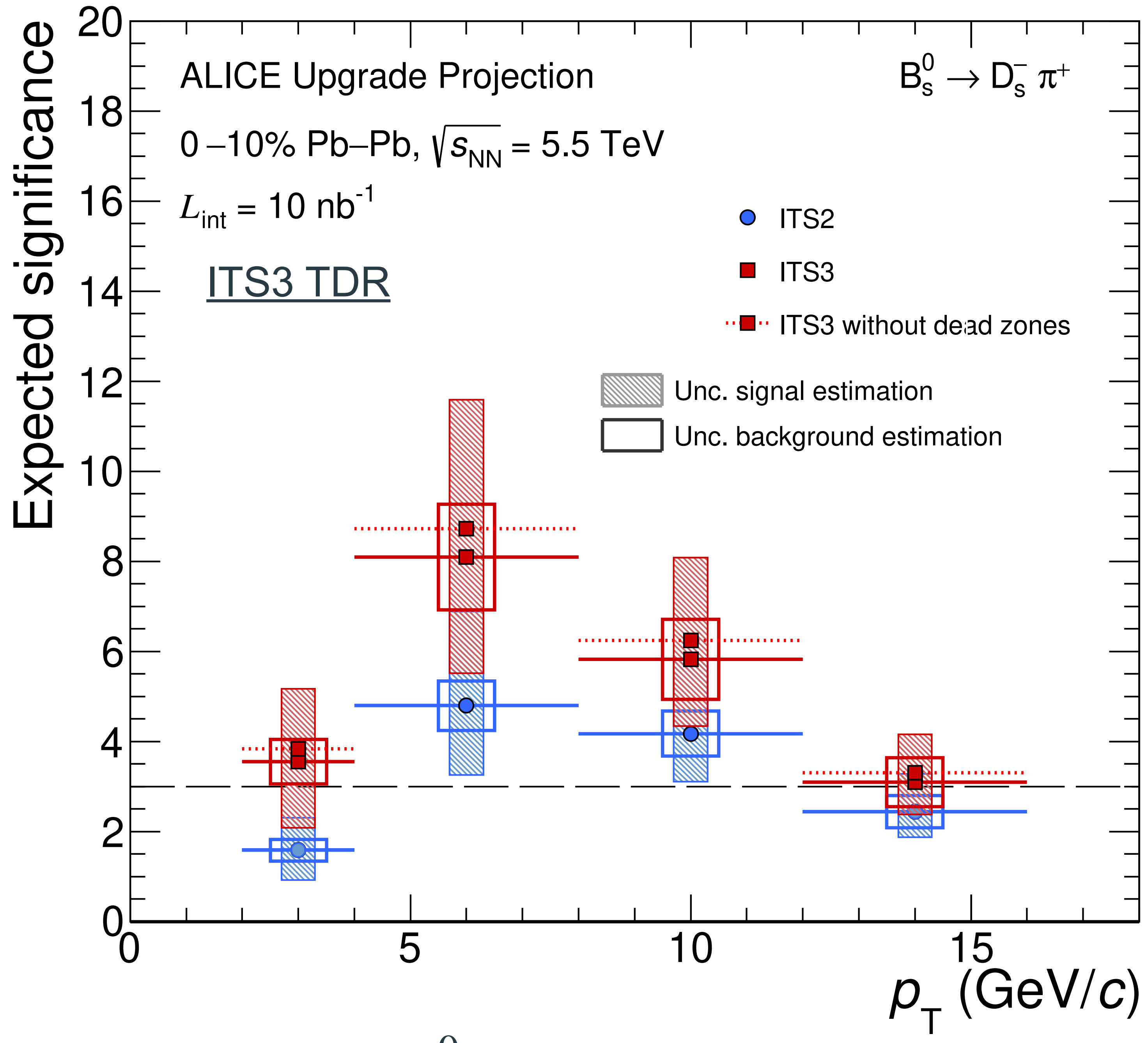
Physics impact



Impact parameter resolution



Λ_b significance



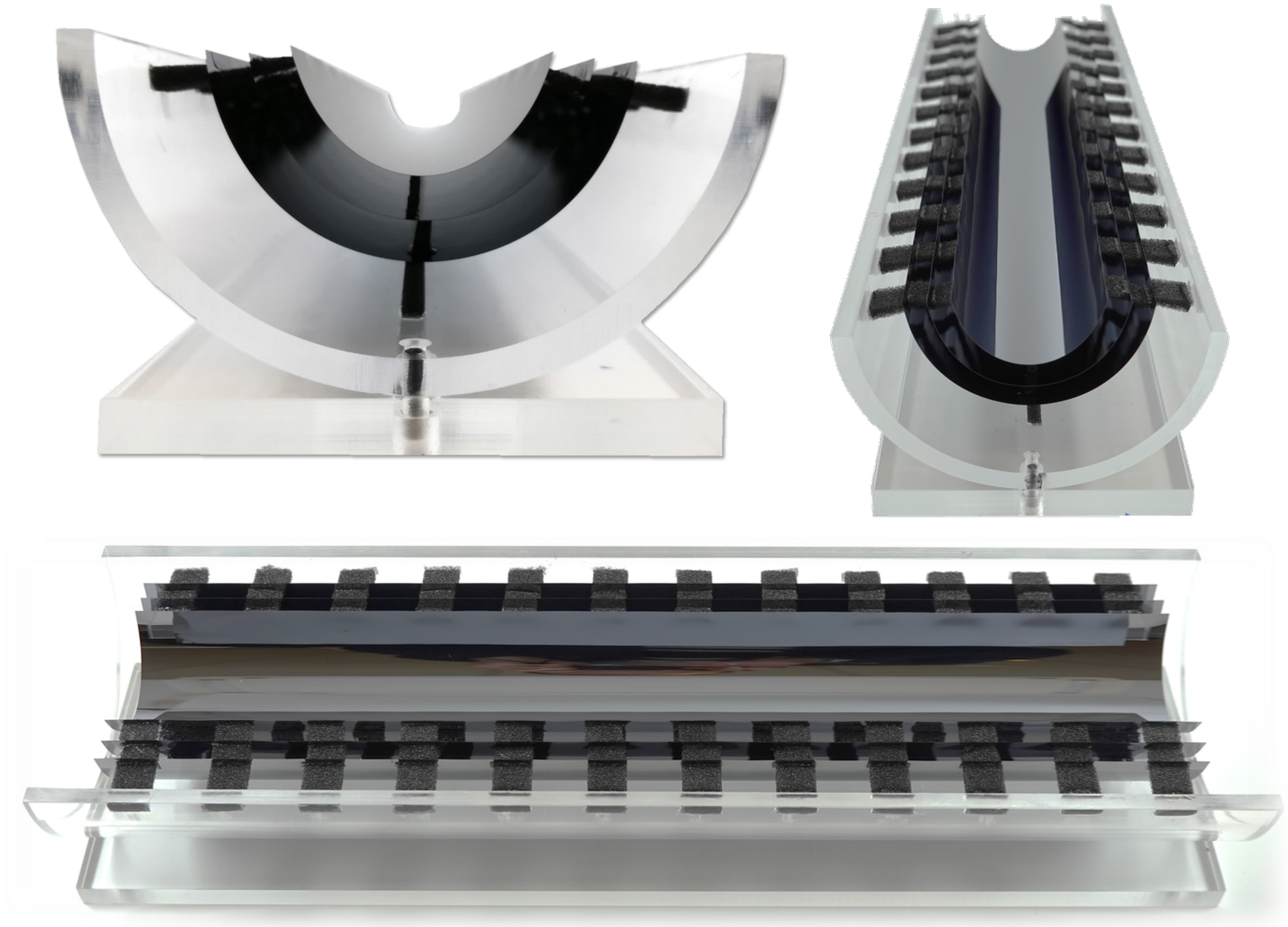
B_s^0 significance

- DCA resolution improved by a about a factor of 2 → improved separation of secondary vertices
- Many fundamental observables strongly profiting or becoming in reach
  - Charmed and beauty baryons
  - Low-mass di-electrons
  - Full topological reconstruction of B_s

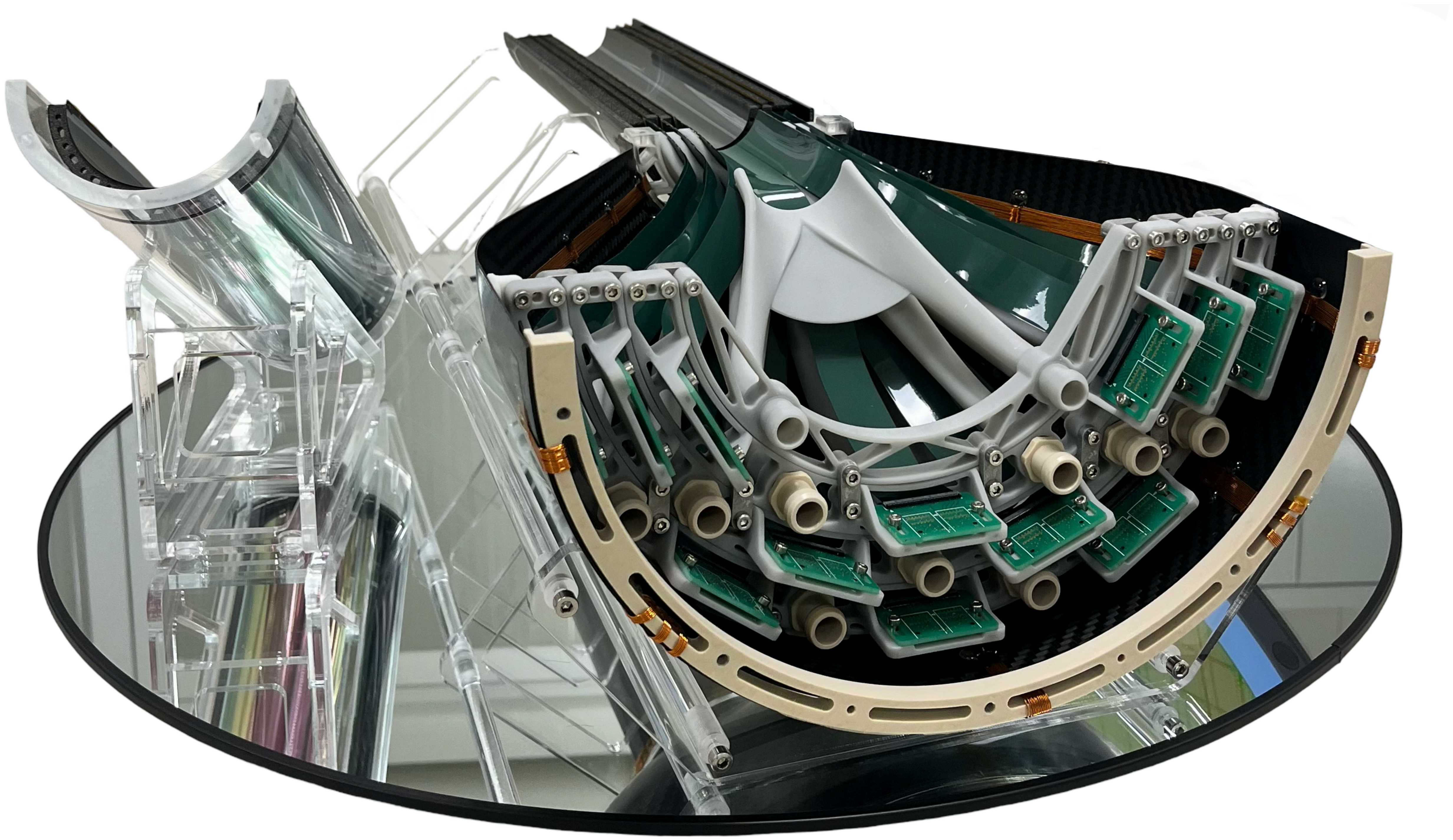
ITS3 physics performance studies: ALICE-PUBLIC-2023-002

Summary

- ITS3 pioneers of bent, wafer-scale MAPS
  - Small inner radius: 19 mm
  - Low average material budget: 0.09% X_0 / layer
- Wafer-scale MAPS feasibility demonstrated with ER-1
  - Detection efficiency and fake-hit rate sufficient
  - Yield studied in detail
- MOSAIX to be submitted in ER-2 in early 2025
  - Full-size, full functionality
  - High segmentation to improve yield
- ITS3 services based on Versatile Link+ and bPOL
- Mechanics design well advanced
  - Assembly procedure and design studied in various models
  - Air cooling demonstrated, vibrations with in 1 µm peak-to-peak
  - Final design models to be built from ER-2 pixel chips



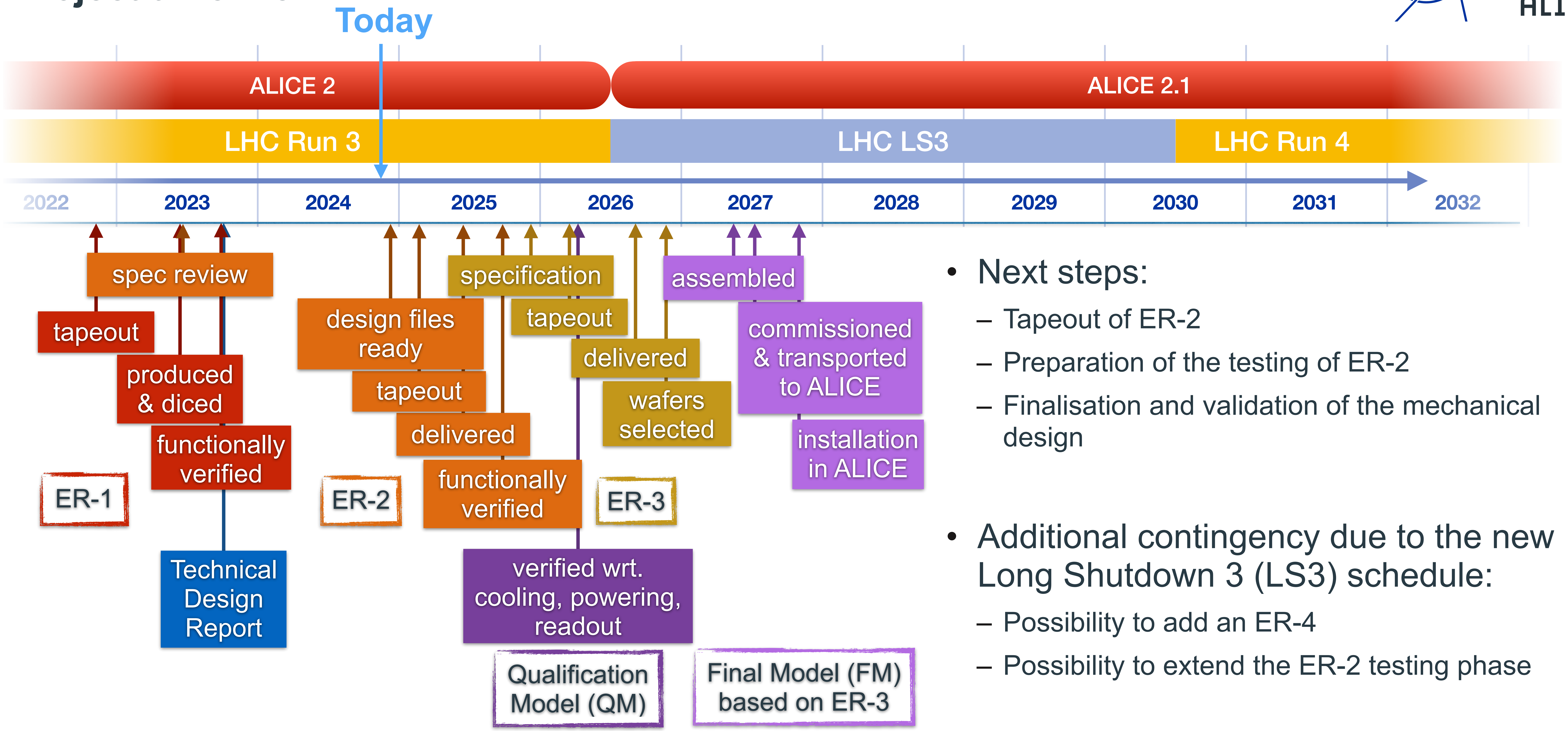
Thanks a lot for your attention!



L. Terlizzi - Characterization of MOSS for the ALICE ITS3 for the LHC Run 4 [Nov 21st, 16:40]
M. Selina - Exploring ALICE ITS3 MOST [Nov 21st, 16:57]
A. Sturniolo - Testing small devices for ALICE ITS3 upgrade [Poster]
A. Lorenzetti - Performance studies of the CE-65v2 MAPS prototype structure [Poster]
I. Sanna - TCAD and charge transport simulations of MAPS in 65nm for the ALICE ITS3 [Poster]
G. Borghello - Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations [Poster]

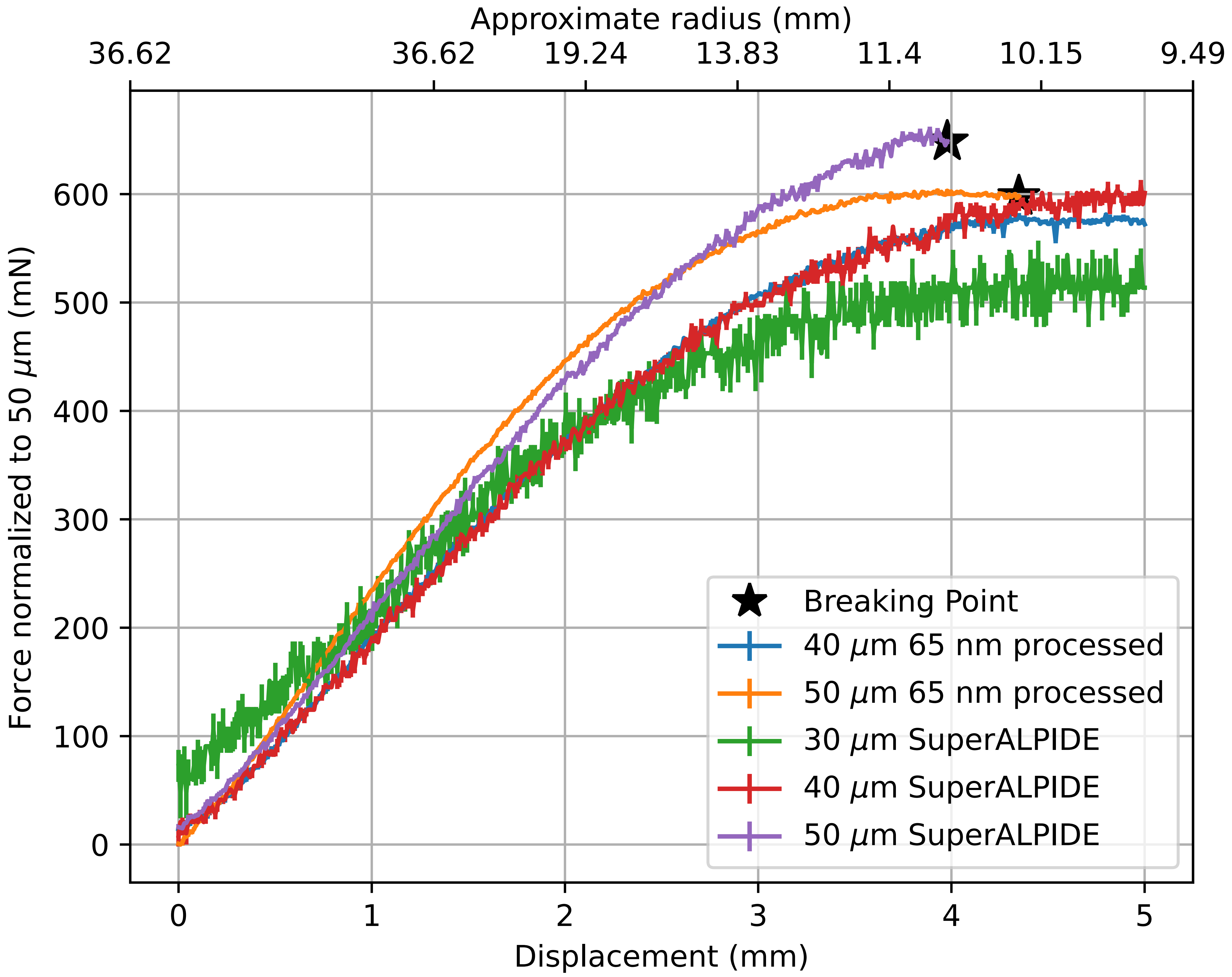
Extra Material

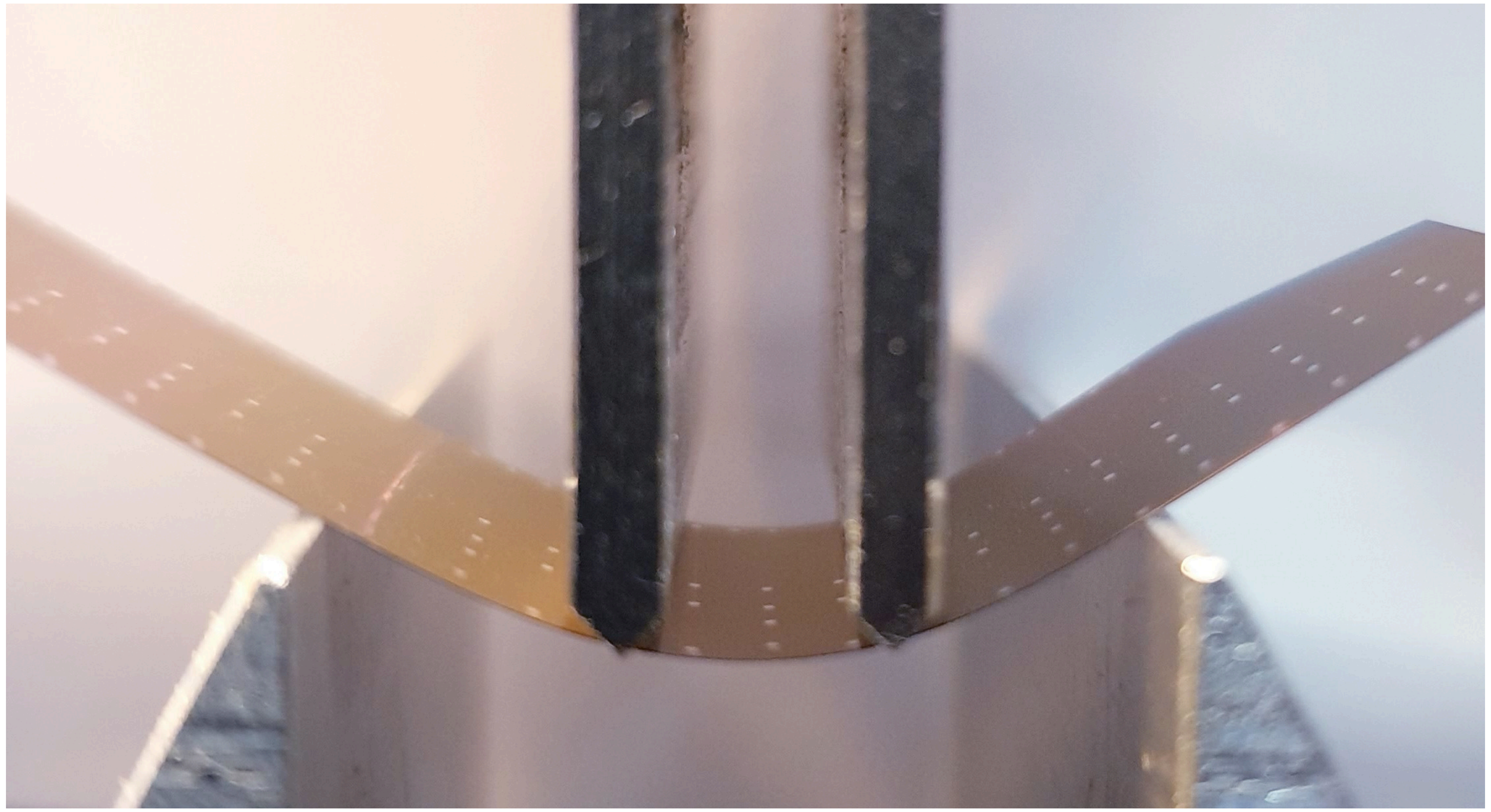
Project timeline



- Next steps:
  - Tapeout of ER-2
  - Preparation of the testing of ER-2
  - Finalisation and validation of the mechanical design
- Additional contingency due to the new Long Shutdown 3 (LS3) schedule:
  - Possibility to add an ER-4
  - Possibility to extend the ER-2 testing phase

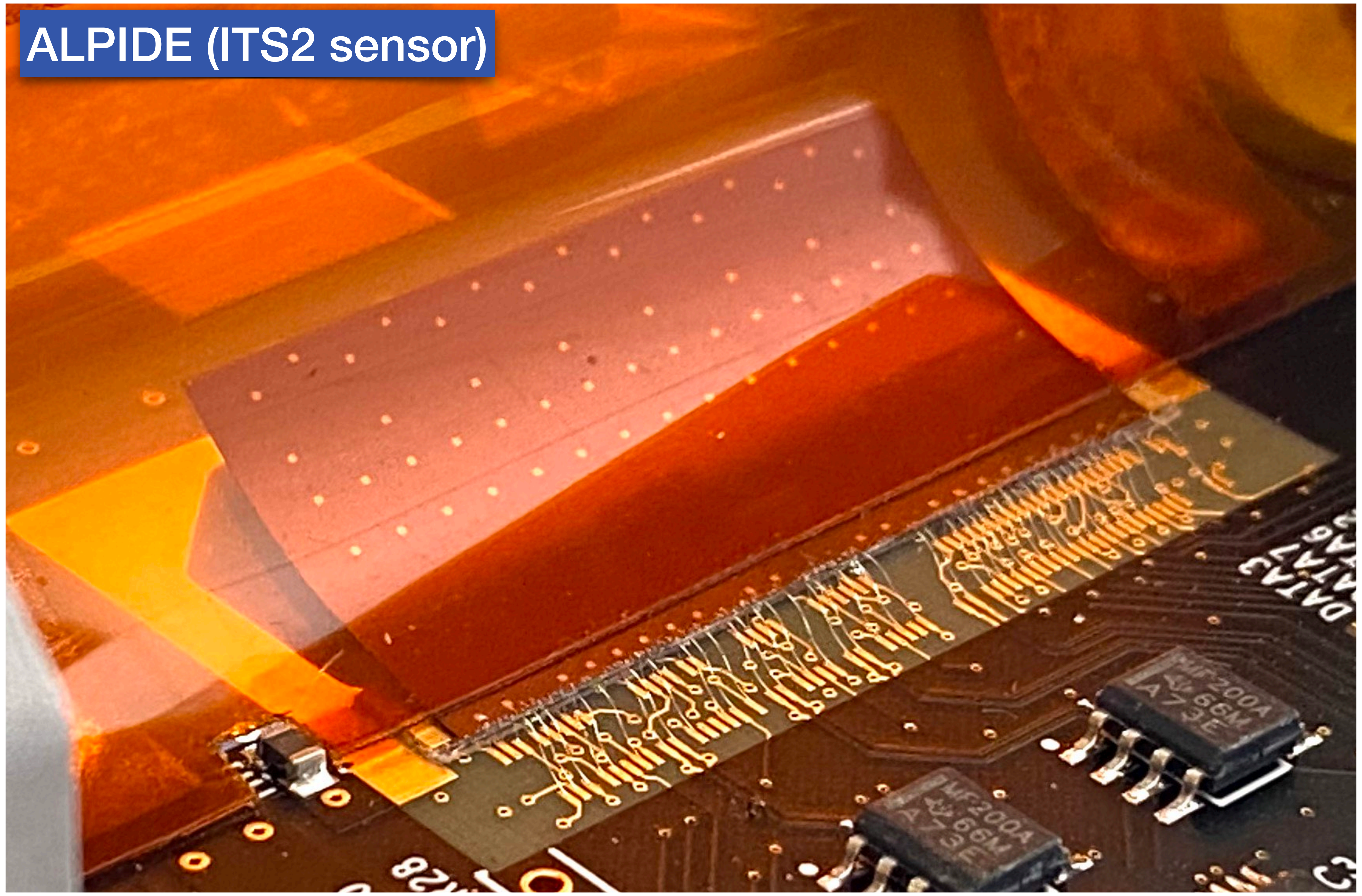
4-point bending tests



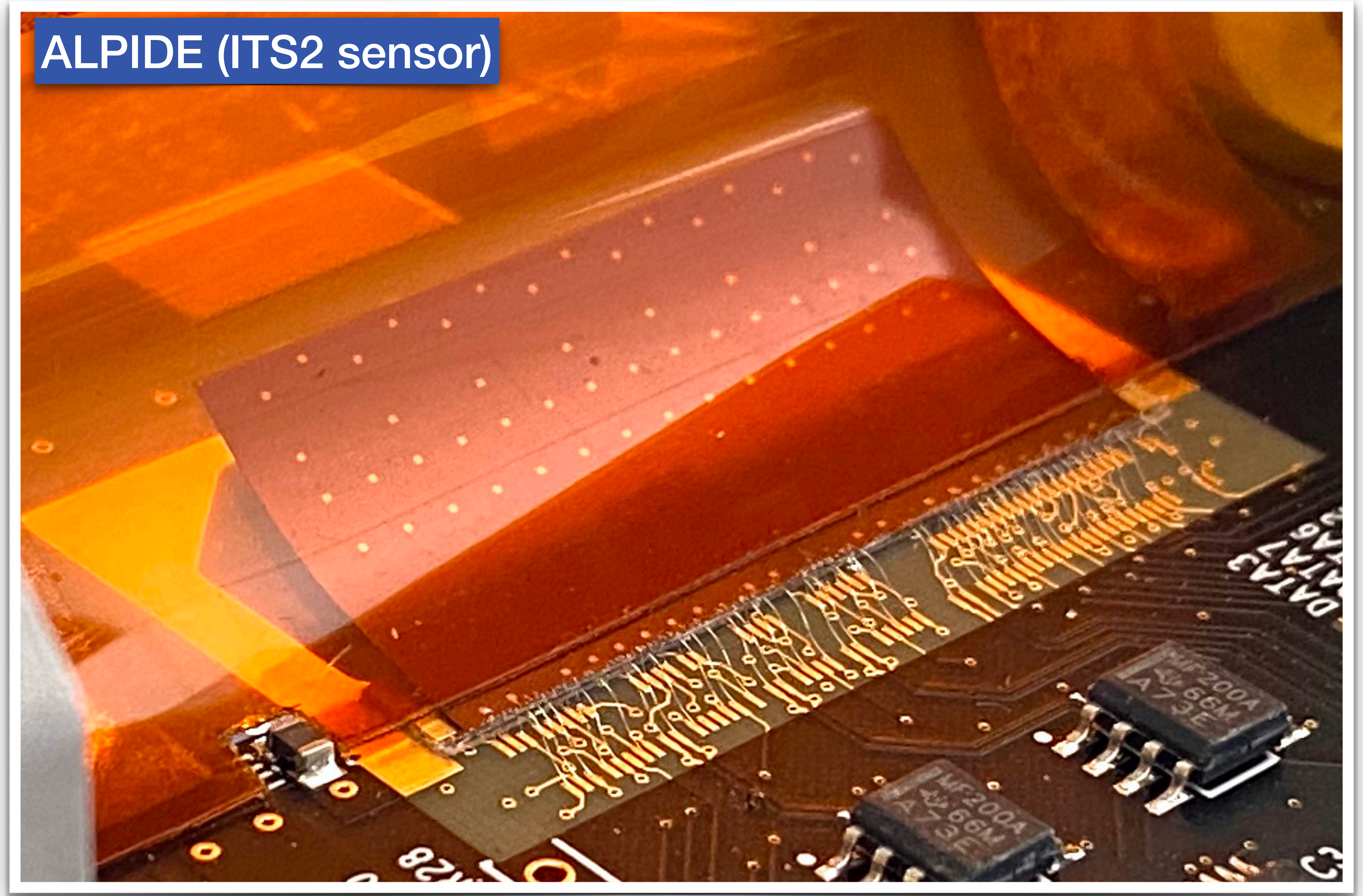


ITS3 TDR — CERN-LHCC-2024-003

Bent MAPS in beam tests



Bent MAPS in beam tests



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Abstract

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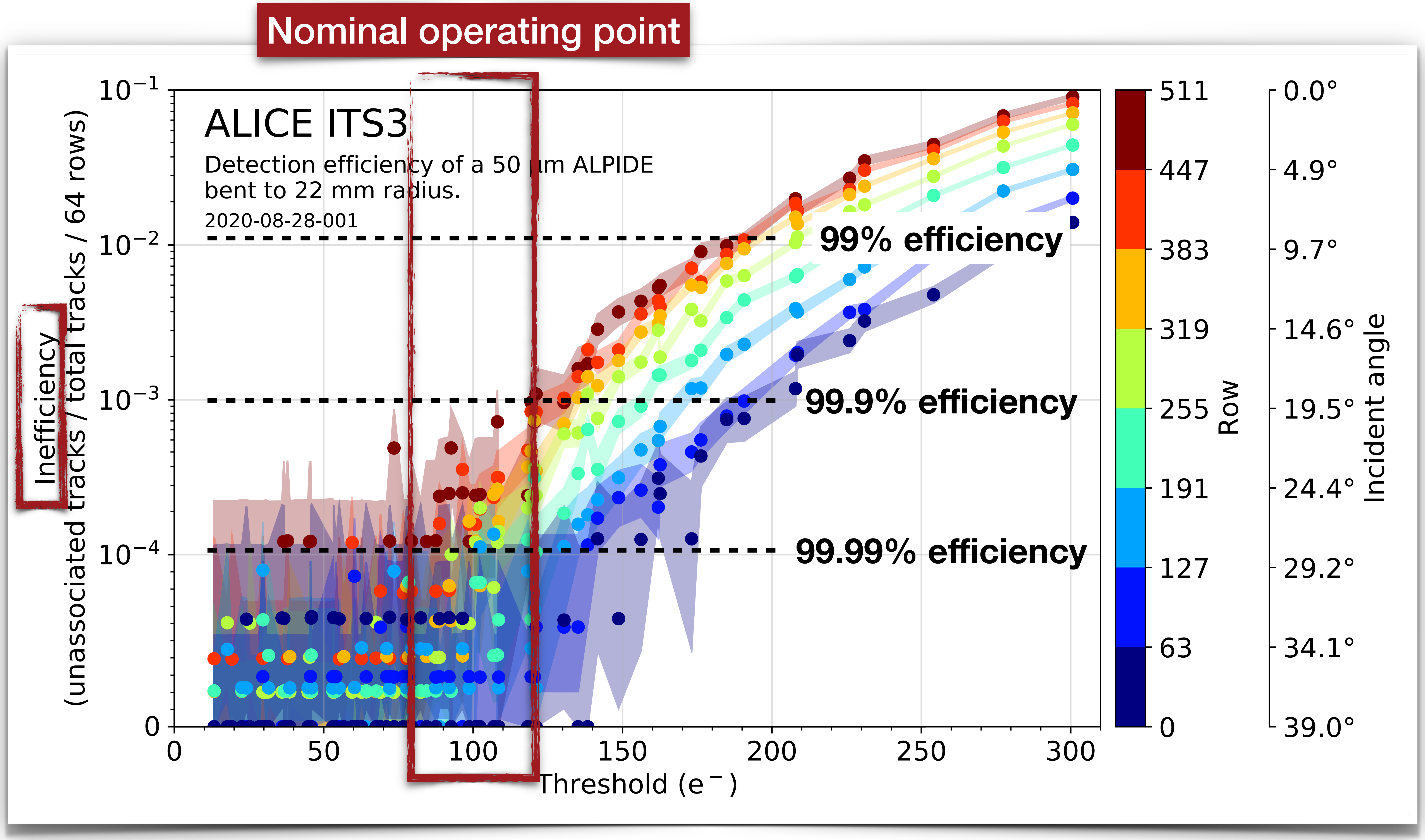
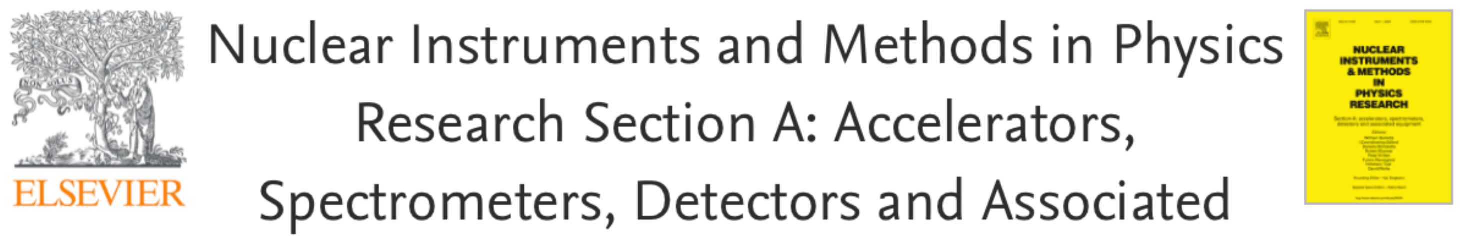
Bent MAPS in beam tests

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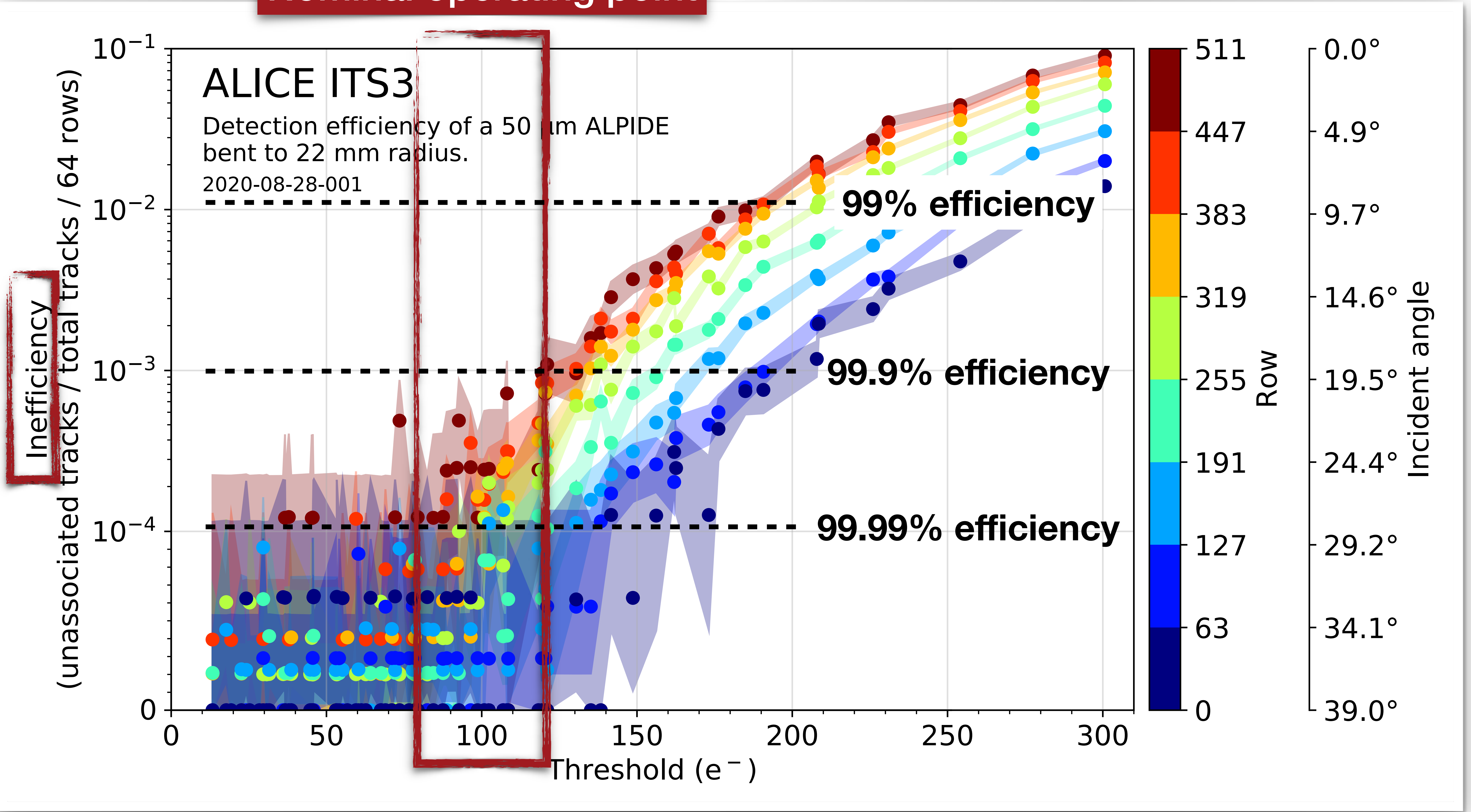
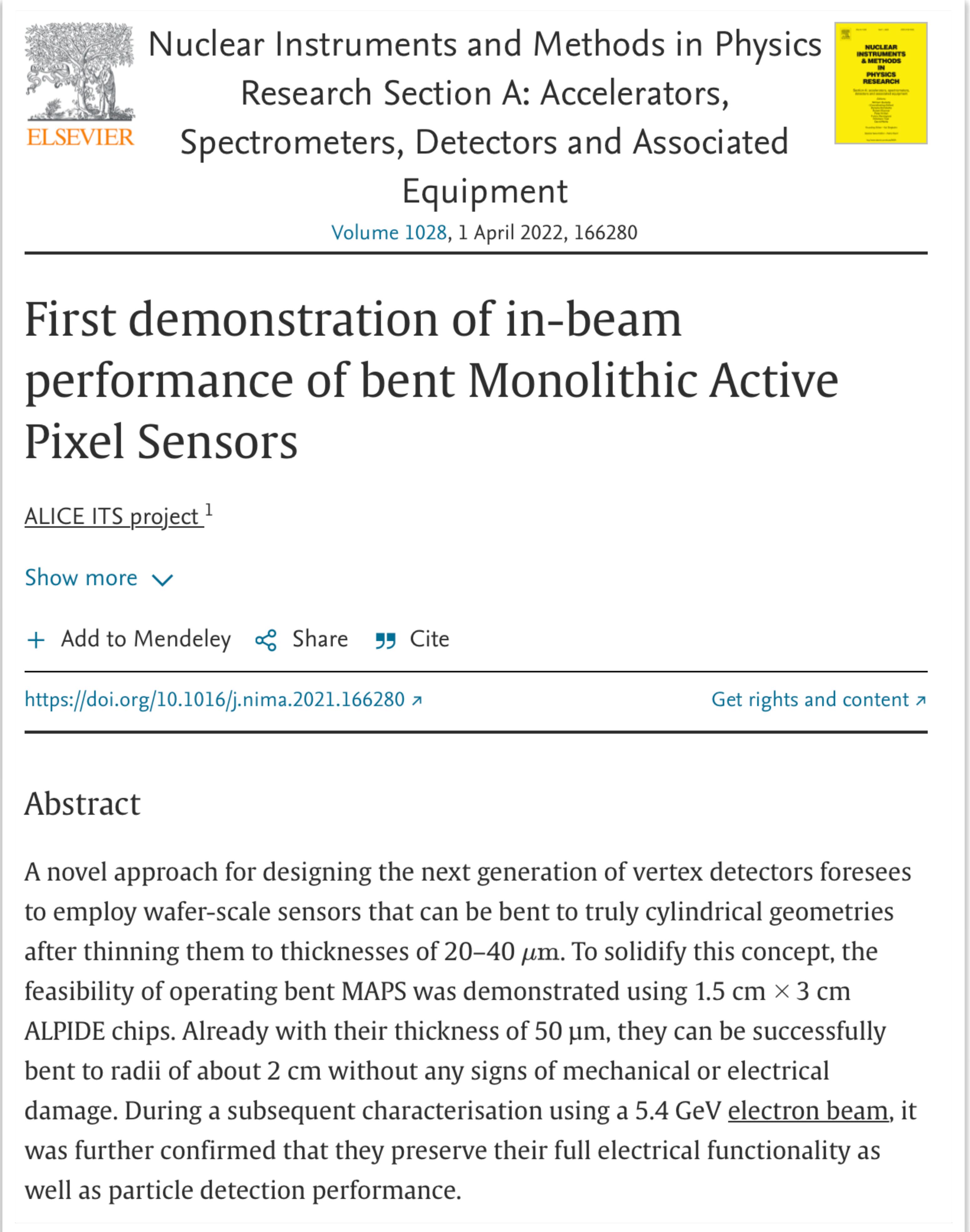
Bent MAPS in beam tests

Nominal operating point





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Clearly proving that bent MAPS are working!

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