CMS Phase-II Inner Tracker System Tests

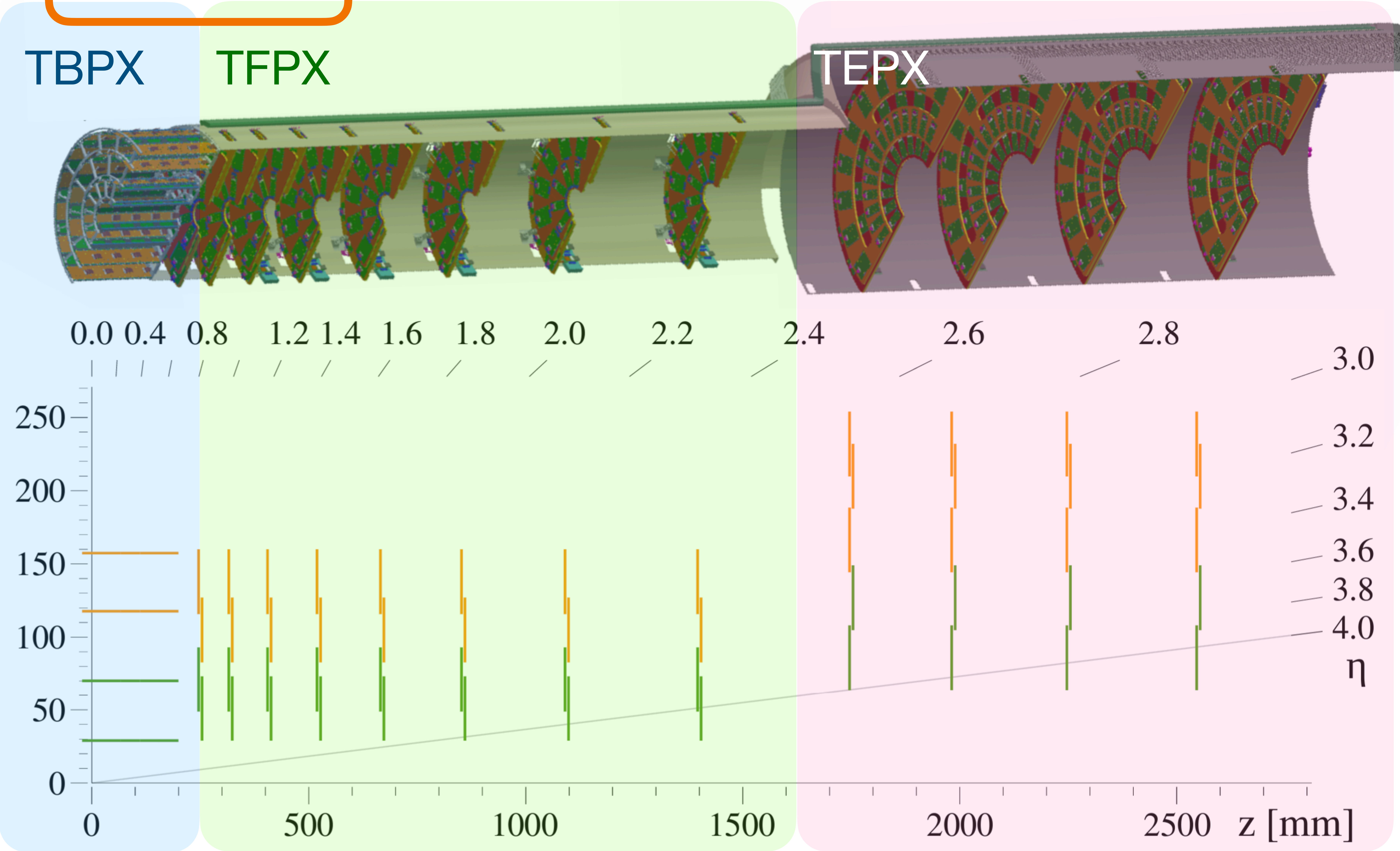
Valeriia Lukashenko, on behalf of the CMS Tracker group

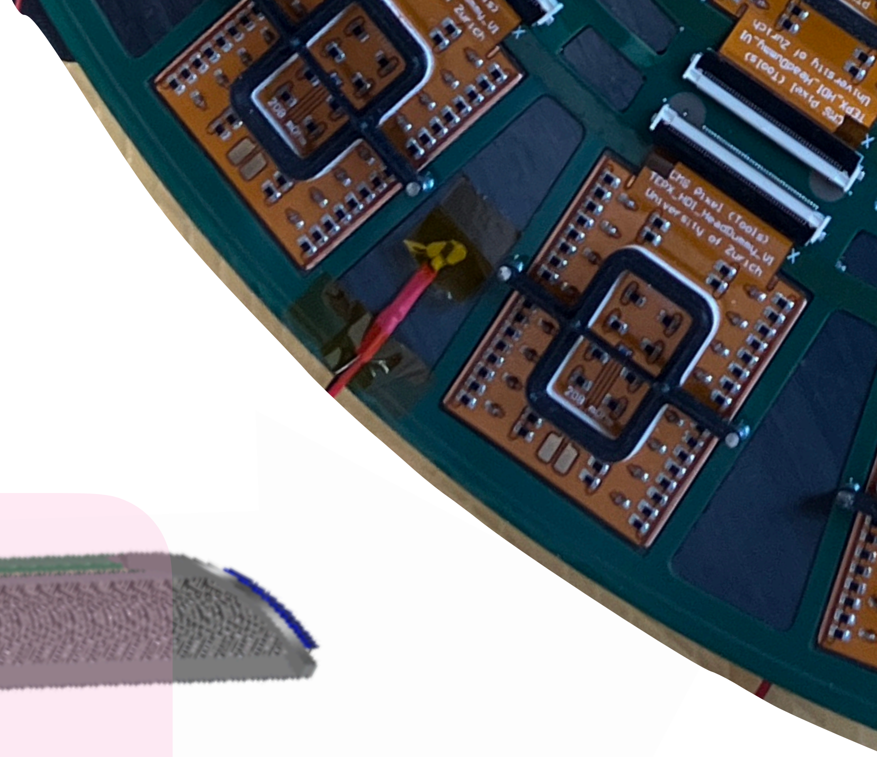
11th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging
Strasbourg, France

Universität Zürich[UZH]

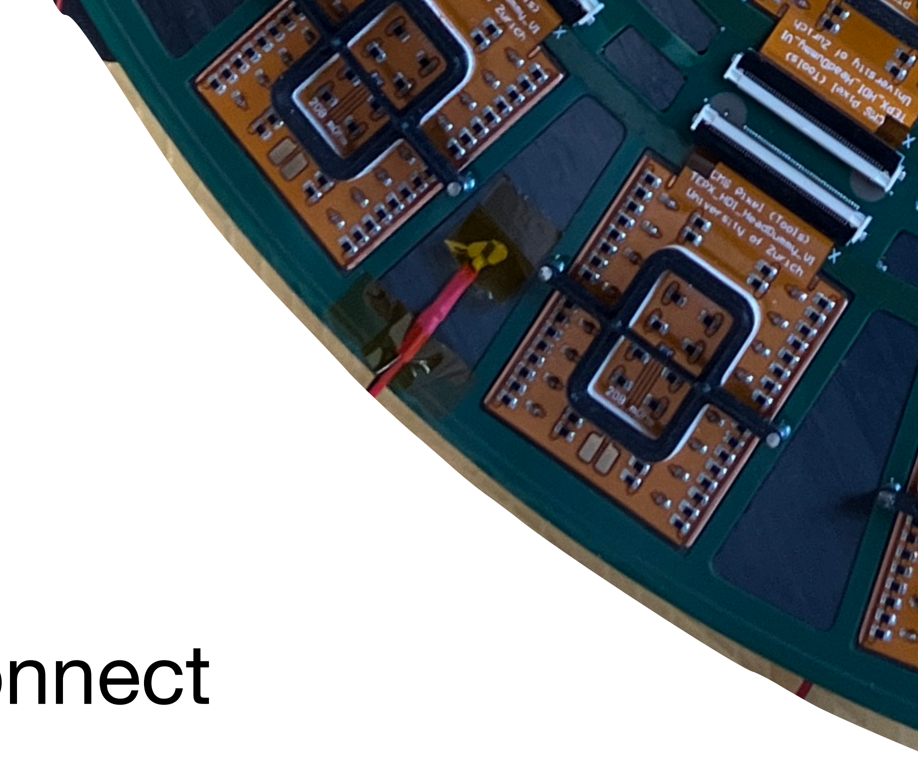
High-Lumi

CMS Phase-II Inner Tracker

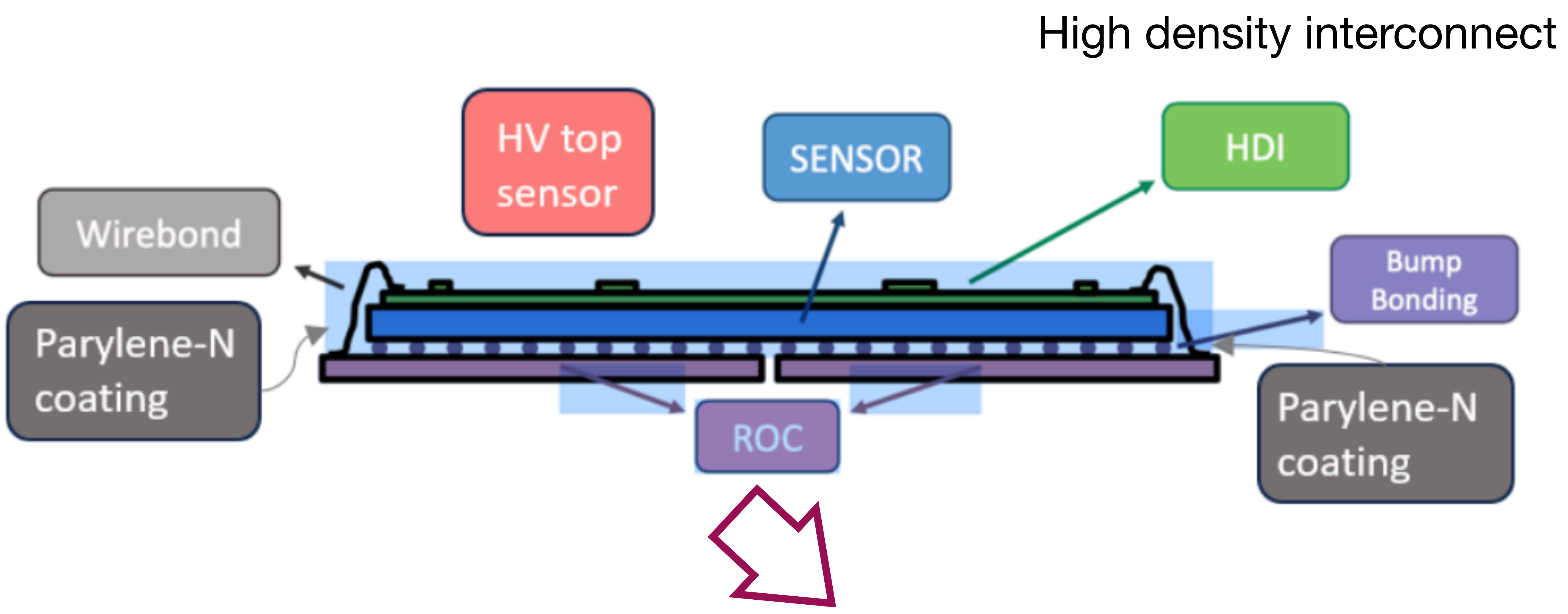




CMS Phase-II Inner Tracker



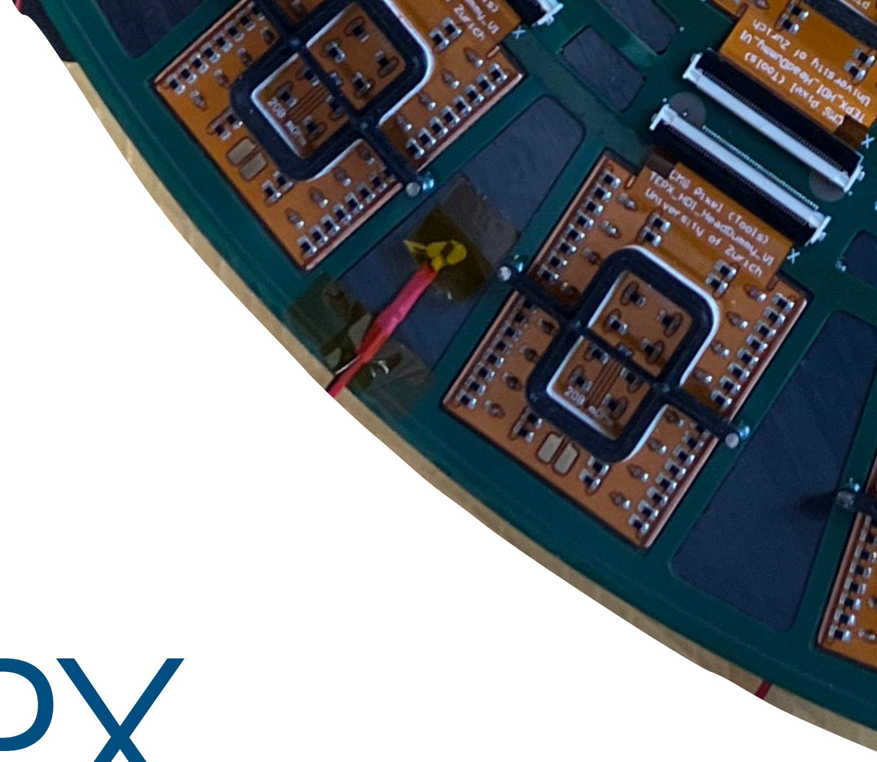
hybrid module



Giorgia Bonomelli
"Performance and Design Validation of CMS Phase-2 Pixel Modules"

Thierry Harte
"Evaluation of pixel sensors produced with a commercial 150nm CMOS process for the CMS Phase-2 Upgrade"

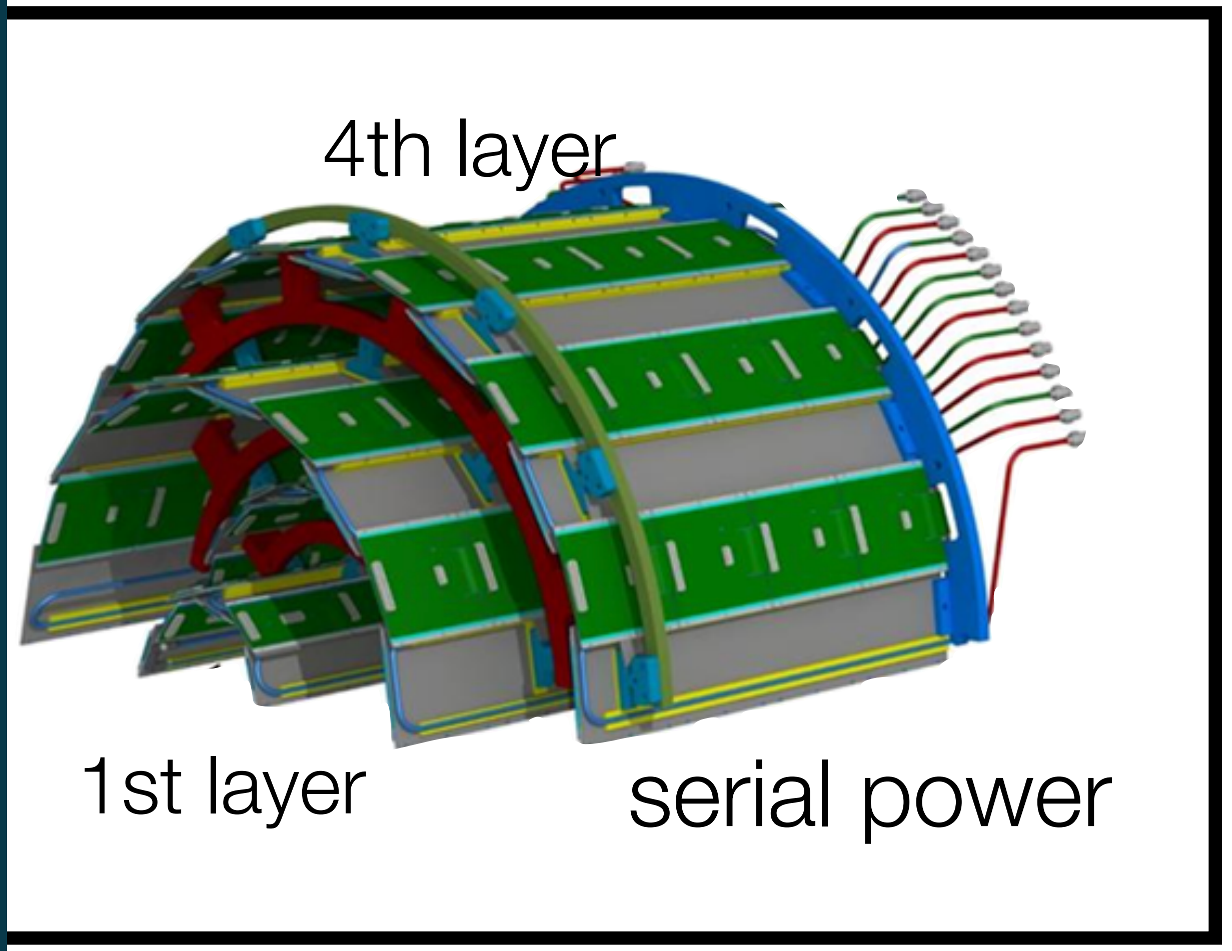
CROC (RD53): 65nm CMOS ASIC; $50 \times 50 \mu m^2$; hit rate 3.5 GHz/cm^2 ; radiation tolerance up to 1 Grad; power < 1 W/cm^2; up to 4x1.28 Gbps output links.



Tracker subsystems design

TBPX

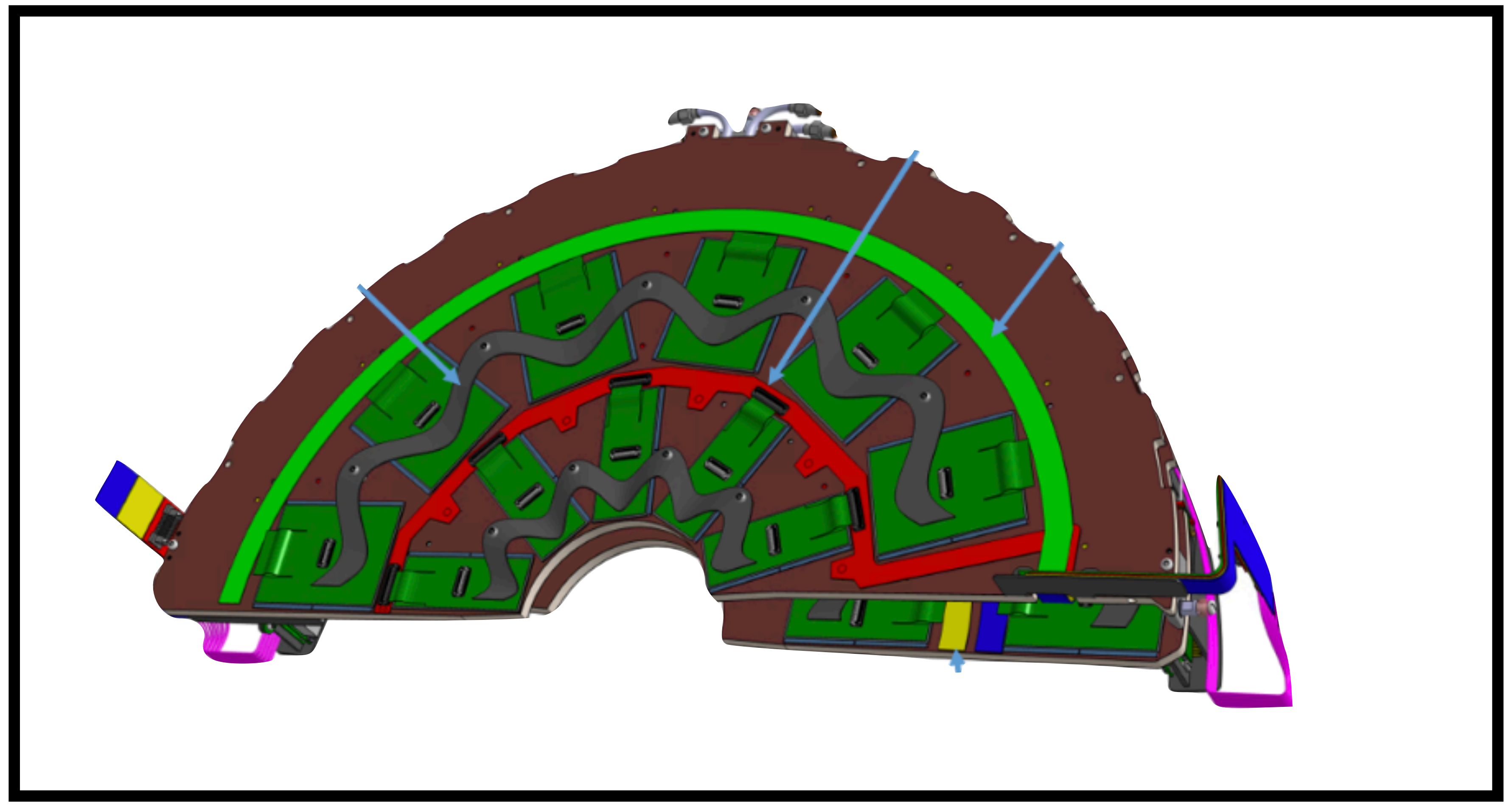
Tracker **B**arrel **P**i**X**el Detector



- 4 layers per quarter (4 quarters)
- modules arranged in ladders
- 3D sensors for 1st layer
- planar sensor double chip modules for 2nd layer
- planar sensor quad chip modules for layers 3 and 4

TFPX

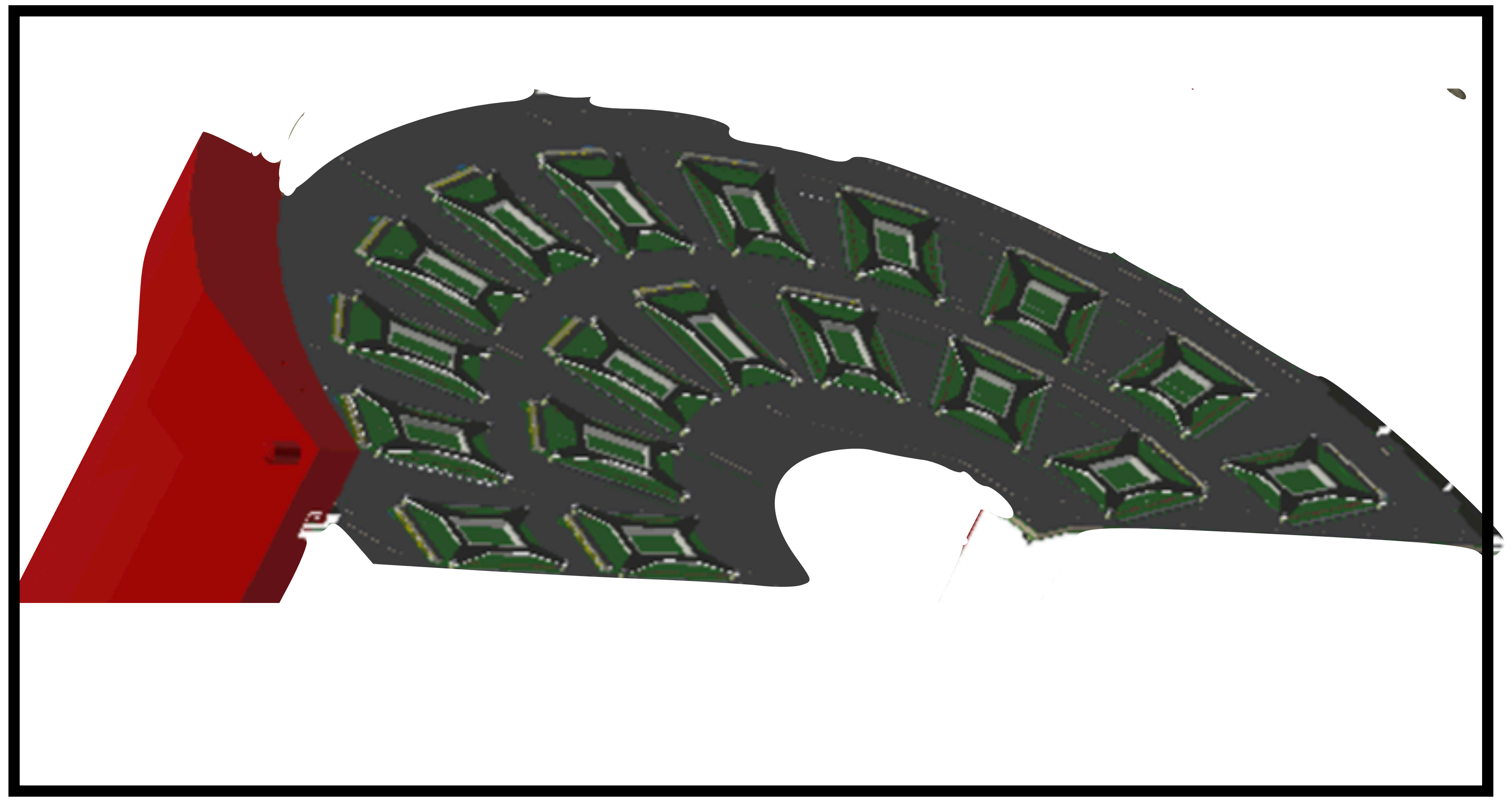
Tracker **F**orward **P**i**X**el Detector



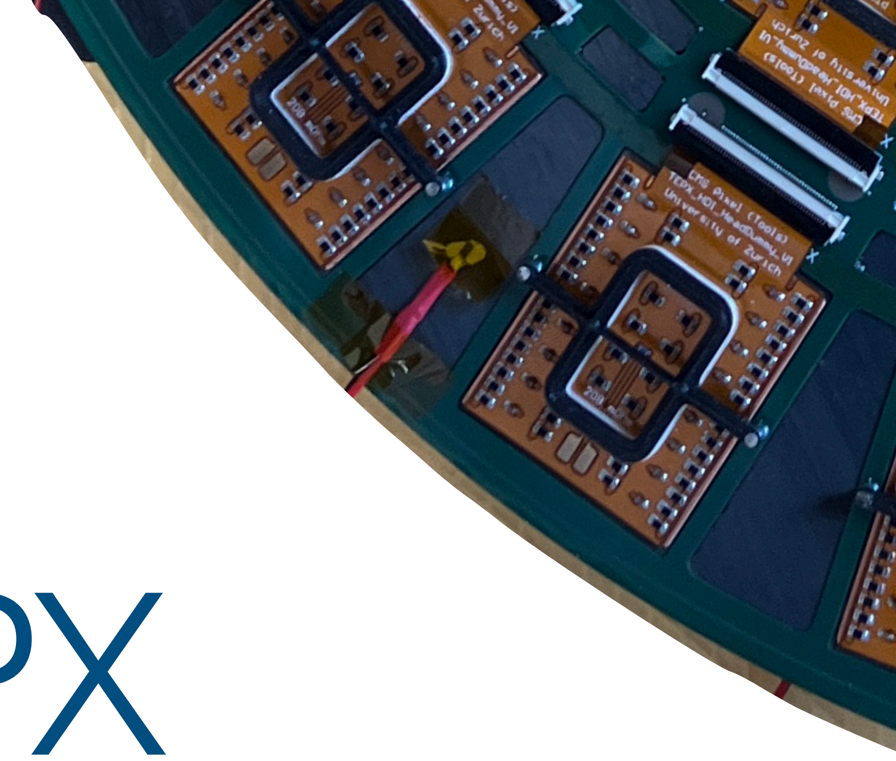
- 2x7 double disks split in halves
- 26 double chip modules per half
- 28 quad chip modules per half

TEPX

Tracker **E**ndcap **P**i**X**el Detector

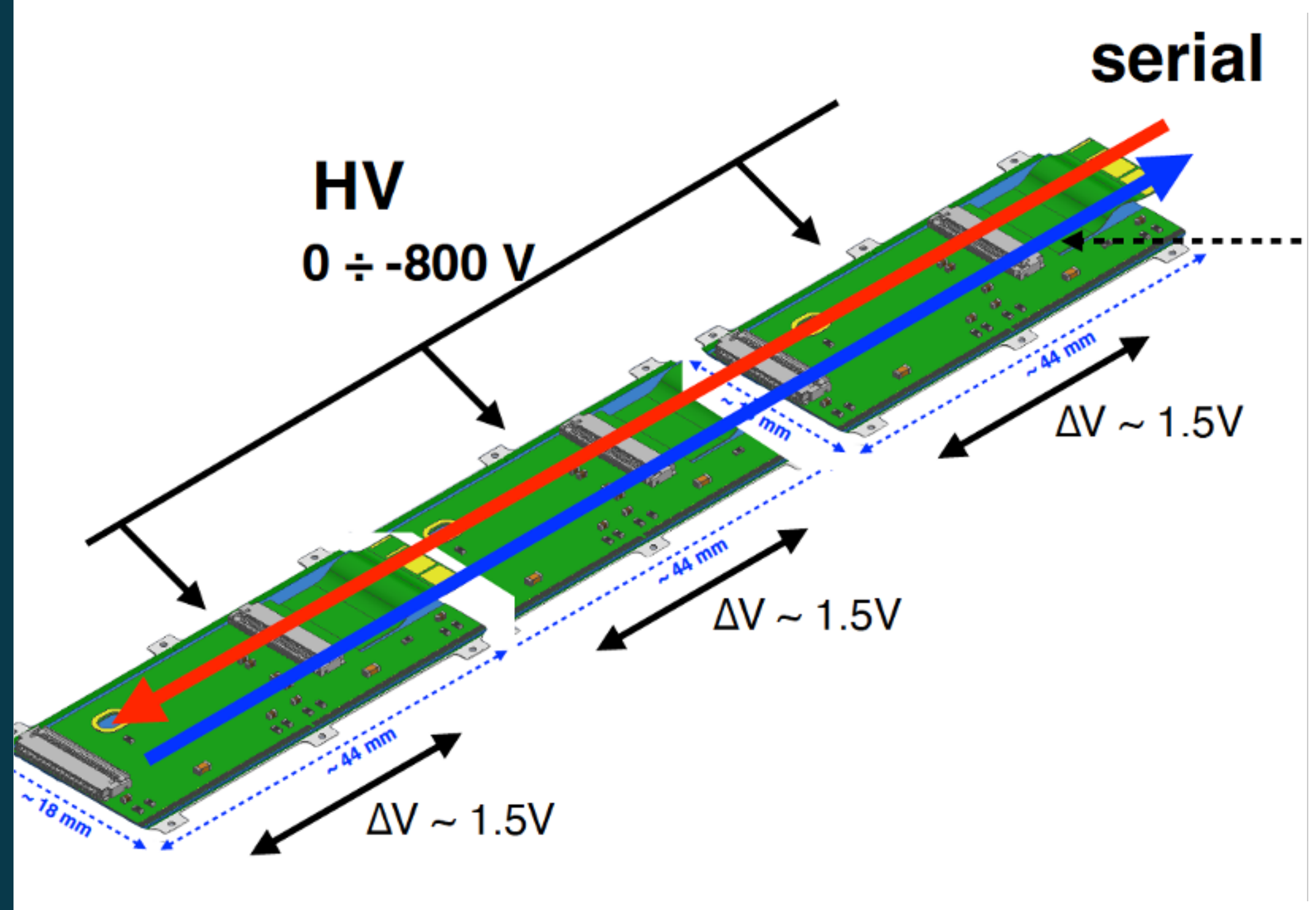


- 2x4 double disks split in halves
- 88 quad chip modules per half

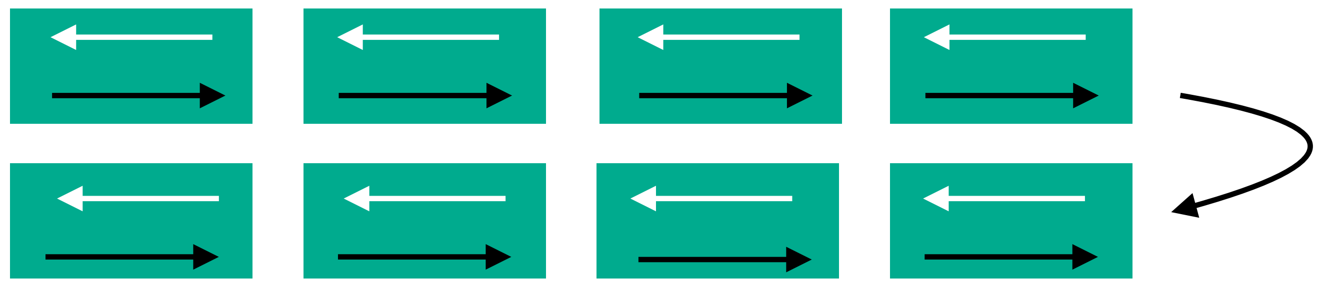


Tracker subsystems serial power chains

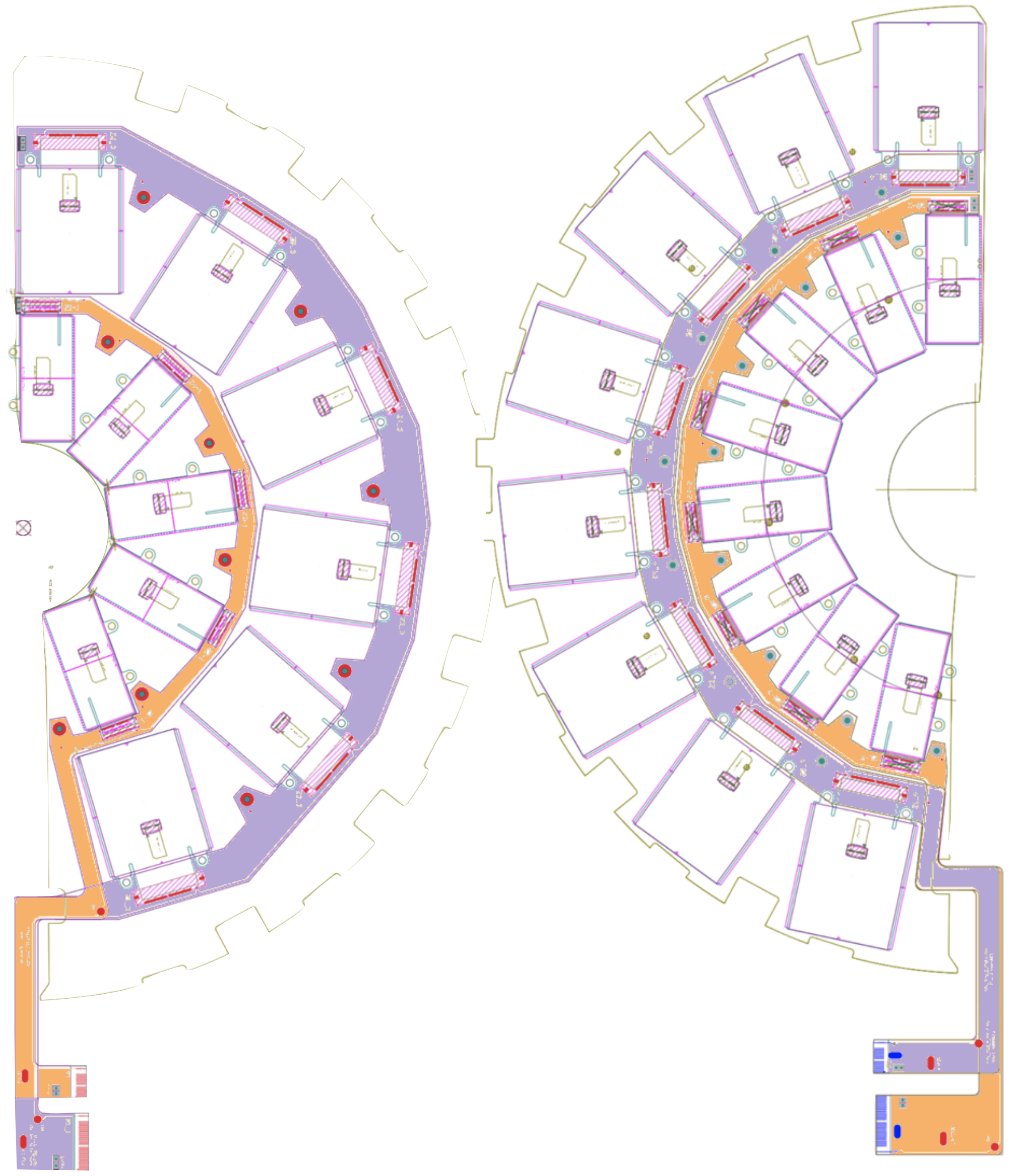
TBPX



8 or 10 modules by 2 half ladders



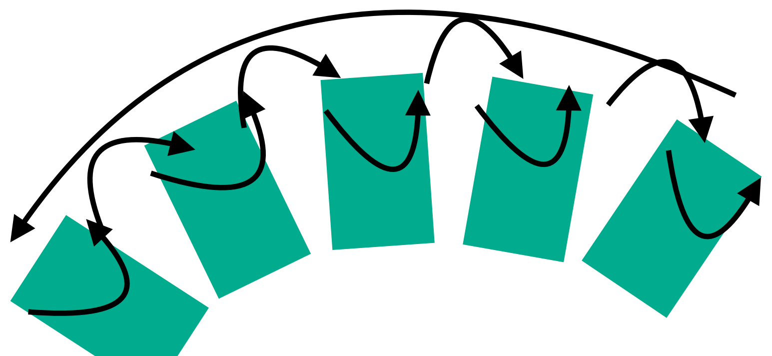
TFPX



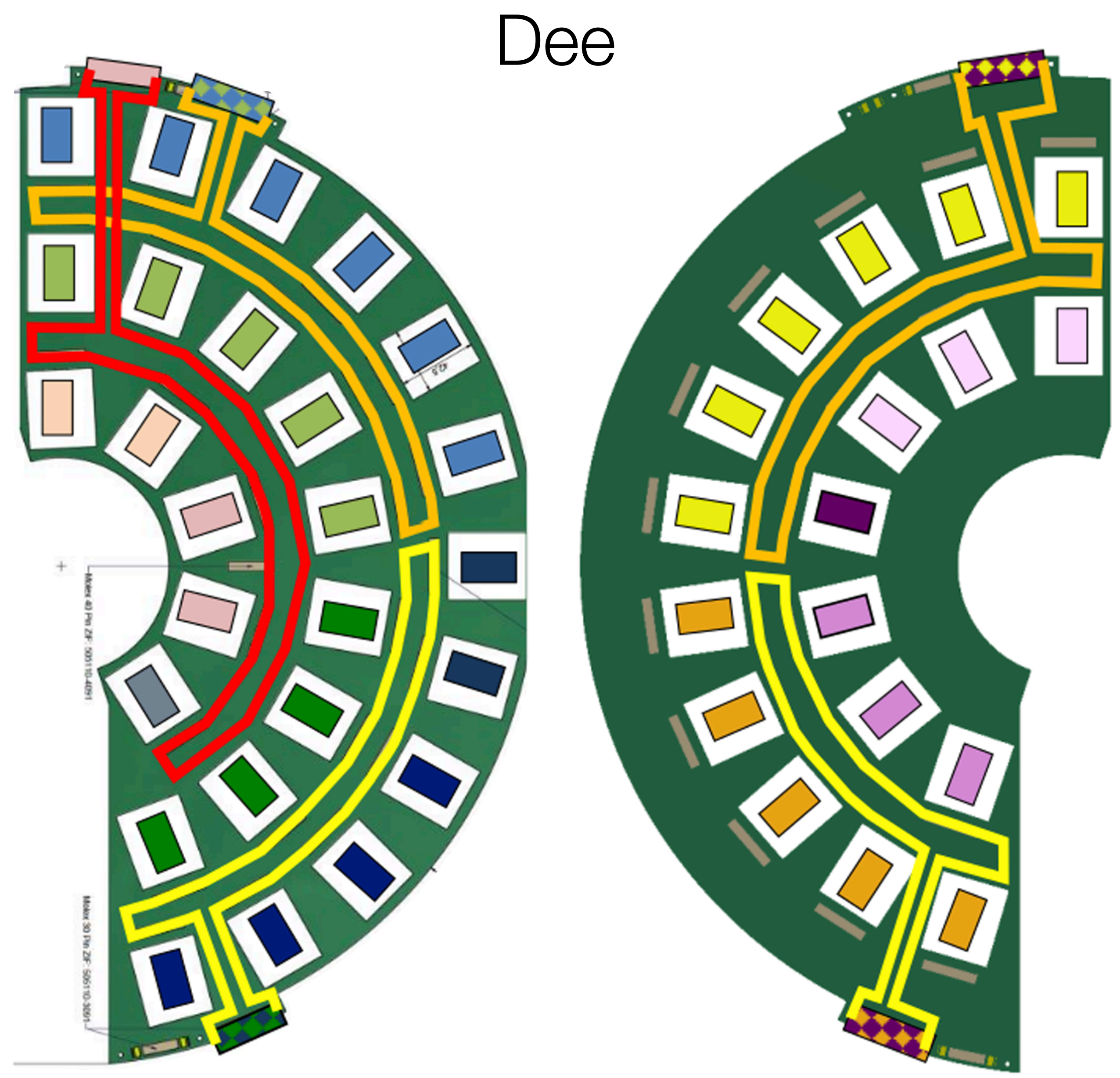
ring 1-3

ring 2-4

5, 6, 8 modules by ring power flex



TEPX

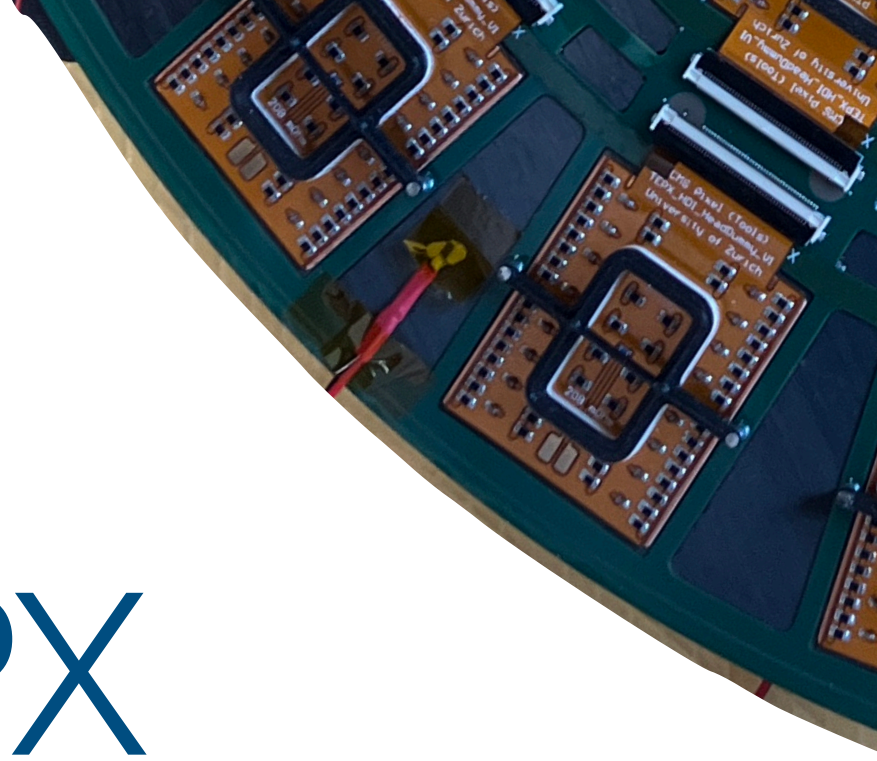


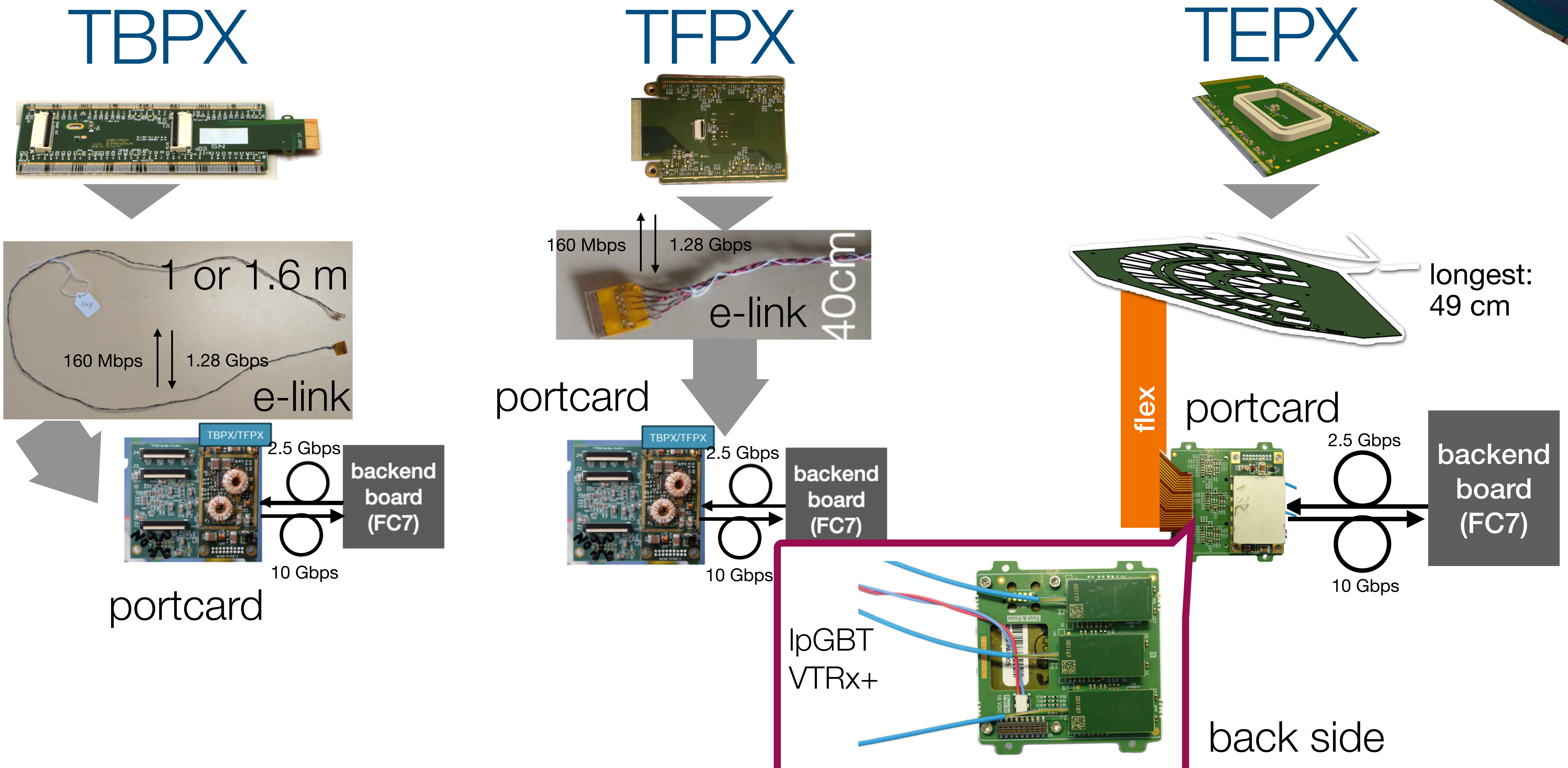
ring 1-3-5

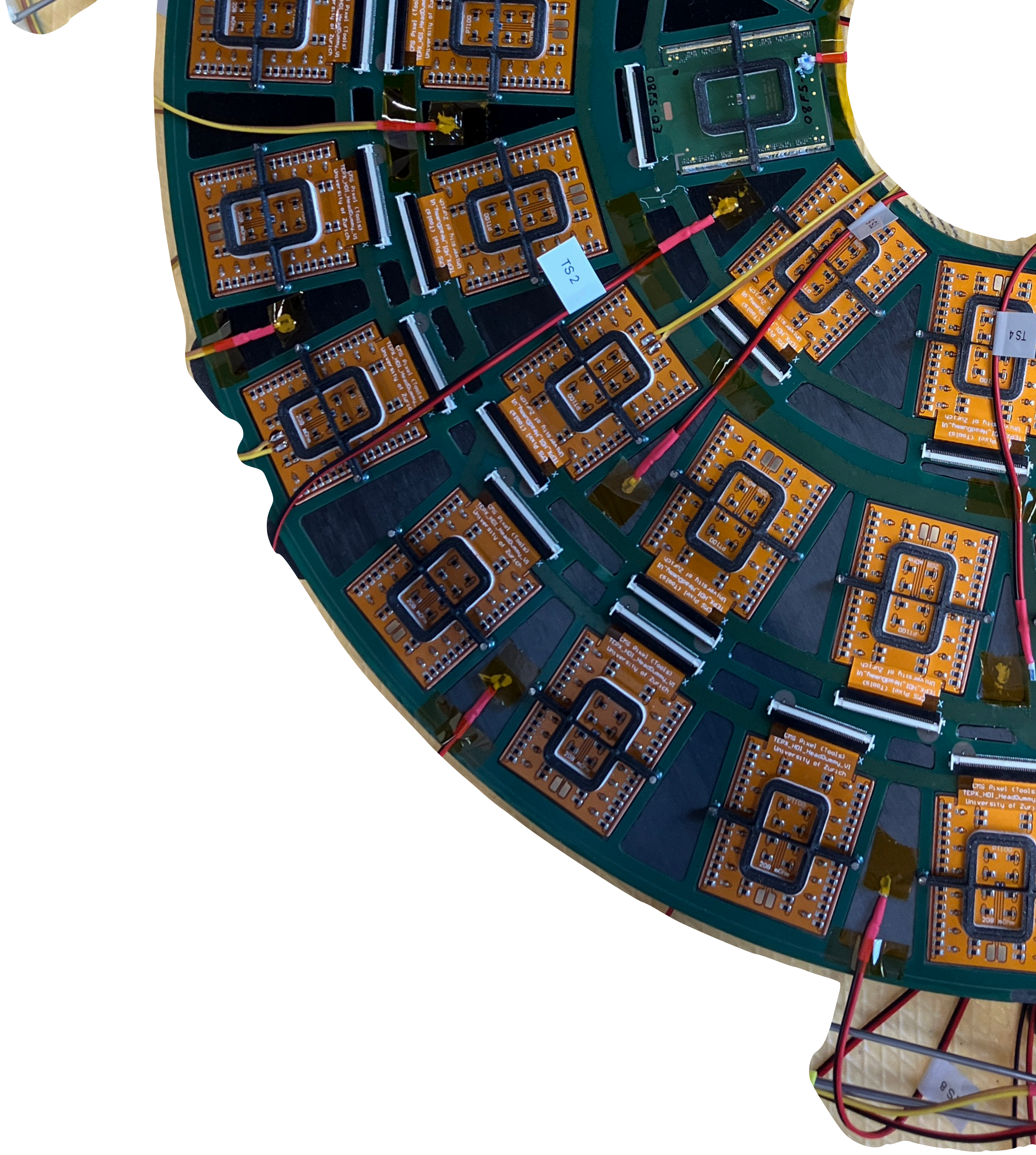
ring 2-4

5-11 modules by power lines on PCB

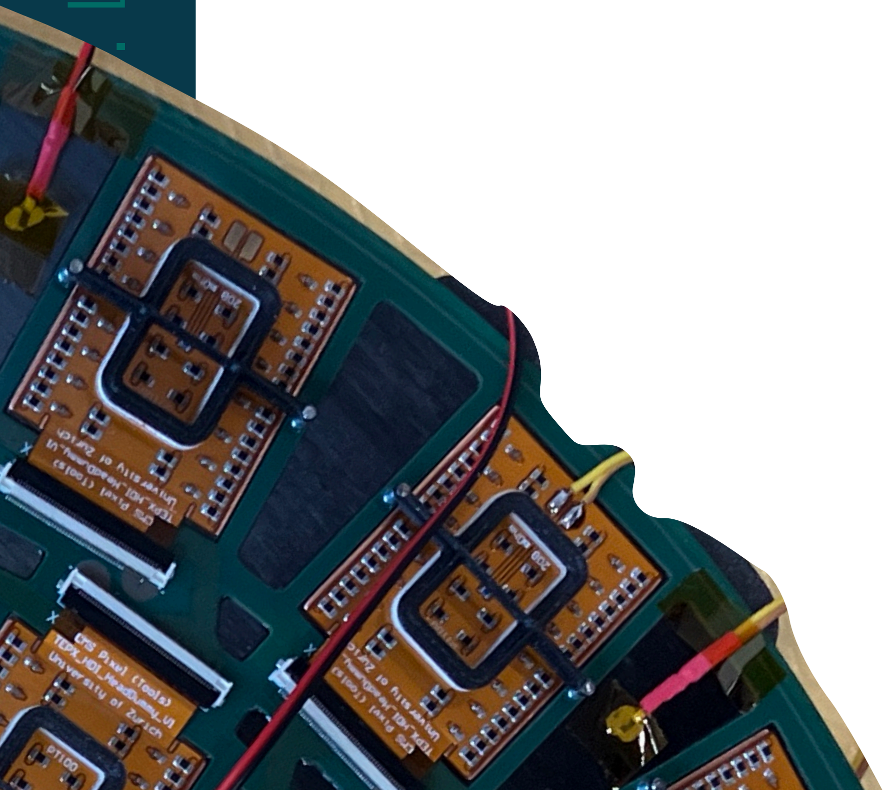
Tracker subsystems readout chain



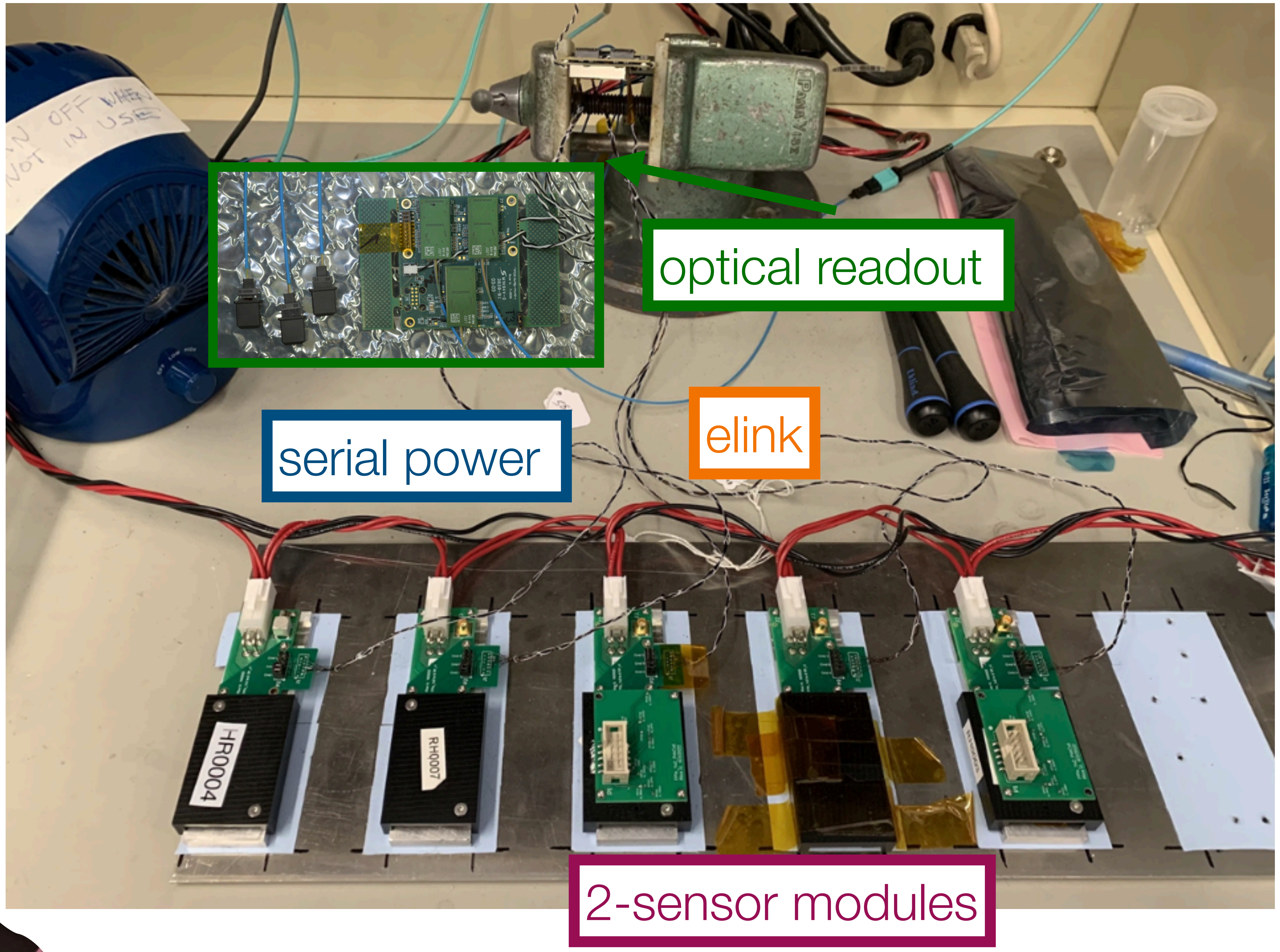




1. Threshold and noise

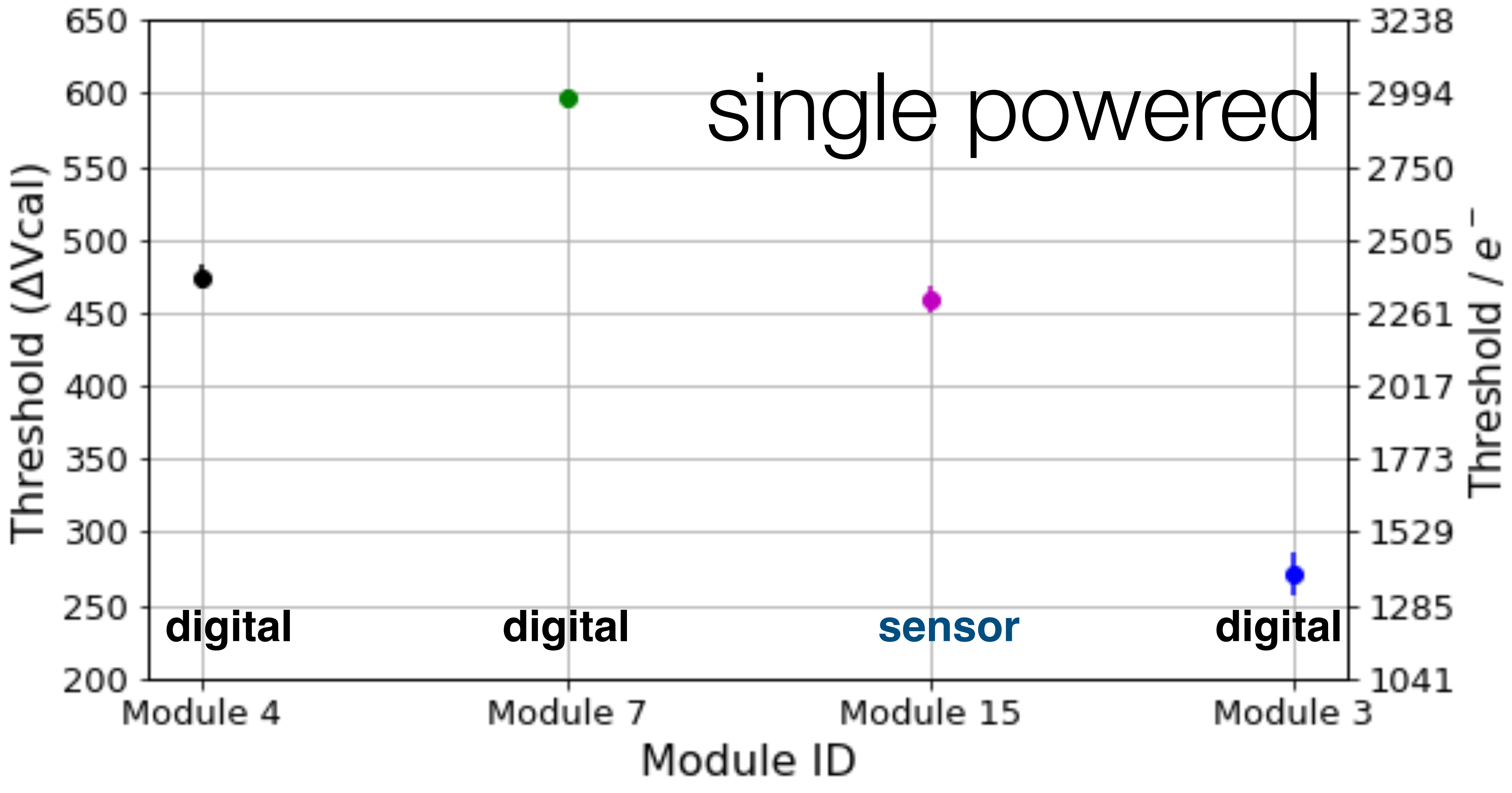


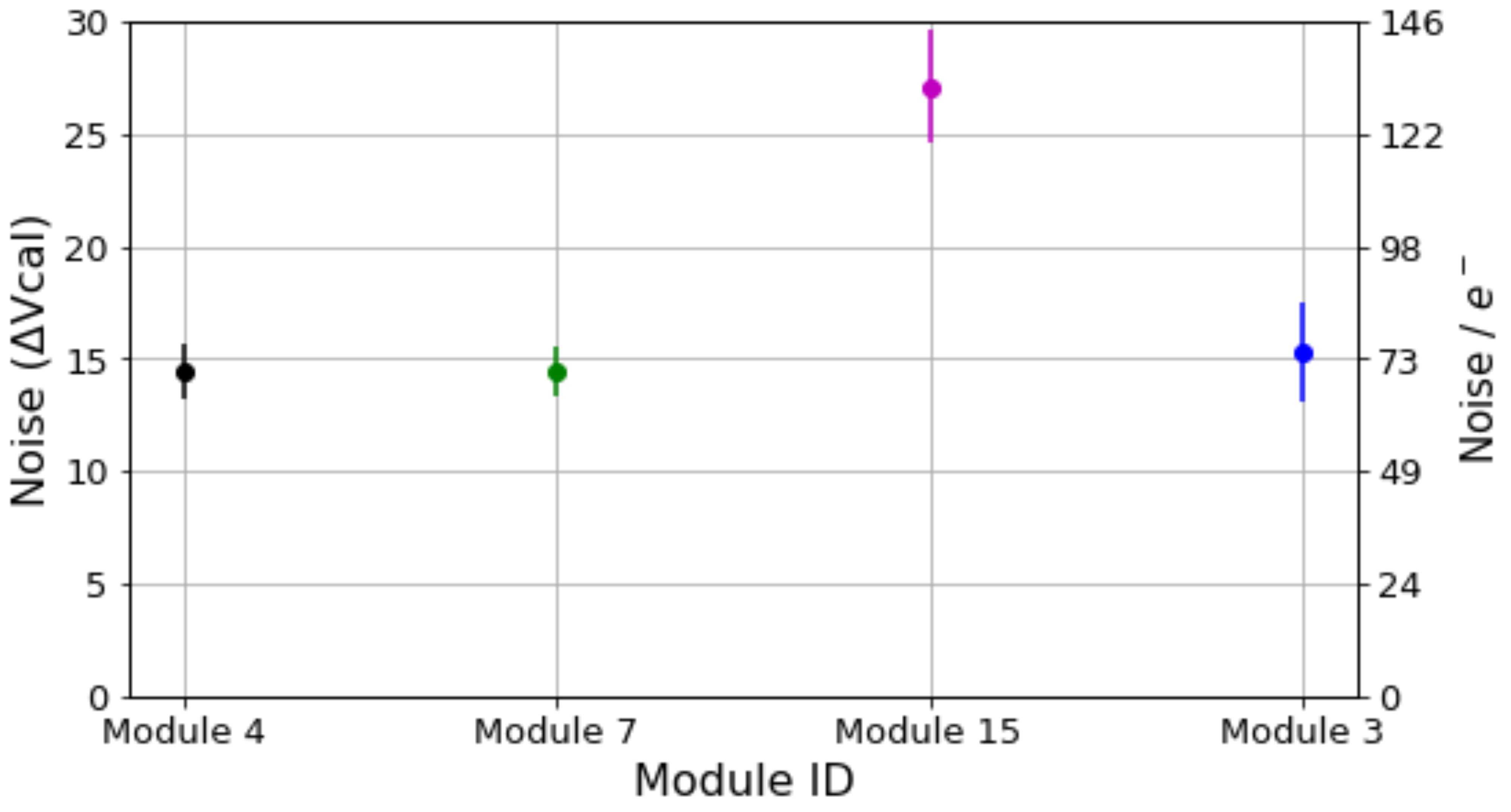
TFPX: threshold and noise dependence on **powering**



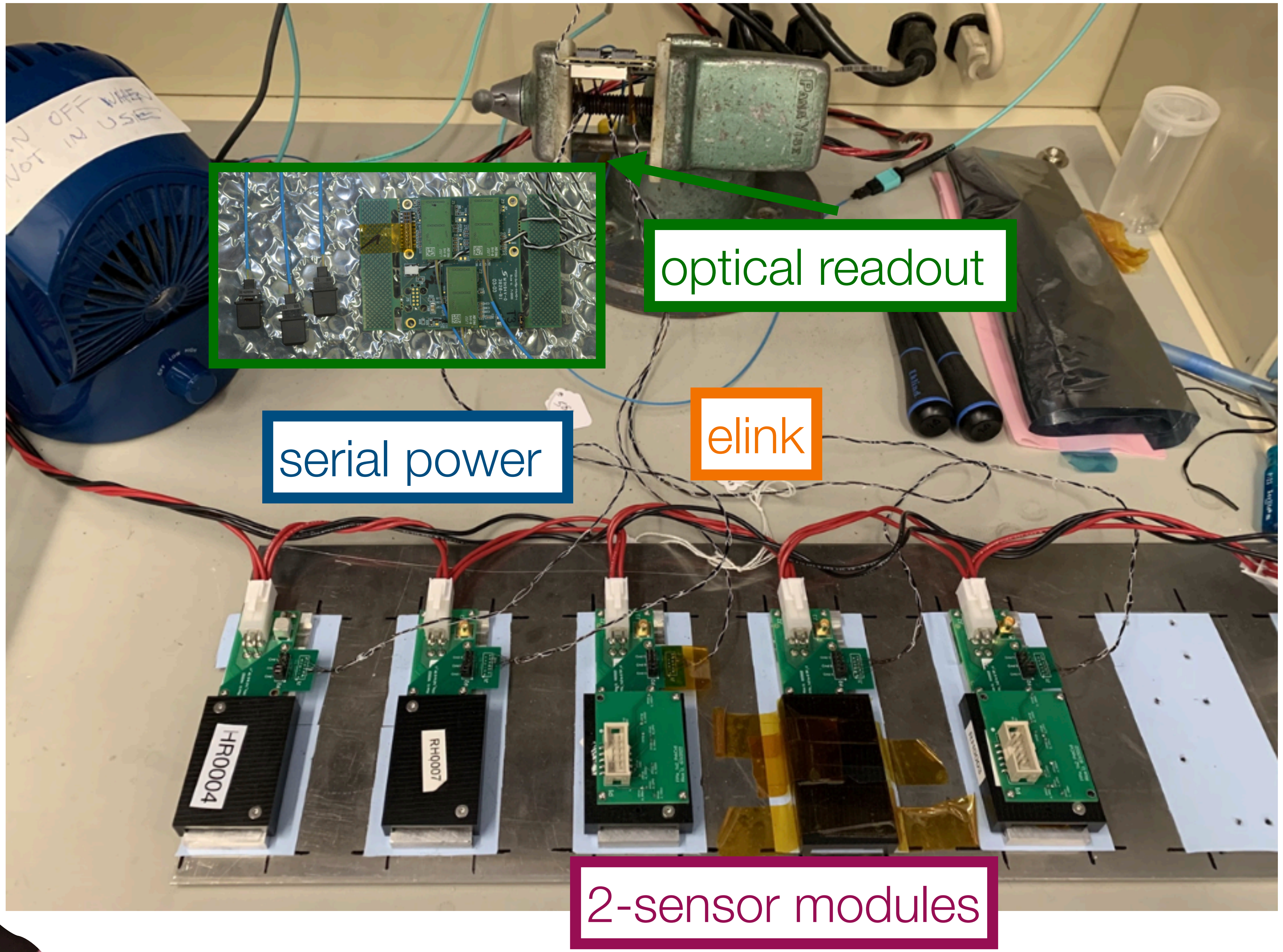
setup at Rice University

no HV



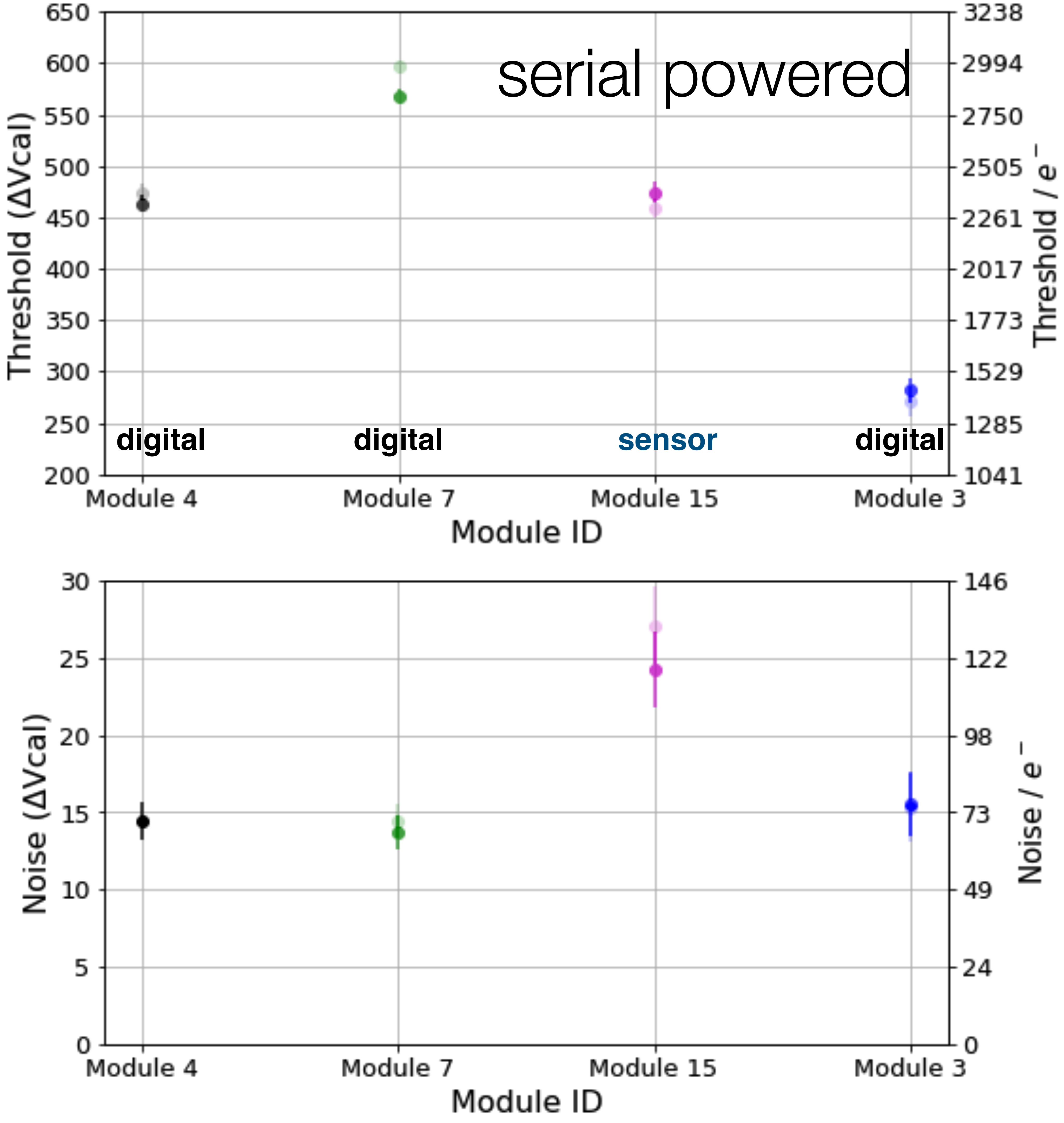


TFPX: threshold and noise dependence on **powering**

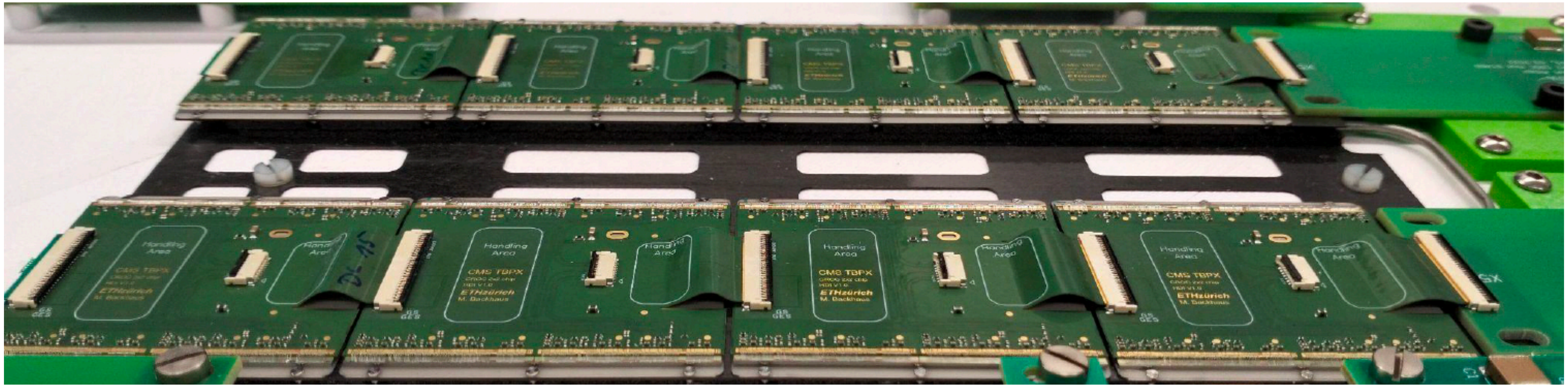


setup at Rice University

no HV

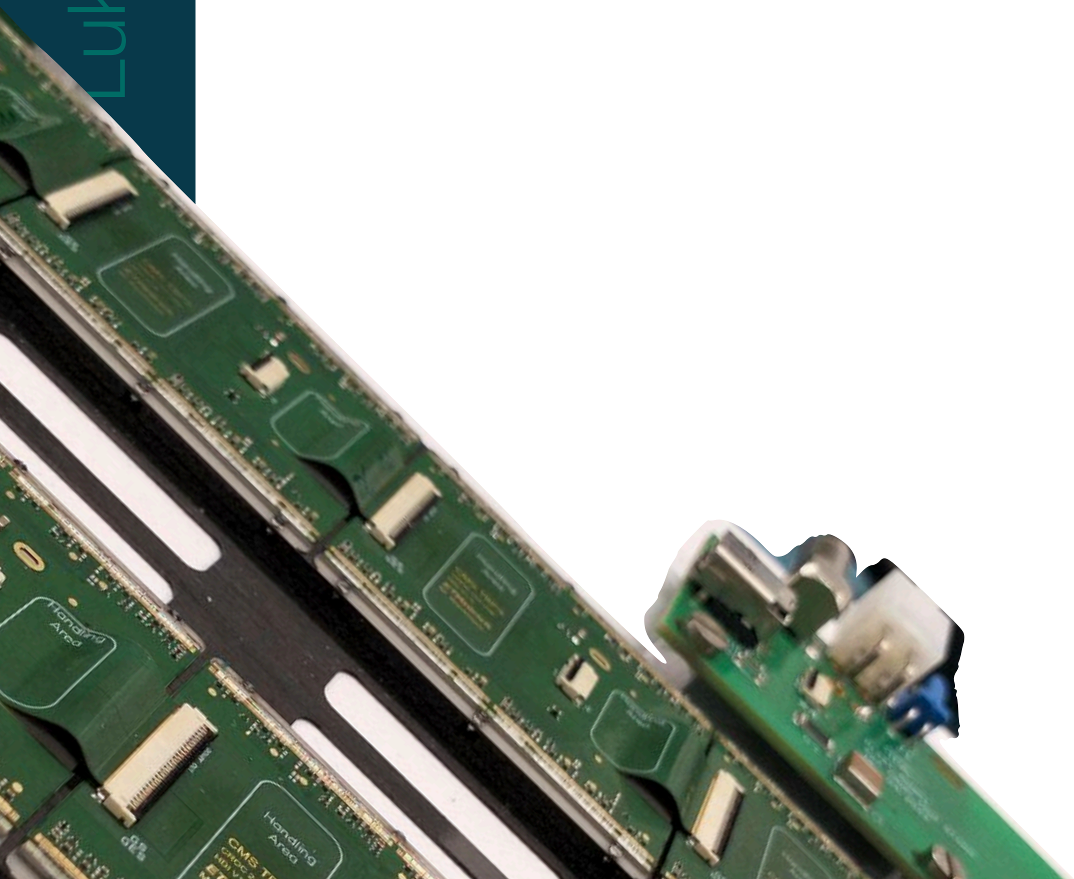


TBPX: threshold and noise with **electrical vs optical** readout

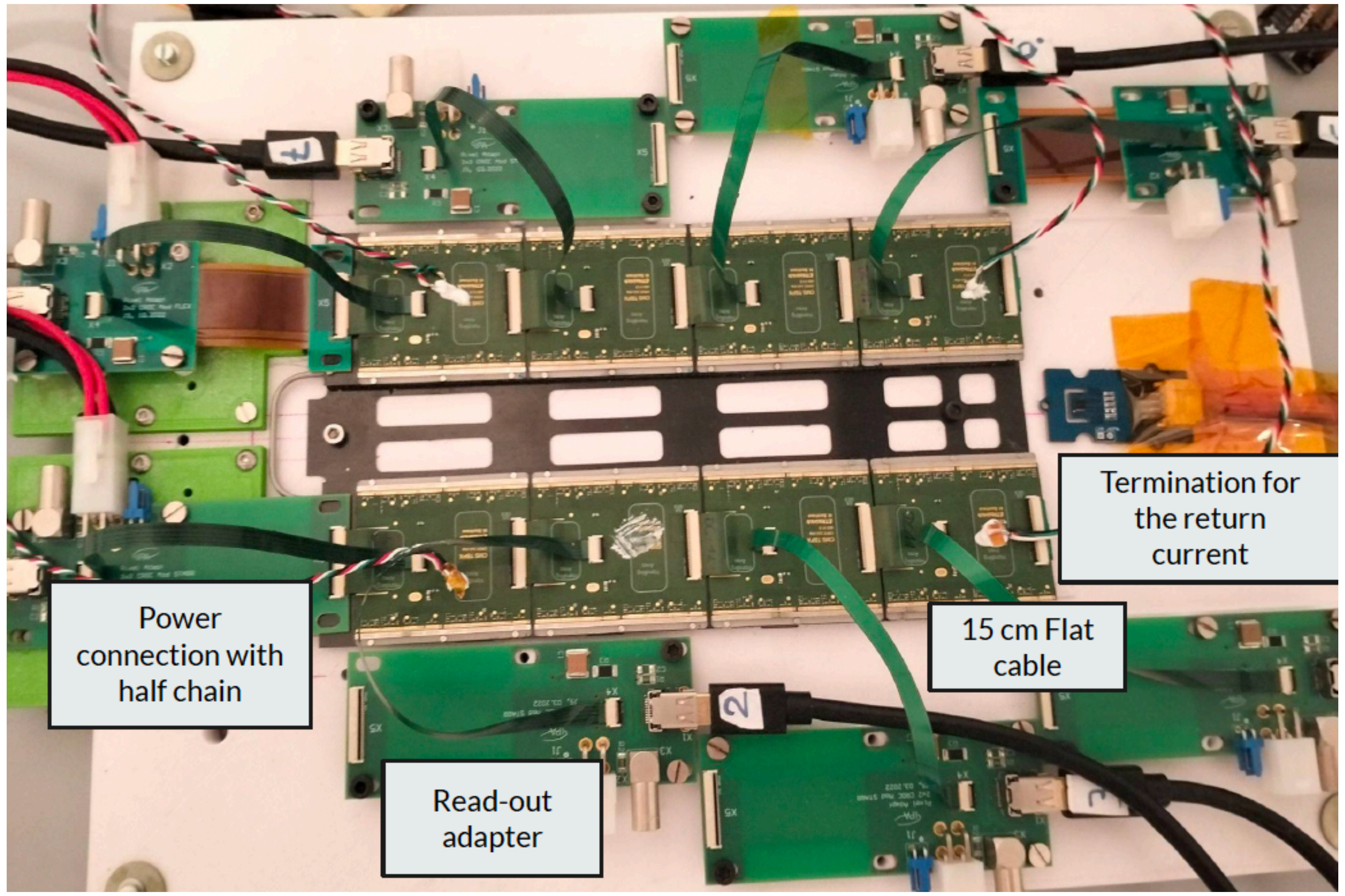


serial power chain assembled at ETHZ

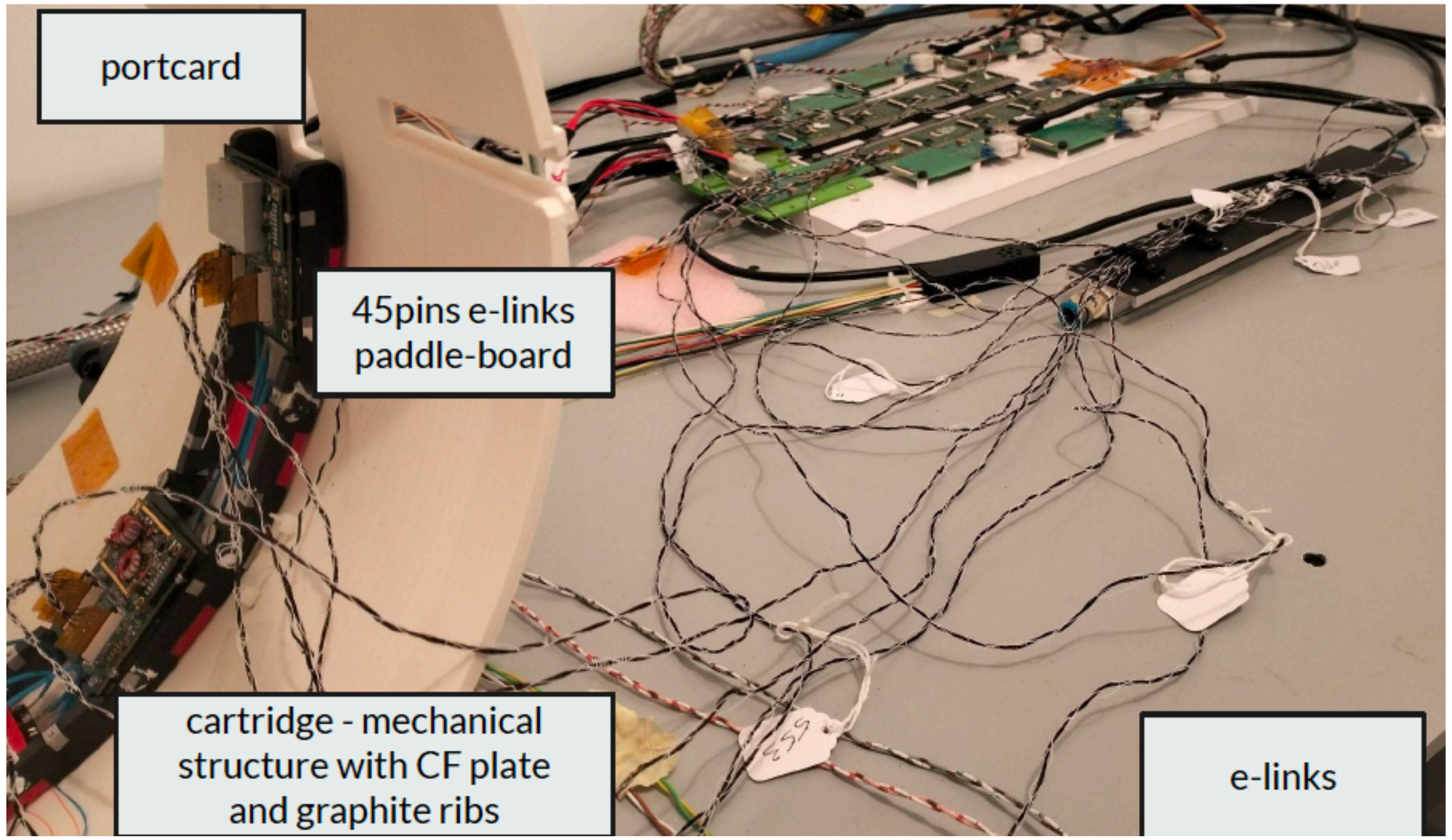
- 8 digital modules
- no thermal grease, just connected with screws
- CO2 cooling



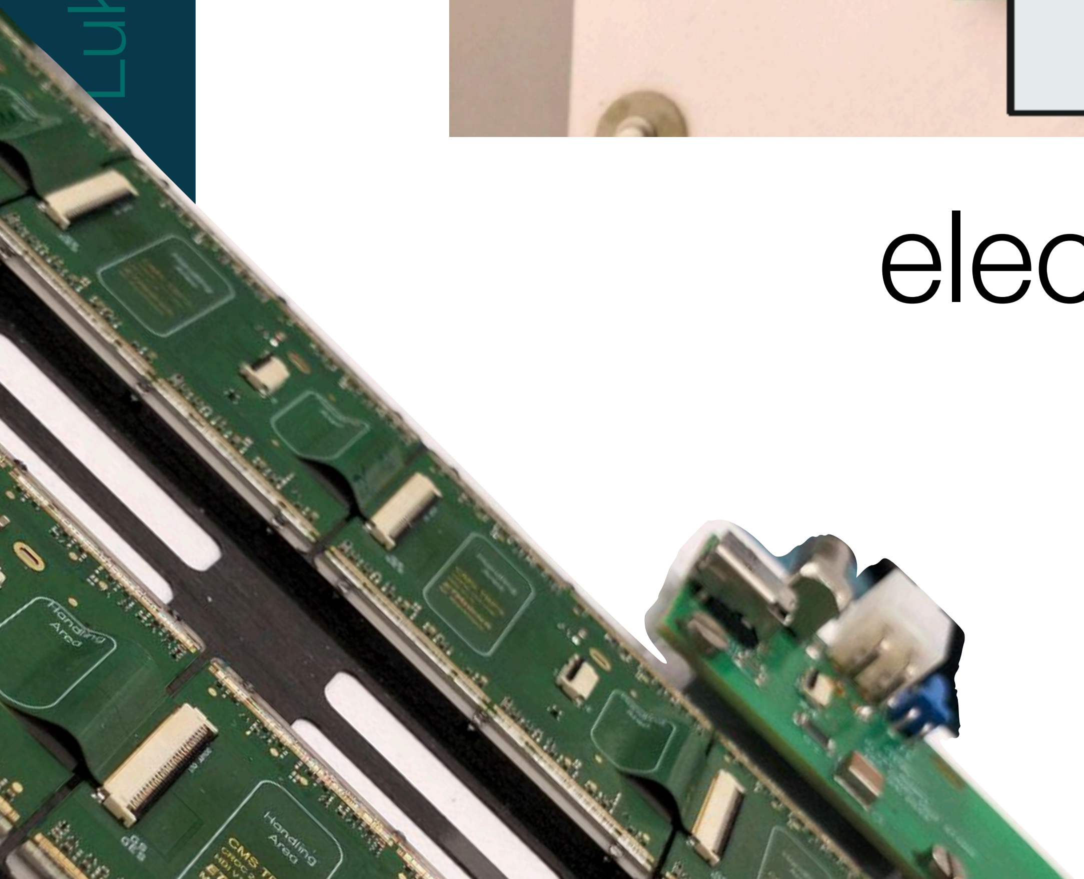
TBPX: threshold and noise with **electrical vs optical** readout



electrical readout



optical readout



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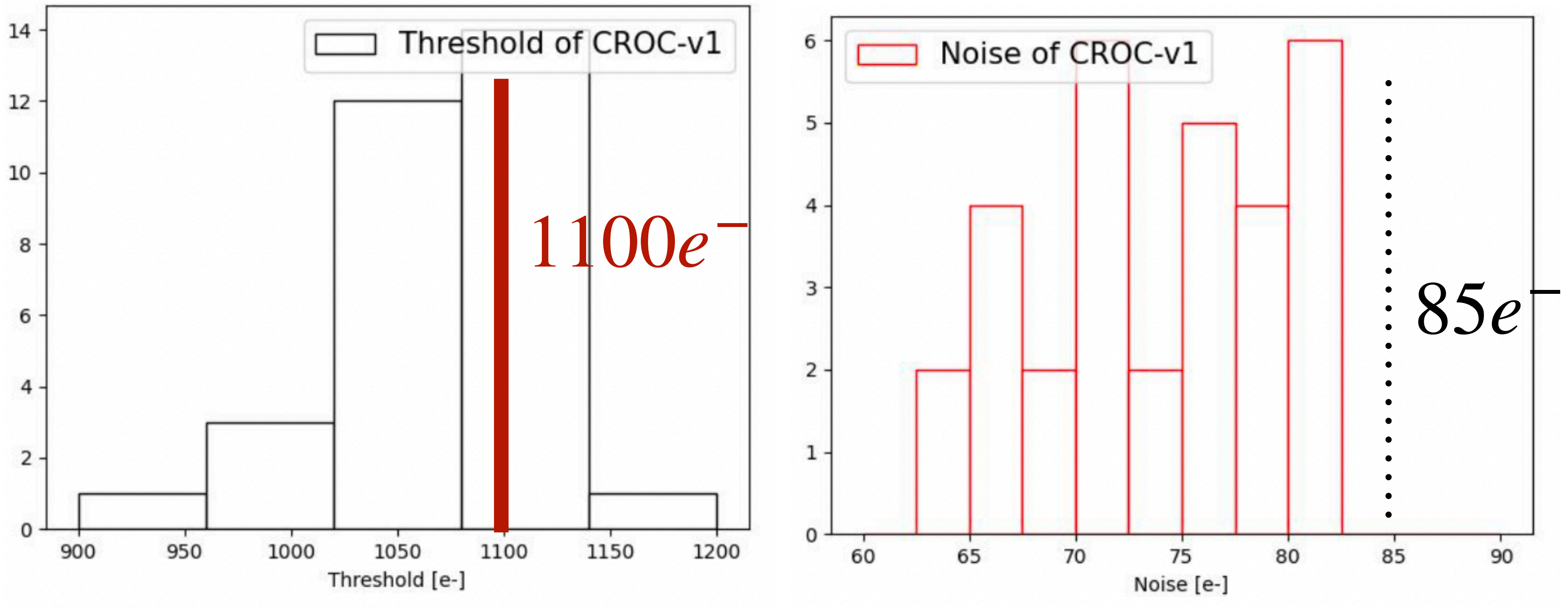
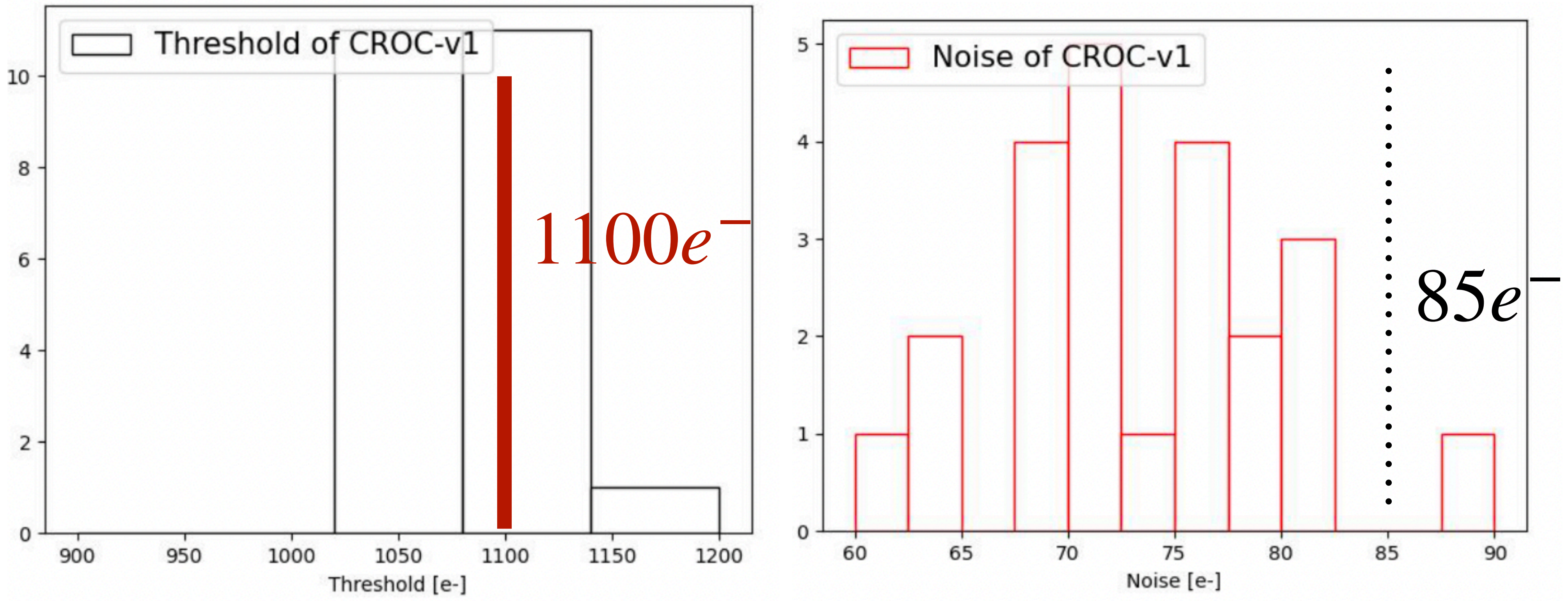
TBPX: threshold and noise with **electrical vs optical** readout

$T_{CO_2} = -32°C$ 32 digital CROCv1



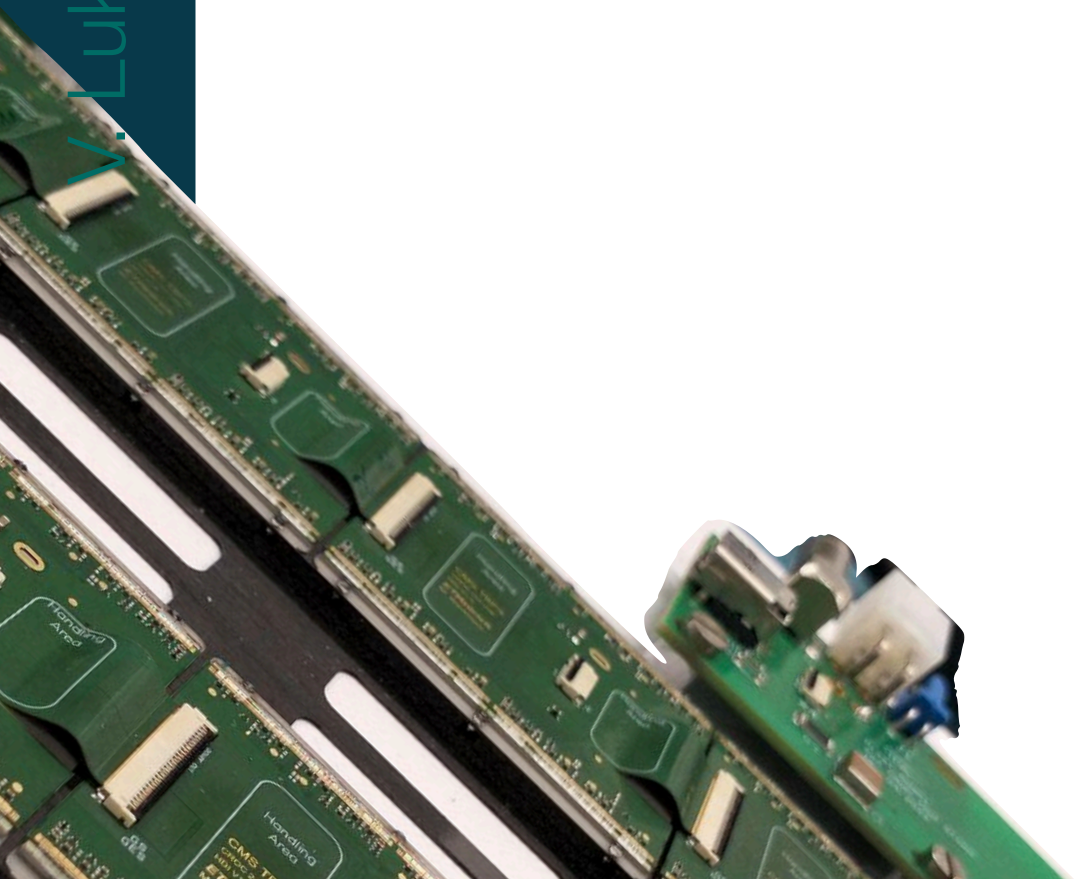
electrical readout

$T_{CO_2} = -28°C$ 32 digital CROCv1



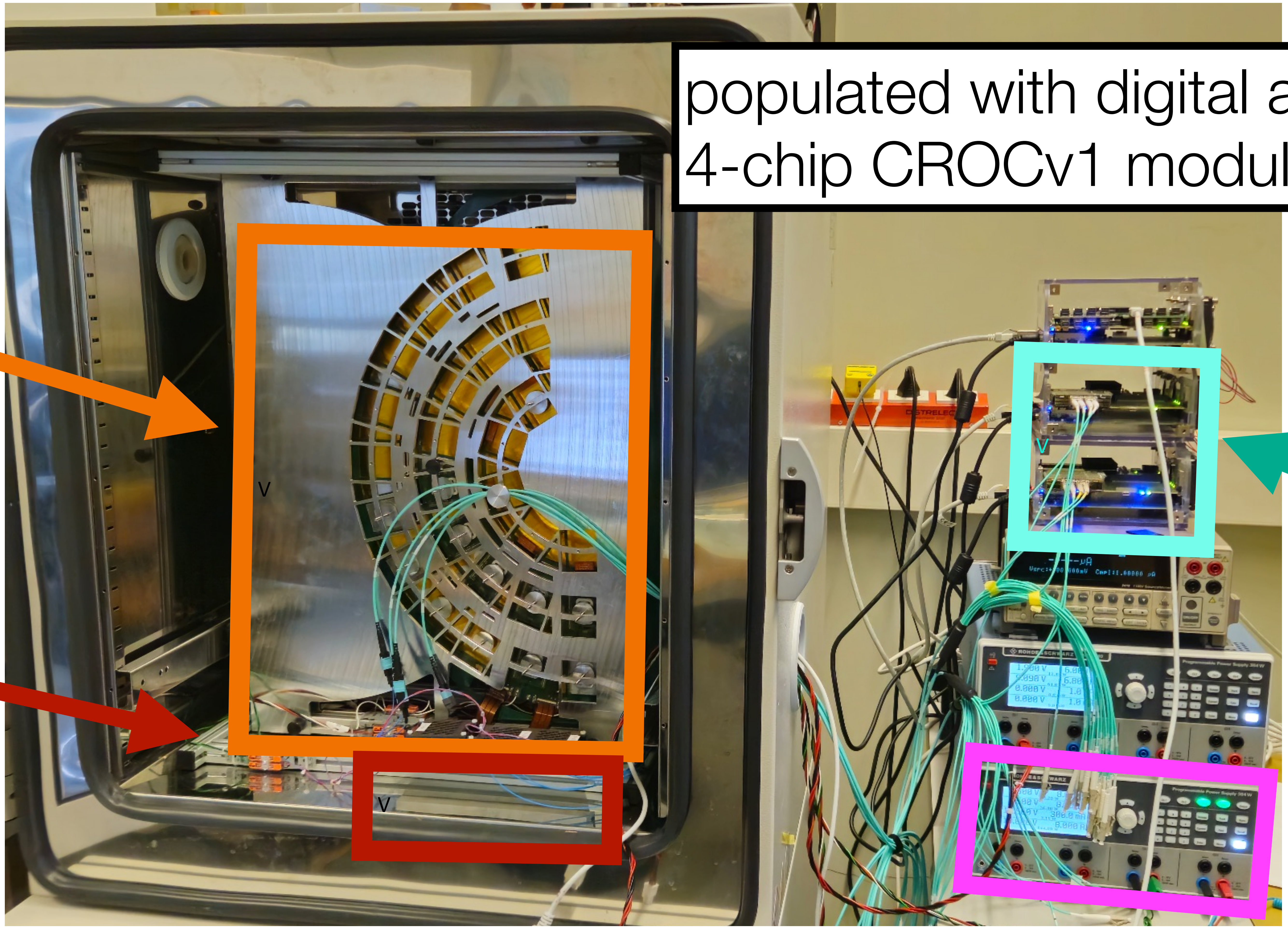
optical readout

no significant difference between electrical and optical readout

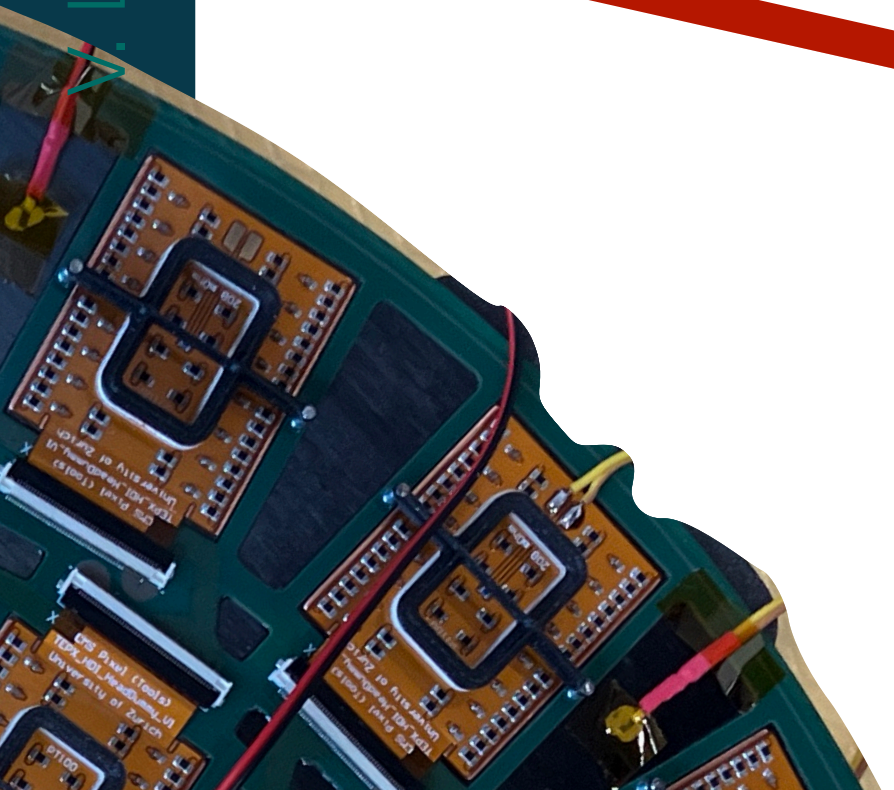


TEPX: PCB tests - threshold and noise

PCB prototype in climate chamber at $T = -40°C$

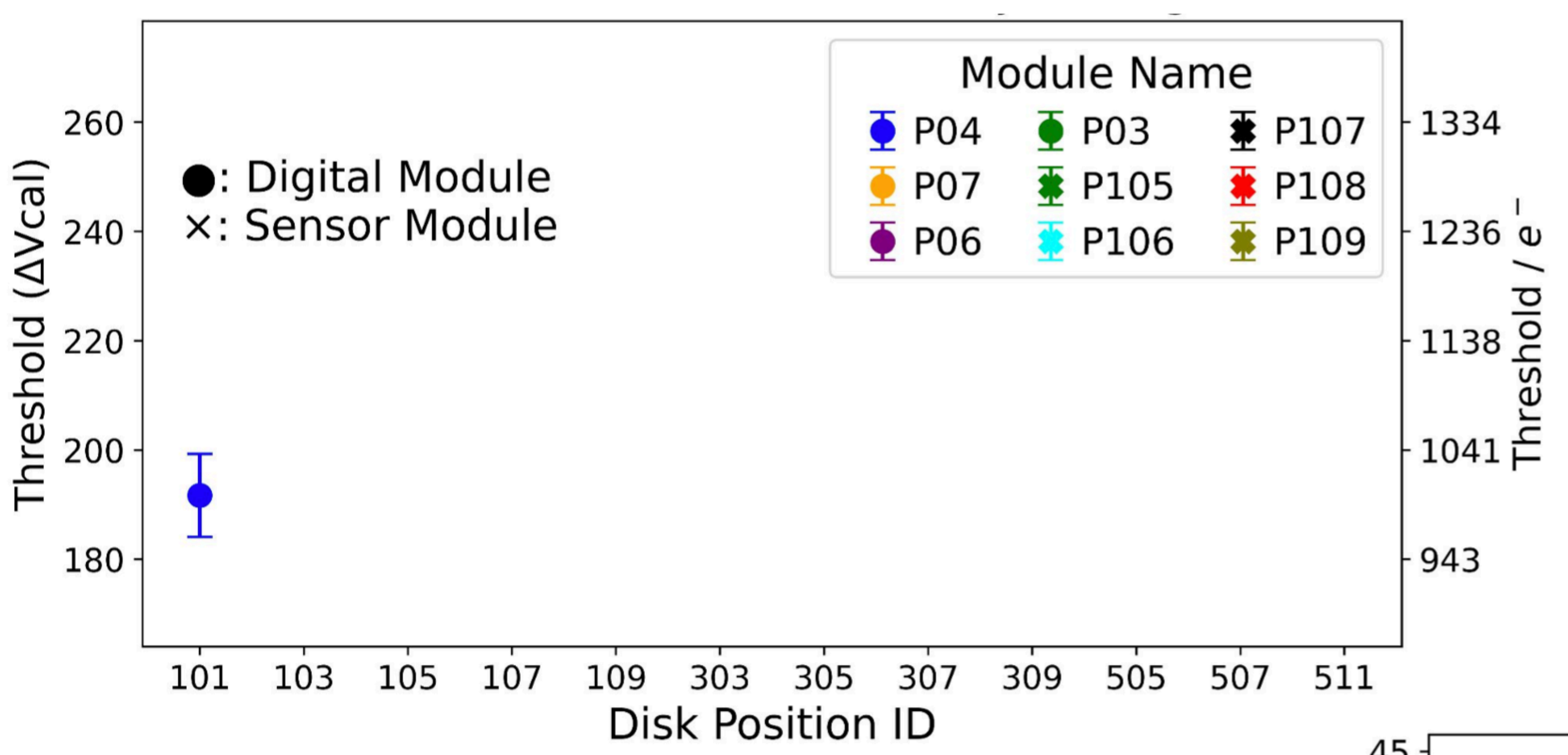


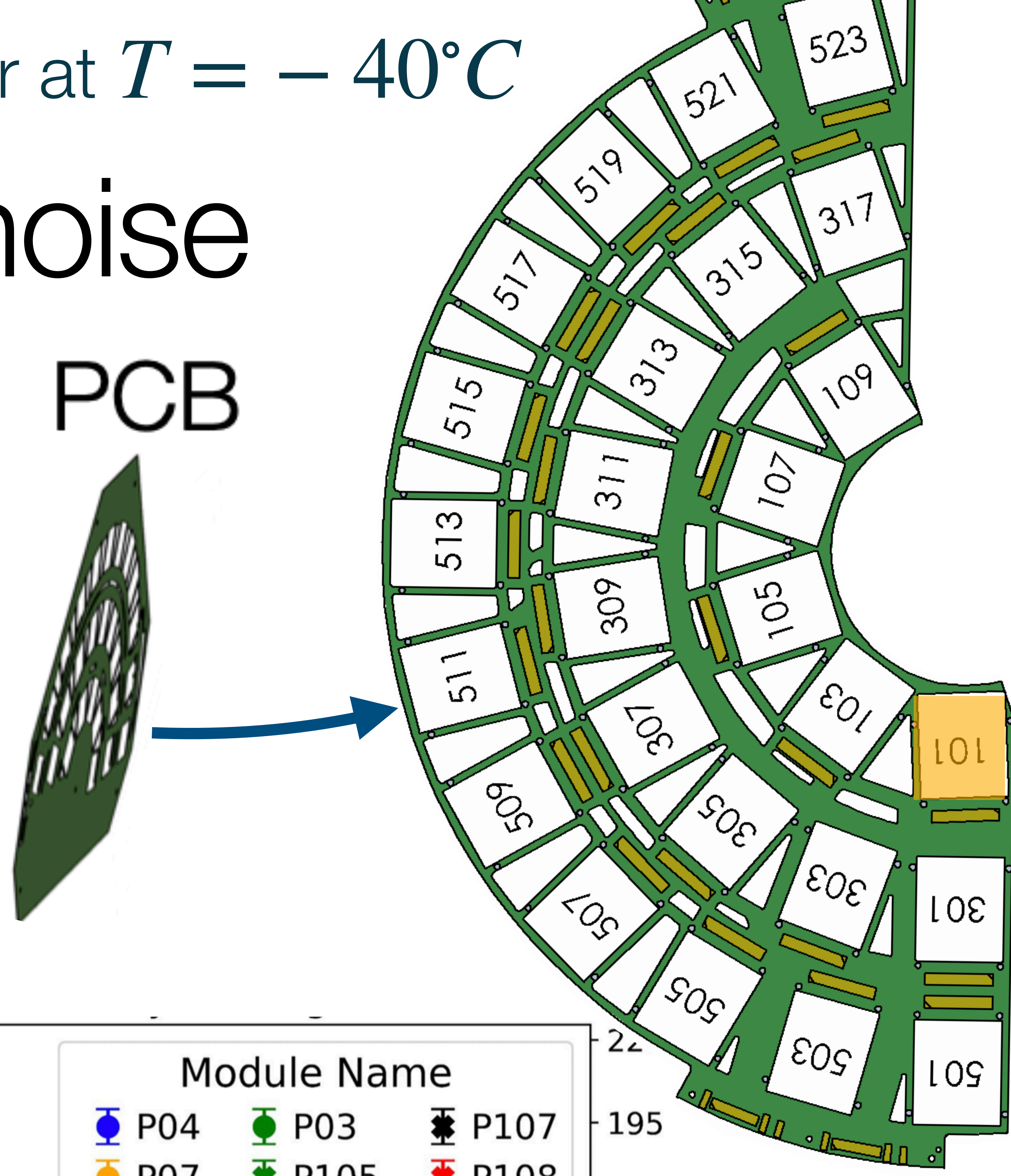
setup at University of Zurich

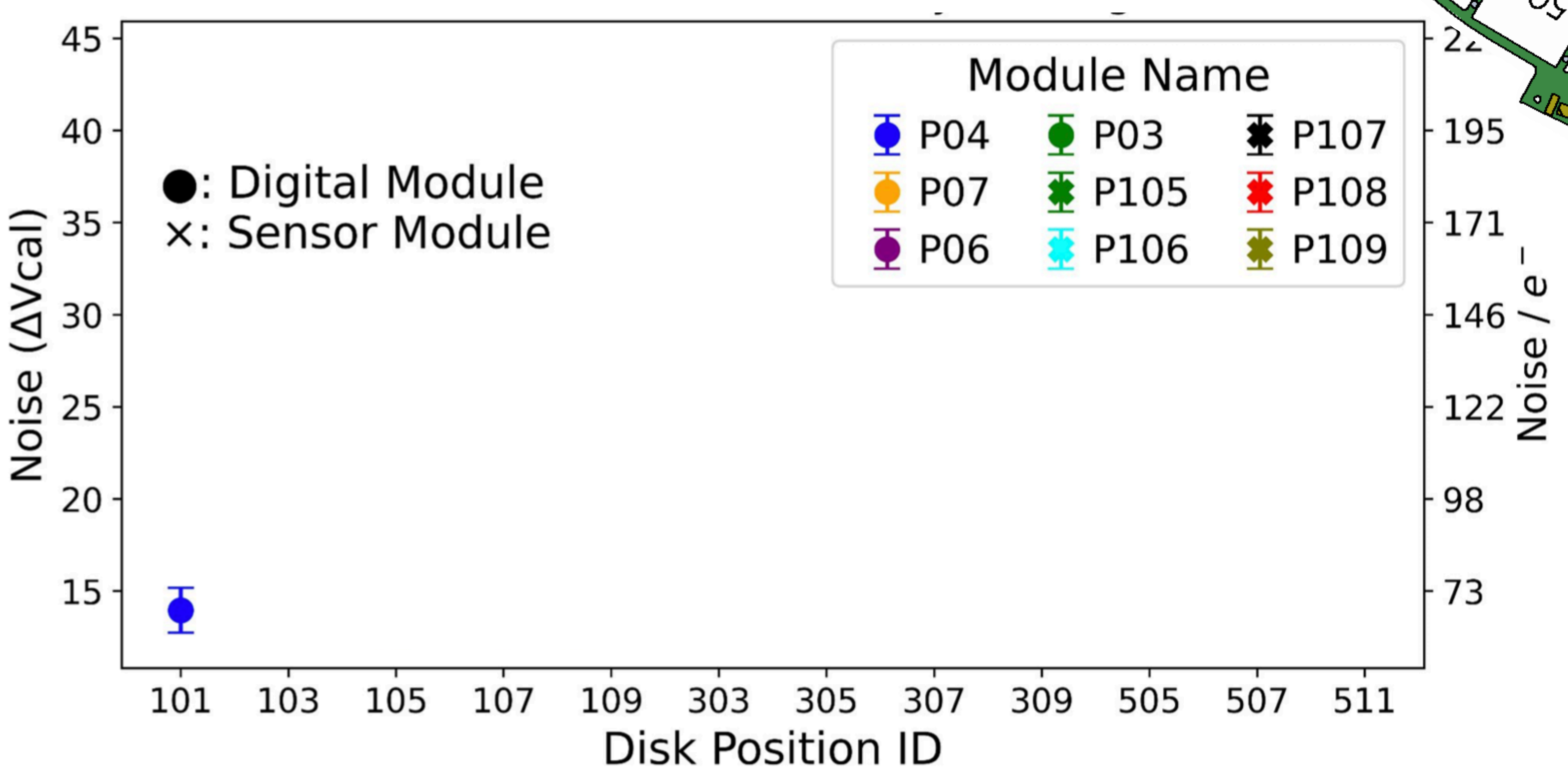


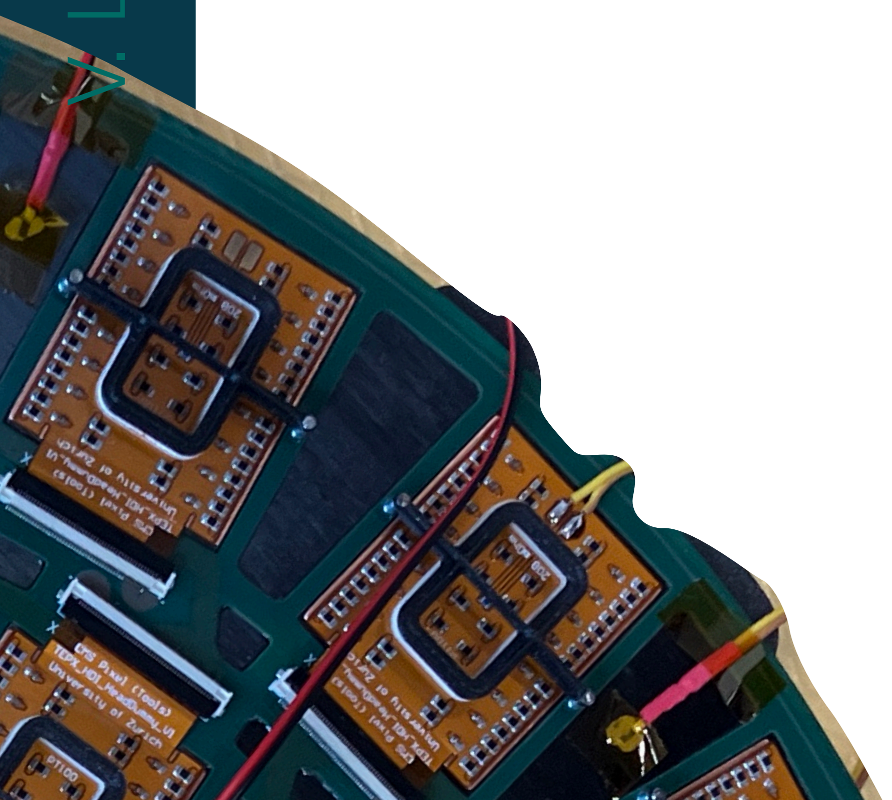
climate chamber at $T = -40^{\circ}C$

TEPX: PCB tests - threshold and noise



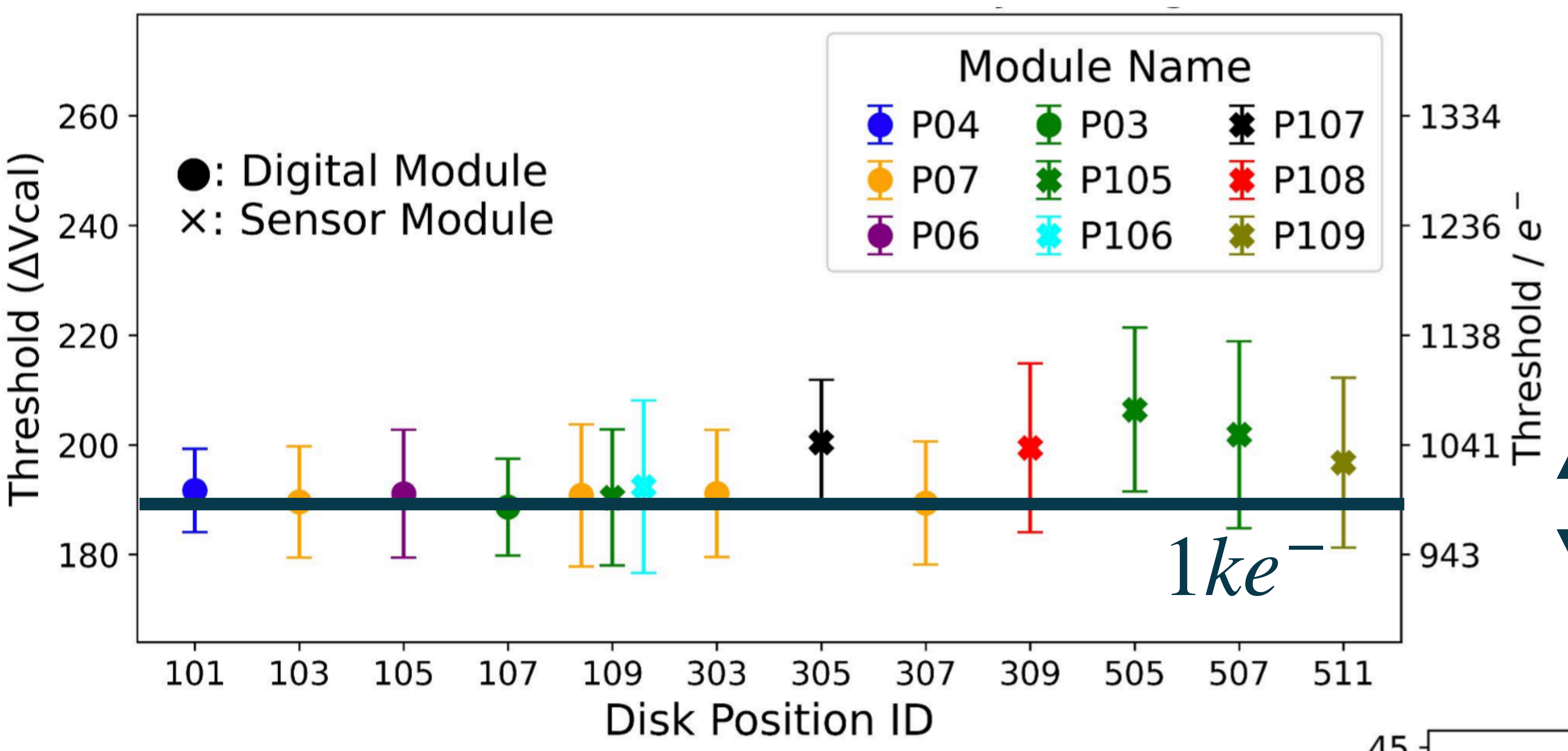




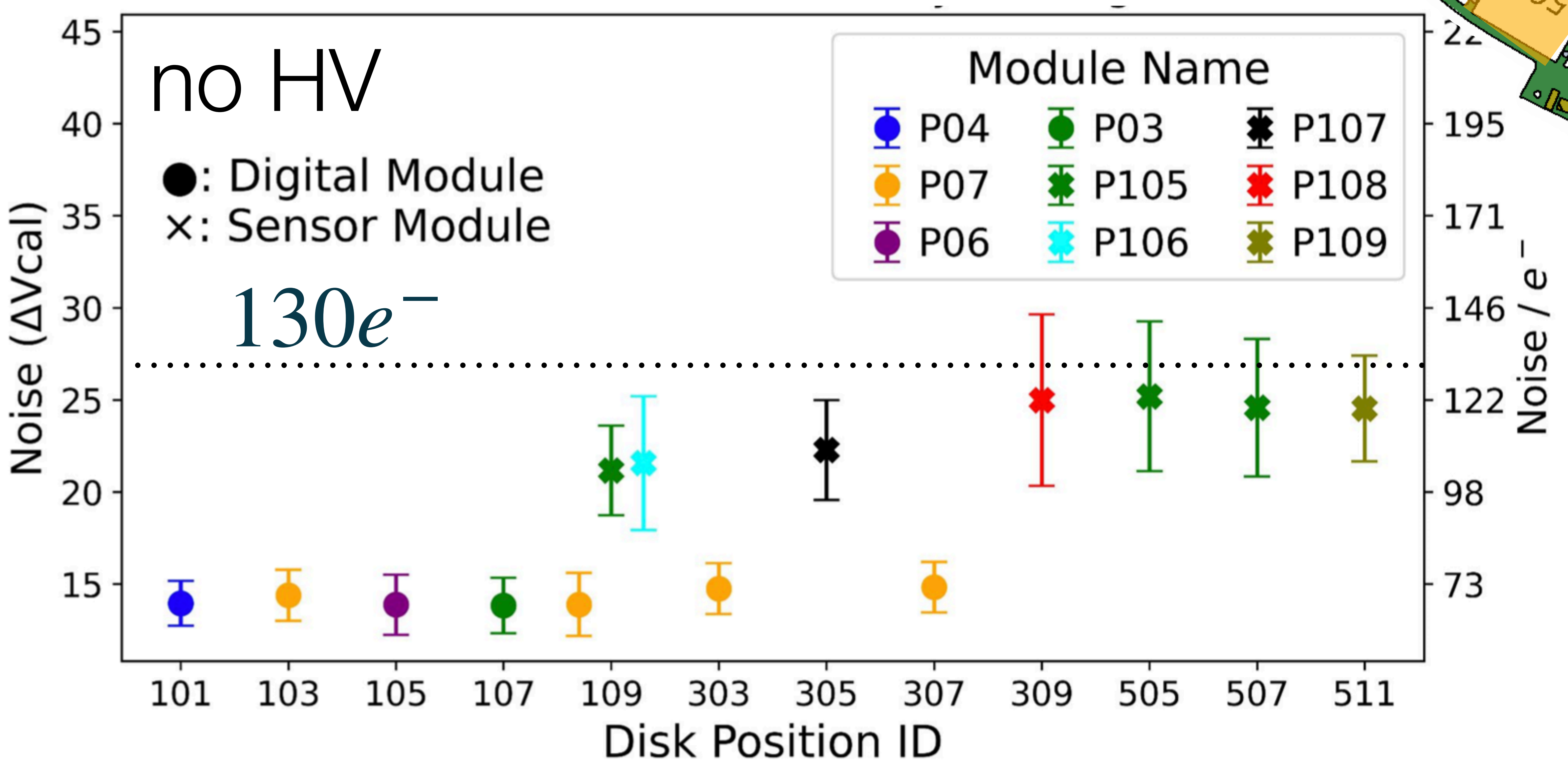


climate chamber at $T = -40°C$

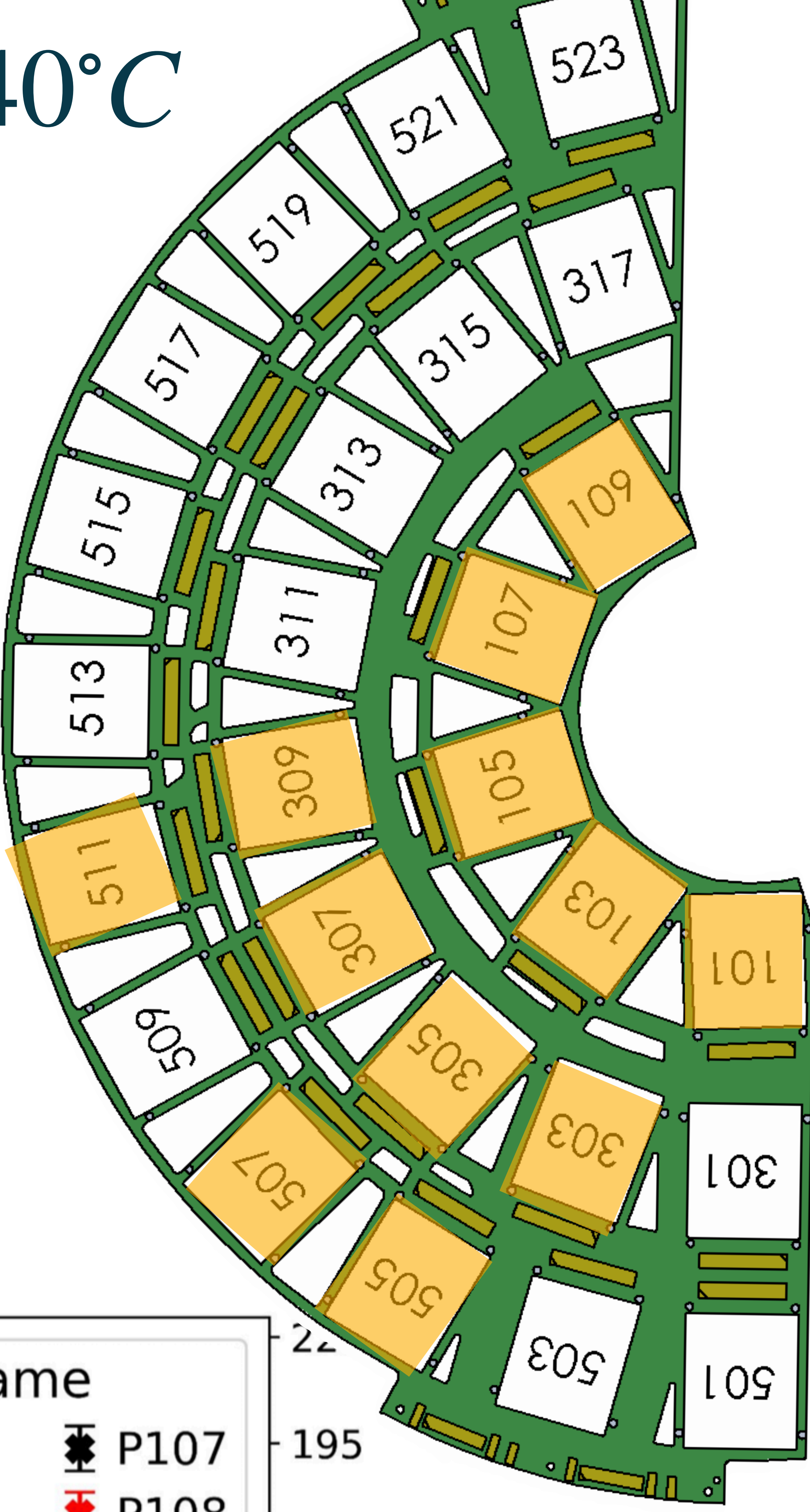
TEPX: PCB tests - threshold and noise

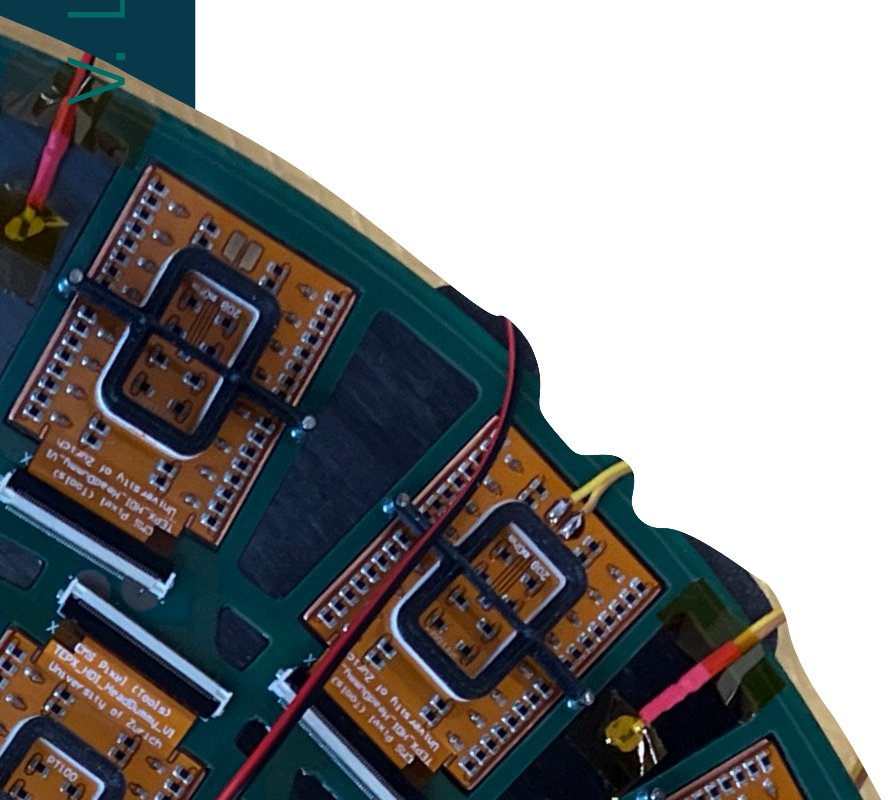


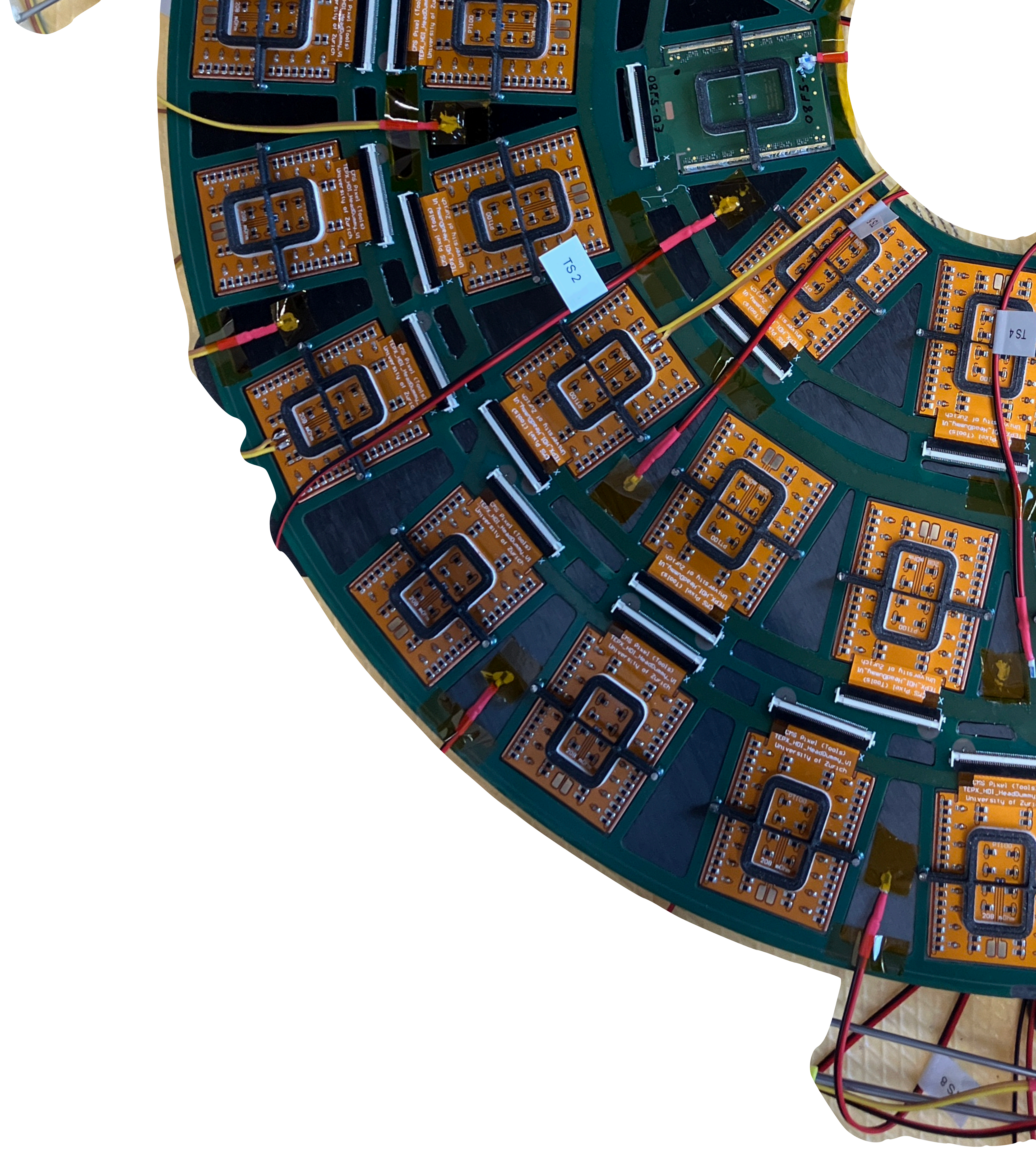
$max(\sigma) :\sim 80e^-$
for sensor modules



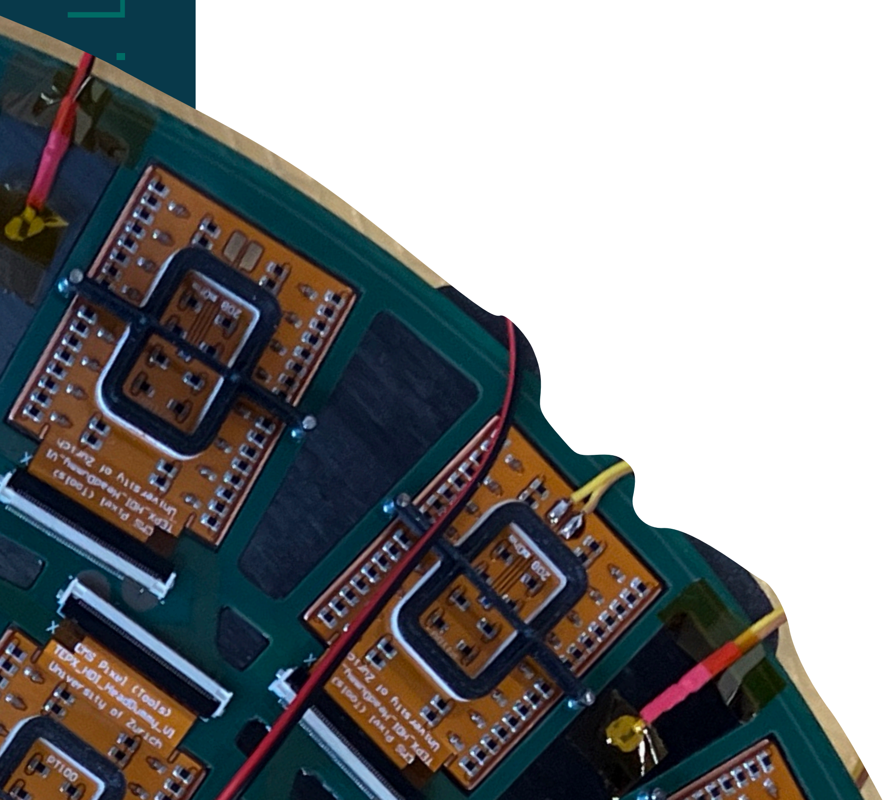
$\sim 30 - 50e^-$





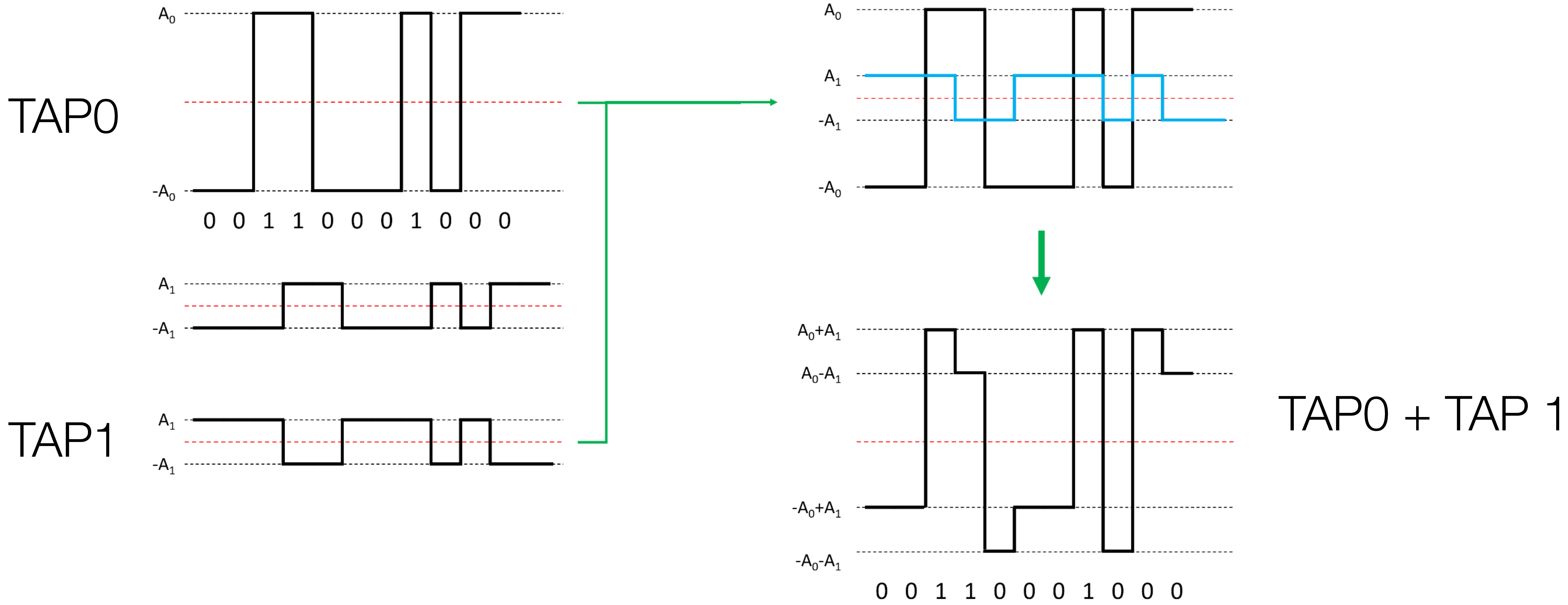


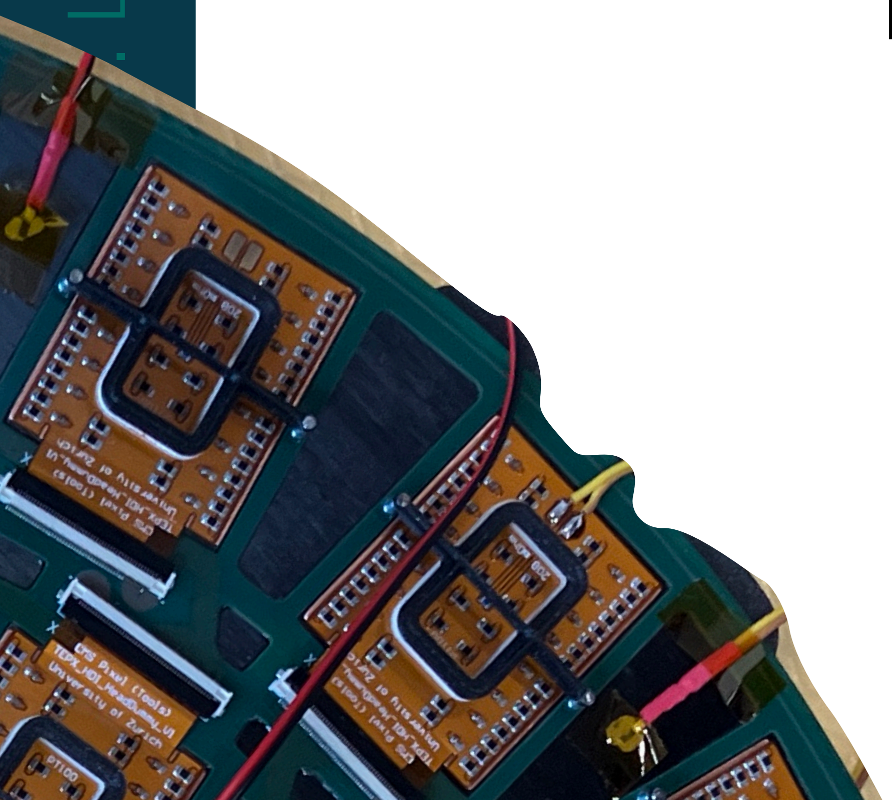
2. Data chain tests



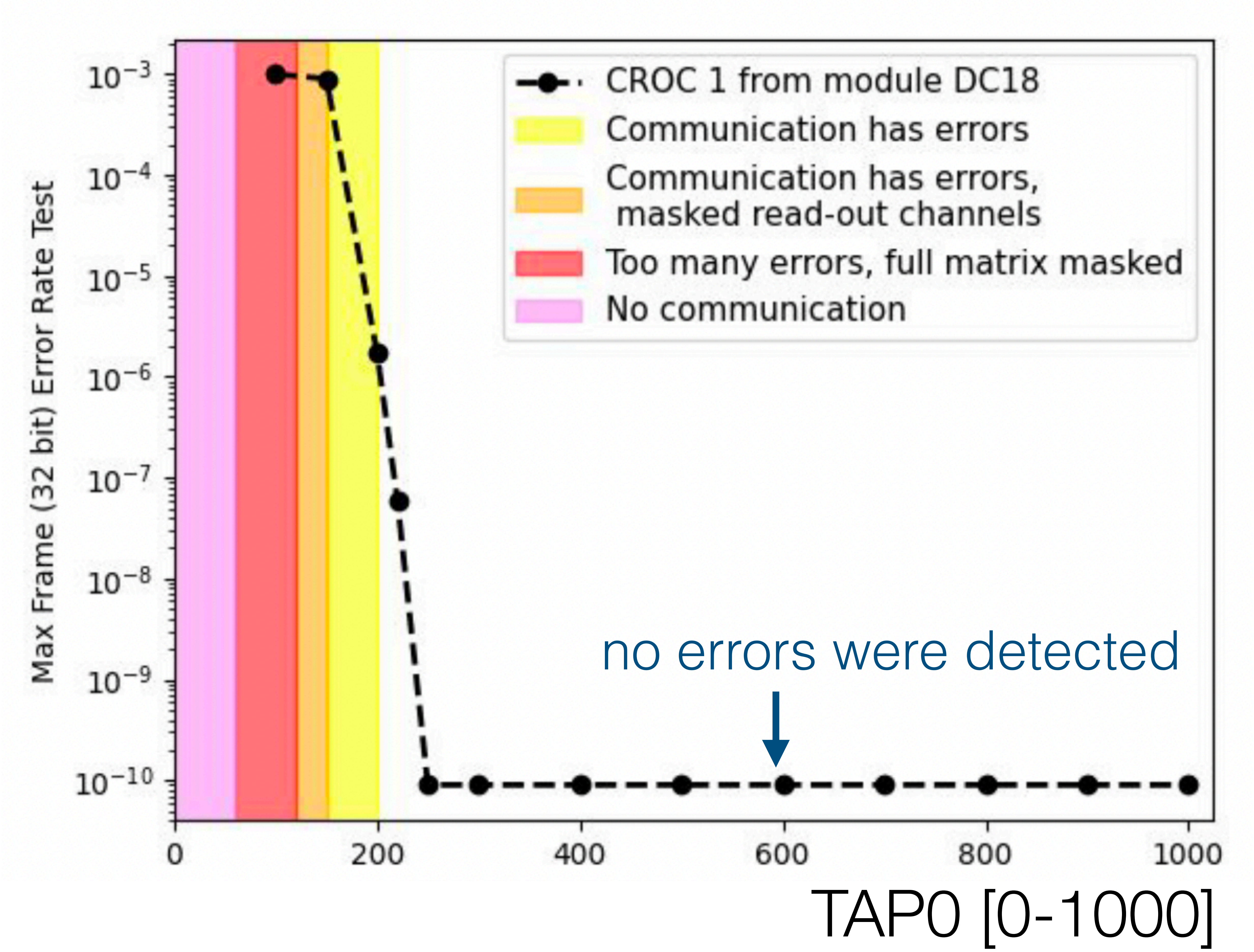
Signal pre-emphasis = TAPs

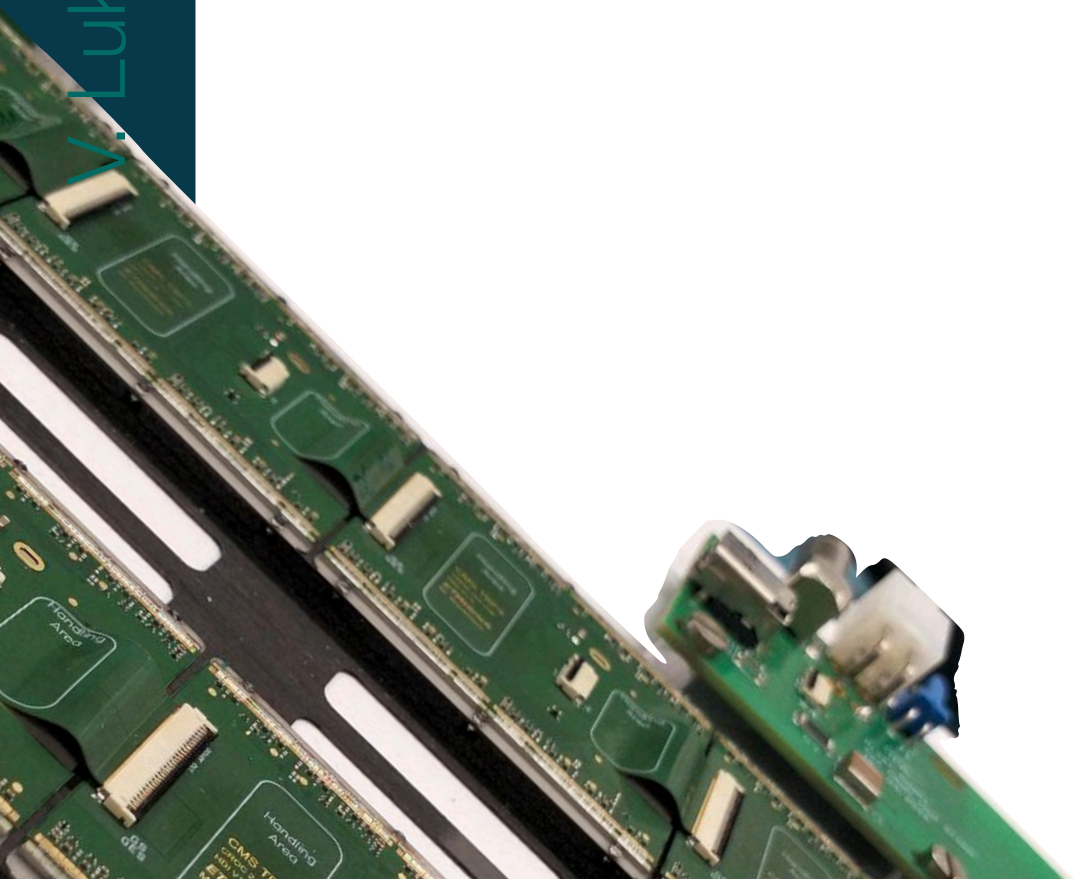
Can set pre-emphasis via three switches - TAP0 (sets signal), TAP1, TAP2





TBPX: data chain





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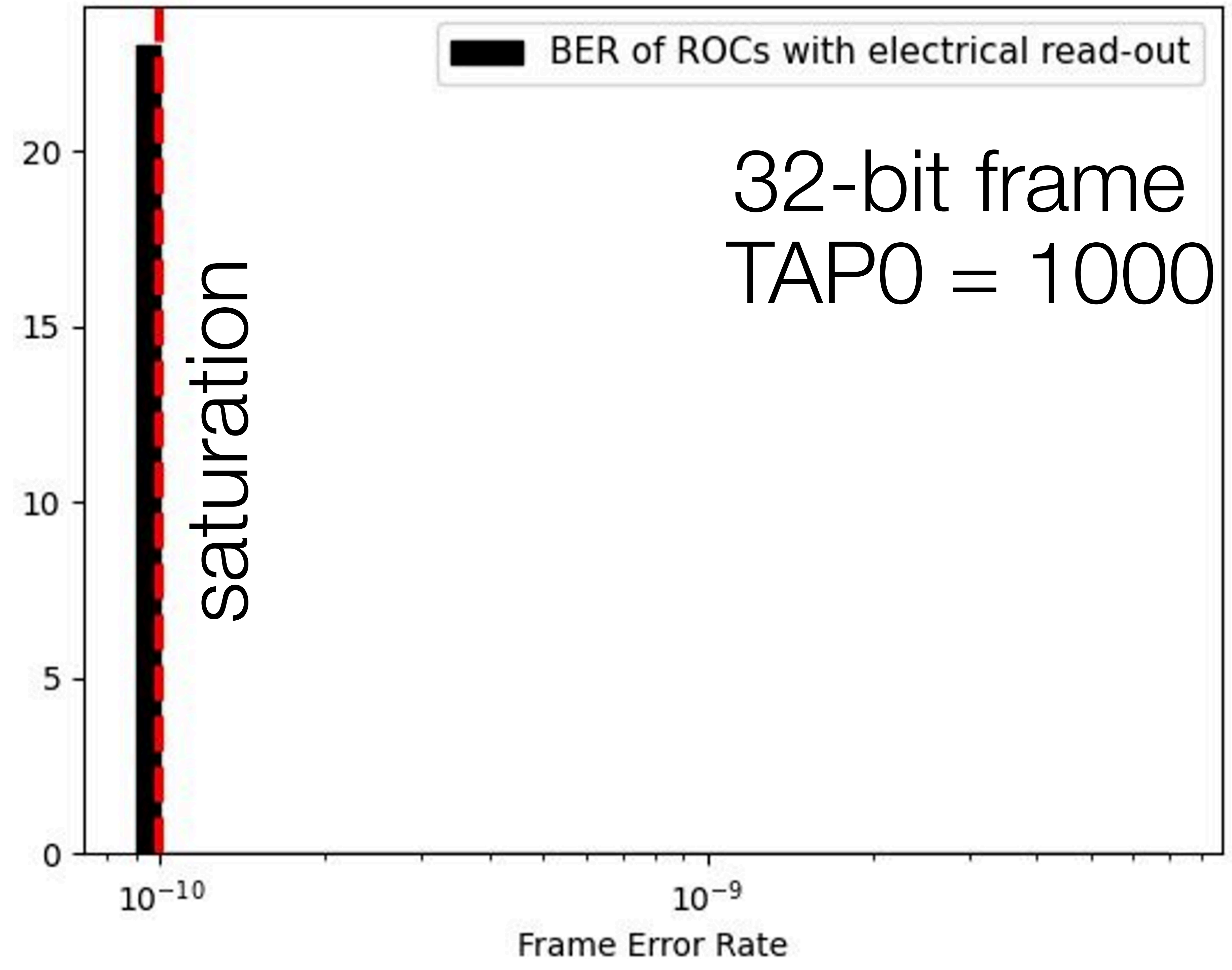
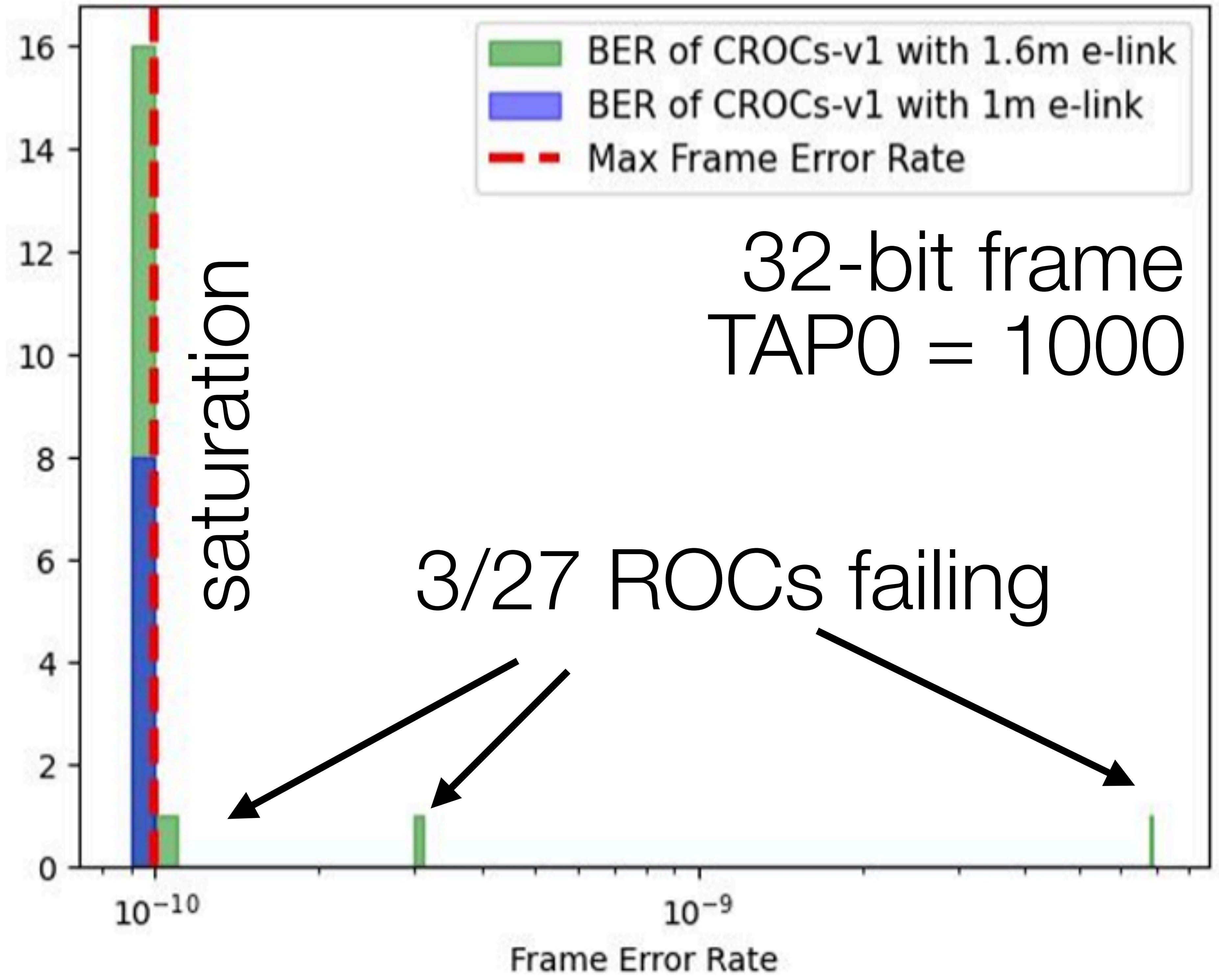
TBPX: data chain

Requirement: Bit Error Rate < 10^{-12}

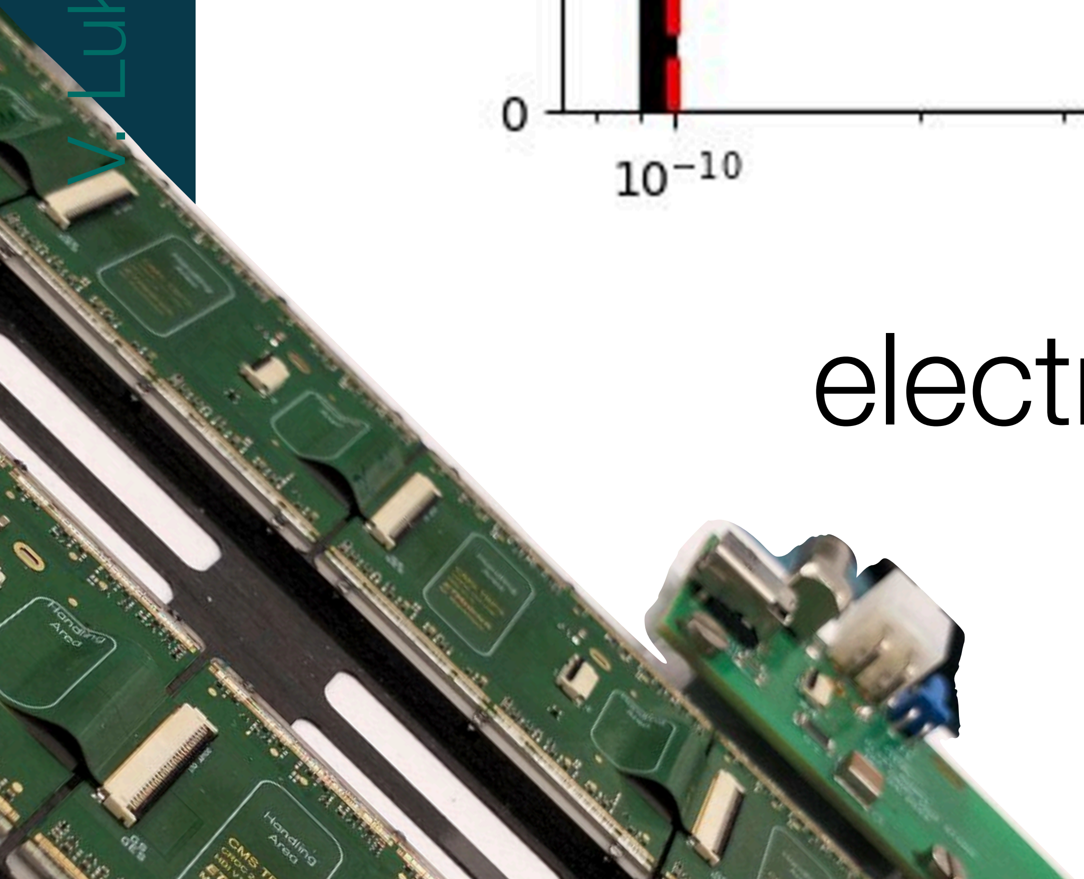


electrical readout

no pre-emphasis

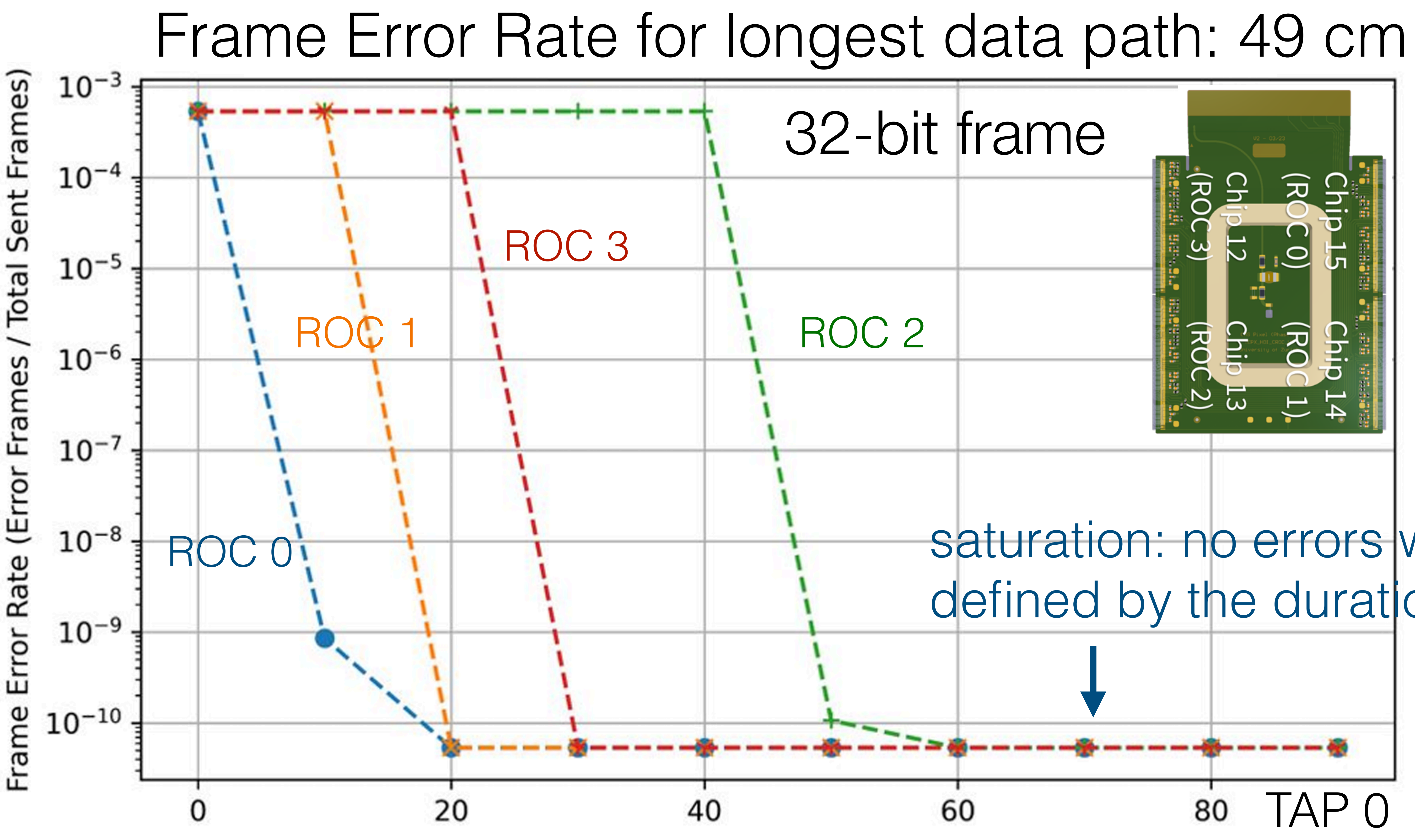


optical readout

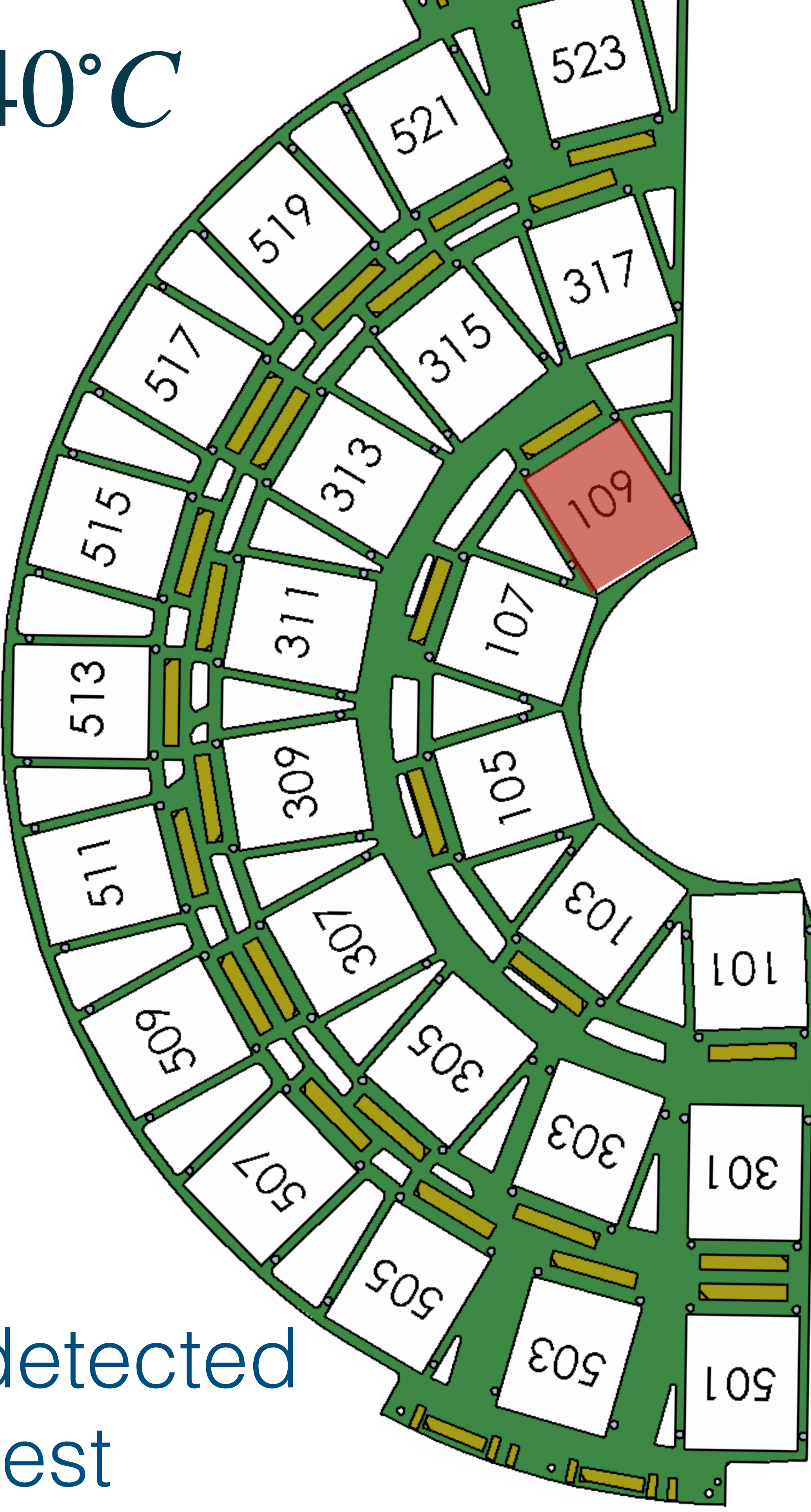


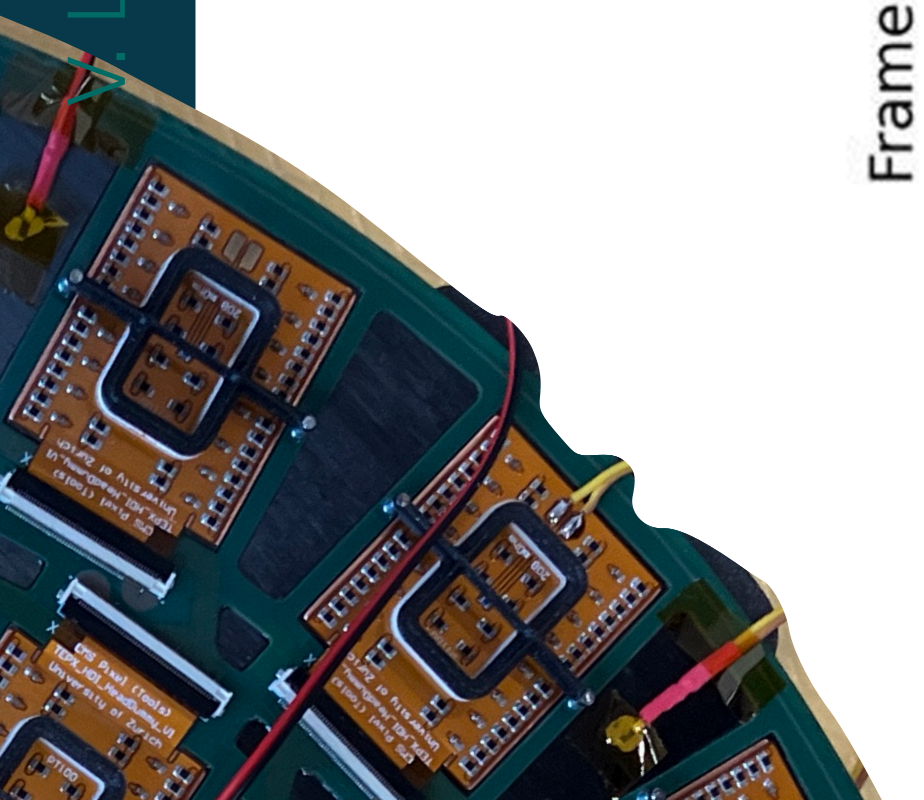
climate chamber at $T = -40^{\circ}C$

TEPX: PCB tests - data chain



saturation: no errors were detected
defined by the duration of test

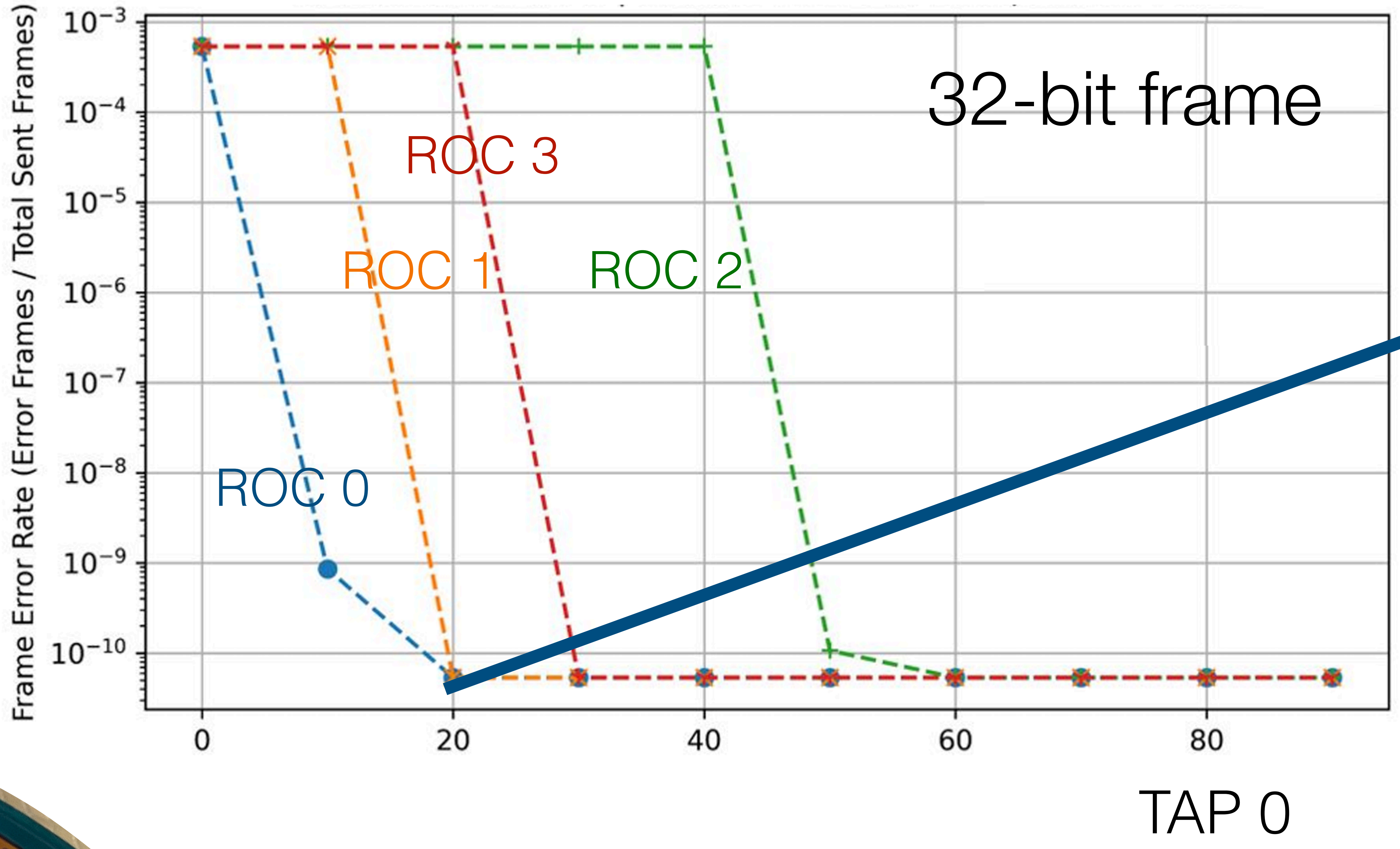


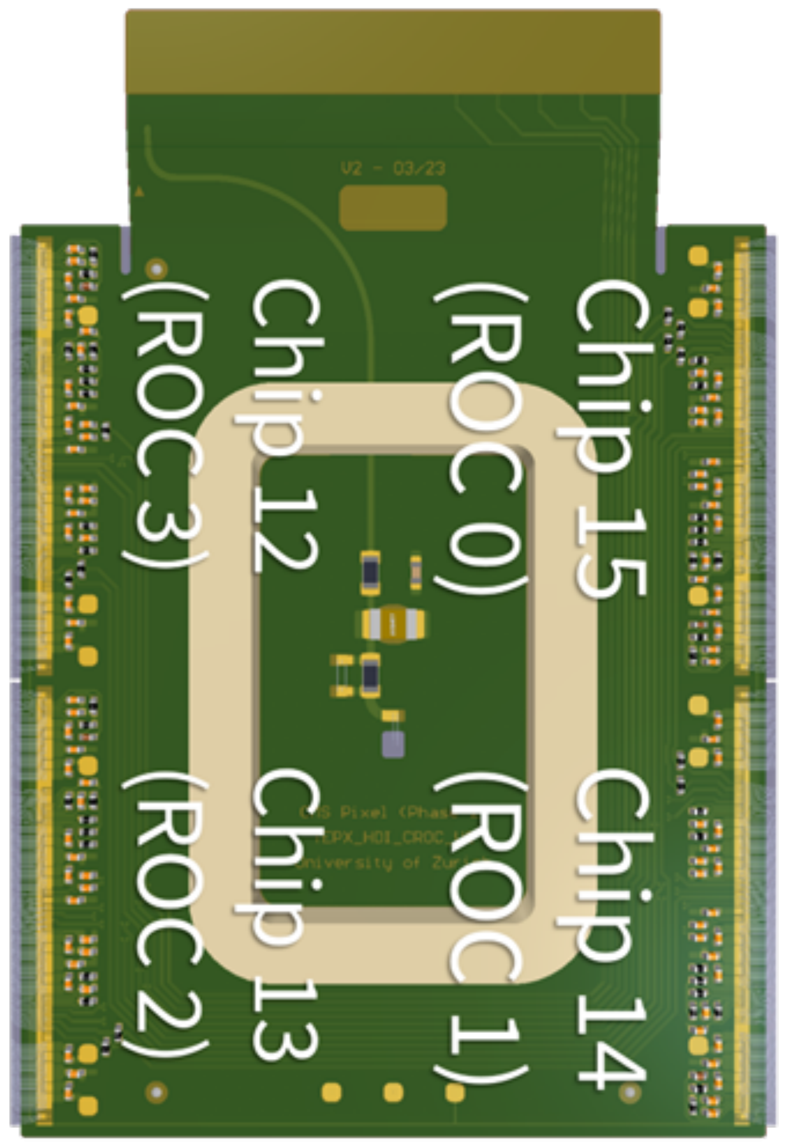


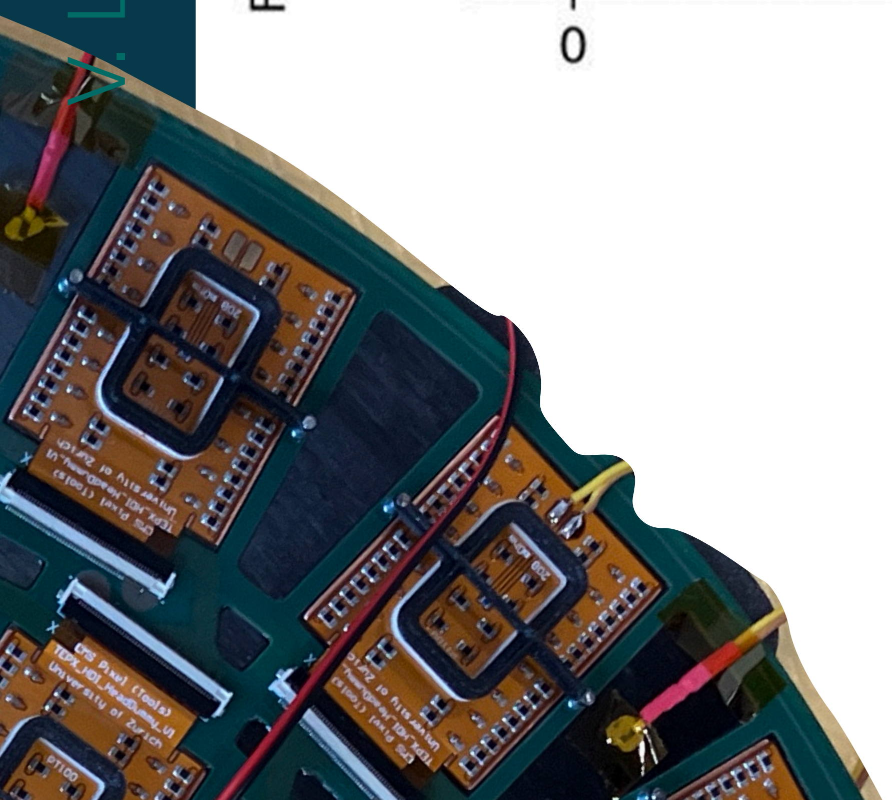
climate chamber at $T = -40°C$

TEPX: PCB tests - data chain

Chip 15 (ROC 0)
Chip 14 (ROC 1)
Chip 13 (ROC 2)
Chip 12 (ROC 3)

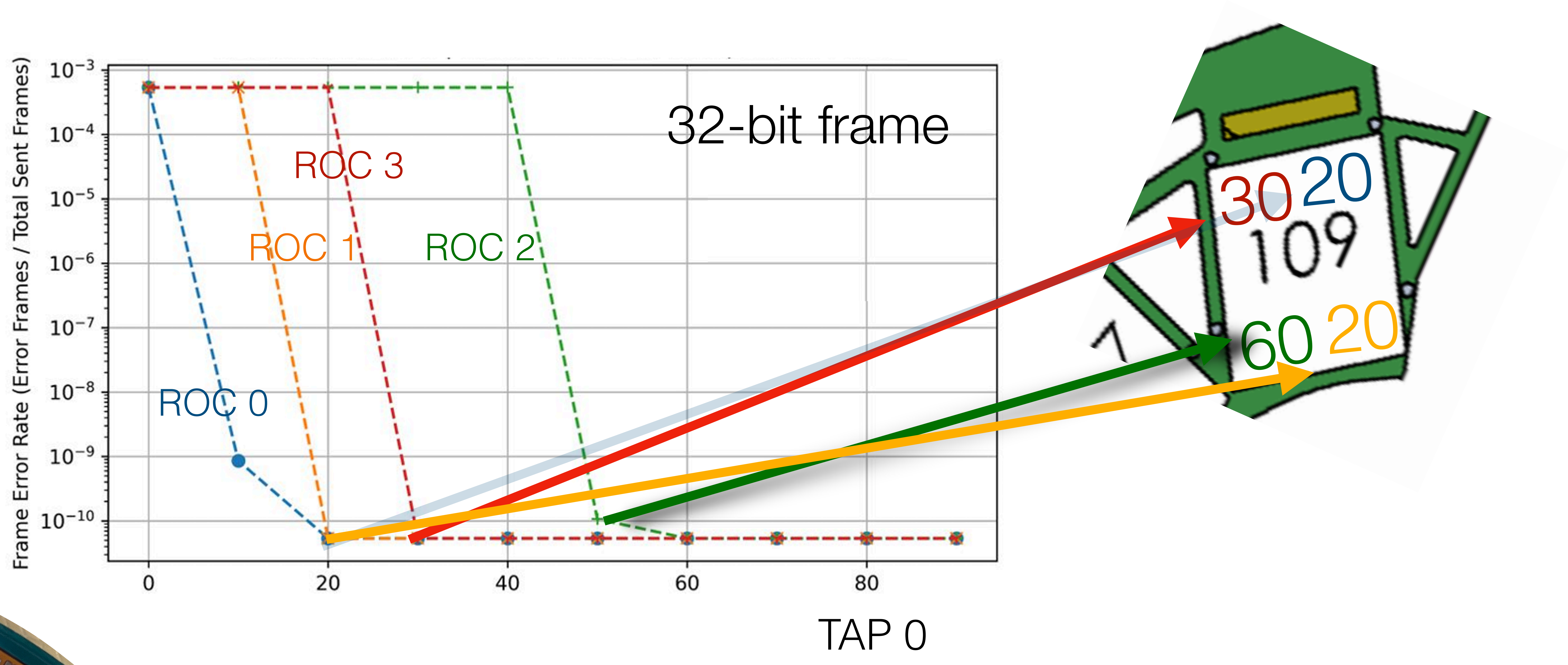


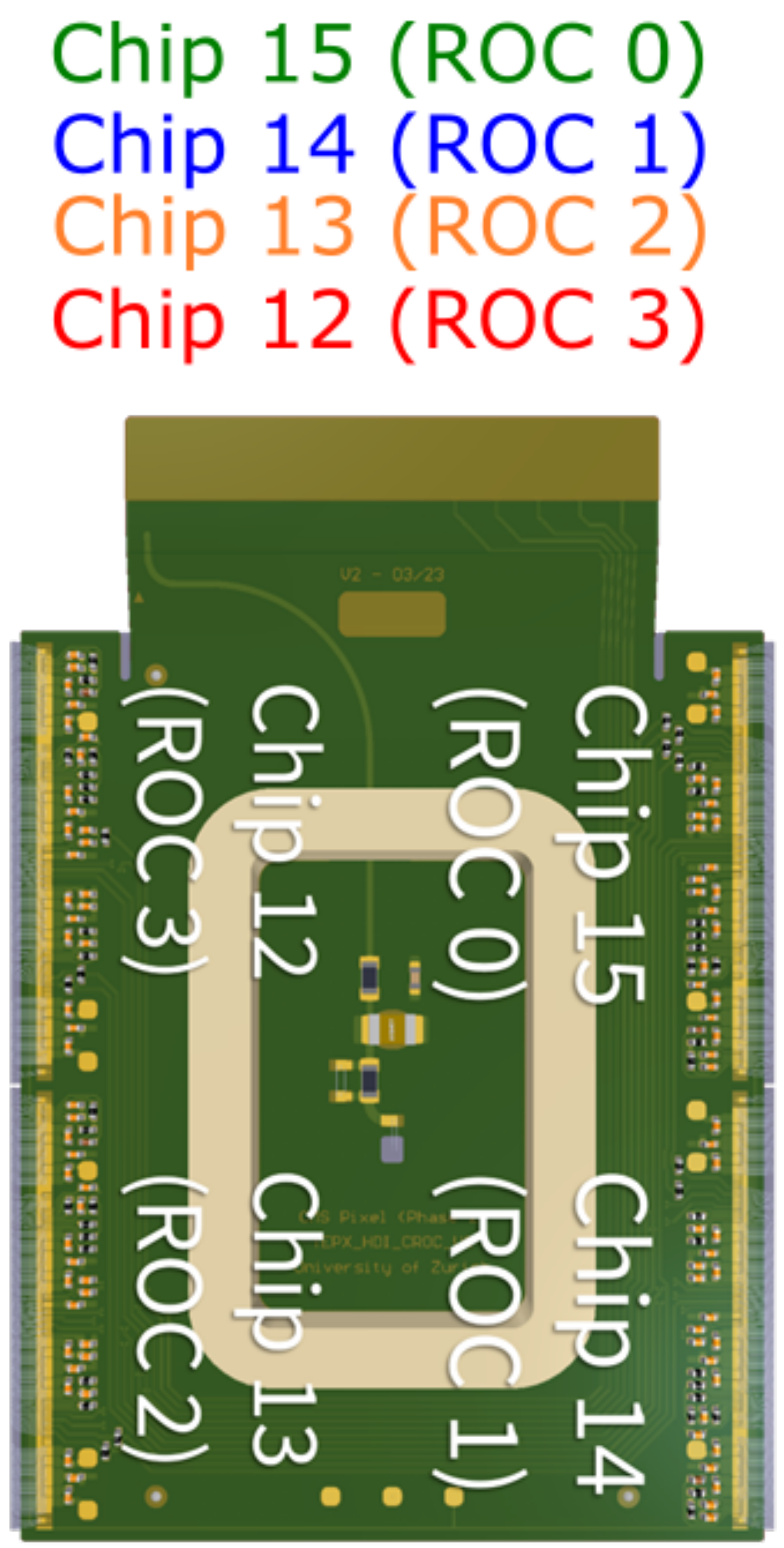


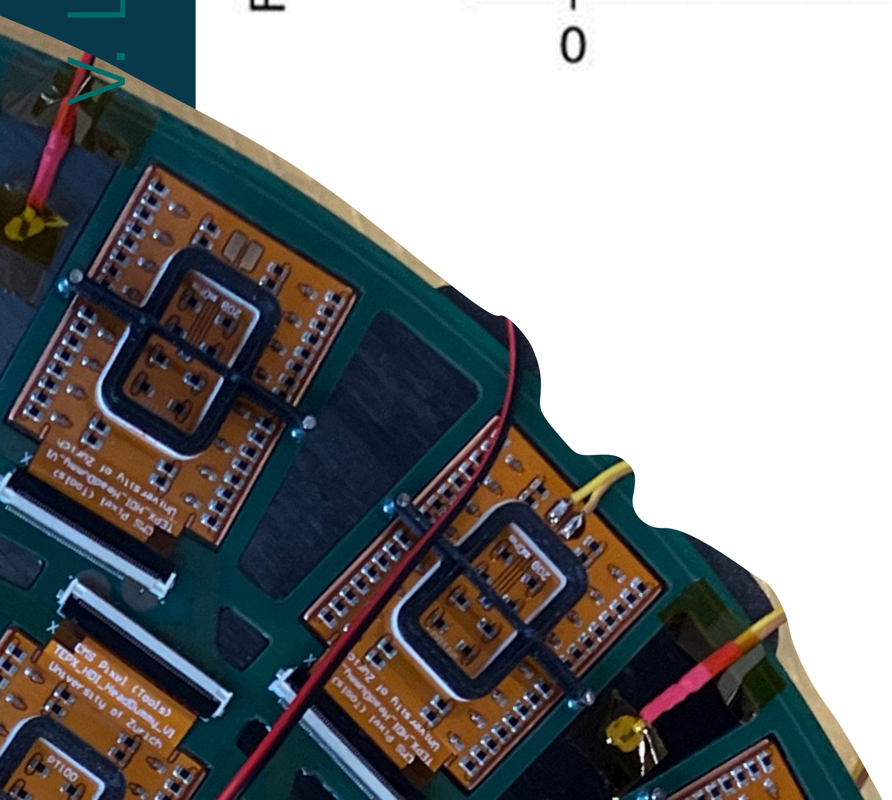


climate chamber at $T = -40^{\circ}C$

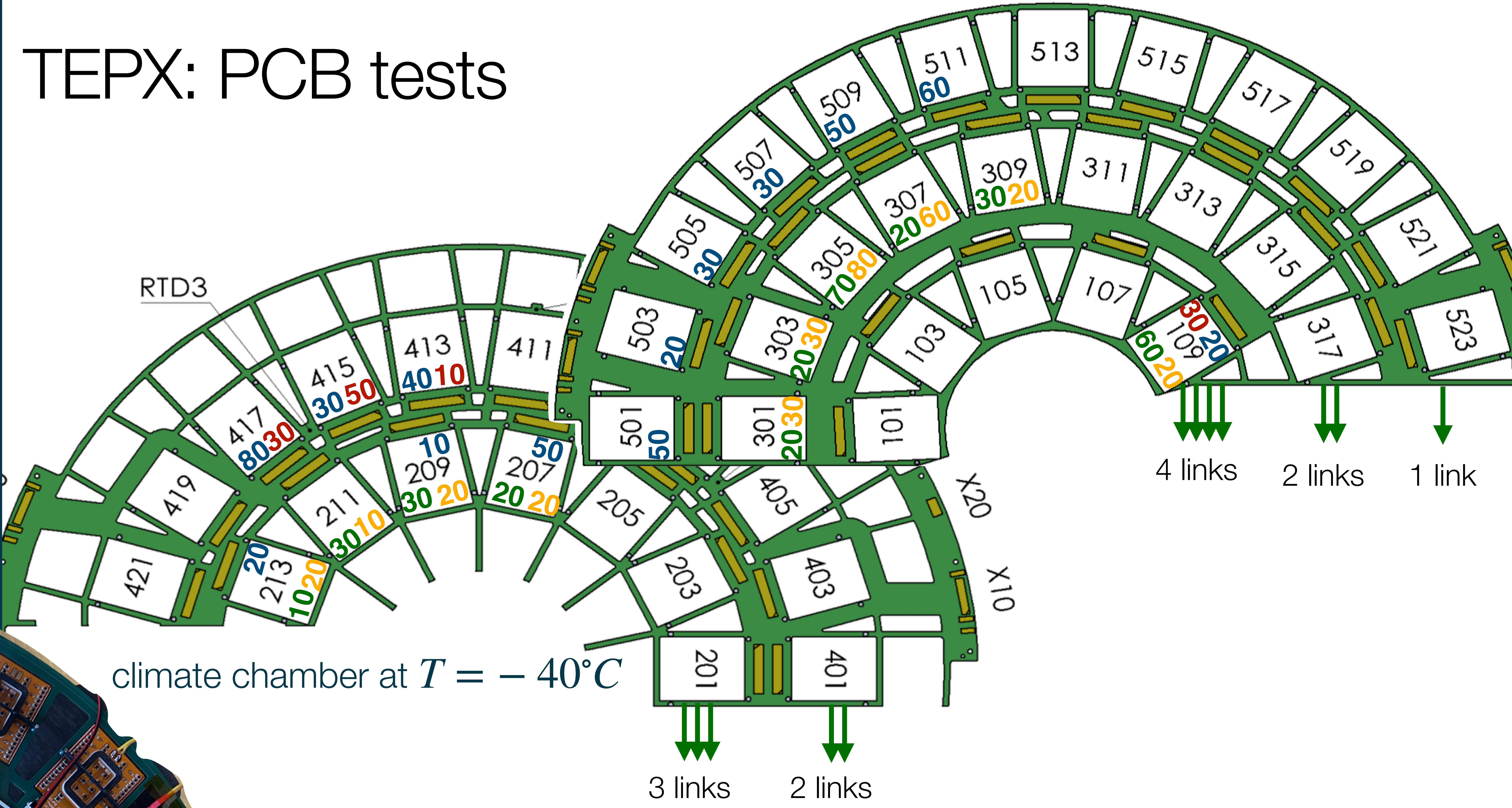
TEPX: PCB tests - data chain





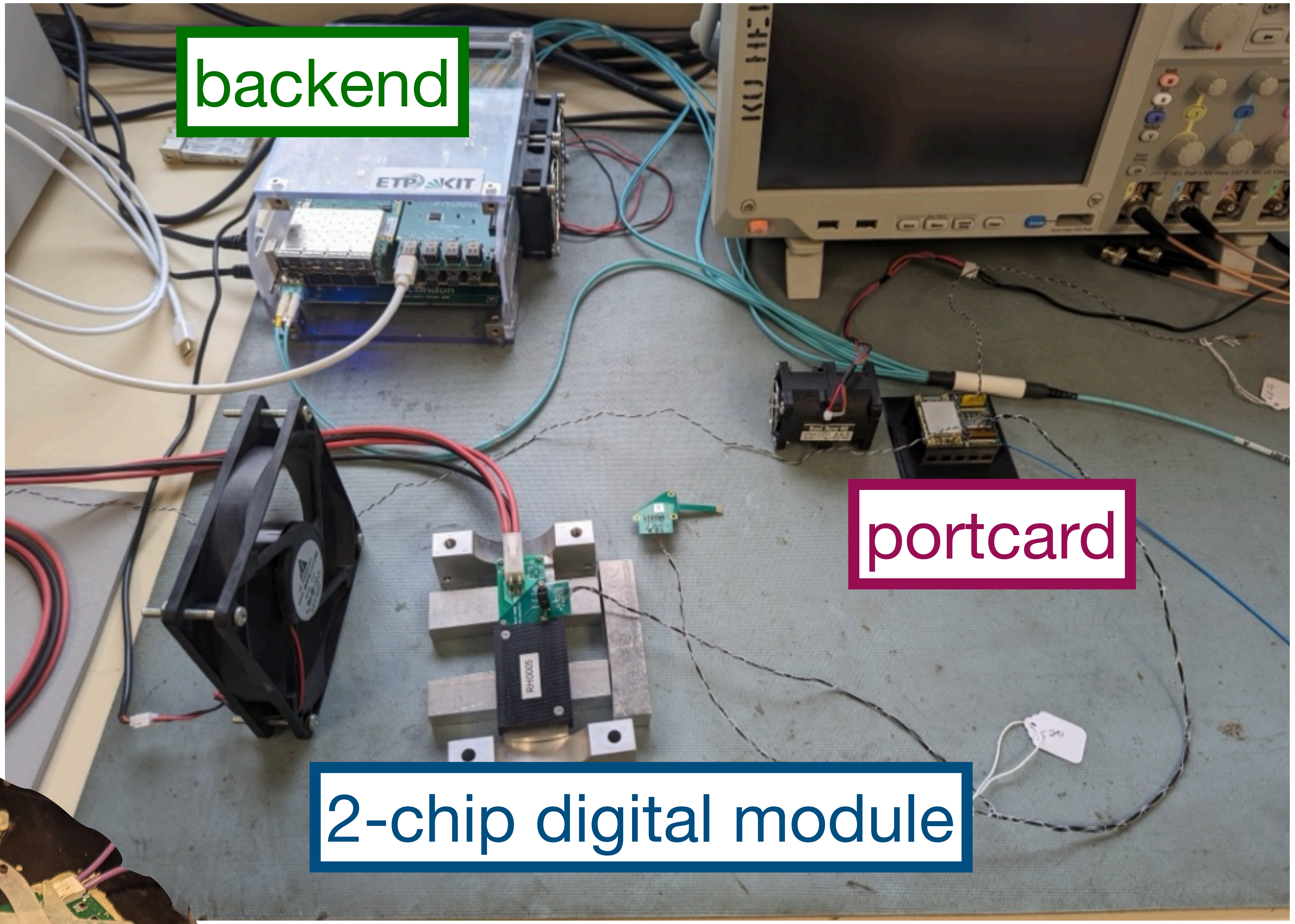


TEPX: PCB tests

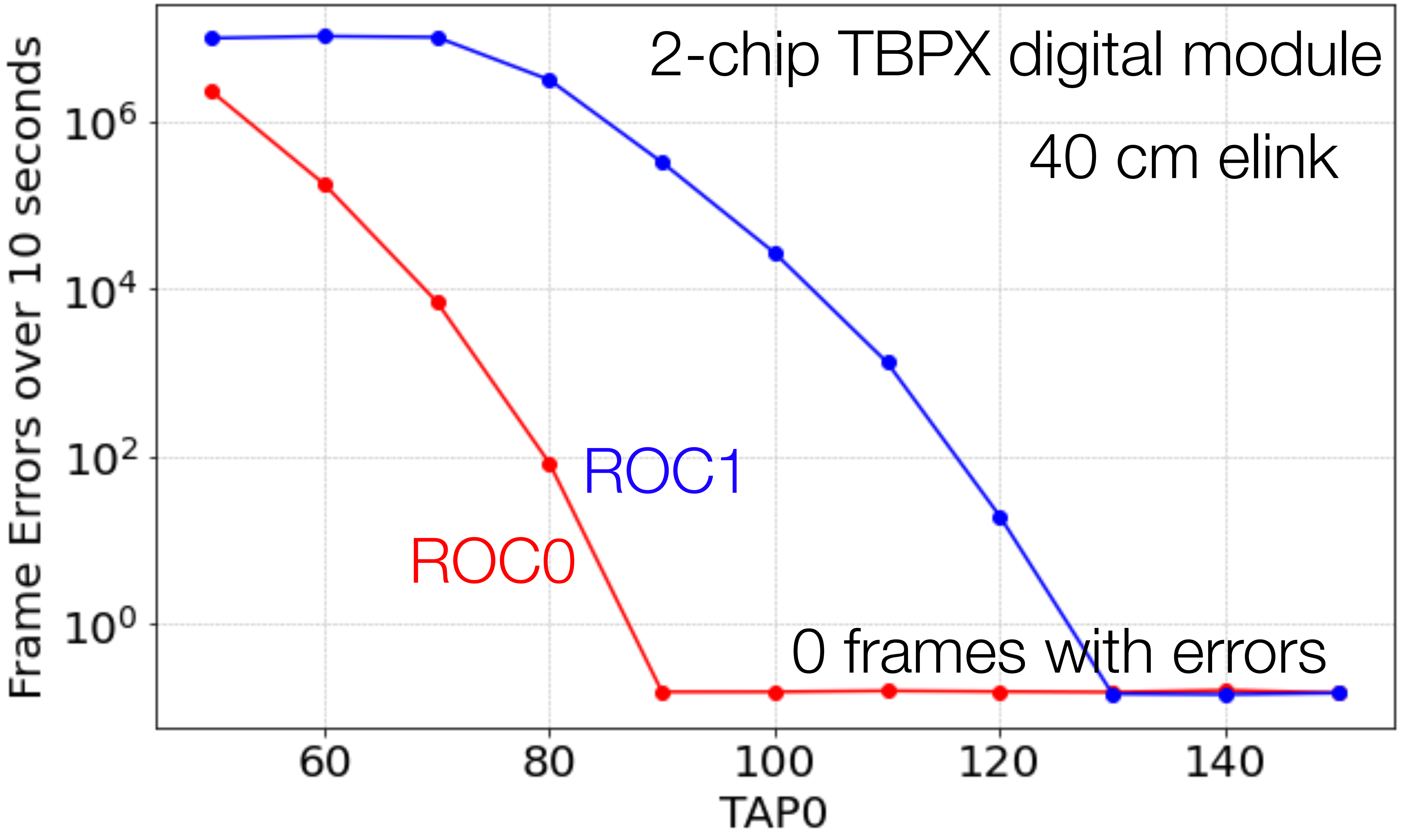


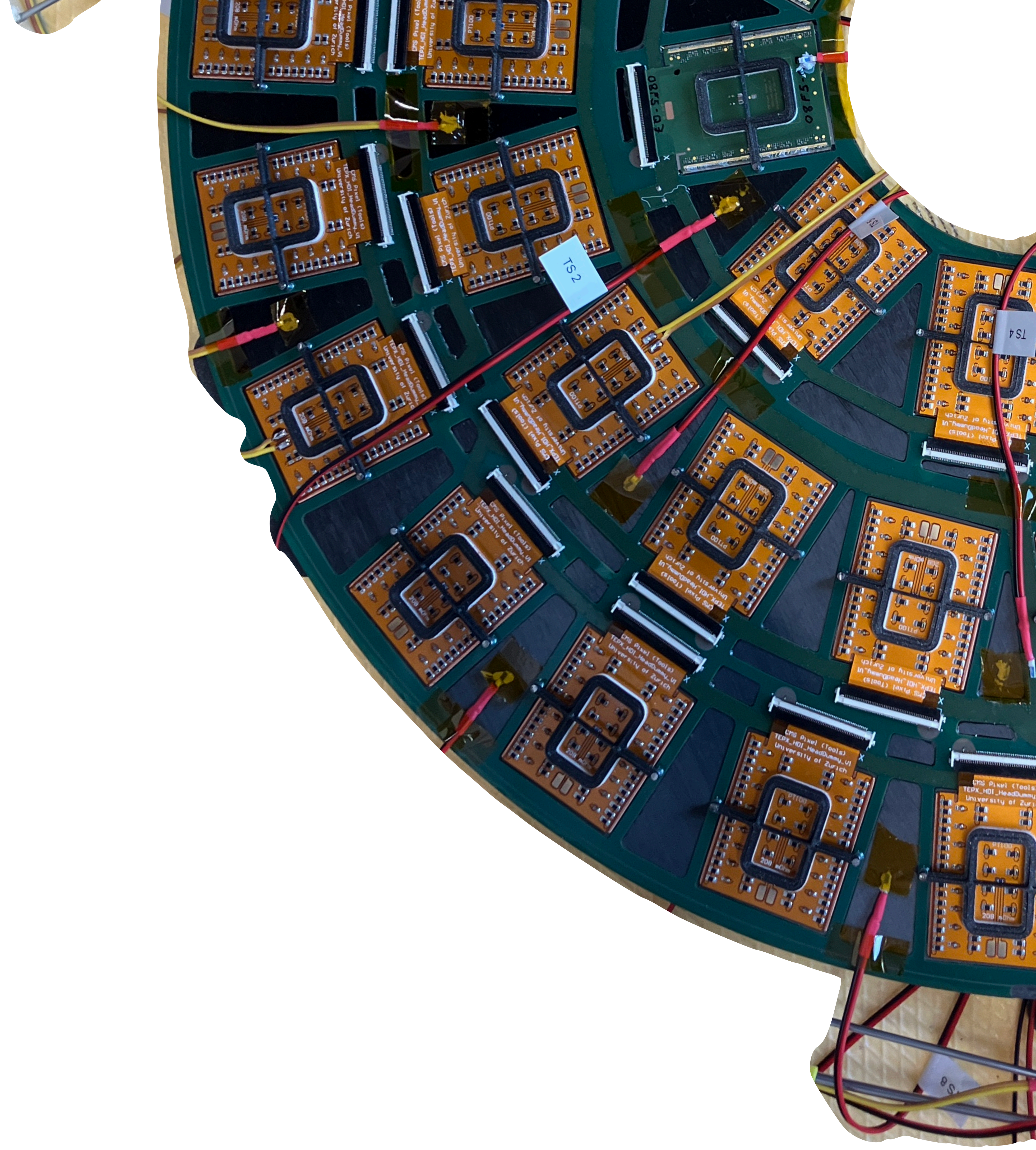
climate chamber at $T = -40°C$

TFPX: data chain tests

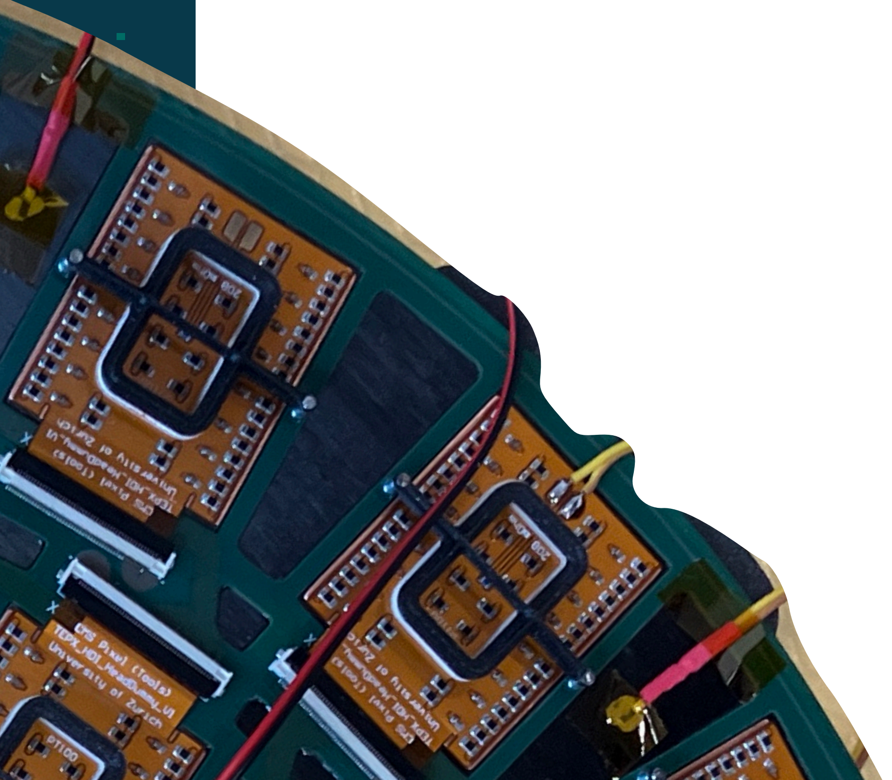


setup at Rice University





3. Thermal tests



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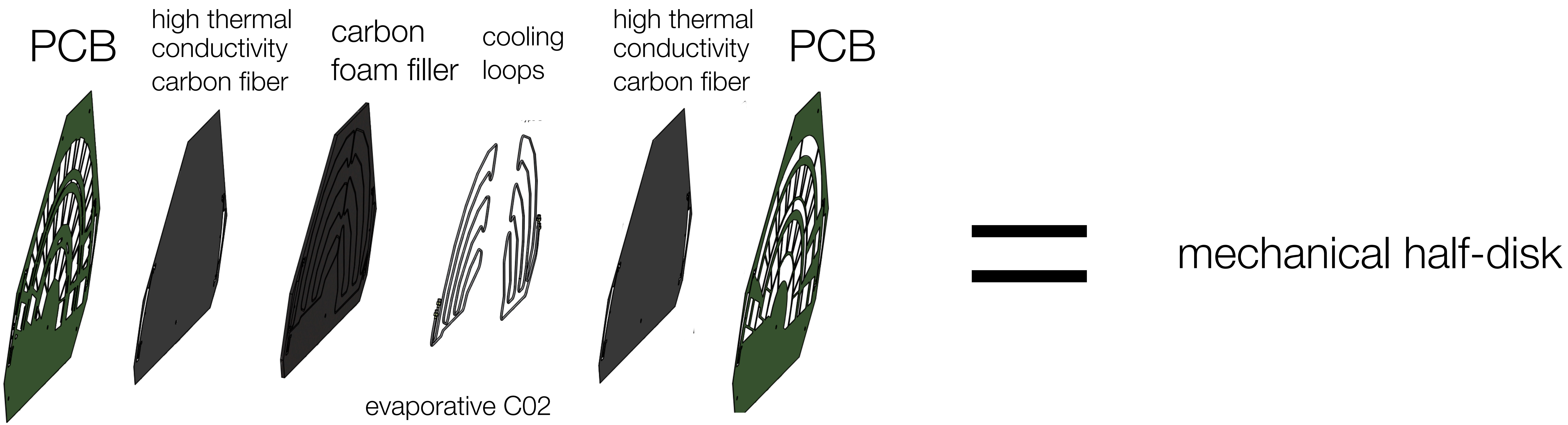
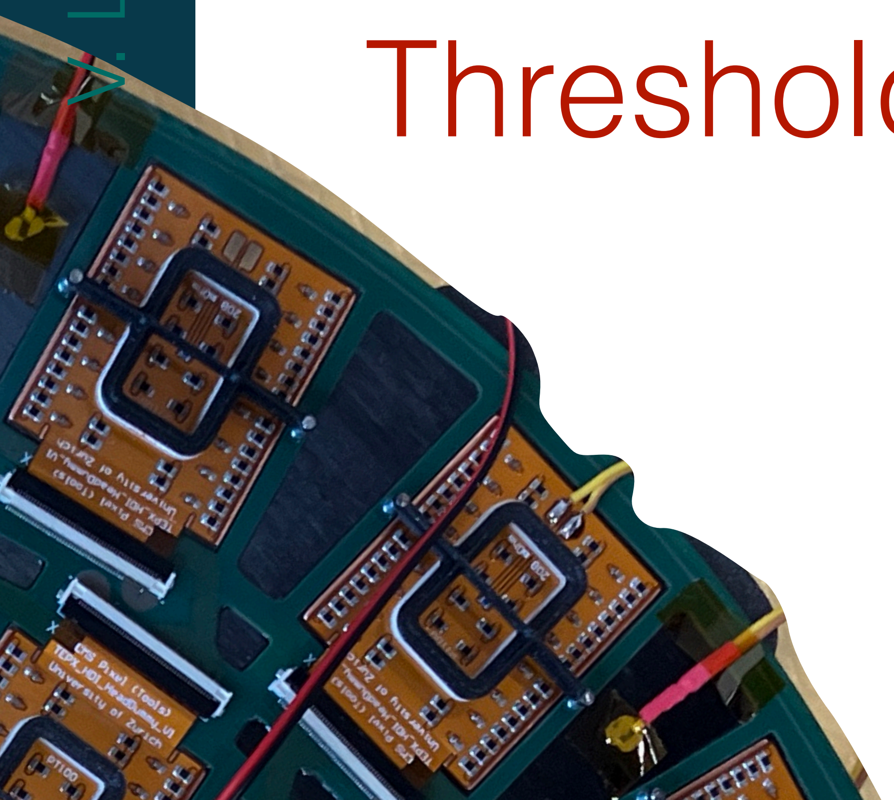
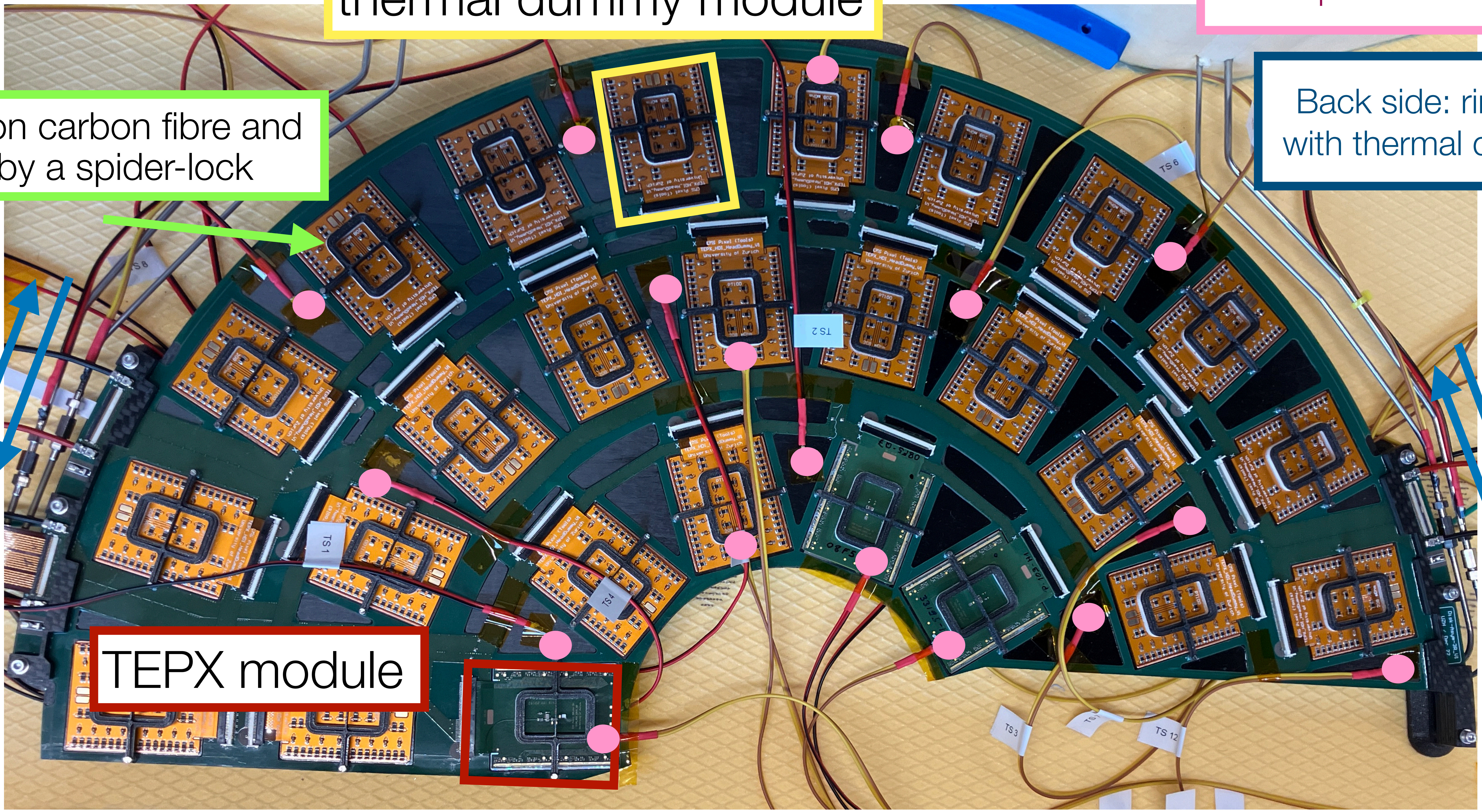
TEPX: mechanical Dee prototype

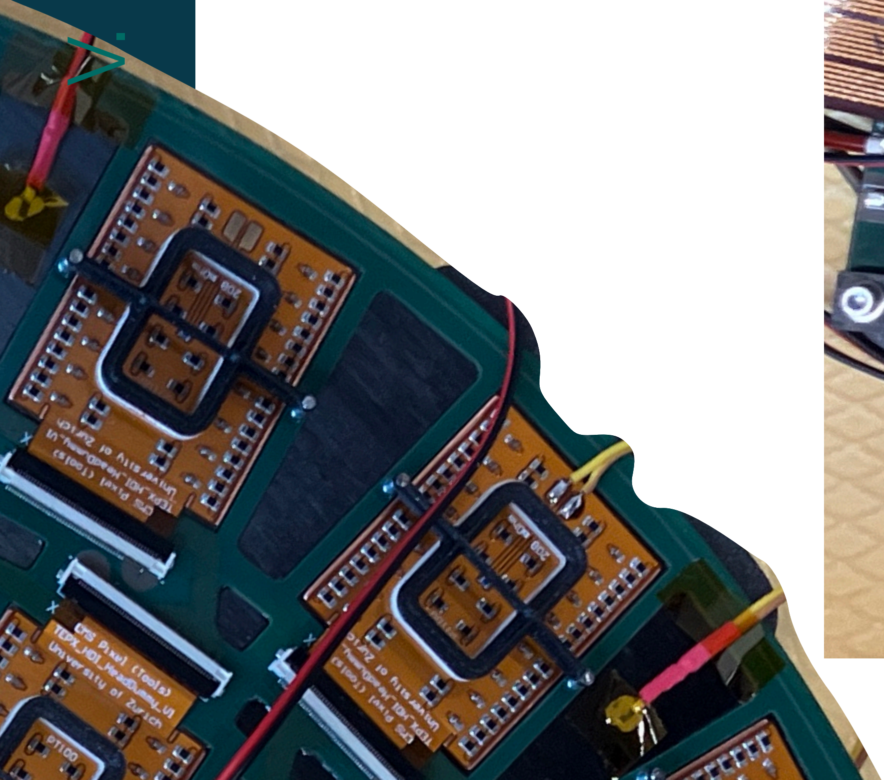


Threshold/noise and data tests: nothing surprising with respect to PCB tests



TEPX: mechanical Dee prototype

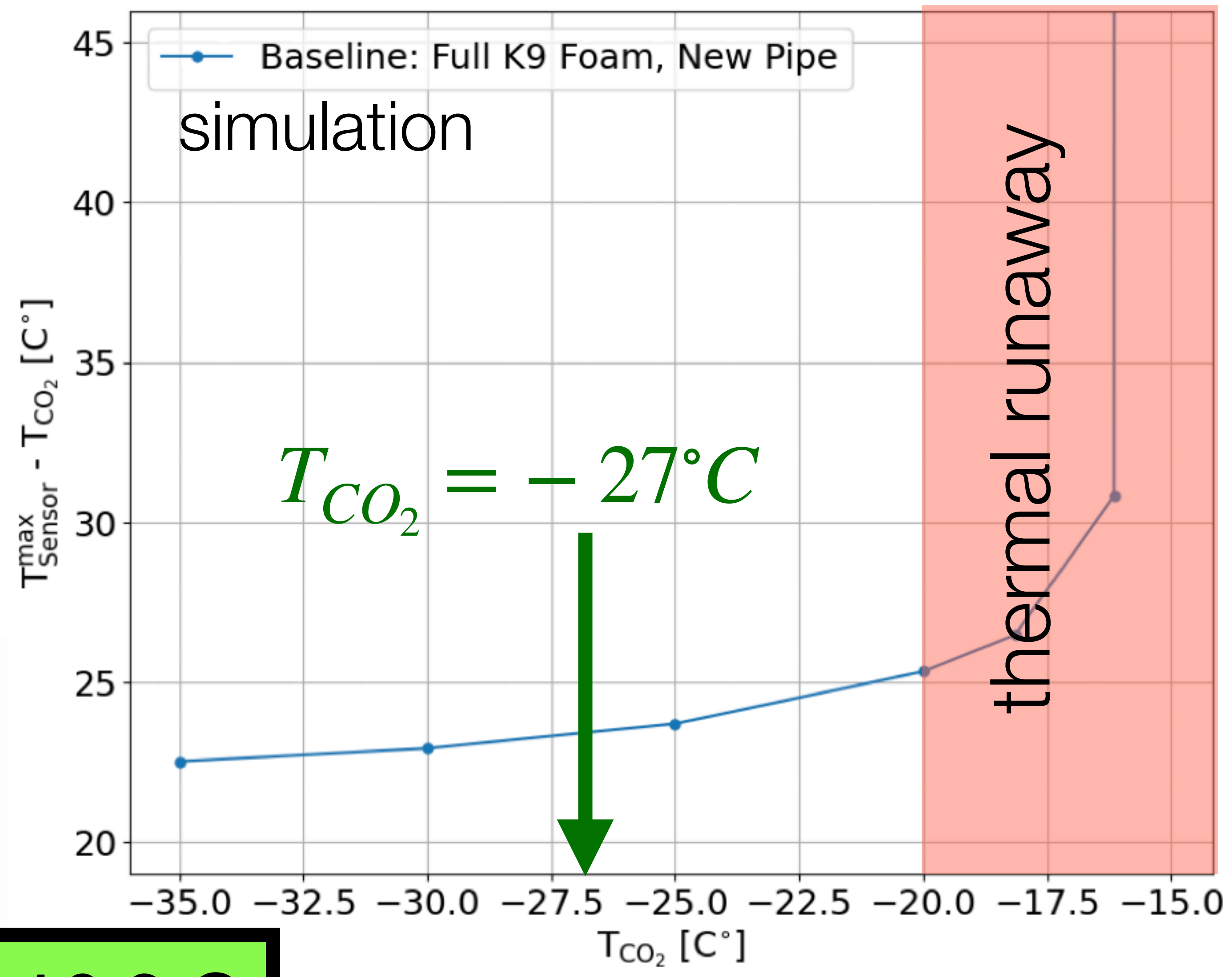




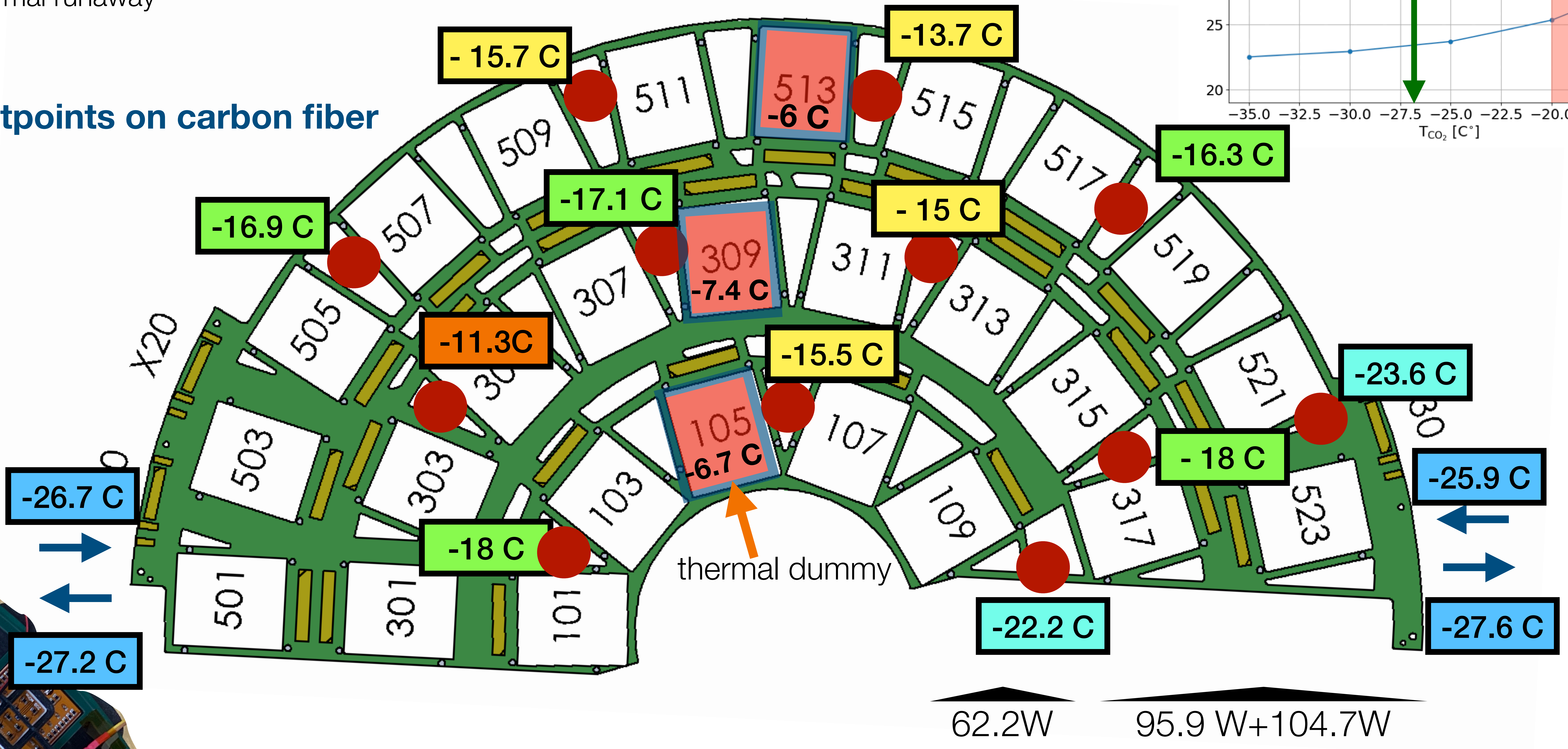
setup at University of Zurich

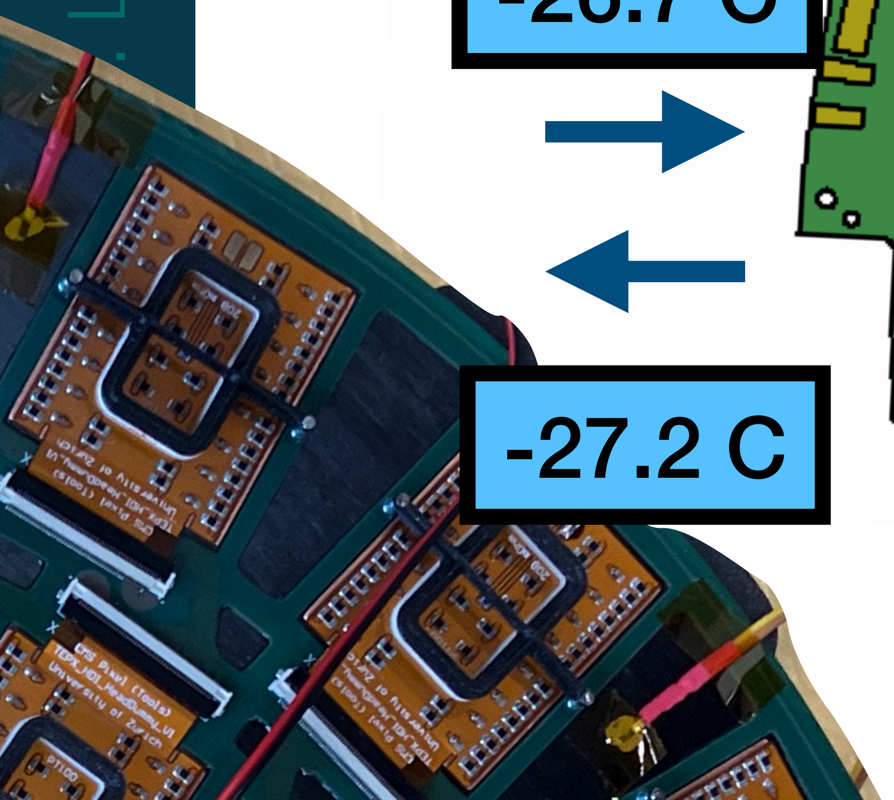
TEPX: mechanical Dee thermal tests

From simulation with a conservative $T_{CO_2} = -27^{\circ}C$ in the evaporator about 7 ˚C safety margin from thermal runaway

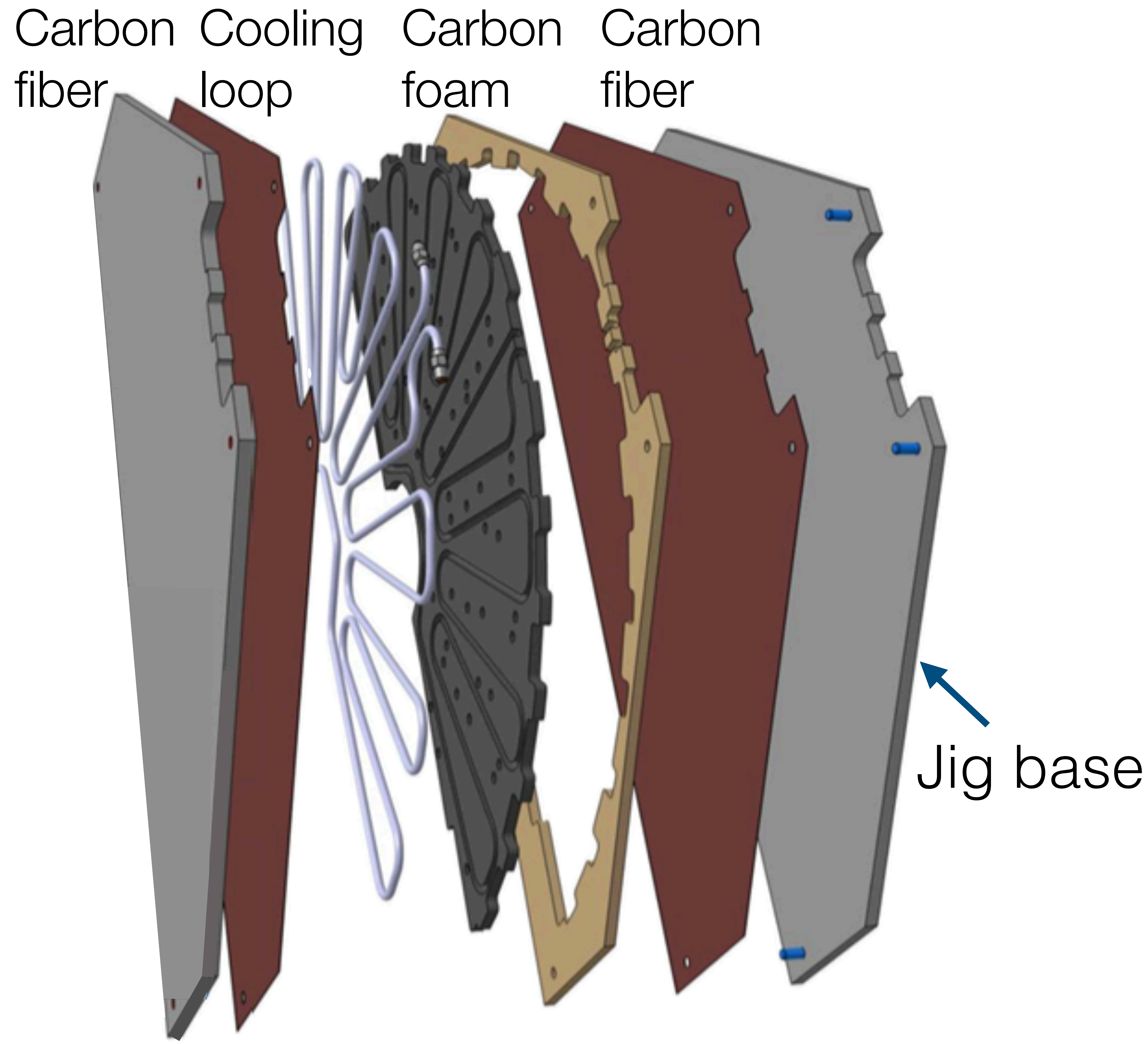


Testpoints on carbon fiber

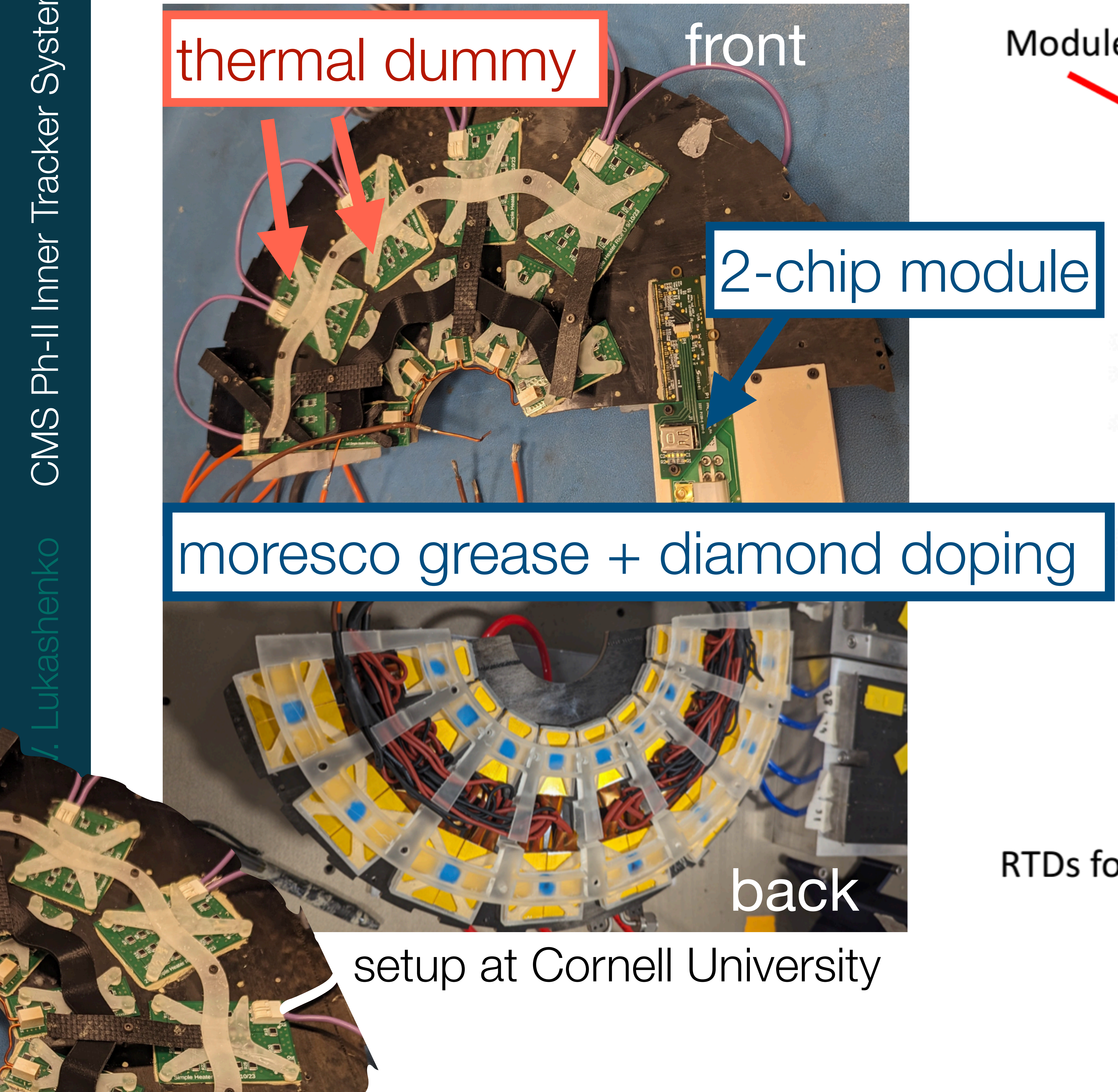




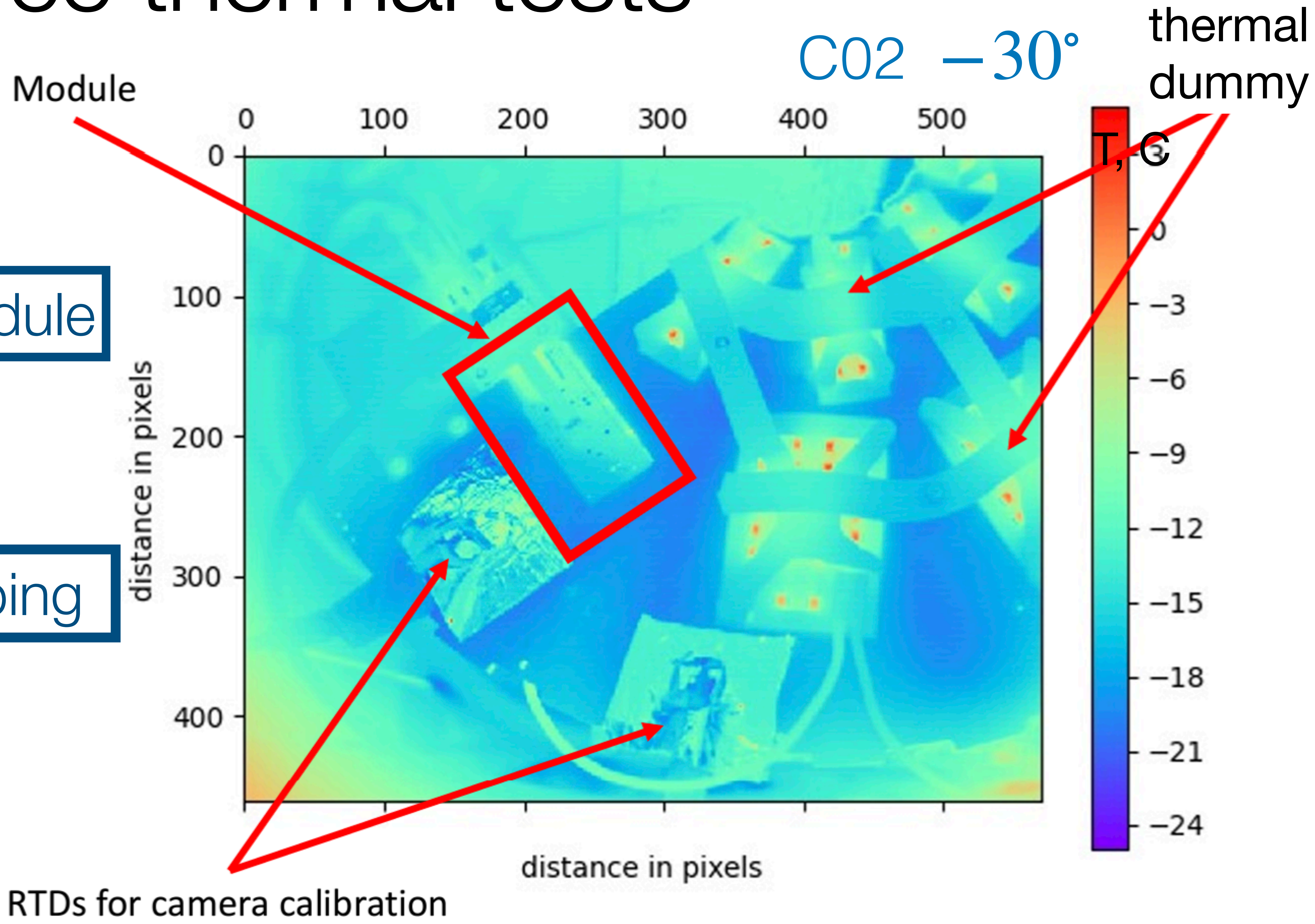
TFPX: mechanical Dee thermal tests



TFPX: mechanical Dee thermal tests



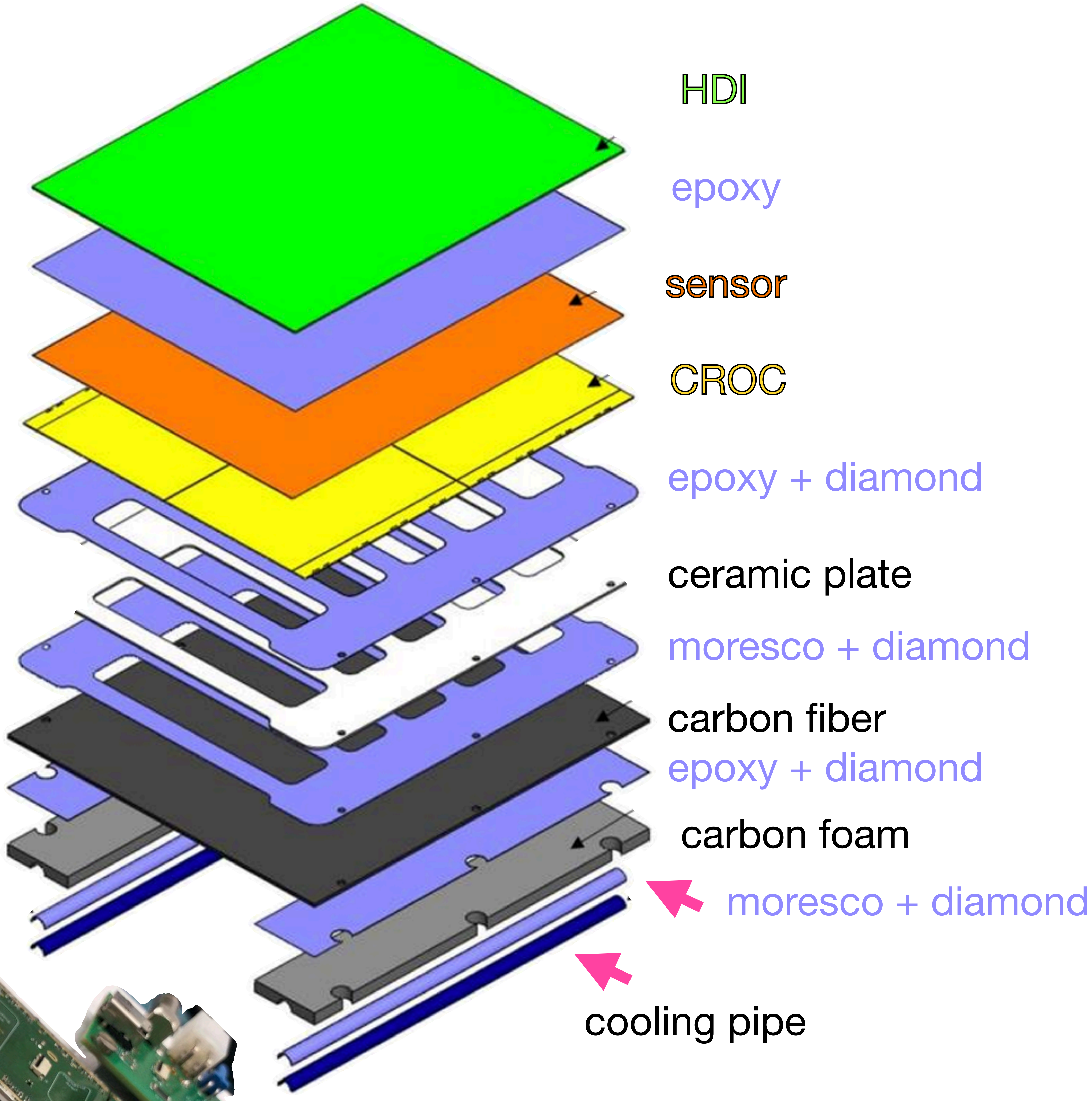
setup at Cornell University

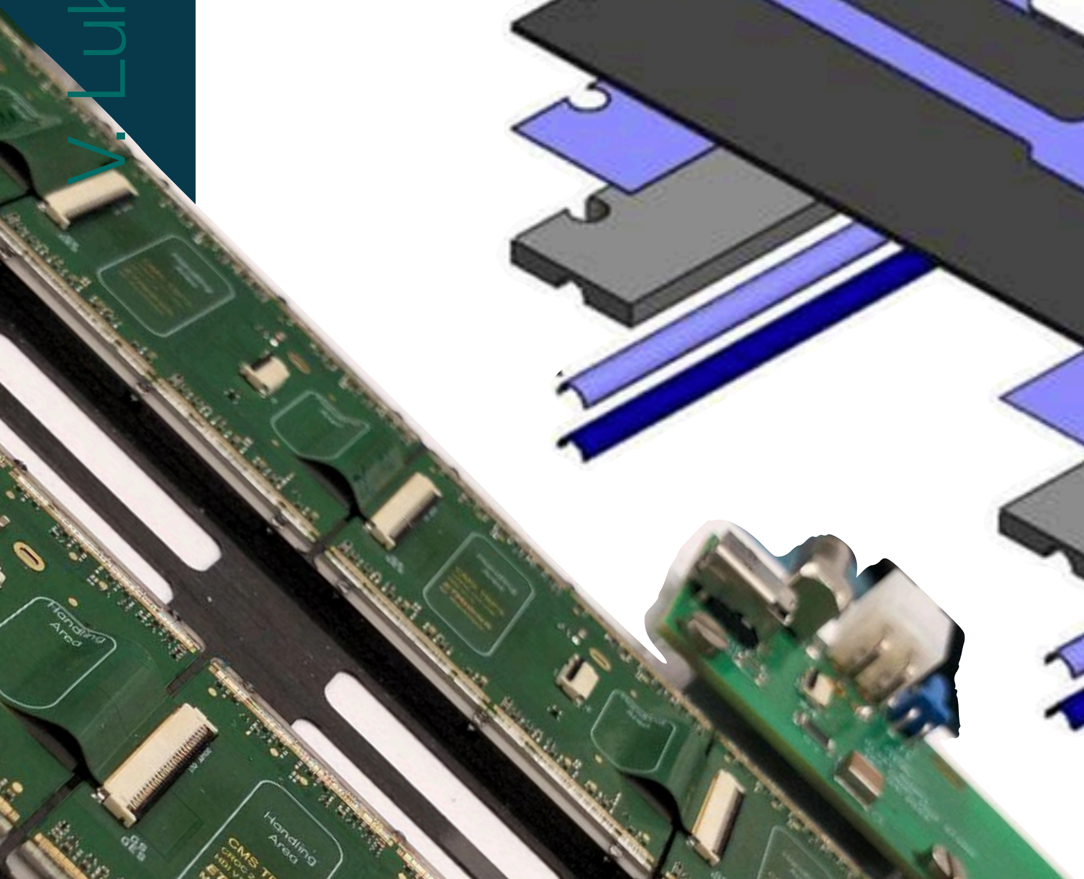


module ≠ heater
hot spots match simulation

TBPX: ladder thermal tests

final structure

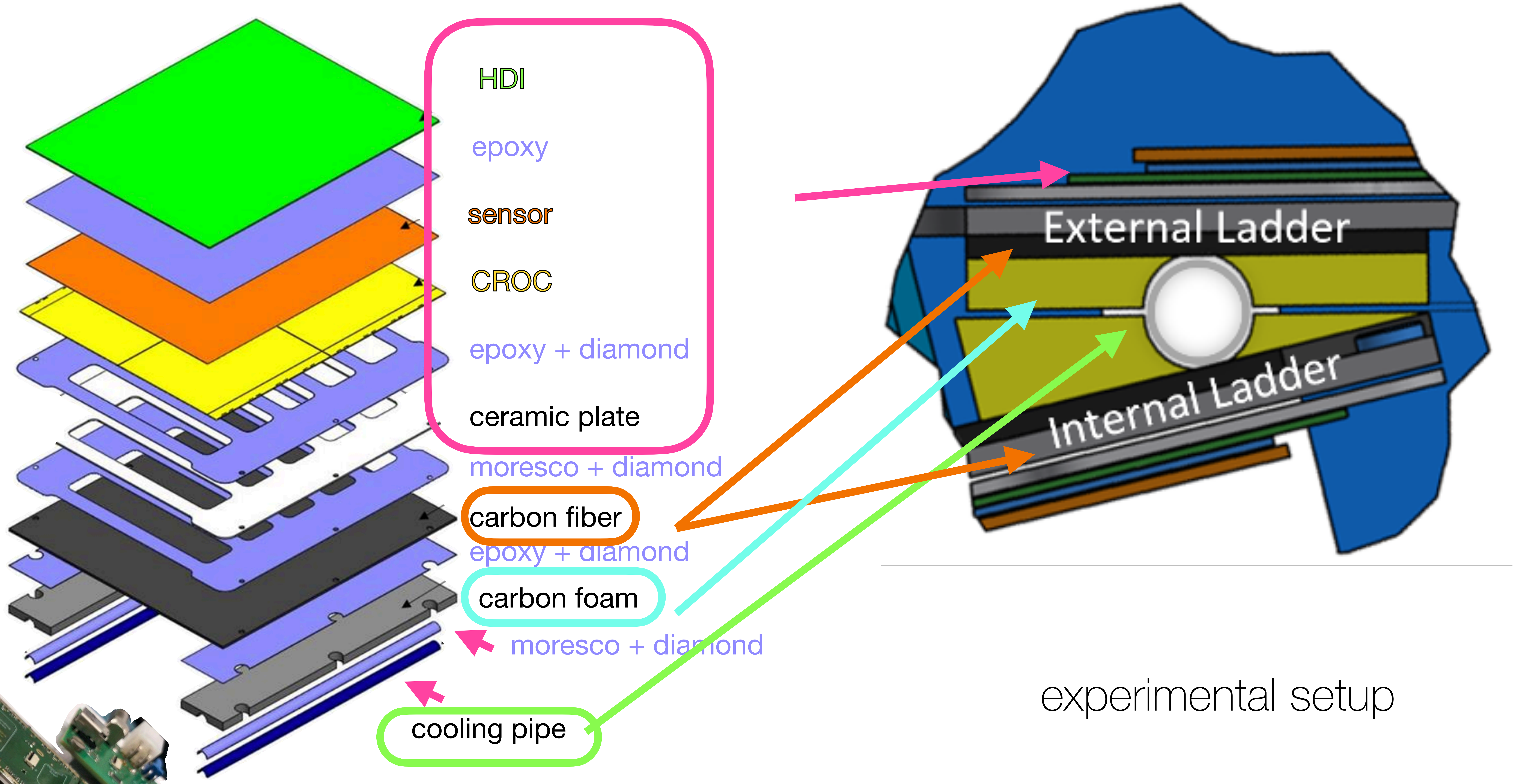




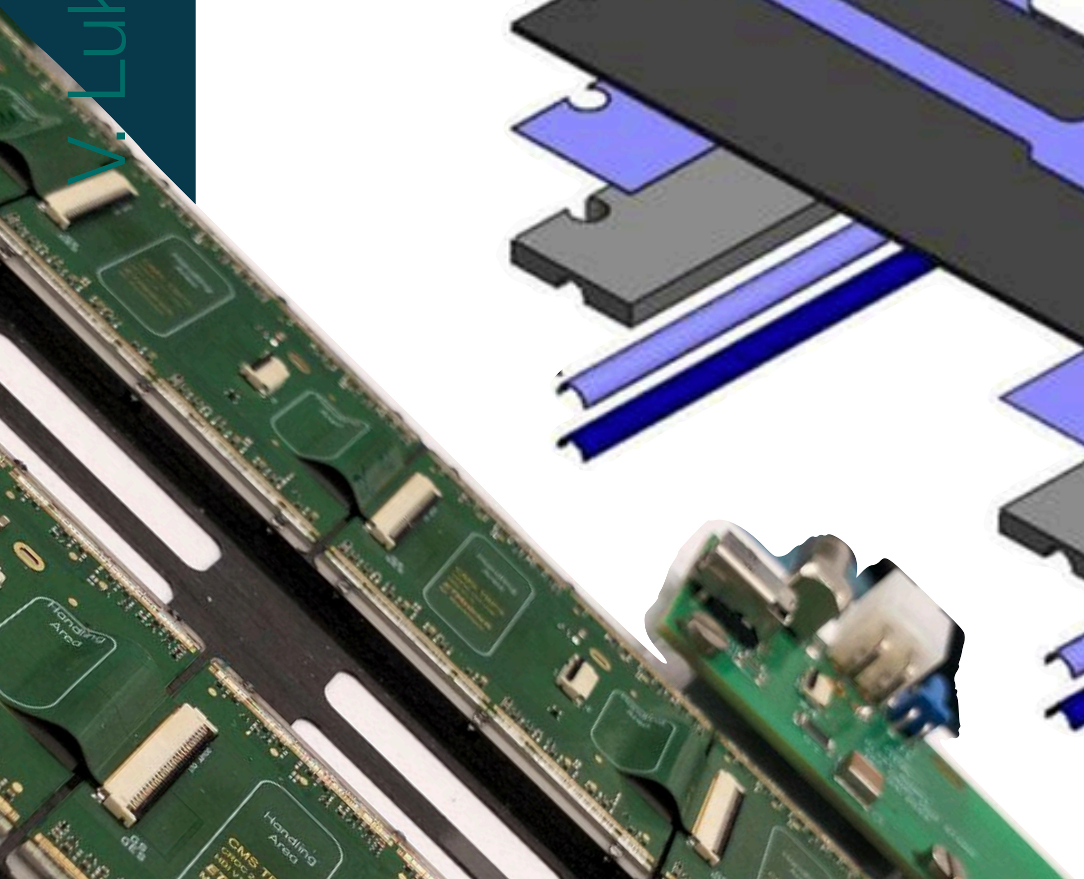
M. Lukashenko

TBPX: ladder thermal tests

final structure

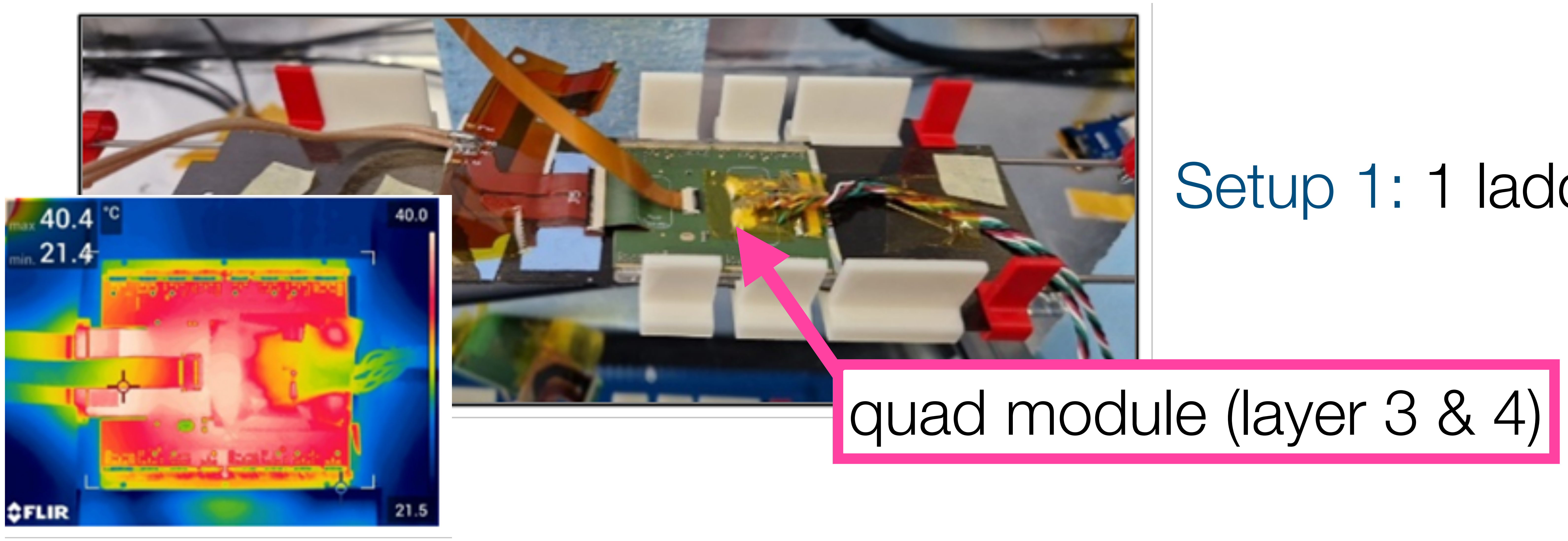


experimental setup

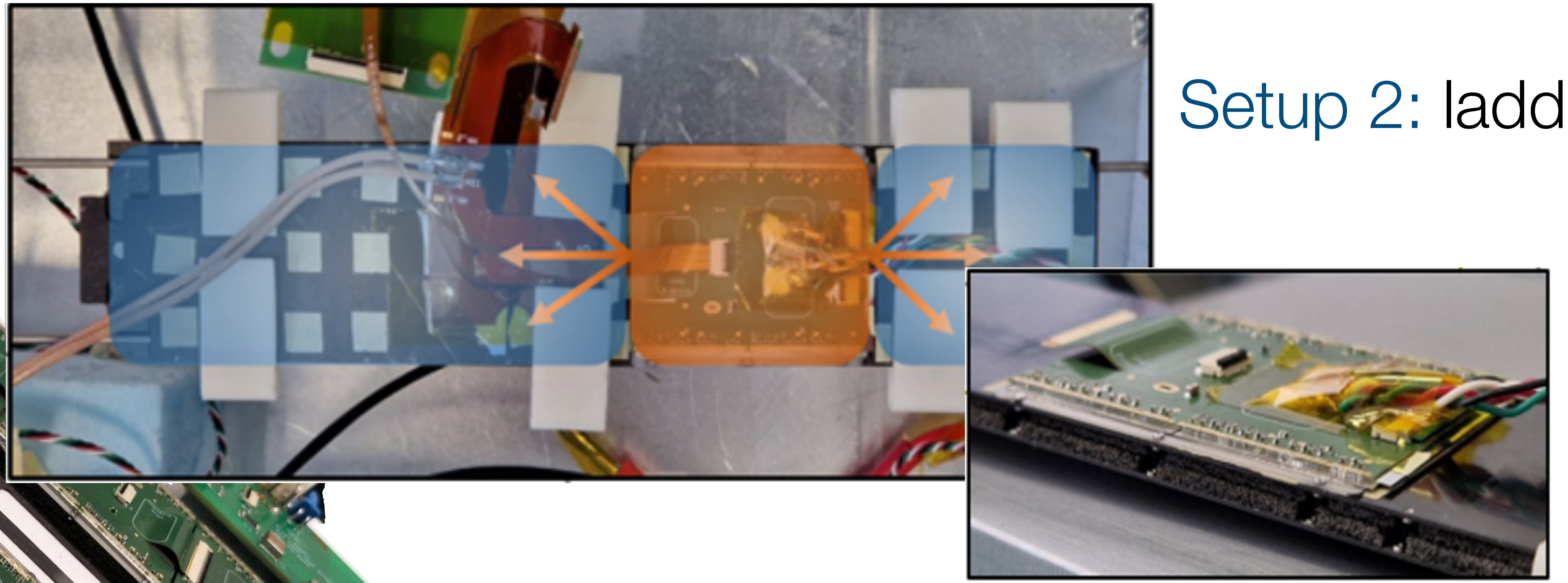


TBPX: thermal tests

Investigating Layer 3: **small thermal margin**

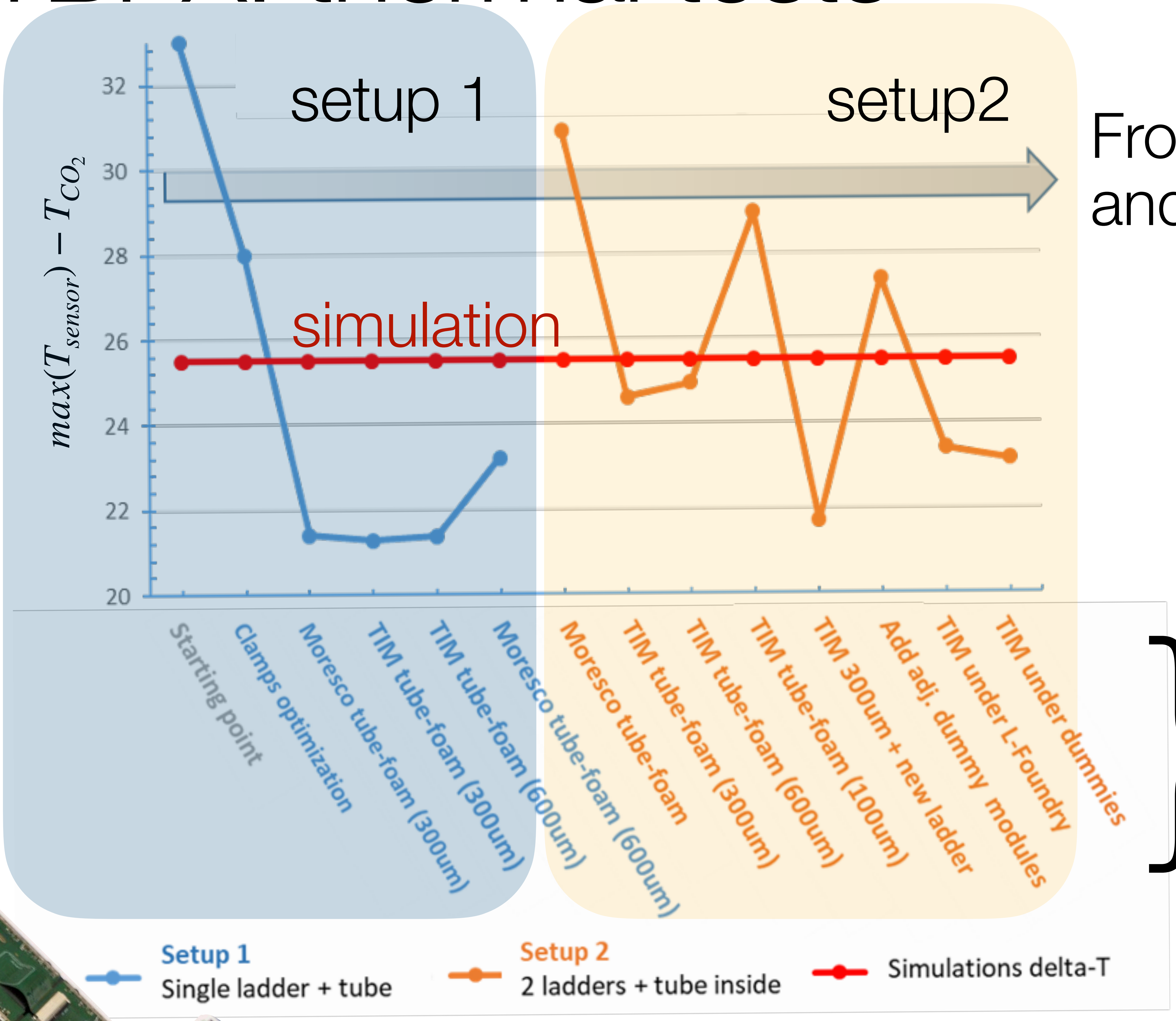


Setup 1: 1 ladder + tube (hold by 3D clamps)



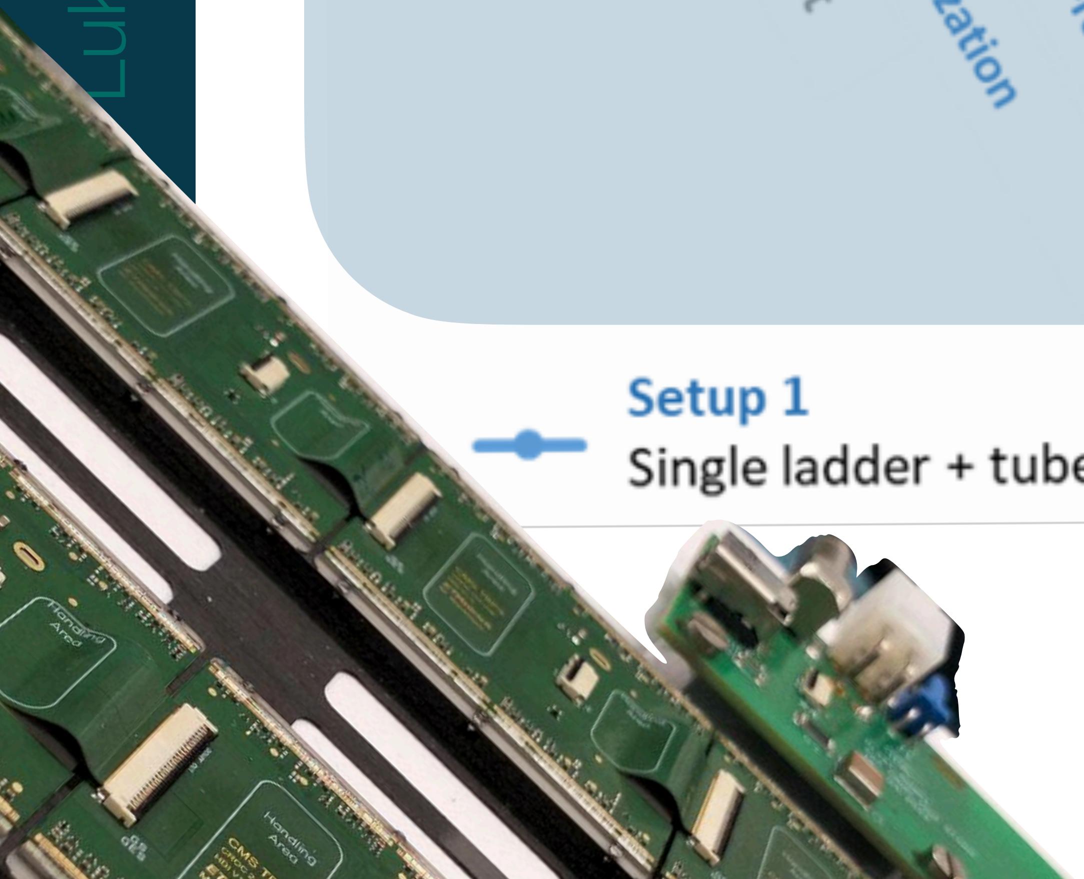
Setup 2: ladder+ladder sandwich

TBPX: thermal tests

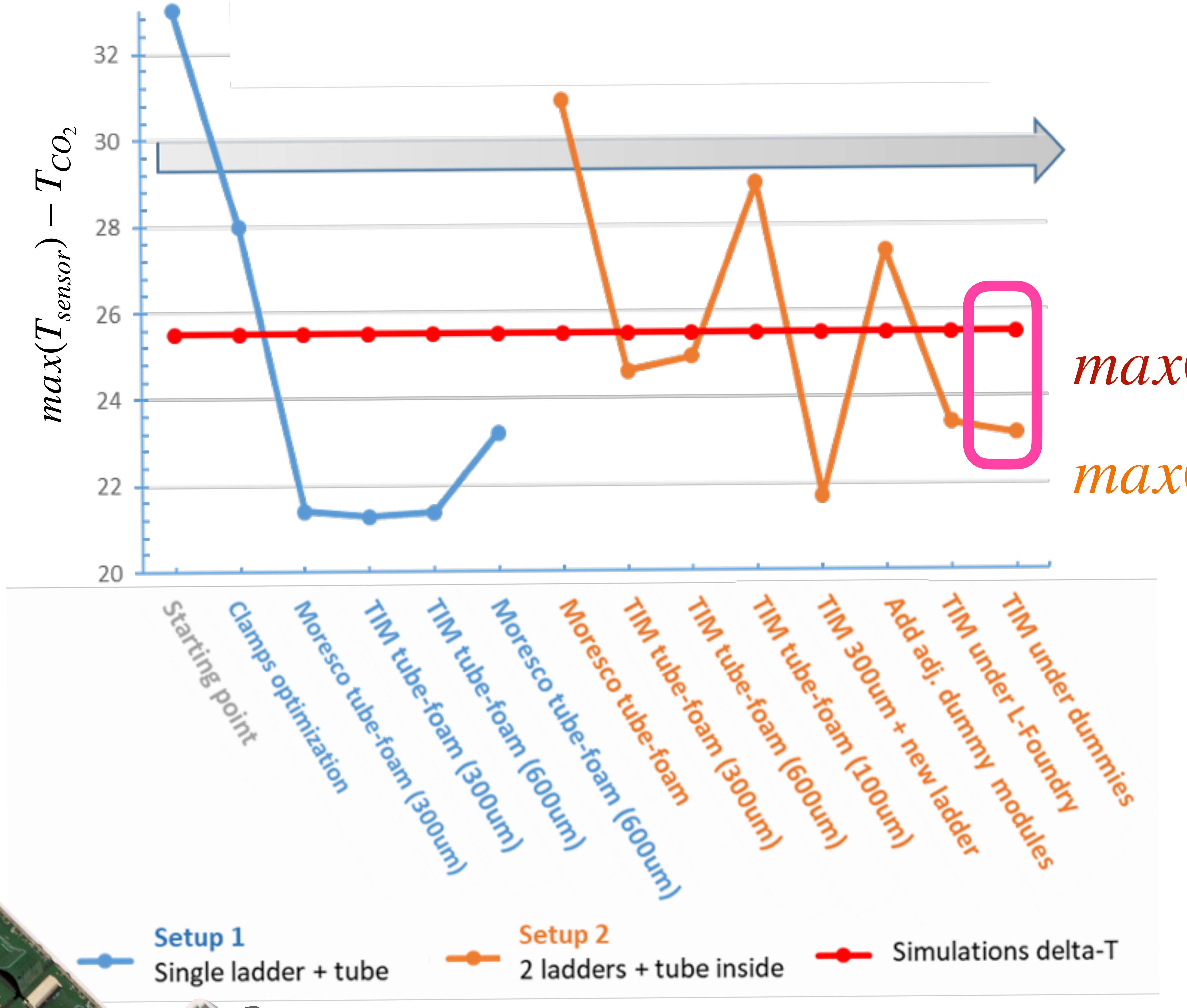


From left to right: approaching more and more real layer 3 mechanics

changes step by step



TBPX: thermal tests

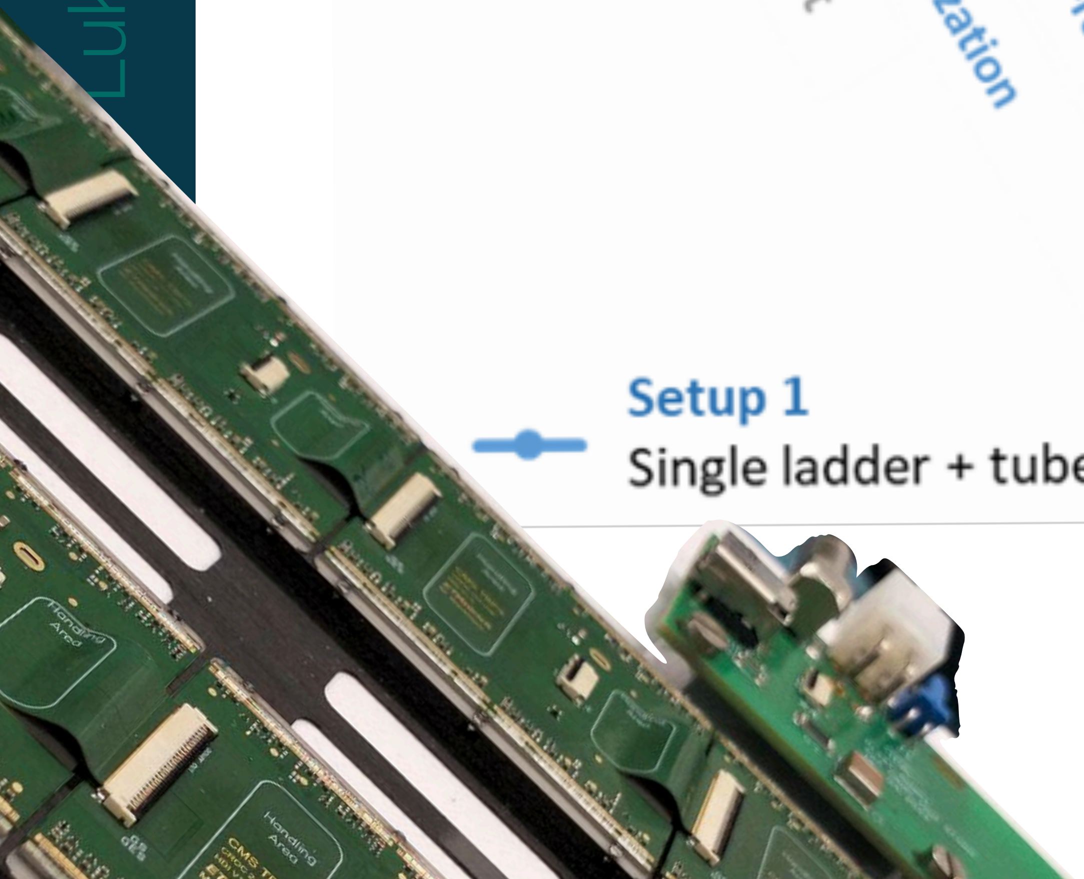


$max(T_{sensor}) - T_{CO_2}|_{sim} \sim 25.5°C$

$max(T_{sensor}) - T_{CO_2}|_{meas} \sim 23°C$

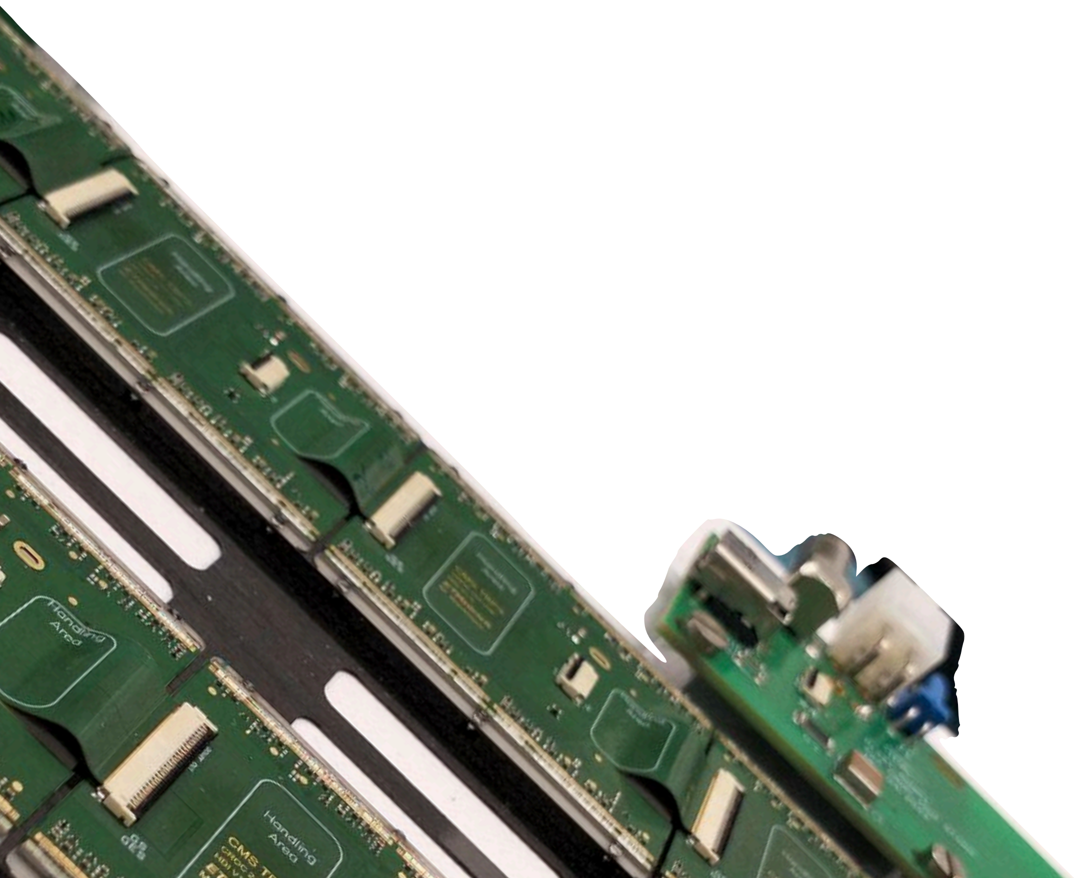
} margin with simulation $3°C$

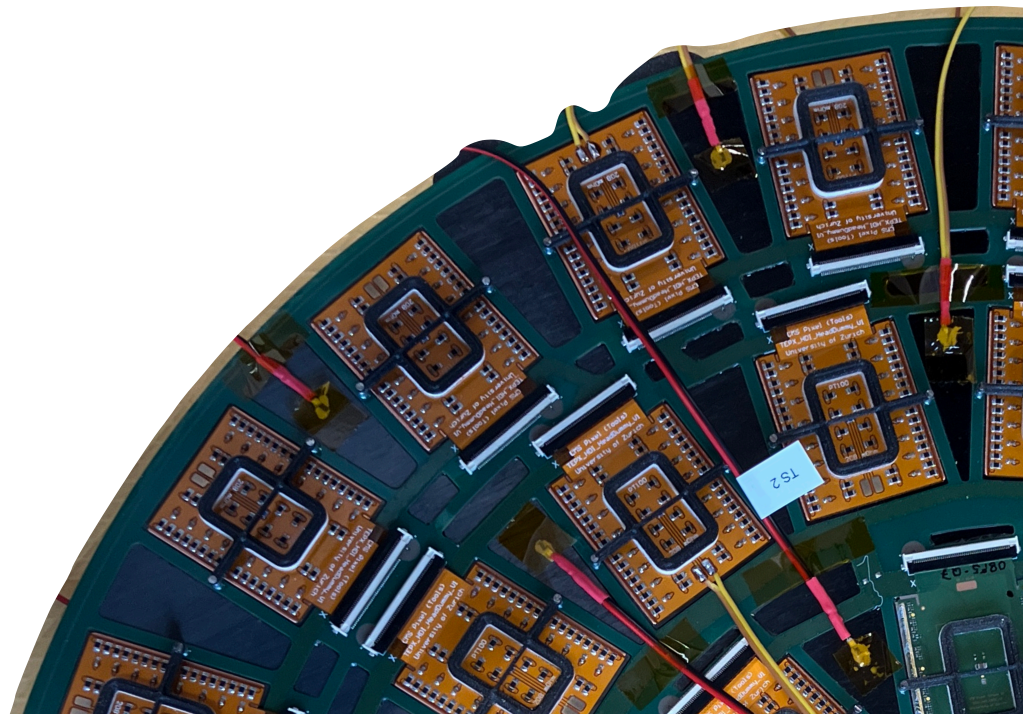
critical layers identified in simulation and confirmed in tests



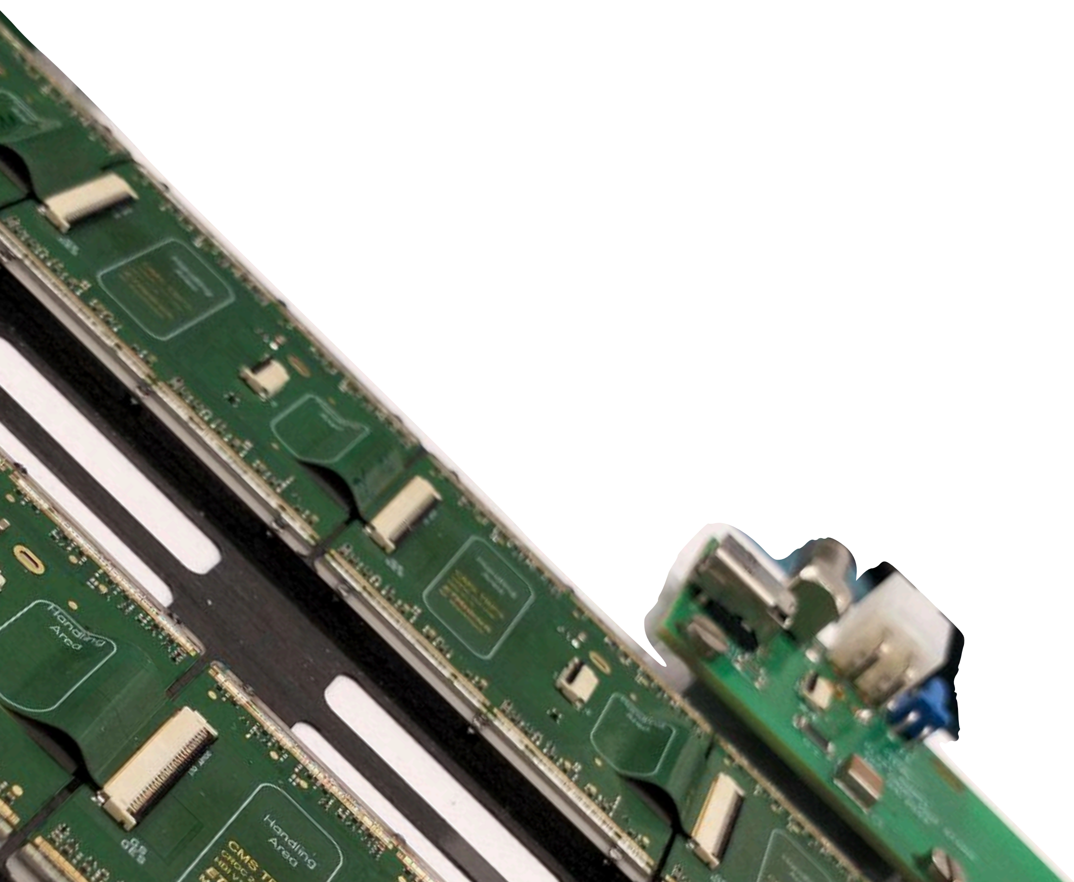
Conclusions

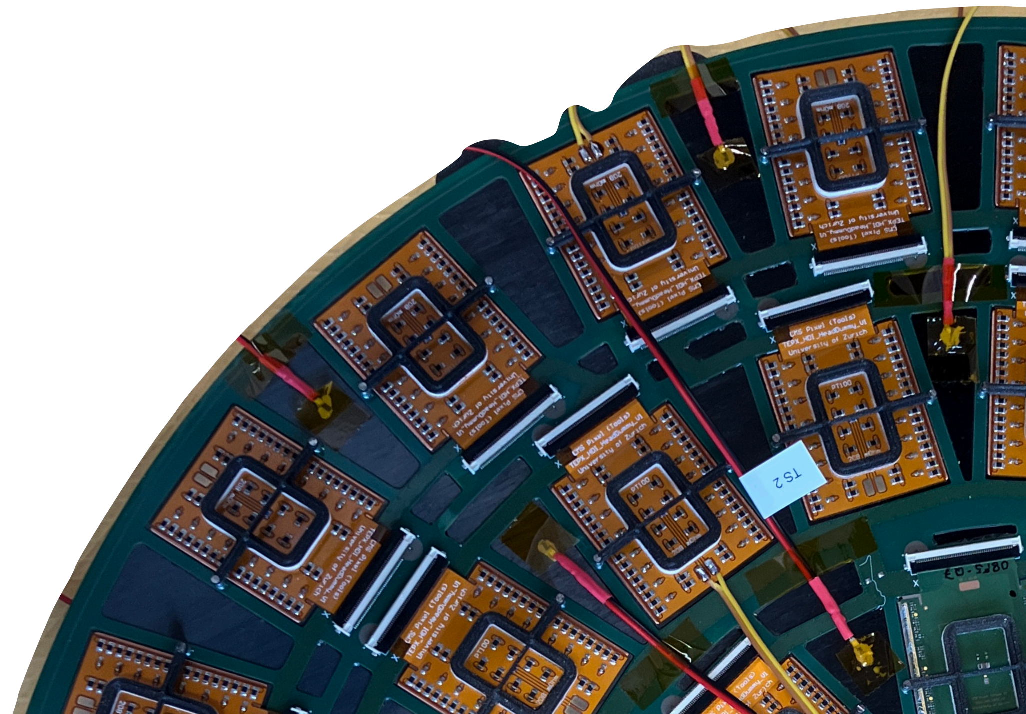
- Systems tests are ramping up. In advanced state for all three subsystems.
- No surprises : expected noise, bit error rate and thermal performance
- Tests with CROCv1 - waiting for mass CROCv2 arrival to repeat the tests





Backup slides

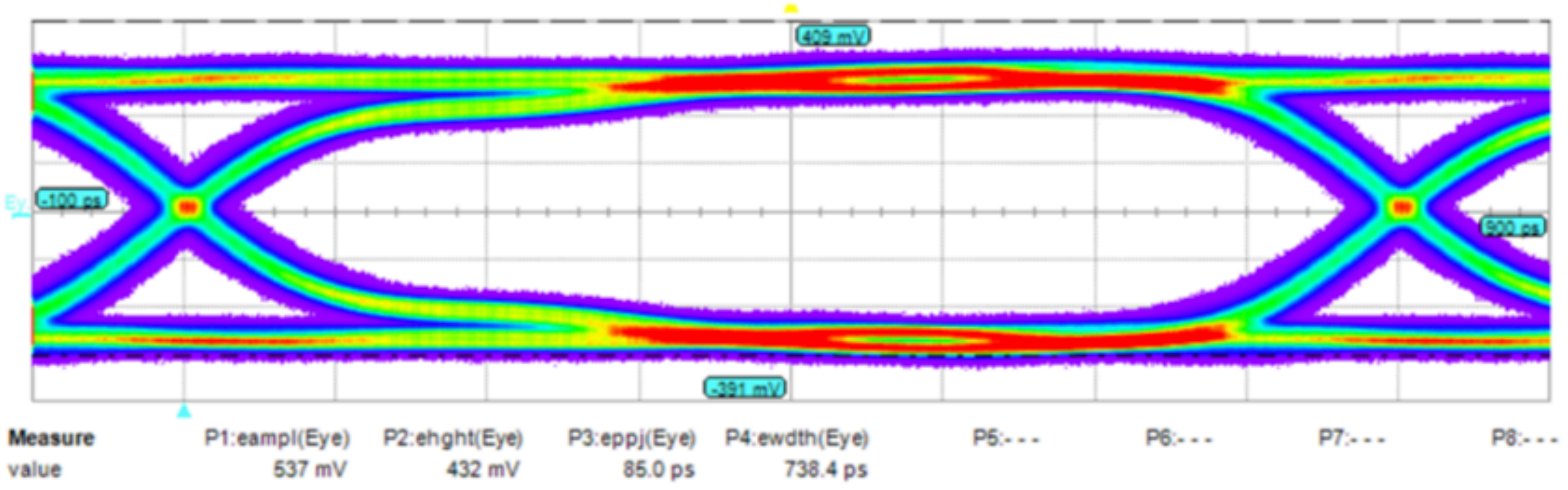




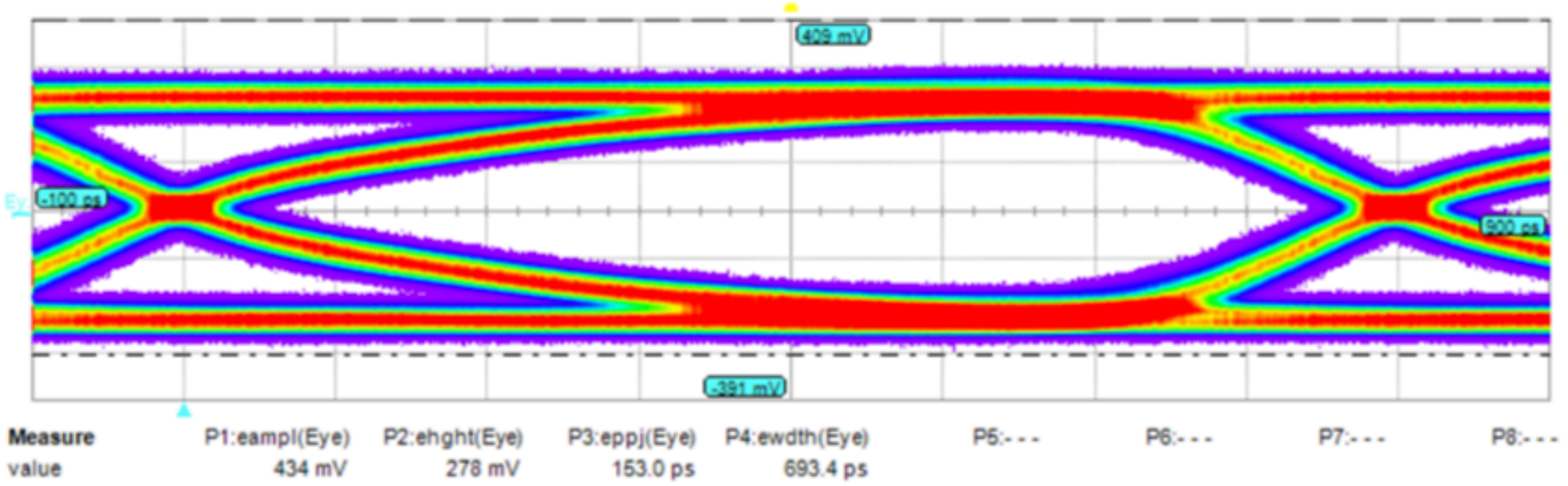
V. Lukashenko

TFPX+TEPX: Eye diagrams

Eye diagram is open. No indication of strong cross-talk or noise

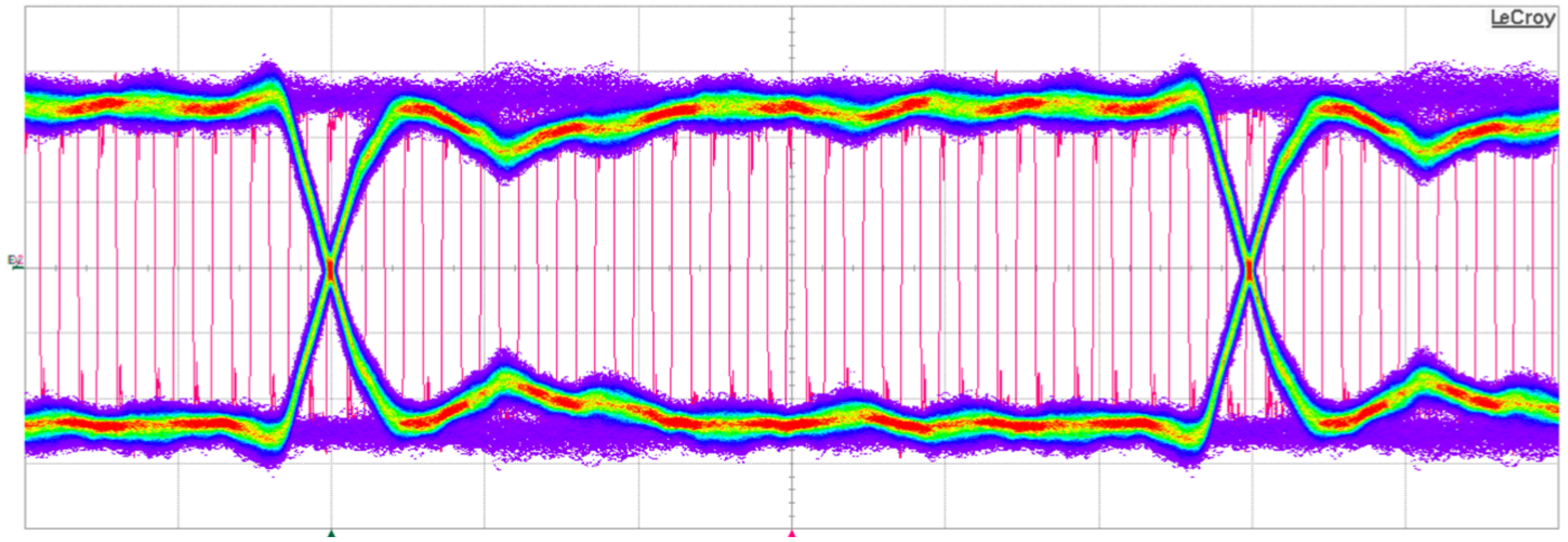


Shortest Trace:
- Length: 85mm
- Module: 53
- Speed: 1.25Gbps



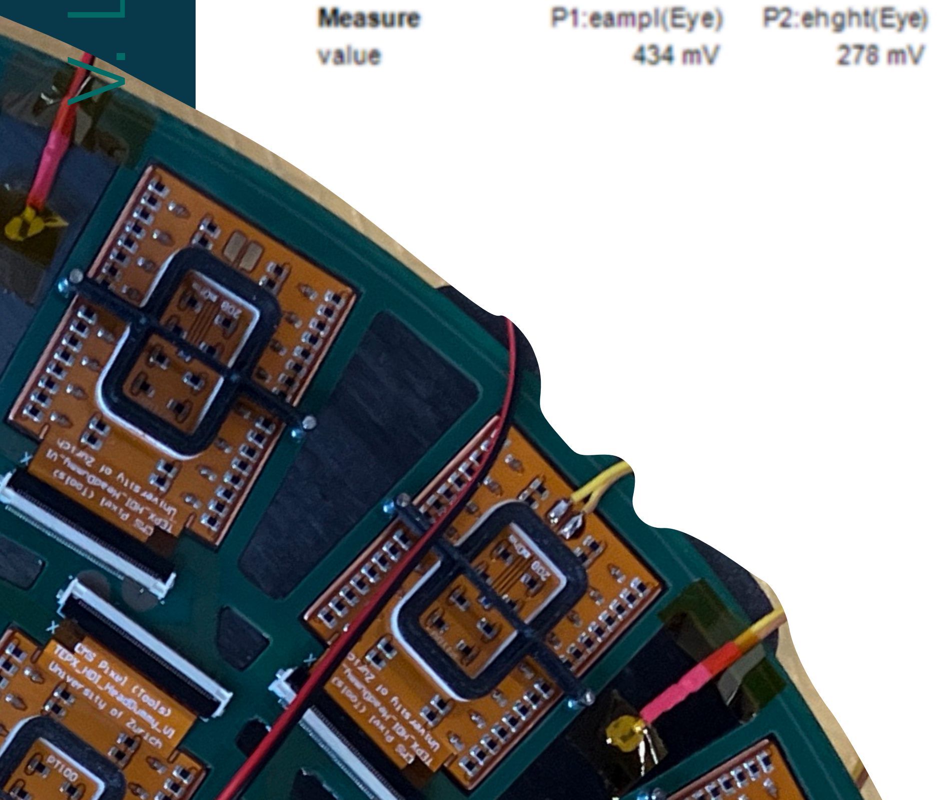
Longest Trace:
- Length: 492mm
- Module: 15
- Speed: 1.25Gbps

TEPX



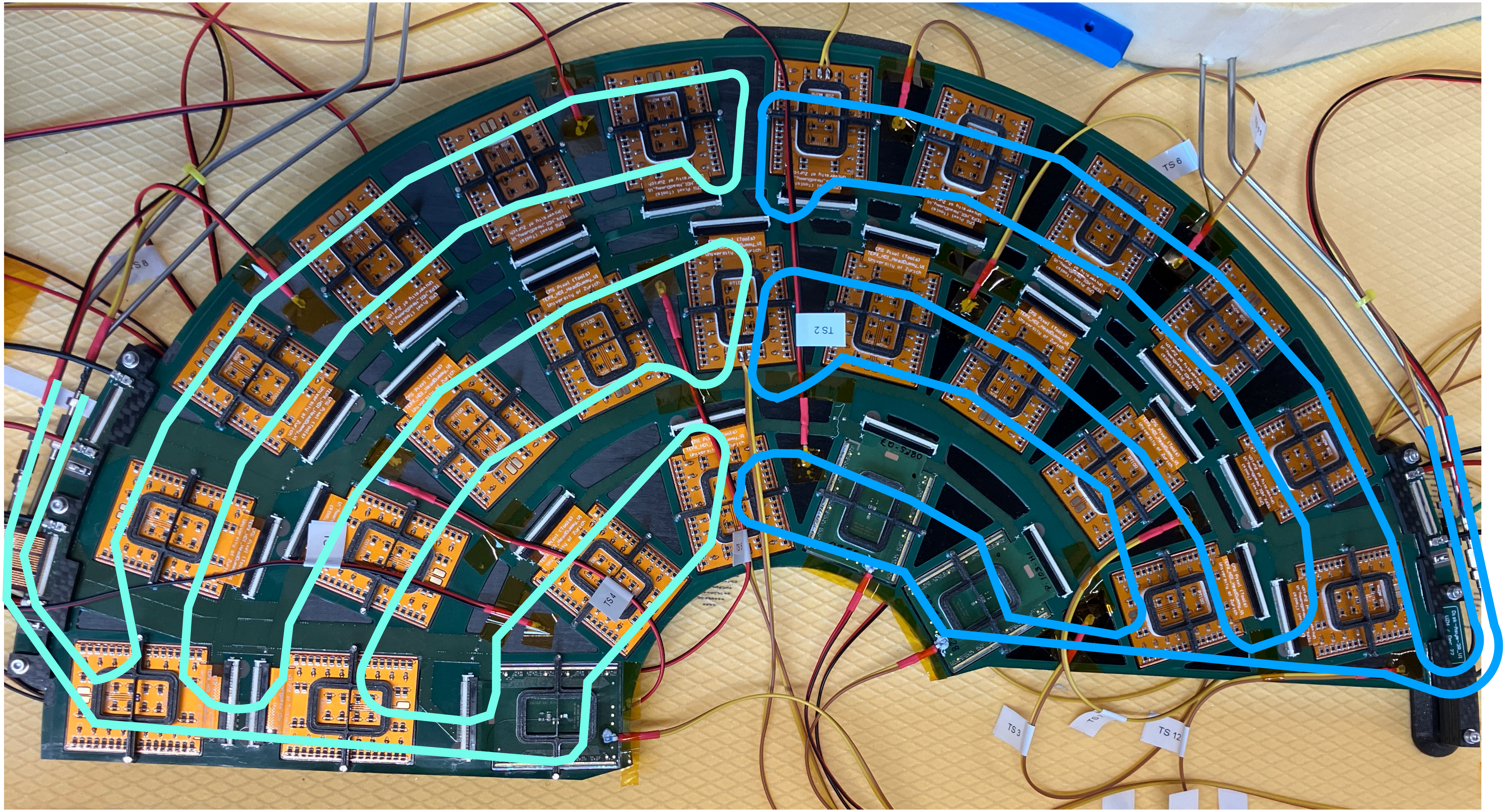
module → portcard

TFPX



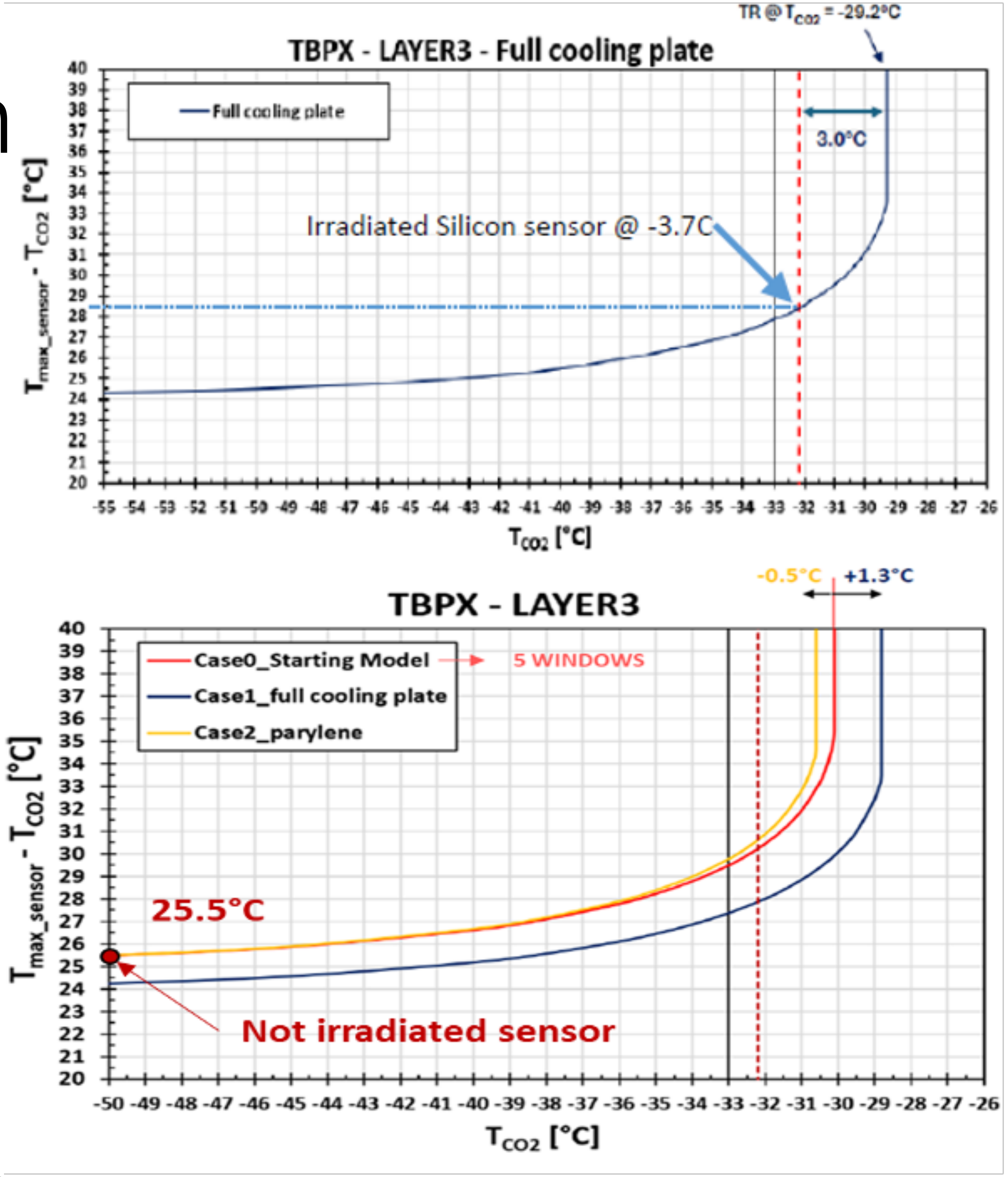
TEPX: mechanical half-disk thermal tests

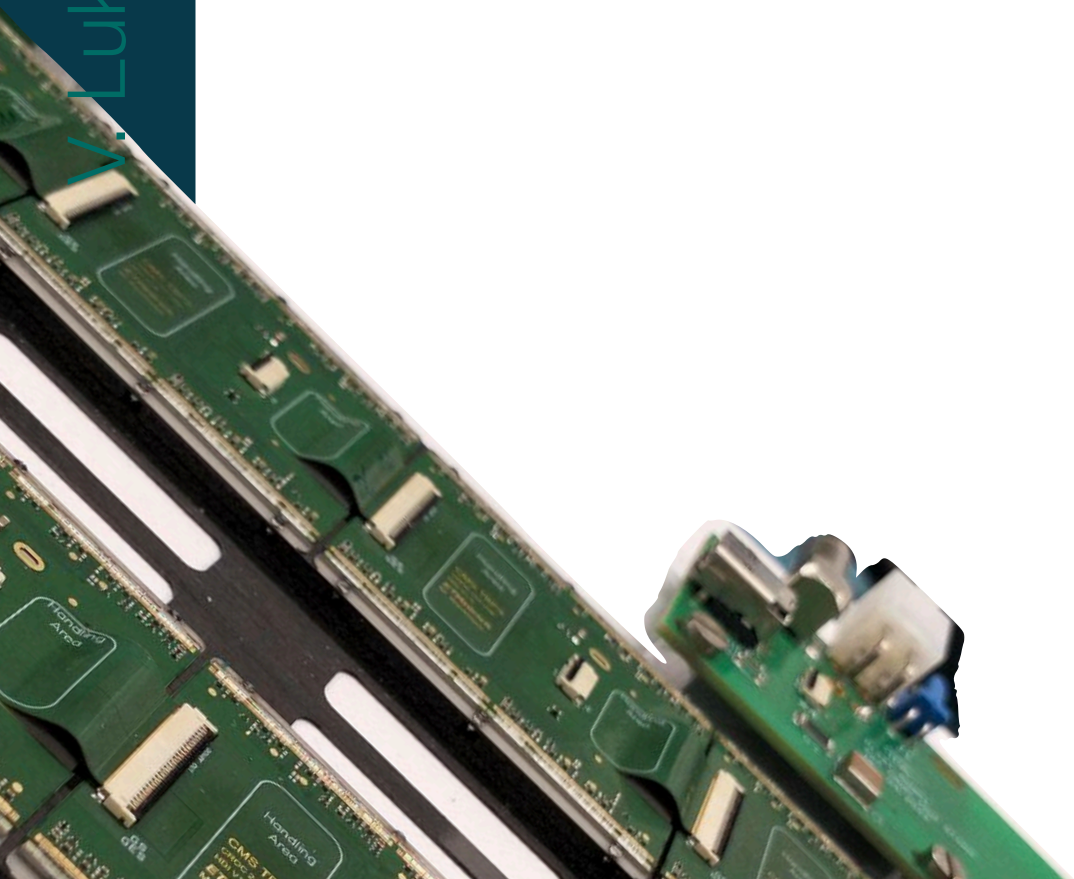
Cooling loops



TBPX: thermal simulation

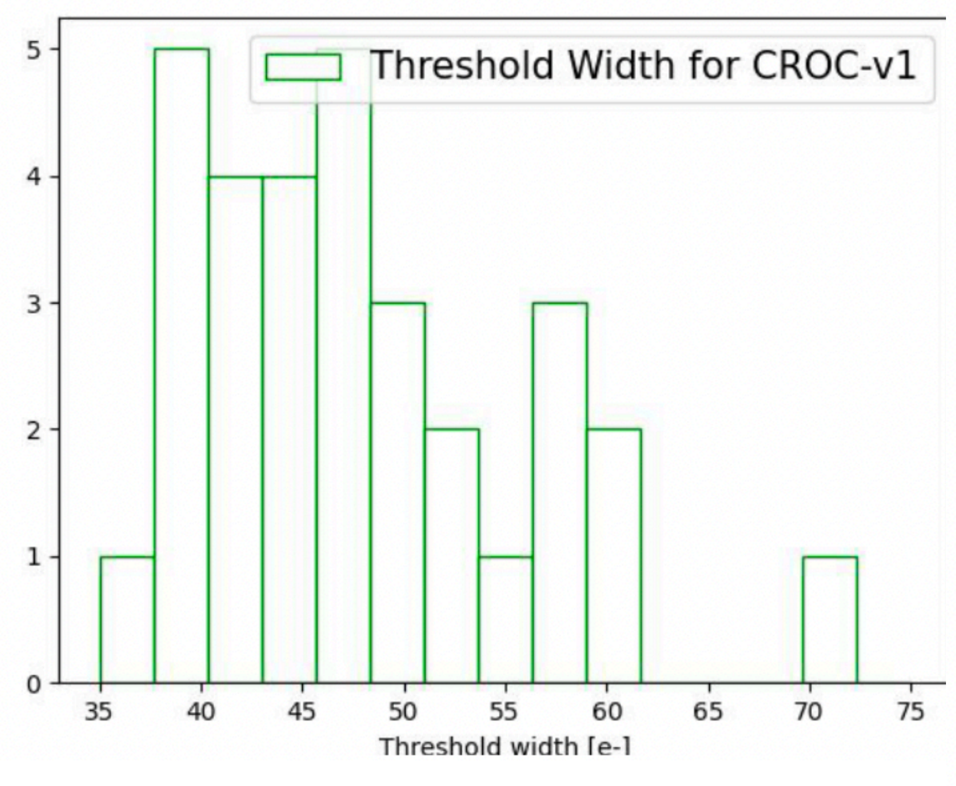
Simulation

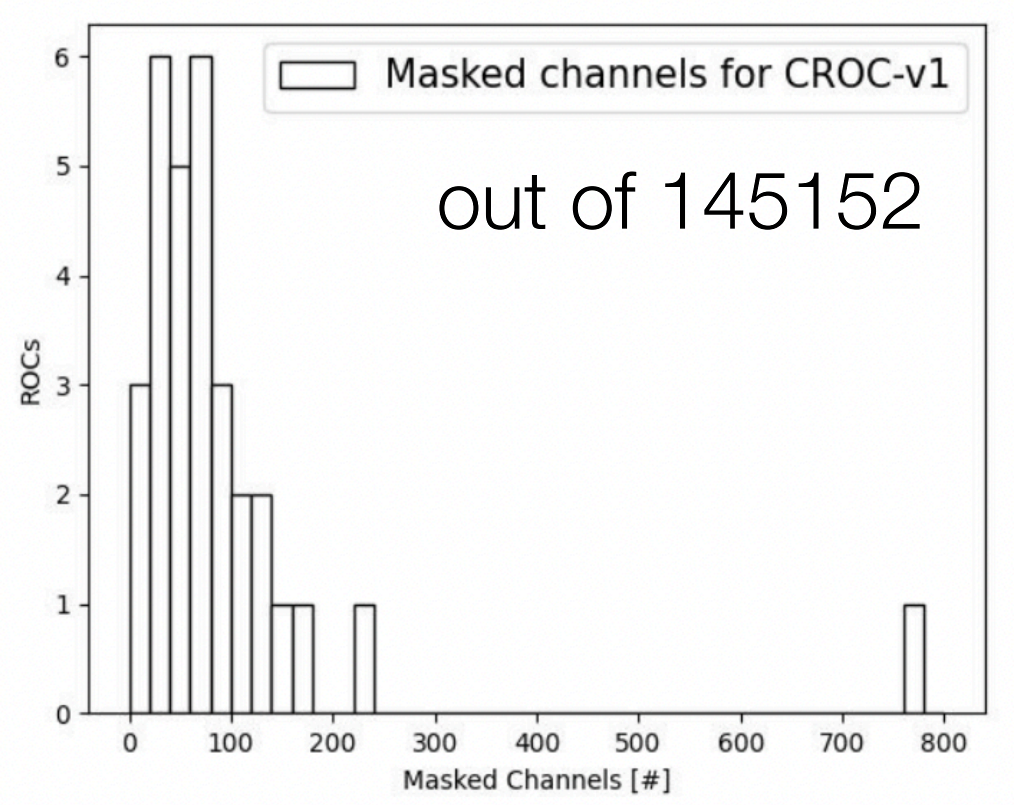




TBPX: extra tests

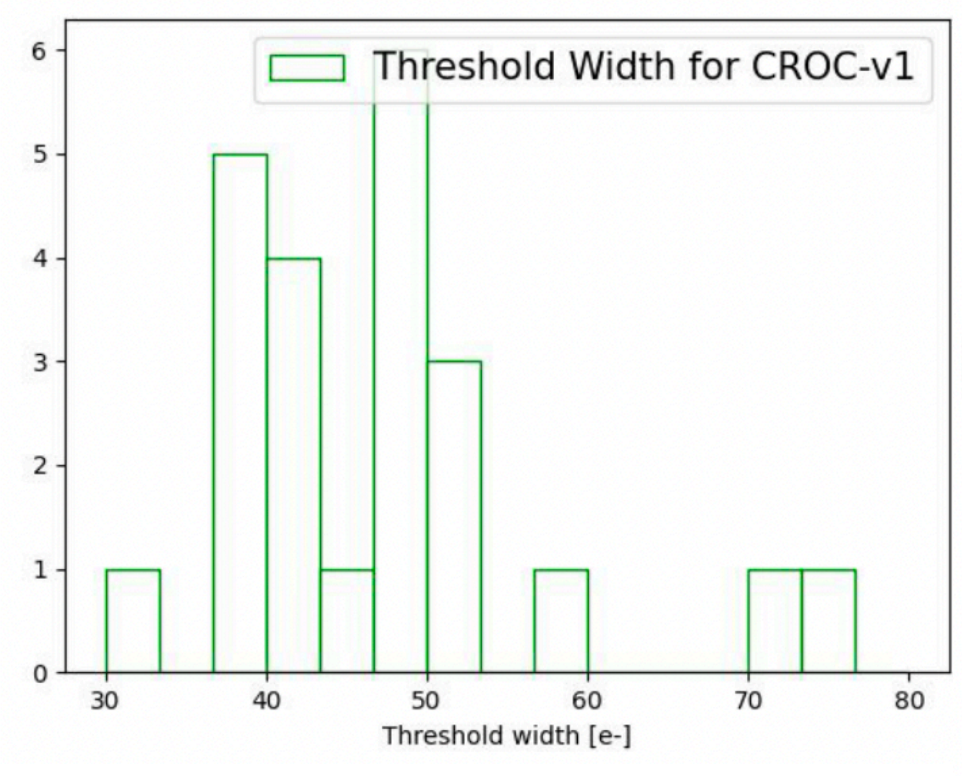
$T_{CO_2} = -32°C$ 32 digital CROCv1

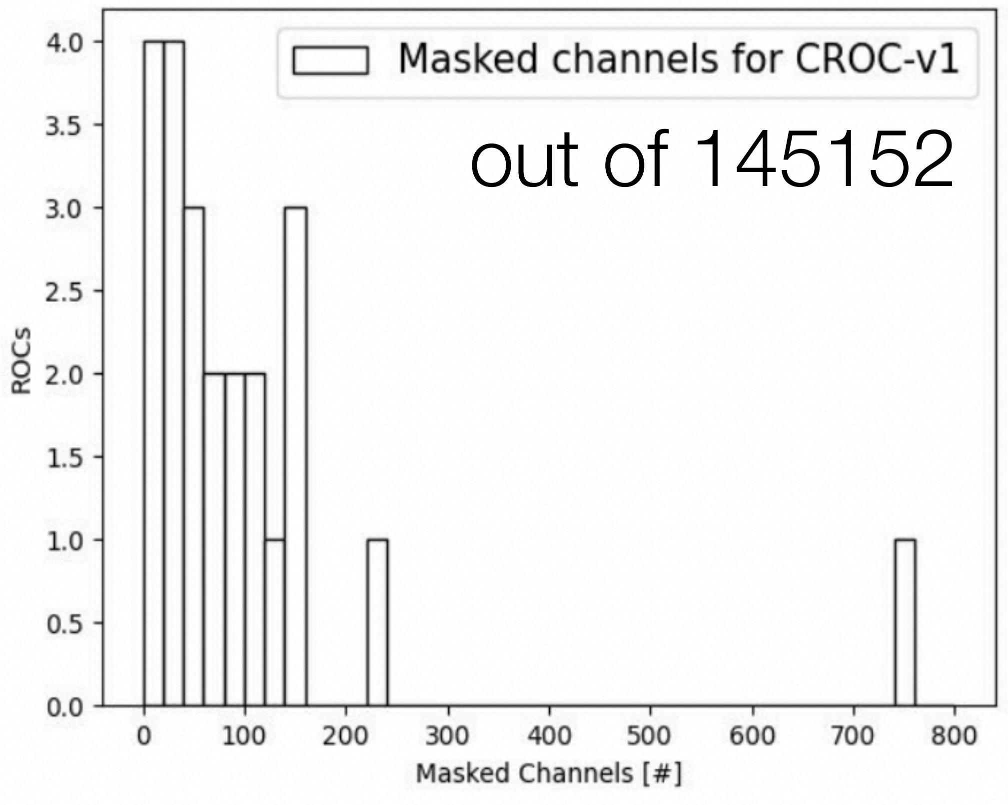




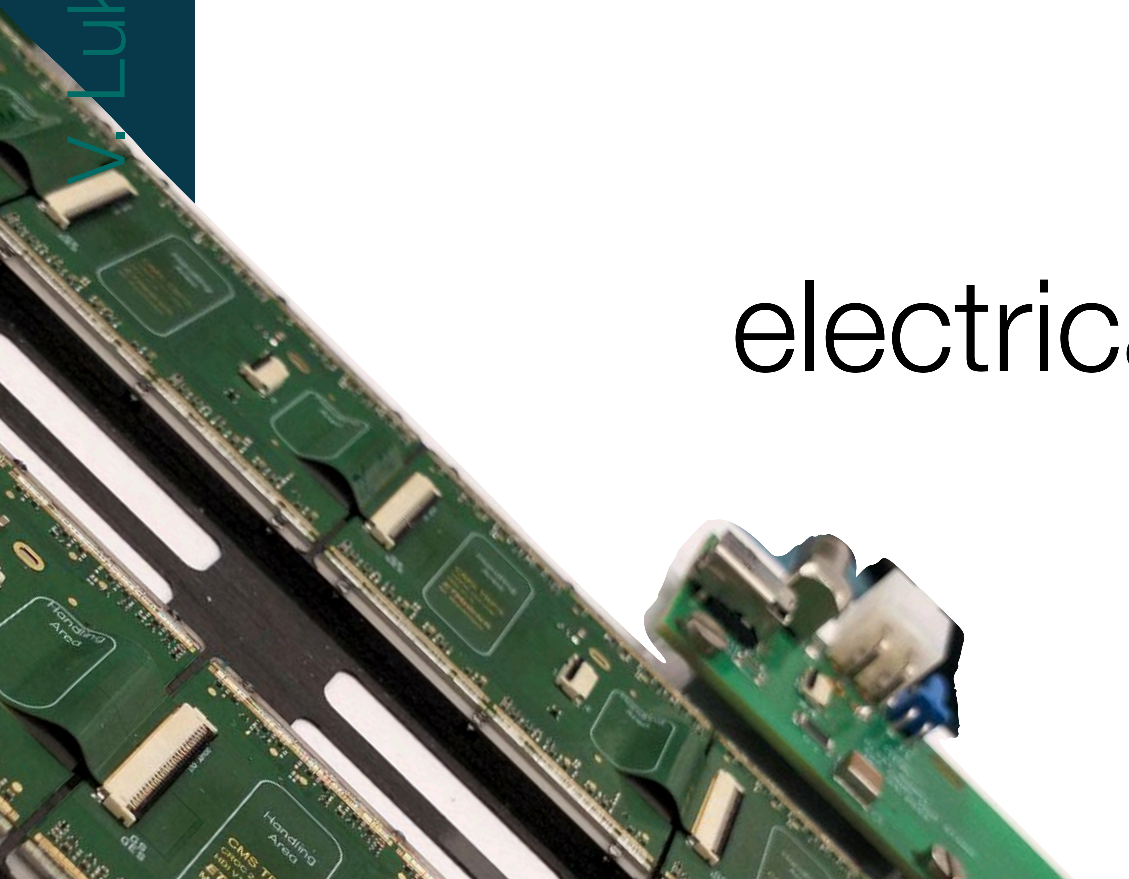
electrical readout

$T_{CO_2} = -28°C$ 32 digital CROCv1

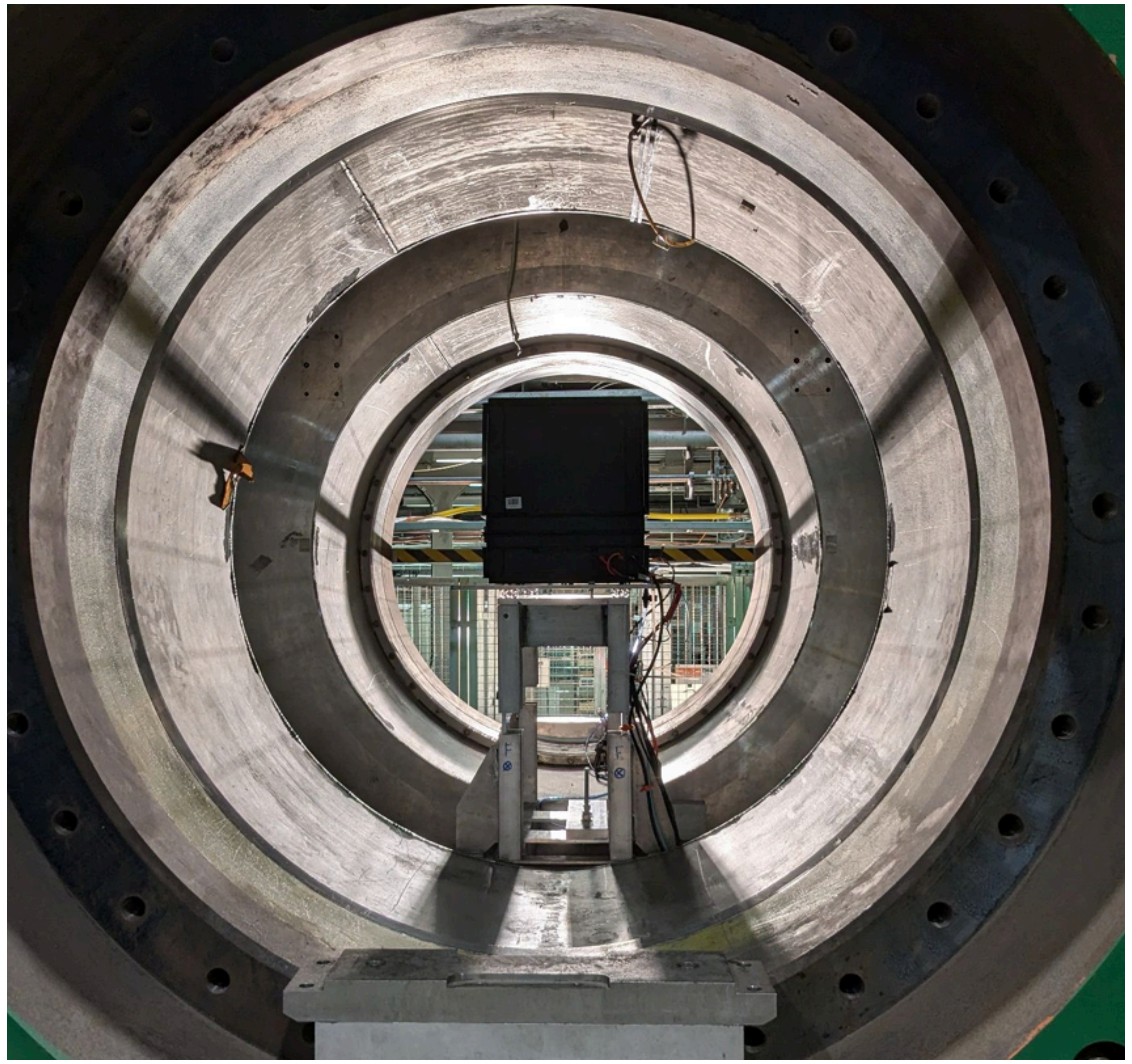




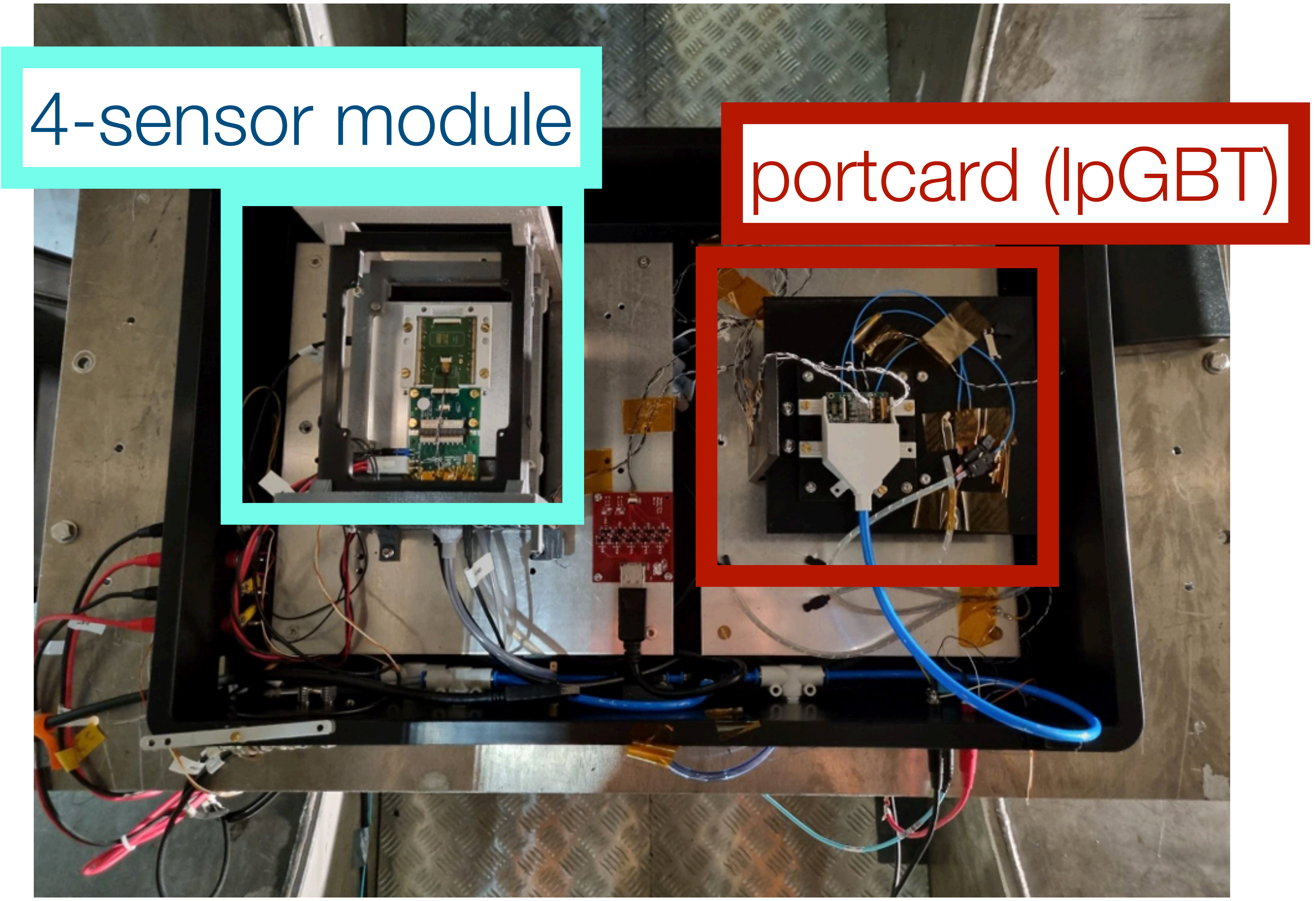
optical readout



TFPX: data chain tests @ 3 Tesla



CERN M1 Magnet



Marginal increase in BER, but threshold & noise the same