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Recueil des résumés

List of accepted abstracts for Pixel 2024 edition.

Contents

Posters / **2**

Effect of 1 MeV neutron-irradiation on the electrical properties of Si-based diodes.

Auteur: Joseph Bodunrin[1]

Co-auteur: Sabata Moloi [1]

[1] *University of South Africa*

Auteur correspondant ebodunjo@unisa.ac.za

The impact of radiation on Si-based detectors has garnered interest due to the observed degradation in their stability in high-radiation environments. In this study, we examined the effects of 1 MeV neutron-irradiation at different fluences on the electrical properties of undoped n-Si diodes using current-voltage (I-V) technique. The irradiation fluences ranged from 0 to 1017 n/cm2. The obtained results indicated that the diodes were well fabricated, and neutron-irradiation resulted in a diode behaviour changing from normal exponential to ohmic I–V behaviour. This ohmic behaviour was explained in terms of irradiation-induced defect levels that were positioned at the centre of the energy gap. An I–V ohmic region increased with fluence indicating that the density of defect levels has increased with neutron-irradiation fluence. A change in diode conduction mechanism domination and parameters with different radiation fluence were also investigated. The obtained I–V properties of neutron-irradiated Si-based diodes were similar to those of the diodes that were fabricated on radiation-hard materials, indicating that neutron-irradiation at certain fluences improve radiation-hardness of Si to be used in high energy physics experiments.

Posters / **3**

ATLASPix3 Serial powering and multi-chip module studies for future HV-CMOS tracker

Auteurs: Attilio Andreazza[1]; Fabrizio Sabatini[1]; Fuat Ustuner[2]; Harald Fox[3]; Ivan Peric[4]; Lingxing Meng[3]; Marco Hübner[5]; Pratik Gheewalla[2]; Riccardo Zanzottera[1]; Ruoshi Dong[4]; Yanyan Gao[2]

[1] *Università degli Studi e INFN Milano*

[2] *University of Edinburgh*

[3] *Lancaster University*

[4] *The Karlsruhe Institute of Technology*

[5] *Hochschule RheinMain*

Auteur correspondant marco.huebner@student.hs-rm.de

High voltage CMOS pixel sensors are proposed in many future particle physics experiments such as the HL-LHC upgrades and future circular colliders. The ATLASPIX3 chip consists of 49000 pixels of dimension 50µm x 150 µm, realised in in TSI 180nm HVCMOS technology. It was the first full reticle size monolithic HVCMOS sensor suitable for construction of multi-chip modules and supporting serial powering through shunt-LDO regulators. The readout architecture supports both triggered and triggerless readout with zero-suppression. With the ability to be operated in a multi-chip setting, a 4-layer telescope made of ATLASPix 3.1 was developed, using the KIT GECCO readout system. To demonstrate the multi-chip capability and for its characterisation, a beam test was conducted at DESY using 3–6 GeV positron beams with the chips operated in triggerless readout mode with zero-suppression. Detailed electrical characterisations of the regulators will be presented as well as multi-chip (quad module) readout and serial powering prototyping.

Timing with pixels / **4**

Performance of 55 micron pitch TI-LGADs on Timepix4

Auteur: Uwe Kraemer[1]

Co-auteurs: Martin van Beuzekom [1]; Tjip Bischoff [1]

[1] *Nikhef*

Auteur correspondant ukraemer@nikhef.nl

In recent years, development of pixel detectors has evolved from only improving the spatial resolution to also improving the temporal resolution. The ultimate goal is to develop a 4 Dimensional tracking (4D tracking) system capable of combining micrometer spatial resolution with a time resolution in the order of tens of picoseconds.

Low-Gain-Avalanche-Detectors (LGADs) provide a promising avenue for detectors with excellent time resolution due to their intrinsic gain.
However, typical LGADs are limited in their spatial resolution due to the large Junction Termination Extension (JTE) which provide no gain. This results in large millimeter sized pads to ensure sufficient ratio of gain to no-gain regions.
Modifications to the process such as Trench-Isolated-LGADs (TI-LGADs) that forego these JTE allow for small pixel structures similar to those found in typical planar sensors.

Many TI-LGADs were tested using external amplifiers and oscilloscopes as readouts in order to determine their performance. Such operation is not suitable for implementation in large scale detector systems and requires more investigation into a fully hybridized system using a dedicated ASIC.

The Nikhef Detector R&D group has connected variants of TI-LGAD produced by FBK for RD50 with 55×55 pixels and a 55 micron pitch to a Timepix4 readout ASIC to investigate the performance of a fully hybridized system using TI-LGADs as sensors.

In this contribution we will present recent results of multiple TI-LGADs on Timepix4 assemblies showing, intrinsic gain, and achieved time resolution as a function of, but not limited to, intrapixel position and angular dependence. Results have been obtained using a picosecond laser, as well as high energy beam particles within the Timepix4 beam telescope.

Monolithic sensors / **5**

Study of MALTA2, a Depleted Monolithic Active Pixel Sensor, with grazing angles of CERN SPS 180 GeV hadron beam

Auteur: Long LI[1]

Co-auteurs: Carlos Solans [2]; Laura Gonella [1]

[1] *University of Birmingham*

[2] *CERN*

Auteur correspondant l.li.8@bham.ac.uk

MALTA2 is a Depleted Monolithic Active Pixel Sensor designed to meet the challenging requirements of future collider experiments, in particular extreme radiation tolerance and high hit rate . It is fabricated in a modified Tower 180 nm CMOS imaging technology to mitigate performance degradation caused by irradiation up to 100 MRad of Total Ionising Dose and 3×10^{15} 1 MeV N_{eq}/cm^2 of Non-Ionising Energy Loss.
Samples of MALTA2 have been tested during the CERN SPS test beam campaign in 2023-2024, before and after irradiation of 1×10^{15} 1 MeV N_{eq}/cm^2. The sensors were inclined at a range of angles with respect to the beam. Particles crossing the sensor at an angle traverse a higher volume, potentially

leading to improved charge collection after irradiation when the sensor is not fully depleted after irradiation.

In this contribution, the tracking efficiency, cluster size and spatial resolution as a function of grazing angles from 0 to 60 degrees will be presented. Additionally, an estimation of the depletion depth with these test beam measurements will be presented. Understanding the sensor depletion is key to study the charge collection properties through drifting in the bulk of the device and to understand radiation effects

Medical imaging applications / **6**

Proton Radiography for adaptive radiotherapy using ATLAS FE-I4 detectors

Auteur: Jens Weingarten[1]

[1] *TU Dortmund University*

Auteur correspondant jens.weingarten@tu-dortmund.de

Due to the physical principles of the energy deposition of charged particles in matter, proton therapy allows a very precise dose deposition in the tumour, which leads to better protection of healthy tissue compared to photon radiotherapy. At the same time, the maximum dose deposition at the end of the proton trajectory is more sensitive to uncertainties in the range of the protons. A significant source of these uncertainties are inter-fractional anatomical changes in the patient during treatment. Adaptive radiotherapy, where the treatment plan is adapted to the anatomy of the day, is an important tool to optimise dose deposition.
Pixelated semiconductor detectors with energy resolution allow the kinetic energy of the protons to be measured in two dimensions. If the detector is placed downstream of the patient, the energy loss in the patient, expressed in terms of their water-equivalent thickness (WET), can be quantised (proton radiography). In this way, the patient's anatomy in the target area can be monitored over the course of treatment with a very small additional imaging dose, allowing the treatment plan to be optimised if the anatomy changes significantly.
In this paper we present a proton radiography system using ATLAS IBL FE-I4 detector modules. The particle flux and the deposited energy are well beyond the intended application of the readout chip. We show first results for the measurement of the proton energy and the WET resolution and demonstrate the applicability of the detector for the acquisition of proton radiography images.

Posters / **7**

Charecterization of CMOS sensor using X-ray irradiation

Auteur: Anusree Vijay[1]

Co-auteurs: Ganapati Dash [1]; Prafulla Behera [1]; Saloni Atreya [1]; Theertha C [1]

[1] *IIT Madras*

Auteur correspondant anusree.vijay@cern.ch

Recent advancements in particle physics demand pixel detectors that can withstand increased energy and luminosity in the future collider experiments. In response, MALTA, a novel monolithic active pixel detector, has been developed with a cutting-edge readout architecture. This new class of monolithic pixel detectors is found to have exceptional radiation tolerance, superior hit rates, higher resolution and precise timing resolution, making them ideally suited for experiments at the LHC. To optimize the performance of these sensors before their deployment in actual detectors, comprehensive electrical characterization has been conducted. This study also includes comparative DAC analyses among sensors of varying thicknesses, providing crucial insights for performance enhancement.

For the further understanding of the effect of radiation, the sensors are being exposed to different fluence using high intensity X-ray source. These results will also be presented.

Posters / **9**

Gain suppression studies at the CENPA tandem accelerator

Auteurs: Adam Molnar[1]; Jennifer Ott[1]; Peter Kammel[2]; Quentin Buat[3]; Simone Michele Mazza[4]; Svende Braun[2]; Yuzhan Zhao[1]

[1] *UCSC*

[2] *UW*

[3] *University of Washington*

[4] *UC Santa Cruz*

Auteur correspondant simone.michele.mazza@cern.ch

Using the CENPA Tandem accelerator at the University of Washington, we studied the response of low gain avalanche detectors (LGADs) to MeV-range deposits from a proton beam. LGADs are thin silicon detectors with moderate internal signal amplification. This type of devices is prone to a gain suppression mechanism, which is the topic of this study, especially for large energy depositions. Several devices with different thicknesses and gain layer configurations were tested as a function of bias voltage, angle and proton energy. Multichannel LGADs such as AC-LGADs and TI-LGADs were studied as well. This work is in the context of the PIONEER experiment, which is a next-generation experiment proposed at the Paul Scherrer Institute to perform high precision measurements of rare pion decays. At the center of the experiment, a high-granularity active target (ATAR) will stop the pion and characterize its decay. The ATAR is being designed to provide detailed 5D tracking information using LGAD sensors, allowing the separation of the energy deposits of the pion decay products in both position and time. Since a range of deposited charge from Minimum Ionizing Particle (MIP, few 10s of KeV) from positrons to several MeV from the stopping pions/muons is expected, the detection and separation of close-by hits in such a wide dynamic range will be the main challenge.

Posters / **12**

Design, performance and future prospects of vertex detectors at the FCC-ee

Auteur: Fabrizio Palla[1]

Co-auteur: Armin Ilg [2]

[1] *INFN Pisa*

[2] *University of Zürich*

Auteur correspondant fabrizio.palla@cern.ch

The CERN proposed e^+e^- Future Circular Collider (FCC-ee) is designed as an electroweak, flavour, Higgs and top factory with unprecedented luminosities. Many measurements at the FCC-ee will rely on the precise determination of the vertices, measured by dedicated vertex detectors.

All vertex detector designs use Monolithic Active Pixel Sensors (MAPS) with a single-hit resolution of ≈3 µm and a material budget as low as 0.25% $X/X0$ per detection layer, which is within specifications for most of the physics analyses.

This contribution presents the status of the R&D on fully engineered vertex detector, together with the challenges due to its cooling and integration with the collider beam pipe. Discussions on an ultra-light vertex detector layout using curved wafer-scale MAPS are also presented, which allows reducing the material budget by about a factor of four, at the expenses of some losses in efficiency.

System integration / **13**

CMS Phase-II Inner Tracker system tests

Auteur: Valeriia Lukashenko[1]

[1] *University of Zurich*

Auteur correspondant valeriia.lukashenko@cern.ch

The LHC will undergo an upgrade known as the High Luminosity LHC (HL-LHC), with the aim of delivering 3000 fb-1. The Compact Muon Solenoid (CMS) detector will be upgraded during the Phase-II upgrade to profit from the increased luminosity delivered by HL-LHC. As a part of the Phase-II upgrade, the CMS tracking detector will be replaced. In the regions closest to the beam, the Phase-II Inner Tracker (IT) will face harsh conditions with high integrated radiation levels of 1.2Grad and 2.3×10^{16} n_{eq}/cm^{2}, a high pileup of up to 200 collisions per bunch crossing, and hit rate up to 3.2 GHz/cm^{2}. Phase-II IT is designed to operate in these conditions while maintaining excellent performance. The IT hybrid pixel modules consist of planar or 3D silicon sensors with a pixel size of 25x100 μm^{2} that are bump-bonded to a readout ASIC developed by the RD53 collaboration and a high-density interconnect to connect power lines and readout signals. The modules are mounted on lightweight structures that provide serial power, cooling, and communication. The electrical signals from the modules are transformed into optical signals by the so-called portcards. The central (barrel) part of IT consists of four cylindrical structures, while the forward part is divided into two subsystems composed of eight small and four large disc-like structures per end. We present the results of the IT system tests from structures to portcards with prototype and final IT modules for the three subsystems and discuss their performance.

Posters / **14**

Design and construction of the Outer Tracker for the Phase-2 Upgrade

Auteur: Irene Zoi[1]

[1] *Fermi National Accelerator Laboratory*

Auteur correspondant irene.zoi@cern.ch

The High Luminosity LHC (HL-LHC) is expected to deliver an integrated luminosity of 3000 - 4000 fb^{-1} after 10 years of operation with peak instantaneous luminosity reaching about 5 - 7.5 $\times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. During Long Shutdown 3, several components of the CMS detector will undergo major changes, called Phase-2 upgrade, to be able to operate in the challenging environment of the HL-LHC. The current CMS silicon strip tracker has to be replaced with a new detector. The Phase-2 Outer Tracker (OT) will have higher radiation tolerance, higher granularity, and the capability to handle higher data rates compared to the current system. Another key feature of the OT will be to provide tracking information to the Level-1 (L1) trigger, allowing trigger rates to be kept at a sustainable level without sacrificing physics potential. For this, the OT will be made out of modules with two closely spaced sensors read out by front-end ASICs, which can correlate hits in the two sensors creating short track segments called stubs. The stubs will be used for tracking in the L1 track finder. The modules come in two flavors: strip-strip (2S) and pixel-strip (PS), which contain different sensor configurations and multiple ASICs. In this contribution, the design of the CMS Phase-2 OT, the technological choices, and the quality assurance (QA) procedures used to ensure the functionality

of the modules will be reported. The contribution will cover the first results with pre-production devices and the different aspects taken into account during the QA: from fulfilling the precision specification of the module assembly procedure to ensuring the proper communication between the different ASICs on the module. The module noise performance is also checked and the full module functionality is verified at different temperatures.

HEP experiments / **15**

ATLAS ITk Pixel Detector Overview

Auteurs: Manabu Togawa[1]; Simone Monzani[None]; Simone Monzani[2]

[1] *High Energy Accelerator Research Organization*

[2] *University of Udine*

Auteurs correspondants: simone.monzani@cern.ch, simone.monzani@uniud.it

In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in up to 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of the ITk will consist of a pixel detector, with an active area of about 13 m^2. To deal with the changing requirements in terms of radiation hardness, power dissipation and production yield, several silicon sensor technologies will be employed in the five barrel and endcap layers. As a timeline, it is facing to pre-production of components, sensor, building modules, mechanical structures and services. The pixel modules assembled with RD53B readout chips have been built to evaluate their production rate. Irradiation campaigns were done to evaluate their thermal and electrical performance before and after irradiation. A new powering scheme –serial –will be employed in the ITk pixel detector, helping to reduce the material budget of the detector as well as power dissipation. This contribution presents the status of the ITk-pixel project focusing on the lessons learned and the biggest challenges towards production, from mechanics structures to sensors, and it will summarize the latest results on closest-to-real demonstrators built using module, electric and cooling services prototypes.

Timing with pixels / **16**

MONOLITH - picosecond capability in a high granularity monolithic silicon pixel detector

Auteurs: Lorenzo Paolozzi[1]; giuseppe iacobucci[2]

[1] *University of Geneva*

[2] *Université de Genève*

Auteur correspondant lorenzo.paolozzi@unige.ch

The MONOLITH H2020 ERC Advanced project aims at producing a high-granularity monolithic silicon pixel detector with picosecond-level time stamping. Such extreme timing exploits: i) fast and low-noise SiGe BiCMOS electronics; ii) a novel sensor concept: the Picosecond Avalanche Detector (PicoAD), that uses a patented multi-PN junction to engineer the electric field and produce a continuous gain layer deep in the sensor volume. The result is an ultra-fast current signal with low intrinsic jitter in a full fill factor sensor.
In 2024, a testbeam with minimum-ionising particles of the monolithic PicoAD prototype provided full efficiency and 11.5 ps time resolution.

In addition, a prototype without internal gain layer was produced featuring the same SiGe HBT electronics. Testbeam measurements showed full efficiency and 20 ps time resolution at a power consumption of 0.9 W/cm^2 and a sensor bias voltage HV = 200 V. This prototype after being irradiated up to 1x10^16 neq/cm2, still provides an efficiency of 99.7% and 45 ps at HV = 300 V.

Medical imaging applications / **18**

100µPET: an ultra-high-resolution silicon-pixel-based PET scanner

Auteurs: giuseppe iacobucci[1]; roberto cardella[2]

[1] *Université de Genève*

[2] *niversité de Genève*

Auteur correspondant roberto.cardella@unige.ch

The 100µPET project is developing a pre-clinical medical scanner for positron-emission tomography (PET) with ultra-high-resolution molecular imaging capabilities. The scanner is composed of multiple layers of monolithic active pixel sensors (MAPS) connected to flexible printed circuits (FPC). With pixels of 150 µm pitch and a thickness of 280 µm + 300 µm (MAPS + FPC), the scanner achieves unprecedented volumetric spatial resolution of 0.02 mm^3, one order of magnitude better than the best current PET scanners, and offers uniform resolution along the scanner's field-of-view (parallax free). The MAPS and its design features will be presented, along with the pixel read-out architecture. The construction and quality control of the scanner and its multiple detection modules, prototyped with pre-production chips and FPCs, will be showcased, and the latest imaging reconstruction with simulated high-definition mouse phantoms will be presented.

Astrophysics applications / **19**

The first MAPS based tracker for space applications

Auteur: Ester Ricci[1]

[1] *University of Trento and INFN-TIFPA*

Auteur correspondant ester.ricci@unitn.it

For decades, silicon microstrip detectors have been the preferred technology for tracking particles in space, allowing the realisation and operation of successful missions as AMS-02 and FERMI LAT, which are providing remarkable scientific results. However, the next generation of experiments aims to push our understanding even further, and will require significant improvements in tracking performance, achievable by transitioning to pixel detectors. Among various pixel designs and technologies, Monolithic Active Pixel Sensors (MAPS) stand out due to their low production costs, simple assembly and readout, and low noise.

The High Energy Particle Detector (HEPD-02), developed by the Italian Limadou collaboration, is set to mark a significant advancement in particle tracking in space. Scheduled for launch on the second China Seismo-Electromagnetic Satellite (CSES-02) at the end of 2024, HEPD-02 will measure electron and proton fluxes within energy ranges of 3-100 MeV and 30-200 MeV, respectively. This experiment will be the first to use Monolithic Active Pixel Sensors as a tracking unit in space.

Designing the HEPD-02 tracker posed several challenges, particularly in keeping power consumption low, with the consequent positive impacts on thermal regulation. Power reduction was achieved through innovative readout techniques and comprehensive strategies. The final tracker design consists of five modules, each containing three sensitive layers with 10 ALTAI units.

The HEPD-02 tracker has undergone successful space flight qualification and scientific performance assessment, demonstrating excellent efficiency and a spatial resolution of less than 10 μm, comparable to the best-performing trackers currently operating in space. Now integrated onto the CSES-02 satellite, HEPD-02 will set a new standard in particle detection from space, opening new frontiers for space-based particle physics research and opening the way for future advancements in the field.

Sensing materials & Radiaiton tolerance / **20**

Operational Experience and Performance with the ATLAS Pixel detector at the Large Hadron Collider at CERN

Auteurs: ATLAS Collaboration[None]; Marcello Bindi[1]

[1] *University of Goettingen*

Auteur correspondant marcello.bindi@cern.ch

The tracking performance of the ATLAS detector relies critically on its 4-layer Pixel Detector. As the closest detector component to the interaction point, this detector is subjected to a significant amount of radiation over its lifetime. At present, at the start of 2024-Run3 LHC collision ATLAS Pixel Detector on innermost layers, consisting of
planar and 3D pixel sensors, will operate after integrating fluence of O(1015) 1 MeV n-eq cm-2.
The ATLAS collaboration is continually evaluating the impact of radiation on the Pixel Detector.
In this talk the key status and performance metrics of the ATLAS Pixel Detector are summarised, putting focus on performance and operating conditions with special emphasis to radiation damage and mitigation techniques adopted for LHC Run3.
These results provide useful indications for the optimisation of the operating conditions for the new generation of pixel trackers under construction for HL-LHC upgrades

Monolithic sensors / **21**

Exploring ALICE ITS3 MOST: Early Results on Power Segmentation and Asynchronous Readout for Timing in a Monolithic Stitched Sensor

Auteur: Mariia Selina[1]

[1] *Nikhef, Utrecht University*

Auteur correspondant mselina@nikhef.nl

The adoption of monolithic active pixel sensors (MAPS) in CMOS technologies for high-energy physics experiments was a breakthrough. These pixel detectors can achieve a material budget as low as 0.1% of the radiation length per layer, as they integrate the readout electronics within the sensor itself.

After the successful installation of the ITS2 detector, covering 10 m² with MAPS, a further upgrade (ITS3) is being developed to replace the three inner vertex layers with wafer-scale stitched sensors bent around the beam pipe. For this investigation, two stitched sensors were developed: the MOnolithic Stitched Sensor (MOSS) and the MOnolithic Stitched sensor with Timing (MOST), each 25.9 cm long and 1.4 cm and 0.25 cm wide, respectively. The MOST contains more than 900,000 pixels with a size of 18 μm x 18 μm. Which are divided into groups and units to minimize output signal collisions in the case of charge-sharing pixels on the four CML outputs of the chip.

In the MOST, one global analog and one global digital power domain for the matrix are implemented, and small fractions of the circuit can be connected to these using conservatively designed switches. This allows a finer granularity for powering and simplifies communication with the chip. This scheme will be used in the final chip for the ITS3.

The MOSS is equipped with a synchronous readout, whereas the MOST has an asynchronous readout in which hit data is transmitted immediately upon the detection of the hit to the endcap of the chip, up to about 26 cm away. Both chips have been tested and found to be functional.

One of the aims of the MOST is to evaluate whether and to what extent the timing information of these asynchronous signals is conserved during this long-distance on-chip transmission without being corrupted by on-chip activity and other factors. If successful, this would open the way to timing architectures that avoid distributing a timing reference over the full pixel matrix.

In this contribution, detailed measurement results of the MOST will be presented, covering basic functionality tests, including characterization of the threshold and noise of the pixel front end, as well as powering tests, validation of the powering scheme, and tests related to the transmission of timing signals.

Sensing materials & Radiaiton tolerance / **22**

Evaluation of pixel sensors produced with a commercial 150nm CMOS process for the CMS Phase-2 Upgrade

Auteur: Thierry Guillaume Harte[1]

[1] *ETH Zurich / CMS*

Auteur correspondant thierry.guillaume.harte@cern.ch

CMS will undergo a major upgrade to prepare for the High-Luminosity phase of the LHC. Within the frame of this upgrade, studies on a novel passive sensor production technique for planar hybrid detectors have been performed. The sensors were produced using a commercial CMOS production process with a feature size of 150nm. This process enables the use of stitching to produce large sensors out of different sub-reticles of $11.5 \times 9.6\ \mathrm{mm}^2$. This provides the possibility to produce sensors larger than the size of a reticle of $\sim 3 \times 2\ \mathrm{cm}^2$ while retaining the small feature sizes enabled through projection lithography. Additionally, the use of commercial production lines enables higher throughput and potentially less expensive development with the possibility to process larger wafers than in conventional productions that apply contact lithography. To evaluate this novel sensor production process, two large prototyping campaigns have been performed for the CMS Phase-2 Inner Tracker. This includes the production of large sensors with a size of up to $\sim 4 \times 4\ \mathrm{cm}^2$ and a pixel pitch of $25 \times 100\ \mu\mathrm{m}^2$. The sensors were irradiated to a non-ionizing radiation dose of up to $1 \cdot 10^{16}\ 1\ \mathrm{MeV}\ \mathrm{n_{eq}}/\mathrm{cm}^2$. Both, before and after the irradiation campaign, the sensors were tested in test beam environments bump-bonded to RD53A and CROC, read-out chips. The prototyping campaigns have shown, that sensors produced with a commercial 150nm CMOS process fulfill the performance requirements for CMS Phase-2 Inner Tracker and are a promising candidate, also for future detectors. In this talk, a summary of the two prototyping campaigns will be presented, including the yield of the sensor production, the performance of the sensors and a comparison of their detection efficiency and spatial resolution before and after irradiation.

Posters / **24**

Performance and Design Validation of CMS Phase-2 Pixel Modules

Auteur: Giorgia Bonomelli[1]

[1] *ETHZ*

Auteur correspondant gbonomelli@student.ethz.ch

In view of the High Luminosity LHC, the current CMS Tracker detector will have to be replaced during Long Shutdown 3 to survive the higher radiation environment and to withstand an increased data rate. To prepare for the so called CMS Phase II upgrade, multiple studies were carried out to characterize the pixel module design and their performance. For this purpose, different aspects were put together to build a module Quality Control (QC) procedure and novel techniques became part of the module design validation process for the full-size prototype chip (CROCv1). Based on the outcome of the results collected on CROCv1 prototype modules and according to the module selection criteria the community agreed on, some changes were introduced in the module design to optimize the performance. This led to the production of the definitive chip (CROCv2) which will be installed in the final CMS detector.
This study presents the quality control test flow performed, both for the 1x2 and 2x2 design, on a big sample of CROCv1 prototypes together with the results that validated this module design. In particular, the validation process includes measurements of the readout chip powering, data transmission tests and open bump bonds identification. Thermal stress tests were instead performed only on a subset of pixel modules to ensure the integrity of the sensor and to provide quick feedback on the quality of the bump bond connectivity after harsh temperature cycles. Moreover, this work contains the latest design validation results on the first production CROCv2 modules which confirm that, even after some minor design changes, the definitive module design still fulfils the requirements.

Posters / **25**

Low dose gamma irradiation study of ATLAS ITk MD8 diodes and miniature strip sensors

Auteur: Marcela Mikestikova[1]

[1] *Institute of Physics, CAS*

Auteur correspondant marcela.mikestikova@cern.ch

Silicon strip detectors developed for the Inner Tracker (ITk) of the ATLAS experiment will operate in a harsh radiation environment of the HL-LHC accelerator. The ITk is thus designed to endure a total fluence of 1.6×1015 1 MeV neq/cm2 and a total ionizing dose (TID) of 66 Mrad in the strip detector region. A radiation-hard n^+-in-p technology is implemented in the ITk strip sensors. To achieve the required radiation hardness, extensive irradiation studies were conducted during sensor development, primarily performed up to the maximal expected total fluence and TID to ensure the end-of-life operations. These studies included irradiations of sensors with various particle types and energies, including the 60Co gamma rays. Our previous results obtained for gamma irradiated diodes and strip sensors indicate a linear increase of bulk current with TID, while a surface current saturates at the lowest TID levels checked, preventing a determination of the exact TID for which the observed saturation occurs.
This contribution presents the results coming from irradiations by 60Co gamma rays to multiple low TIDs, ranging from 0.5 to 100 krad. The detailed study of total, bulk, and surface currents of miniature strip sensors and diodes explores an unknown dependence of surface current on the TID, temperature and annealing. Additionally, the effect of the p-stop implant between the guard ring and the bias ring of measured samples will be discussed, which reveals the characteristics of the surface current, in the central region of the miniature sensors and in the edge region of the diode. The observations are relevant for the initial operations of the new tracker.

Monolithic sensors / **26**

Suitability of a 65 nm CMOS imaging process to reach the position resolution required by a vertex detector at FCCee

Auteur: Ziad El Bitar[1]

Co-auteurs: Ajit Kumar [2]; Alessandra Lorenzetti ; Anna Macchiolo ; Armin Ilg [3]; Eduardo Ploerer ; Emmanuel Medernach [4]; Gaëlle Sadowski [5]; Jerome Baudot [1]; Serhiy SENYUKOV [6]; auguste besson [7]; jeremy andrea [1]

[1] *IPHC*

[2] *IPHC Strasbourg*

[3] *University of Zürich*

[4] *CNRS IN2P3 IPHC*

[5] *iphc*

[6] *Institut Pluridisciplinaire Hubert CURIEN (IPHC)*

[7] *Institut Pluridisciplinaire Hubert Curien*

Auteur correspondant ziad.elbitar@iphc.cnrs.fr

The performance of monolithic CMOS pixel sensors depends on their fabrication process and especially the feature size which directly drives the pixel size. A consortium led by the CERN EP R&D program, the ALICE experiment, and various European projects (AIDAinnova, EURIZON) is investigating the benefits of a 65~nm CMOS imaging process to design a new generation of pixel sensors. These developments have enabled the upgrade of the inner layers (ITS3) of the ALICE experiments and are fostering further studies for detectors including those for future e+e- colliders that are still currently unmatched by any technology.

Three fabrications of a variety of prototype sensors already took place, in 2020, 2022, and 2023. The present contribution reports on the characterization of the second version of the CE-65-v2 (Exploratory Circuit) sensor family. The CE-65-v2 sensor includes AC-coupled and analog output pixels either in a squared or staggered arrangement. They include analog output matrices featuring 48×24 (1152) pixels with either 15-µm, 18-µm or 22.5-µm pixels. Three versions of the sensing node were fabricated to modify the charge sharing between pixels. Sensors were irradiated to non-ionizing fluences between 10^{13} and 5x10^{14} n_{eq} as well as to few hundreds Mrad as ionizing dose. Illumination with Fe source allowed us to estimate the equivalent collection node capacitance and its pixel-to-pixel fluctuation, as well as the leakage current before and after irradiation. Non-irradiated sensors were tested in beams with 4-GeV electron or 120-GeV mixed hadrons to study in detail the charge sharing among pixels and extract the sensor detection efficiencies as well as their position resolutions. The evolution of the latter with digitization strategies, simulated from the data, was also investigated to explore the potential of pixels with binary or few bits output, designed in this 65-nm process, to match the excellent resolution expected for the inner layers of an FCCee detector. We pursue to continue developing the 65-nm process to fulfill all FCCee vertex detector requirements and improve upon them.

HEP experiments / **27**

ALICE Inner Tracking System 3 Overview

Auteur: Felix Reidt[1]

[1] *CERN*

Auteur correspondant felix.reidt@cern.ch

The Inner Tracking System 3 (ITS3) is the next generation vertex detector for ALICE, the heavy-ion focused experiment at the CERN Large Hadron Collider foreseen to be installed during the Long Shut- down 3. The ITS3 will replace the innermost three layers of the current Inner Tracking System 2. ITS3 will consist of bent, wafer-scale monolithic pixel sensors manufactured in the TPSCo 65 nm process. The mechanical support structure based on carbon foam allows to reduce the average material budget to 0.9% X_0. Moreover, the radius of the innermost layer will be reduced from 23 mm to 19 mm. Reduction of material budget and radius of the inner most layer are projected to improve the impact parameter resolution by a factor of two at a transverse momentum of 1 GeV/c.

After a successful R&D phase in 2019 –2023 leading to the ITS3 Technical Design Report, the final sensor and mechanics are being developed right now.

This contribution will review the ALICE ITS3 detector concept and will give an overview on recent R&D achievements, current activities, the road to completion and installation as well as a projection of the improved physics performance.

Posters / **29**

Testing small scale devices for ALICE ITS3 upgrade

Auteur: Alessandro Sturniolo[1]

[1] *University of Messina and INFN-CT*

Auteur correspondant a.sturniolo@cern.ch

During the Long Shutdown 2 (LS2), the ALICE Inner Tracking System was upgraded to its second version ITS2, consisting of 7 layers of silicon CMOS Monolithic Active Pixel Sensors, the ALICE Pixel Detectors (ALPIDE MAPS). Thanks to the integrated read-out circuitry, ALPIDE MAPS thickness in terms of radiation length X_0 has already been reduced to $0.36\%X_0$ per layer in ITS2, but this could be further reduced to an average of $0.09\%X_0$ per layer by removing the non-silicon contribution to detectors'material budget.
This is the goal of the ALICE ITS upgrade to ITS3, to be carried out during the upcoming Long Shutdown 3 (scheduled for 2026-2028). After the upgrade the 3 innermost ITS2 layers (Inner Barrel, or IB) will be replaced by 3 flexible, truly cylindrical layers of stitched MAPS chips. The reduced need for supporting frames, as well as the substitution of the present water cooling system with air cooling, is expected to lead to a dramatic drop in material budget. Higher tracking precision and approximately twice a better pointing resolution than ITS2 (especially at low momenta) are also expected. Such improvements will greatly benefit physics studies on heavy-flavored particles with few tens μm long mean paths cτ.
The ITS3 sensors are produced using a 65 nm process, instead of the current 180 nm used in ITS2. A wide range of Multi-Layer Reticle 1 (MLR1) small test devices have been developed to validate this new technology, including Analog and Digital Pixel Test Structures (APTS and DPTS), designed to optimize pixel charge collection process and front-end configuration, respectively.
In this contribution results of MLR1 device tests will be shown. Measurements have been performed both under charged particle beams and in laboratory with a ^{55}Fe source, in order to investigate the MLR1 65 nm small test device performances and to compare them with the upcoming ITS3 goals (99% detection efficiency and 5 μm spatial resolution under up to 10 kGy TID + 10^{13} 1 MeV n_{eq}/cm^2 NIEL). APTS laboratory measurements have shown high charge collection efficiency after a low-dose n-type blanket implantation, while test beam results both on APTS and DPTS have proven that the expectations for ITS3 sensor detection efficiency and spatial resolution are met.

Monolithic sensors / **30**

Characterization of silicon Monolithic Stitched Sensors (MOSS) for the ALICE ITS3 for the LHC Run 4

Auteur: Livia Terlizzi[1]

[1] *Università and INFN Torino*

Auteur correspondant livia.terlizzi@cern.ch

ALICE (A Large Ion Collider Experiment) is one of the four main experiments at the CERN Large Hadron Collider (LHC), and it is mainly designed to study heavy-ion collisions at ultra-relativistic energies. In view of the LHC Run 4, foreseen to start in 2029, ALICE will replace the three innermost cylindrical layers of its current inner tracking system (ITS2) during the Long Shutdown 3

(2026-2028).
The new system, ITS3, will improve the pointing resolution by a factor of two over a large momentum range and the tracking efficiency at low transverse momenta of pT < 0.3 GeV/c. It will consist of ultra-thin, i.e. ≤ 50 µm, stitched wafer-scale Monolithic Active Pixel Sensors (MAPS), built using the 65 nm CMOS imaging process. These sensors can be bent, allowing the formation of truly cylindrical barrel with a radial distance from the beam pipe as low as 19 mm for the innermost layer and a very low material budget of 0.09 X/X0 in average per layer.
The development of the ITS3 includes a number of cutting-edge R&D efforts: the production and characterization of the MAPS in the 65 nm CMOS process, the fabrication of the stitched wafer-scale MAPS, and the development of an ultra-light detector mechanics and a new air cooling system. In particular, the 65 nm CMOS technology for particle tracking and radiation hardness was validated with a set of test structures called Multi-Layer Reticle 1 (MLR1). In mid 2023 the first stitched prototypes called MOnolithic Stitched Sensors (MOSS) have been produced with the primary goals of demonstrating the feasibility of the stitching process and of studying the yield and performance of wafer-scale sensors, in view of the production of the ITS3 final-size full-functionality prototype sensor chip.
A single MOSS chip measures 1.4×25.9 cm2 and has a total of 6.7 million pixels. It is composed of one left endcap, 10 repeated sensor units with eight pixel matrices each, to increase power granularity and hence resilience to manufacturing faults: 256×256 pixels with 22.5 µm pitch in each top matrix and 320×320 pixels with 18 µm pitch in each bottom matrix. The different layouts are used to compare the yield depending on the densities and spacing margins.
This presentation will focus on the results from the characterisation campaign of the stitched sensors in the laboratory and in beam tests, including the verification of power domain impedances, DAC performance, pixel front-end readout response, threshold and fake-hit rate scans. Test results have proven that MOSS has an efficiency higher than 99% with a Fake Hit Rate lower than 0.1 pixel−1 s−1 , which satisfies ITS3 sensor
requirements for LHC Run 4.

Posters / 31

A prototype pixel readout chip with column-level ADC for high frame rate XFEL applications

Auteurs: Shijie Lu[1]; Tianyang Wang[2]

Co-auteurs: Fuwan Gan [1]; Tao Sun [1]; Zhen Sheng [1]; Zhi Liu [3]; Zizhao Ji [1]

[1] *Shanghai Institute of Microsystem and Information Technology*

[2] *Zhangjiang Laboratory*

[3] *ShanghaiTech University*

Auteur correspondant lusj@mail.sim.ac.cn

X-ray free electron laser (XFEL) facilities can delivery femtosecond X-ray pulses with ultra-high peak brightness, which in turn calls for high performance integrating type pixel detectors. State-of-the-art pixel read chips for detectors commissioning at XFEL facilities usually employ amplifiers with multi-gain stages within the pixel to reach high dynamic range, typically from 1 to 10^4 photons per pixel per X-ray pulse. However, the pixel readout chips of these detectors mostly adopt direct analog signal readout, limiting their frame rate to 100 −1kHz [1,2]. Such performance is no longer in line with the evolvement of XFELs towards high repetition rate beyond 10kHz. This work proposes a pixel readout ASIC (Application Specific Integrated Circuit) chip with digital readout architecture for applications at next generation high repetition rate XFELs. Instead of multiplexing the analog signals from the pixel matrix to a few output ports like conventional XFEL detectors, the proposed chip incorporates a low power, small area ADC (analog-to-digital converter) at each column end to digitize the pixel analog signal transmitted sequentially from the column. Further on-chip data processing in the digital domain can be more robust and versatile than in the analog domain. Modern high speed serial interface can be used to transmit the digital stream off chip with high throughput, enabling a significant increase in frame rate as compared to the analog readout scheme.

A small-scale prototype chip with a pixel array of 16 × 16 was designed and fabricated in a 130 nm CMOS process. The goal is to demonstrate the proposed chip architecture for high dynamic and high frame rate X-ray imaging at XFELs. The pixel size is 150 μm × 150 μm. The dynamic-gain-switching amplifier like the AGIPD and JUNGFRAU pixel readout ASIC chips is implemented to achieve a high dynamic range required by XFEL applications. The pixel array is read out row by row. Each column is terminated by an 11-bit SAR ADC working at the nominal speed of 2MS/s. The digital signals are further readout by a serial chip interface. First tests show full chip functionality and the analog front-end can accommodate an equivalent input signal up to 10^4 12keV photons. The measurement of individual ADC channels and calibration of the full readout chain are ongoing. In the conference, the design and measurement results of the prototype chip will be presented.

[1] A. Allahgholi, et al., The Adaptive Gain Integrating Pixel Detector at the European XFEL, Journal of Synchrotron Radiation 26 (2019) 74
[2] A. Mozzanica, et al., JUNGFRAU Detector for Applications at Synchrotron Light Sources and XFELs, Synchrotron Radiation News 31 (2018) 16

Posters / **32**

Radiation damage effects in ATLAS Pixels and their simulations: status, results and and perspectives.

Auteurs: ATLAS Collaboration[None]; Marco Bomben[1]

[1] *APC*

Auteur correspondant marco.bomben@apc.in2p3.fr

Signal reduction is the most important radiation damage effect on performance of silicon tracking detectors. Adjusting sensor bias voltage and detection threshold can help in mitigating the effects, but it is important to have simulated data that reproduce the evolution of performance with the accumulation of luminosity, hence fluence.
The two innermost pixel layers of ATLAS (Insertable B-Layer and B-Layer), consisting in both planar and 3D sensors, have already integrated fluences in excess of 1x10^15 n_eq/cm^2 and show significant charge collection loss and cluster modification.
ATLAS collaboration developed and implemented an algorithm that reproduces signal loss, cluster modification and changes in Lorentz angle due to radiation damage. This algorithm is now the default for Run3 simulated events. In this talk the algorithm will be
presented and results compared to Run3 collision data, with emphasis on cluster properties and higher level objects performance.

Posters / **33**

Towards the construction of the ATLAS ITk Pixel innermost layer

Auteur: Simone Ravera[1]

[1] *CERN*

Auteur correspondant simone.ravera@cern.ch

With the beginning of the High Luminosity program of the Large Hadron Collider (HL-LHC) the ATLAS detector will have to face an increased instantaneous luminosity up to 7.5· 10^{34} cm^{-2} s^{-1} and an average of 200 proton-proton collisions per bunch-crossing. To be ready for these challenging beam conditions the ATLAS Inner Detector will be completely replaced with a new all-silicon Inner Tracker, the ITk, made of a Pixel detector at a small radius and a large area Strip detector surrounding

it. The design phase of the ITk has been completed and the project is now moving into the production phase.
The new Pixel tracker is based on hybrid detectors, made of a readout chip implemented in the 65 nm technology and a silicon pixel sensor, the interconnection between the two parts is made via the bump-bonding technology. Two technologies have been chosen for the pixel sensors: planar sensors for the outermost layers and 3D pixel sensors for the innermost layer. The choice for 3D sensors is driven by their built-in radiation hardness since the innermost layer will reach a fluence up to $2{\cdot}10^{16}$ n_{eq}/cm^2 (with a 1.5 safety factor) which is not suitable for planar sensor operation. To reduce the budget material of the detector the serial powering scheme will be implemented. Moreover, to cope with the increased luminosity, the system has been design to sustain high-speed data transmission at 1.28 Gb/s.
This talk aims to give an overview of the status of the ITk innermost layer. The ITk innermost layer, placed at 34 mm from the beamline, will play a crucial role in the tracker performance, driving the accuracy of the track impact parameters and, as such, the reconstruction of primary/secondary vertices, the identification of primary leptons, up to the performance of high-level objects like b-tagging and light-jet rejection. \par
The talk will focus on the performance of 3D pixel sensors, measured in several test beam campaigns, after irradiation up the ITk innermost layer end-of-life fluence (2e16 n_{eq}/cm^2, considering a 1.5 safety factor). Then it will present the results of the assembly procedure in the production sites, quality control and assurance of the pixel modules assembly and testing, mainly focusing on the quality of the bump-bonding connection, that has been validated through dedicated bumps delamination studies. Finally, the talk will cover the results of the data transmission tests carried out at 1.28 Gb/s with the Time Domain Reflectometer technique.

Posters / **34**

ATLAS ITk Production Database use and tools for ITk Pixels community

Auteurs: Kenneth Gibb Wraight[1]; Luka Selem[None]

[1] *University of Glasgow*

Auteur correspondant luka.selem@lpsc.in2p3.fr

The ATLAS experiment will undergo major upgrades for operation at the high luminosity LHC. The high pile-up interaction environment (up to 200 interactions per 40MHz bunch crossing) requires a new radiation-hard tracking detector with a fast readout.
The Inner Tracker (ITk) upgrade is an international effort to meet this challenge.

The scale of the upgraded tracker is much larger than the current ATLAS tracker. The tracker consists of ~4000 modules while ITk is designed to have ~9,500 pixel modules (and ~18,000 strip modules). The manufacture of the different detector components follows a complex production flow involving institutes around the globe. To maintain the tight production schedule, a continuous monitoring of production rates is essential.

The ITk Production Database (PDB) is a custom database developed to track the location of ITk components, monitor production progress, and retain component information to support data-taking performance during 10 years of running. Results from QC/QA tests carried out over multiple production steps must be uploaded, production rates and yields extracted, and component shipments and inventories monitored to ensure no institute lacks material. In addition, the PDB is a resource for CERN's dual export license oversight used for some items such as frontend chips, where all materials must be returned to CERN even if they are faulty.

In the case of ITk pixel production the database currently hosts data for more than 200 component types, including sensors, front-end chips, flexes, assembled modules and larger structures and cables. Each component has associated data on component tests and tracks production stages. Roughly 60 production sites and more than 300 users are registered for pixels production including vendors, research laboratories and universities.

User interaction with the PDB such as component registration and test data uploads is done either via a dedicated PDB web GUI (shared with all ITk projects) or through an API. APIs are a common tool to mediate user interactions with databases and provide flexibility in custom GUI development. Interface development is provided by a community of PDB experts who have pursued several options to meet collaboration needs: a pythonic API wrapper, data-acquisition GUIs with integrated scripts, commandline scripts. Tools have been distributed via git repositories, containerised applications, and CERN hosted platforms such as Openshift.

A complimentary effort is made to report data from the PDB to monitor production evolution. Reports are prepared for specific user audiences to meet specific tasks, including management oversight and collaboration reviews. This information helps to quickly identify and remedy any production issues.

Examples will be provided of ITk Pixel community tools for PDB population and reporting.
Though the examples are ATLAS ITk Pixels specific, the general themes of large-scale data management and multi-user global accessibility are now standard to LHC-scale detector production. These concepts are relevant to modern high-energy particle physics and large experiments beyond HEP. The goal of this presentation is to promote information exchange and collaboration of tools which can support production.

HEP experiments / **35**

The vertexing challenge at FCC-ee

Auteur: Armin Ilg[1]

Co-auteurs: Anna Macchiolo ; Fabrizio Palla [2]

[1] *University of Zürich*

[2] *INFN Pisa*

Auteur correspondant armin.ilg@cern.ch

Following in the footsteps of the LHC, the Future Circular Collider (FCC) will be the next multi-generational international collider project. In the first stage, FCC-ee will collide intense beams of electrons and positrons at centre of mass energies between 88 and 365 GeV, making it an electroweak, flavour, Higgs and top factory. The unprecedented statistical precision requires FCC-ee experiments to limit their systematic uncertainties to the very minimum.
The precise reconstruction of the interaction vertices is core to most measurements at FCC-ee such as, for example, rare flavour physics processes and the measurement of Higgs and Z decays to bottom and charm quarks and taus.
This contribution will discuss the requirements of FCC-ee vertex detectors, covering the necessary impact parameter resolution, needed rate capability given beam-induced backgrounds, and radiation tolerance, while keeping the material budget below $\approx 0.3\%\ x/X_0$ per detection layer.
These detector requirements translate into requirements on the sensors used for the vertex detector. As discussed in this contribution, they need to feature $\leq 3\mu$m spatial resolution and provide timing information of $\mathcal{O}(\mu$s-ns$)$ while keeping power consumption minimal to allow for air-cooling of the detector –minimising the detector material budget.
The only type of sensor capable of aiming to fulfil such requirements are CMOS Monolithic Active Pixel Sensors (MAPS), which combine signal generation, amplification and readout into a single silicon die. Therefore, the rest of this contribution will present an overview of existing and planned MAPS technologies and prototypes towards fulfilling the stringent FCC-ee vertex detector requirements.
Lastly, a short outlook towards novel FCC-ee vertex detector designs will be given.

Astrophysics applications / **36**

Survey of sub-electron noise CMOS image sensors

Auteur: Prayag Wakale[1]

Co-auteurs: Bart Dierickx [2]; Filip Tavernier [3]

[1] *Caeleste and KU Leuven*

[2] *Caeleste*

[3] *MICAS, KU Leuven*

Auteur correspondant prayag.wakale@caeleste.be

Low-light imaging applications, such as astronomy or microscopy, require low-noise image sensors. Noise levels far below 1 e^-_{rms} are pursued. Single-photon detection is considered the holy grail of image sensing.

Existing imaging technologies capable of detecting and resolving individual photons like Photomultiplier Tubes (PMT), Single Photon Avalanche Diodes (SPAD), and Electron Multiplication Charge-Coupled Devices (EMCCD) employ internal multiplication of the primary electron. Although these have sub-fractional e^-_{rms} noise, these methods suffer from two performance-limiting properties: dark counts and excess noise.

This paper surveys solutions for photo charge integrating active pixel sensors (APS) and classic CMOS image sensor (CIS) technology. For integrating image sensor pixels to have quantum-limited photon detection, the readout noise at the pixel front needs to be substantially less than 0.3 e^-_{rms} [1].

APS pixel separates the photo charge sensing and the charge to voltage conversion node. This results in a high in-pixel conversion gain and the cancellation of the kTC noise with correlated double sampling (CDS). The pinned photodiode in APS has benefits regarding dark current and rivals the charge-coupled devices (CCD) performance. Continuous improvement of CIS over the last two decades has led to the replacement of CCD by CIS.

In this survey, we review the publications that report a noise figure close to 0.3 e^-_{rms} or lower. Based on the device and circuit techniques used and breakthroughs reached, we classify the publications into the following categories:

1. Pixel circuit topologies
    - CCD-based skipper in CMOS [2][5],
    - Classic PPD-based pixel with source follower readout,
    - In-pixel capacitive trans-impedance amplifier (CTIA) [8], etc.
2. Circuit operation techniques
    - Non-destructive readout [2][5],
    - In-pixel amplification [6],
    - Oversampling methods [2][4][8], etc.
3. Device optimizations
    - Floating gate skipper in CMOS [2],
    - Reduction in floating diffusion (FD) capacitance [4][7][9],
    - Reset gateless pixel [4][7], etc.
4. Transistor selection
    - Buried channel transistors [9],
    - Thin oxide transistors [4],
    - Standard transistors, etc.

At the conference, we will give an outlook on recent developments at Caeleste.

References

[1] N. Teranishi, Electron Devices, 2012
[2] Lapi, Agustin J. *et al.*, TBD, 2024
[3] W. Deng *et al.*, IEEE Transactions on Electron Devices, 2022

[4] A. Boukhayma *et al.*, IEEE Electron Device Letters, 2020
[5] Stefanov KD *et al.*, Sensors, 2020
[6] M. Sato *et al.*, IEEE International Solid-State Circuits Conference, 2020
[7] M. Seo *et al.*, IEEE Electron Device Letters, 2015
[8] Q. Yao *et al.*, Proceedings of the International Image Sensor Workshop, 2015
[9] S. Wakashima *et al.*, Symposium on VLSI Circuits, 2015

Electronics / **37**

The LHCb VELO Upgrade II: design and development of the read-out electronics

Auteurs: Daniel Johnson[None]; Kazuyoshi Akiba[1]; Stefano De Capua[2]; Victor Coco[3]

[1] *Nikhef*

[2] *University of Manchester*

[3] *CERN*

Auteur correspondant daniel.johnson@cern.ch

The LHCb Upgrade-I detector is currently operating at the Large Hadron Collider at CERN and it is expected to collect about 50 fb−1 by the end of Run 4 (2032), when many sub-systems of the detector will reach their end of lifetime. In order to fully exploit the High-Luminosity LHC potential in flavour physics, the LHCb collaboration proposes a Phase-II Upgrade of the detector, to be installed during the LHC Long Shutdown 4 (2032-2034). This Upgrade will consist of a re-designed system with the capability of operating at an instantaneous luminosity of 2×10^{34} $cm^{-2}s^{-1}$, i.e. a factor 10 larger than that of the Phase-I Upgrade detector and will allow the experiment to accumulate an integrated luminosity of about 300 fb−1.
Operating in the HL-LHC environment poses significant challenges to the design of the upgraded detector, and in particular to its tracking system. The primary and secondary vertices reconstruction will become more difficult due to the increase, by a factor 8, of the average number of interactions per bunch crossing (pile-up). Similarly, the track reconstruction will become more challenging, as well as time-consuming, because of the large increase in the track multiplicity. Finally, the much harsher radiation environment will make the design of the sub-systems quite challenging, with the radiation damage expected to be more severe for most detectors. In particular, the performance of the VErtex LOcator (VELO), which is the tracking detector surrounding the interaction region, is essential to the success of this Phase-II Upgrade. With the expected higher particle flux, the VELO Upgrade-II detector will have to tolerate a dramatically increased data rate: assuming the same hybrid pixel design and detector geometry, the front-end electronics (ASICs) of the VELO Upgrade-II will have to cope with rates as high as 8 Ghits/s, with the hottest pixels reaching up to 500 khits/s. With this input rate, the data output from the VELO will exceed 30 Tbit/s, with potentially a further increase if more information is added to the read-out.

The VELO collaboration is currently exploring new sensor technologies, and the benefits that would derive from adding a time stamp to the track reconstruction, such that interactions in the same bunch crossing can be more effectively disentangled. The VELO case is extremely challenging, as the high granularity required for the spatial measurement severely limits the area in each pixel of the ASIC where the time-stamping circuitry can be implemented. With a 50 ps hit resolution, each VELO track would have multiple time measurements from the traversed pixels and thus a precise estimation of the production time of charged particles. The most recent advances in this field, and the potential candidates that can meet the VELO Upgrade-II requirements, will be presented. In particular, the current state-of-the-art prototypes in the development of ASICs with TDC-per-pixel architecture, the PicoPix ASIC (which is an evolution of the Timepix4 design) and the TIMESPOT ASIC, will be discussed.

Sensing materials & Radiaiton tolerance / **38**

10µm Global Shutter Pixel for Radiation Tolerant CMOS Image Sensors

Auteur: Pedro Nuno T. Santos[1]

Co-auteurs: Idham Hafizh [1]; Paul Leroux [1]; Guy Meynants [1]

[1] *KU Leuven Association*

Auteur correspondant pedronuno.teixeiradossantos@kuleuven.be

This article presents a new global shutter pixel design with radiation-hardened-by-design(RHBD) device modifications and correlated double sampling (CDS). Global Shutter Imagers presents undeniable advantages by exposing all pixels simultaneously. Once in-pixel storage is included, the pixel readout can be operated simultaneously with exposure, enabling faster operation and flashed light. Additionally, this architecture is robust against motion defects and easy to operate in synchronous mode. The Radiation tolerance of the outlined pixel is targeted up to 1MGy SiO2 Total Ionizing Dose (TID). A partially pinned photodiode structure, combined with an enclosed transistor layout known as a "butterfly"[1] [2] is used to withstand such a high TID value. The use of P+ implant on SENSOR implant and recessed shallow trench isolation (STI) are specially used to reduce the dark current from the TID-induced interface traps and SiO2 interface while also shielding the photodiode region from TID-induced positive charges in the SiO2. Correlated double sampling (CDS) [3] is required to reduce the read noise by suppressing important noise sources such as photon shot noise, thermal noise (kTC) and flicker noise contributions. Two in-pixel memory and two readout paths are implemented to allow CDS. The pixel operation includes a sample phase where the pixel signal is locally stored followed by a reset phase and the pixel reset store. The in-pixel storage is designed with enclosed butterfly MOS devices that allow great charge density for low area and with limited leakage due to the RHBD. The readout is performed by operating two output SF and two output buses. The pixel is designed using 180nm CMOS Image Sensor (CIS) technology.

HEP experiments / **39**

The LHCb VELO detector: design, operation and first results

Auteurs: Kazu Akiba[1]; Pawel Kopciewicz[None]; Stefano De Capua[2]; Victor Coco[3]

[1] *Nikhef*

[2] *University of Manchester*

[3] *CERN*

Auteur correspondant pawel.kopciewicz@cern.ch

LHCb is a high precision experiment, operating at the LHC accelerator at CERN. The experiment is primarily devoted to the search for new physics beyond the Standard Model by studying CP violation and rare decays in the b and c-quark sectors. During the second long shutdown of the Large Hadron Collider at CERN, the LHCb experiment has been upgraded and the new detector is currently operating at the LHC. The Vertex Locator (VELO) is the detector surrounding the interaction region of the LHCb experiment, responsible of reconstructing the proton-proton collision (primary vertices) as well as the decay vertices of long-lived particles (secondary vertices).
The VELO consists of 52 modules with hybrid pixel detector technology. Compared to the previous VELO detector, the upgrade VELO encompass an enhanced track reconstruction speed and precision, even at the expected higher occupancy conditions of the upgrade, due to its pixel geometry as well as a closest distance of approach to the LHC beams, with the first sensitive pixel being at just 5.1 mm from the beam line. Cooling is provided by evaporative CO2 circulating in 500 µm thick silicon microchannel substrates. The sensors consist of 200 µm thick n-on-p planar silicon sensors, read out via 3 front-end ASICs. The detector contains 41 million 55 µm x 55µm pixels, read out by a custom developed front-end ASIC (VeloPix). The VELO operates in an extreme environment, which poses significant challenges to its operation. During the lifetime of the detector, the sensors are foreseen to accumulate an integrated fluence of up to $8x10^{15}$ 1MeV neq cm^{-2}, roughly equivalent to a dose of 400 MRad. Moreover, due to the geometry of the detector, the sensors will face a highly non-uniform

irradiation, with fluences in the hottest regions expected to vary by a factor 400 within the same sensor. The highest occupancy ASICs foresee a maximum pixel hit rate of 900 Mhit/s and an output data rate exceeding 15 Gbit/s. The detector has started operation together with the rest of the upgraded LHCb experiment after the LHC LS2 shutdown, in 2022. The new detectors have performed very well throughout the first two years of Run 3 of the LHC, but face new operational challenges with increased radiation damage foreseen till the end of this run. The cumulative radiation damage poses challenges in reaching full depletion in the most irradiated zones of the detectors, which have highly non-uniform exposure. The overall damage is monitored through regular measurements of the leakage current and charge collection efficiency (CCE) as function of the bias voltage.
The design, operation and early results evaluating the radiation damage and detector performance throughout the first years of operation in LHC run 3 will be presented.

Monolithic sensors / **40**

H2M: Porting a hybrid readout architecture into a monolithic 65 nm CIS

Auteurs: Adriana Simancas[None]; Ana Dorda[None]; Anastasiia Velyka[None]; Christian Reckleben[None]; Corentin Lemoine[None]; Dominik Dannheim[None]; Eric Buschmann[None]; Finn Feindt[None]; Gianpiero Vignola[None]; Håkan Wennlöf[None]; Ingrid-Maria Gregor[None]; Iraklis Kremastiotis[None]; Judith Schlaadt[None]; Karsten Hansen[None]; Larissa Mendes[None]; Lennart Huth[None]; Manuel Alejandro Del Rio Viera[None]; Michael Campbell[None]; Philipp Gadow[None]; Rafael Ballabriga[1]; Raimon Casanova Mohr[None]; Sara Ruiz Daza[2]; Sebastien Rettie[None]; Simon Spannagel[None]; Stefano Maffessanti[None]; Tomas Vanat[None]; Walter Snoeys[None]; Yajun He[None]; Younes Otarid[1]

[1] *CERN*

[2] *DESY*

Auteur correspondant sara.ruiz.daza@desy.de

The high energy physics community recently gained access to a 65 nm CMOS imaging process, which enables a higher density of in-pixel logic in monolithic active pixel sensors (MAPS). To explore this novel technology, the H2M (Hybrid-to-Monolithic) test chip has been designed and manufactured. The design followed a digital-on-top design workflow and ports a hybrid pixel-detector architecture, with digital pulse processing in each pixel, into a monolithic chip. The chip matrix consists of 64×16 square pixels with a size of 35x35 μm2, and a total active area of 1.25 μm2. The charge collection in the sensitive layer is improved by employing process modifications and layout optimizations.

This contribution introduces the H2M chip, its in-pixel analog and digital front-end, the four acquisition modes (time-of-arrival, time over-threshold, hit-counting, and triggered), and its integration into the Caribou readout system. It will also cover parameter optimization through laboratory measurements, threshold equalization, and noise characterization. Furthermore, laser measurements and test beam results from the SPS and DESY-II show a non-uniform charge collection pattern across the pixel cell. The origin and impact of this pattern on efficiency, timing, and spatial resolution will be discussed. This effect is less visible at lower thresholds, where a hit detection efficiency above 99% has been achieved in triggered mode.

Posters / **41**

Caribou: A versatile data acquisition system for silicon pixel detector prototyping

Auteurs: Dominik Dannheim[None]; Eric Buschmann[None]; Mathieu Benoit[1]; Simon Spannagel[None]; Tomas Vanat[None]; Younes Otarid[1]

[1] *CERN*

Auteur correspondant younes.otarid@cern.ch

Caribou is a versatile data acquisition system used in multiple collaborative frameworks (CERN EP R&D, DRD3, AIDAinnova) for both bench-top and test-beam qualification of novel silicon pixel detector prototypes. The system is built around a common hardware, firmware and software base shared accross different projects, thereby drastically reducing the development effort and cost. The current version consists of a custom Control and Readout (CaR) board and a commercial Xilinx Zynq 7000 series Sytem-on-Chip (SoC) platform. The CaR board provides a hardware environment featuring various services such as powering, slow-control and high-speed data links that can be used by the target detector prototype. The SoC platform is based on a ZC706 evaluation board running a fully featured Yocto-based Linux distribution (Poky) and a custom data acquisition software (Peary). Migration to a Zynq UltraScale+ architecture is ongoing with the additional objective of merging the SoC and the CaR board into a single hardware platform. This talk describes the current Caribou system architecture, its capabilities, examples of projects where it is used, and the foreseen system upgrade.

HEP experiments / **42**

The High-Granularity Timing Detector for ATLAS at HL-LHC

Auteurs: Hella Snoek[1]; Irena Nikolic[2]; Zhijun Liang[3]

Co-auteur: Christian Ohm [4]

[1] *Nikhef / UvAh*

[2] *LPNHE Université Paris Cité CNRS*

[3] *Institute of High Energy Physics, CAS*

[4] *KTH*

Auteur correspondant liangzj@ihep.ac.cn

The increased particle flux expected at the HL-LHC poses a serious challenge for the ATLAS detector performance, especially in the forward region which has reduced detector granularities. The High-Granularity Timing Detector (HGTD), featuring novel Low-Gain Avalanche Detector silicon technology, will provide pile-up mitigation and luminosity measurement capabilities, and augment the new all-silicon Inner Tracker in the pseudo-rapidity range from 2.4 to 4.0. Two double-sided layers will provide a timing resolution better than 50 ps/track for MIPs throughout the HL-LHC running period, and provide a new timing-based handle to assign particles to the correct vertex. The LGAD technology provides suitable gain to reach the required signal-to-noise ratio, and a granularity of 1.3 × 1.3 mm2 (3.7M channels in total). Requirements, specifications, technical designs, recent updates, and the project status will be presented, including the on-going R&D efforts on sensors, the readout ASIC, etc.

System integration / **43**

Thermomechanical design validation for quad pixel modules for the ITk

Auteur: Liam Cunningham[1]

[1] *University of Glasgow*

Auteur correspondant william.cunningham@glasgow.ac.uk

The current programme of upgrades to the ATLAS detector to take advantage of the opportunities presented by the HL-LHC will include a complete replacement of the tracking system. This upgrade will install an all-silicon tracker called the ITk, the innermost five layers will be made up of Si Pixel detectors.
The majority of the installed Si detectors are Quad Pixel detectors. These are ~4x4 cm2 assemblies consisting of a Si sensor tile which is attached using a flip chip bonding process to four Front End readout ASICs (ITkPix) to make a bare Quad module. Each of the Quad modules has over 600,000 50x50 ⊠m pixels, ~150,000 pixels per FE. A flexible PCB is mounted on the bare module and connected to the FE-ASICs and the sensor tile by means of wedge wire bonding and provides connectivity for power, DCS and data. After assembly the modules are coated in parylene for HV isolation. Once the module is completed it is attached to a support structure made from materials with a low coefficient of thermal expansion (CTE) and a high thermal conductivity, which hold the module in position and supply cooling and route power and data services to the module.
Quad modules will operate in extremely challenging radiation environments. The total radiation doses ranging from 1.7 MGy for the outer barrel, 3.5 MGy for the outer endcap and 7.3 MGy for the inner system with fluences of 2.3 × 1015cm21MeV neq to 9.2 × 1015cm21MeV neq. To ensure long term survival while operating in this very high radiation environment the modules are operated cold, the minimum coolant temperature will be -45oC and the upper operating temperature is controlled by an interlock system to +40oC. However, because the quad module is made from a range of materials with widely varying CTE's and is attached to the local supports using a high CTE adhesive they needed to be carefully designed to ensure bump disconnections are not caused by thermal stresses.
FEA was used to model the stresses within a module, particularly on the solder bumps, during temperature cycling of a quad module attached to the local supports material. The design space covers several parameters including the thickness of the copper traces in the PCB and the thickness and stiffness of the adhesives to ensure that the stresses induced by the CTE mismatch of the components do not cause catastrophic failure of the module. Design was validated with prototype modules. The design validation utilised 100 cycles over an extended temperature range of 55 to +60oC to ensure that the modules are robust enough to cope with the various temperature regimes it will be exposed to over 10yrs of operation and pre-installation transportation.
Here we present the FEA carried out to guide the design of the flex PCB and the module testing regimes, and compare the results from design validation of prototype modules.

Posters / **47**

DuTiP Vertex Detector for Belle II Upgrade and ILC

Auteur: Miho Yamada[1]

[1] *Tokyo Metropolitan College of Industrial Technology*

Auteur correspondant myamada@metro-cit.ac.jp

Belle II ugpgrade is expected around 2028 to mitigate the high background induced by electron and positron beams. We have invented a new pixel detector concept named Dual Timer Pixel (DuTiP) for the vertex detector upgrade. This pixel detector concept can be also used for the layer 7 and 8 of the ILD vertex detector. The first prototype was fabricated with lapis semiconductor 200 nm FD-SOI technology and characterization is ongoing. We will present the status and prospects of the development.

Posters / **48**

HEPS-BPIX4 : Process in 6M hybrid pixel detector design and engineering prototype for HEPS

Auteur: Zhenjie Li[1]

Co-auteurs: Hangxu Li [1]; Jie Zhang [2]; Mingyi Dong [1]; Peng Liu [1]; Si Ma [1]; Wei Wei [3]; Xiaolu Ji [1]; Xueke Ma [4]; Yan Zhang [1]; Yaoguang Liu [1]; Yuanbai Chen [1]; Zhe Li [1]; Ziyu Bao [1]

[1] 中国科学院高能物理研究所

[2] *IHEP*

[3] *IHEP, CAS*

[4] 陕西科技大学

Auteur correspondant lizj@ihep.ac.cn

HEPS-BPIX4 is a new engineering generation hybrid pixel detector prototype with 6M pixels with 140μm×140μm following the previous one with a pixel size of 150um×150um and frame rate up to 1.2kHz at 20-bit dynamic range. The 6M pixel detector is design for the Biological macromolecule experiment station of HEPS(BA beamline), which will be operational by 2025. The BPIX chip, fabricated in a radiation tolerant design with a standard 0.13μm CMOS process, was used to construct multichip modules with a active size of 82.2×36.8mm2 comprising 256×576pixels.
The BPIX4 readout chip was improved in terms of pixel size, electronic noise, number of threshold compared with the previous ones. The comparator threshold of each pixel is adjusted with a global threshold voltage (VCMP) and can be individually trimmed with a 5 bit digital-to-analog converter (5 bit DAC). There are two comparators and two counters in each pixel and a digital pulse from the comparator increments the each 16bit counter, leading to completely digital storage of the number of detected X-rays in each pixel.
The silicon sensors used for the modules were designed at IHEP and fabricated by inhouse fab. Each pixel consists of a pn-junction realized by a highly doped p-electrode implanted into a high-resistivity n-bulk. The sensors with a thickness of 450um are fully depleted at about 60 V and normally biased with 100 V.
A detector module consists of a single, fully depleted monolithic silicon sensor bump-bonded to an array of 2×6 ROCs. A model of the hybrid architecture is shown in Fig.1. Each sensor pixel is electrically connected to its corresponding ROC pixel with an Sn-Cu bump ball of 25μm to 35μm diameter. Wire-bonds are used to connect the pads on the side of the ROC to further readout electronics.
One module together with a detector control board (DCB), a data acquisition computer and a power supply forms a standalone detector system with 1.2KHz readout frame rate. A multi-module setup of 6M engineering prototype can be realized by mounting modules on a high-precision mechanical frame. The 6 M is an array of 5×8 modules comprising 5898240 pixels on an active area of 411 mm 294 mm achieving 100 Hz maximum frame rate. It is used at the macromolecular crystallography beamline BA at the HEPS.
All presented calibrations and characterizations were carried out at the BSRF using monochromatic X-rays since better results were achieved with X-rays than with the internal calibration signal of the readout chip. Either the direct synchrotron beam in combination with absorbing filters or an elastic scatter for homogeneous detector illumination were used.

Timing with pixels / 49

High precision 4D tracking with large pixel RSD coupled to the FAST3 ASIC

Auteur: Nicolo' Cartiglia[1]

Co-auteurs: Federico Siviero [1]; Leonardo Lanteri [2]; Luca Menzio [3]; Marco Ferrero [1]; Robert White [2]; Roberta Arcidiacono [3]; Valentina Sola [2]

[1] *INFN*

[2] *Univ. of Torino - INFN*

[3] *UPO - INFN*

Auteur correspondant nicolo.cartiglia@to.infn.it

This contribution will report the first beam test results obtained coupling 450-micron pixel RSD sensors with the FAST3 ASIC. The sensors are part of the RSD2 FBK production, and FAST3 is the

latest ASIC developed at INFN Torino for the read-out of thin sensors with internal gain. The results, obtained at the DESY testbeam site using 5 GeV electrons, demonstrate the possibility of concurrently reaching a spatial resolution smaller than 5% of the pitch and a temporal resolution below 50 ps using large pixels: a necessary condition to reduce the power consumption of large systems.

Photon science applications / **50**

Performances of the first full-scale HYLITE readout chip and the prototype module of SHINE XFEL

Auteurs: Mujin Li[1]; Wei Wei[2]

Co-auteur: Jie Zhang [3]

[1] *Institute of High Energy Physics, Chinese Academy of Sciences*

[2] *IHEP, CAS*

[3] *IHEP*

Auteur correspondant limujin@ihep.ac.cn

SHINE (Shanghai HIgh repetitioN rate XFEL and Extreme light facility) is the first XFEL facility working in the hard X-ray region in China. To fulfill the special requirements of SHINE, a new pixel array detector, STARLIGHT (SemiconducTor Array detectoR with Large dynamIc ranGe and cHarge integrating readout), is being developed. HYLITE (High dYnamic range free electron Laser Imaging deTEctor)) is the front-end readout chip of STARLIGHT, which works in the charge-integration mode with a dynamic range of 1~10000 photons @ 12 keV.

The initial phase of HYLITE development focuses on creating a 64×64-pixel chip with a 200-μm pixel pitch. HYLITE200F, the first full-scale chip in the HYLITE series, was manufactured using a 130 nm CMOS process. The maximum frame rate of HYLITE200F is 6.3 kHz in successive readout mode, with plans to enhance it to 12 kHz in the final version. To enable such high speed, a 10-bit Analog-to-Digital Converter (ADC) is integrated into each pixel, ensuring that the pixel outputs are in digital format. Performances of the HYLITE200F chip are fully tested. The signal-to-noise ratio is 8.7, which indicates the ability of single-photon resolution.

A prototype module was manufactured and preliminary tested. As the first step, four HYLITE200F chips are bump-bonded with a specially designed PIN sensor to make the 2×2-size module. The prototype module is mounted on a 2×8-size front-end PCB and read out via the back-end electronics which will be adopted in the final detector system. Imaging tests show that the function of the prototype and the architecture of the detector are correct. To verify the dynamic performance, a rotating chopper was placed before the module to block the X-ray. The frame rate of the detector was 1 kHz and the rotate frequency of the chopper was 100 Hz. Test results show that the images have the same pattern after every 10 frames, which indicates that the detector can work at the frame rate of 1 kHz.

Astrophysics applications / **51**

Characterization of large area LGADs for space applications

Auteurs: Ashish Bisht[1]; Francesco Ficorella[1]; Giovanni Paternoster[1]; Leo Cavazzini[1]; Marcos Fernandez Garcia[2]; Matteo Centis Vignali[1]; Maurizio Boscardin[3]; Michael Moll[4]; Moritz Wiehe[4]; Omar Hammad Ali[1]

[1] *Fondazione Bruno Kessler*

[2] *Postdoc*

[3] *FBK Trento*

[4] *CERN*

Auteur correspondant lcavazzini@fbk.eu

Abstract- Experiments that study charged cosmic rays in space combine a tracker and calorimeter to measure the charge magnitude, the energy, and the momentum of the incoming particles. However, secondary particles created in the calorimeter and entering the tracker will degrade the reconstruction capability of the instrument. Most of the tracker systems in these experiments use micro-strip sensors to provide spatial information of the charged particles passing through the tracker. In such sensors, the energy deposited by the primary particles cannot be separated from the energy deposited by the back-scattered secondaries. However, it has been shown that measuring the timing of charged particles crossing the tracker layers with a precision better than 100 ps can help separate the primary from the secondary particles. Low Gain Avalanche Diodes (LGADs) are silicon detectors that use the impact
ionization process to achieve gain values of about O(10) and timing resolution of 30 ps for Minimum Ionizing Particles. In High Energy Physics, the state of the art LGADs have an active thickness of 50 μm and a channel size in the order of O(1 mm2). Current experiments like AMS and DAMPE could therefore benefit from a Time of Flight system composed by these sensors. Scaling up the technology to match the typical channel area of the micro-strip sensors used in space-borne experiments deteriorates the timing capabilities of the LGADs due, in first approximation, to the increased capacitance. The devices used in this study consist of pad sensors with thickness 50 μm, 100 μm or 150 μm and presents different gain layer profiles to cope with the capacitance variation. Each thickness presents three active areas (6.25 mm2, 25 mm2 or 100 mm2) and three layout designs for each area to better understand
their consequences on the device performance. Different layout designs and gain layers are compared to determine the best time resolution. The timing performance of these devices is evaluated using Transient Current Technique and radioactive sources, to simulate the passage of a Minimum Ionizing Particle, along with Current and Capacitance against Bias Voltage characterisation. By evaluating gain, noise, and jitter, this work demonstrates it is possible to obtain 1 cm2 LGADs with a jitter as low as 40 ps. At the same time, the signal propagation and uniformity are studied since it was observed the channel size makes these features relevant for the timing capabilities.

Monolithic sensors / 53

Sagara1212: A wafer-scale, 5,000 frames per second, 4 megapixel CMOS Image Sensor for direct electrons and light detection

Auteurs: A Bofill[None]; A Font[None]; A Mollà[None]; Andrew Scott[None]; C Bauzà[None]; M Gargallo[None]; M Giulioni[None]; M Sannino[None]; R Gifreu[None]; R Turchetta[None]; Ò Lladós[None]

Auteur correspondant andrew.scott@imasenic.com

CMOS image sensors (CIS) are the leading imaging technology today. Sensors as large as a wafer can be manufactured thanks to the so-called stitching method. The architecture of existing wafer-scale CIS products is fairly simple, with the sensors representing only a relatively limited advantage in terms of speed, with respect to other technologies, e.g. a-Si panels or CCDs. This work presents the design and characterisation of a high-speed, 5,000 fps (frames per second), 4-megapixel CIS. The pixel rate of this sensor exceeds 20 Gpixel per second. This represents a step-change in frame rate for sensors of this type and the sensor architecture used to achieve this is patented.

The sensor was developed for cryo-TEM (Transmission Electron Microscopy). Cryo-TEM has utilized CIS since the early 2010s, a transformation that played a crucial role in its progress, culminating in the Nobel Prize in Chemistry in 2017 for advancements in cryo-electron microscopy (cryo-EM). For example, the COVID structure was determined using Cryo-TEM with CIS.

Cryo-TEM demands high frame rates to mitigate radiation damage to samples, which occurs rapidly when exposed to electron beams. Recent developments in TEM have focused on reducing the electron beam energy from 300keV to 100keV. This shift presents new challenges for detector technology. At 100 keV, electron interactions cause increased spreading within the detector's pixels, necessitating larger pixels and, consequently, a larger imaging array to maintain image resolution.

Our CIS Sagara1212 was developed for TEM at lower electron energies. It features a wafer-scale 4-megapixel array with frame rates up to 5,266 fps at 8-bit resolution. The sensor has a programmable bit depth, allowing the trade-off between frame rate and pixel bit depth to be explored. The chosen accuracy can vary between 4 and 10 bits, with the frame rate changing from 7,267 to 3,303 fps. The radiation-hardness as well as other performance of the pixel were tested in a prototype. The CIS works in rolling shutter and it features column-parallel programmable gain amplifiers and ADCs. The total number of ADCs is 24,384 for the whole sensor. The high frame rate requires 216 sub-LVDS lines running at 1GSa/s. To connect the sensor with the TEM computer, we also developed the readout electronics, which is capable of capturing data at a rate of 216Gbit/s.

These capabilities ensure that the sensor can capture high-quality images at high speeds, which is essential for applications like cryo-EM. Although the sensor was designed for this application, it is also sensitive to light, thus making it suitable for other applications requiring a large number of pixels and high frame rate.

The paper details the Sagara1212 sensor's architecture, the measures taken to achieve its high frame rate, its corresponding camera for data capture, and the test results which have been acquired. Figure 1 shows the sensor integrated into the Chip-On-Board (COB) assembly, highlighting the design and integration process. Figure 2 presents the sensor's floorplan. The system is currently undergoing tests within a Cryo-TEM microscope.

Photon science applications / **54**

Matterhorn, a high flux detector for 4th generation synchrotrons

Auteur: Roberto Dinapoli[1]

[1] *Paul Scherrer Institut*

Auteur correspondant roberto.dinapoli@psi.ch

The development of the new fourth-generation storage rings (or diffraction-limited storage rings, DLSR) poses new challenges to detectors in many aspects, the main one being the much-increased photon flux, exceeding the count rate capabilities of many of the actual single photon-counting detectors.
For this reason, the PSD detector group of the Paul Scherrer Institut (PSI, Switzerland) started the development of Matterhorn, a hybrid pixel detector capable of meeting the requirements of DLSRs and in particular of the SLS2. 0, the new storage ring being developed at PSI and which is supposed to be operational in 2025/2026.
The Matterhorn ASIC features a pixel pitch of 75 μm and is designed in UMC 110nm technology. Each pixel contains a charge-sensitive amplifier and a shaper, with selectable polarity, gain and shaping time, connected to four comparators. Each comparator has an independent threshold, gate signal and trim bit set to reduce threshold dispersion. Depending on the mode of operation, the pixel counting logic can trigger one of the four 16-bit counters. The counters state can be saved to a local memory to enable continuous operation.
In high-flux mode, the additional comparator thresholds can be set to values exceeding 100% of the incoming beam energy, thus detecting the pile-up of two or more photons, and effectively extending the count rate capabilities of the pixel to values exceeding 20MHz at 10% counting loss with an ENC<200e-rms.
This contribution will first explain the working principle and functionalities of Matterhorn, and then present the test results of our two prototypes.
Matterhorn 0.1 features a digitally synthesized control periphery, responsible for the chip control and readout, connected to two serial links working at the clock frequency of 1.6 GHz provided by an on-chip PLL.
Matterhorn 0.2 fixes some problems of the first version, and adds to that on-chip DACs for biasing, more debugging capabilities and an improved readout circuitry reaching a data rate of 3.125 Gb/s per data channel.
Finally, the plans for the design and production of the full-scale ASIC, Mattherhorn 1, planned for 2025, will be presented.

Posters / **56**

A small area 11-bit SAR ADC for integrating pixel detectors at high repetition rate XFELs

Auteurs: Tianyang Wang[1]; zizhao Ji[2]

Co-auteurs: Fuwan Gan [2]; ShiJie Lu [3]; Tao Sun [2]; Xudong Ju [4]; Zhen Sheng [2]; Zhi Liu [4]

[1] *Zhangjiang Laboratory*

[2] *Shanghai Institute of Microsystem and Information Technology*

[3] *Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS)*

[4] *ShanghaiTech University*

Auteur correspondant jizz@mail.sim.ac.cn

The charge-integrating pixel detector is one of the major enablers of new science at X-ray free electron laser (XFEL) facilities. Such detector must revolve high dynamic range diffraction images resulting from interaction between the sample and ultra intense X-ray pulses with duration in order of femtosecond. Ideally, the frame rate of the detector should match the repetition rate of the laser machine. Some state-of-the-art integrating pixel detectors read out analog signals directly, which usually have limited frame rates of a few kHz. The CSPAD detector designed for LCLS (Linac Coherent Light Source) implements a single-slope ADC (Analog-to-Digital Converter) in each pixel, establishing a digital readout architecture with a frame rate of 120 Hz [1]. One recent work utilizing a similar pixel architecture as CSPAD intends to develop a high frame rate detector system up to 10 kHz with dedicated pixel readout chip design combined with high throughput data acquisition system [2-3]. However, none of the existing pixel detectors can satisfy the needs of future high repletion rate XFELs beyond 100 kHz, necessitating new detector development with the frame rate matching the laser machine. The high data throughput arising from high frame rate requires new digital readout architectures for the pixel readout chip with high speed and high resolution analog-to-digital conversion followed by fast digital signal processing and transmission.

This work proposes a small area and low power 11-bit SAR ADC suitable for massive on-chip integration in a pixel readout chip for high dynamic and high frame rate X-ray imaging at XFELs. The ADC circuit has been designed and implemented in a prototype chip using a 130 nm CMOS process. The area of the SAR ADC is typically dominated by the CDAC (capacitor digital-to-analog converter) array. In order to reduce the total number of unit capacitors, the CDAC employs a bridge capacitor to split the CDAC into an LSB (least significant bit) array and an MSB (most significant bit) array, with the weights of LSB array attenuated by the bridge capacitor. The susceptibility of the bridging CDAC structure to capacitor mismatches and parasitics is mitigated by using a non-binary radix with redundancy, which allows for correction of the missing level errors caused by capacitor mismatches through simple foreground calibration. A small unit capacitor of ~10fF was used for the CDAC and the ADC core circuit occupies an area of only 0.026 mm^2. The ADC design is expected to be implemented within the pixel array and one ADC will be shared by a 4 × 4 pixel group. At an ADC sampling rate of 2 MS/s, the pixel array can be readout with a frame rate of 125 kHz.

First measurement of the prototype chip shows that the ADC can achieve an ENOB of ~10 at 2 MS/s after calibration. Further measurements are ongoing. The design and measurement results of the prototype chip will be presented in the conference.

System integration / **57**

The upgrade of the Belle II Vertex Detector: Thermomechanical characterization of prototype ladders and system integration.

Auteurs: Jerome Baudot[1]; STEFANO BETTARINI[2]

[1] *IPHC*

[2] *University of Pisa and INFN*

Auteur correspondant baudot@in2p3.fr

The Belle II experiment is planning an all-pixel upgrade of the vertex detector around 2029-2030, aiming to be more performant in terms of tracking efficiency and more robust against the machine background expected at higher luminosity.
The design of the new Vertex Detector (VTX) is based on five barrel-shaped layers spanning from 14 to 140 mm in radius, equipped with the depleted MAPS chip named OBELIX supported by a light support structure.

The two inner layers (iVTX) feature the "all-silicon ladder"concept, with a material budget less than 0.2% X/X0 per layer.
Four contiguous OBELIX chip blocks are diced out of the production wafers to build a mechanical standalone 12 cm long sensitive ladder. A post-processing step deposits metal strips on redistribution layers (RDL) to interconnect the sensors along this ladder.
The back side of the sensor regions can then be thinned down to 50 Xm.
The first demonstrator, based on a silicon wafer processed with dummy heater structures in place of the sensors, allows to characterize the electrical, mechanical and thermal performance of the inner ladder prototype.
The specific power dissipated on the periphery of the chip is almost one order of magnitude greater than on the area covered by the matrix. Thermal simulations and measurements on a dedicated thermal bench facility have been performed to evaluate an effective low mass cooling system to evacuate the average power of 200 mW/cm2, considering the maximum operational temperature of the chip, with a thermal gradient still acceptable in terms of threshold dispersion. Several options are now being explored with air cooling only or combination of air cooling with thin pipes for liquid cooling at the edge of the silicon ladder.

A more traditional approach has been adopted for the ladders of the three outer layers (oVTX), which extensions along the beam axis reach 70 cm. We are also exploring the engineering and performance aspects of the 4 layer option. Their design has been optimized in order to have ladders occupying a limited radial space. By accumulating four layers over 7 cm towards large radii, the efficiency in the Ks reconstruction can be preserved or improved. The high stiffness of the ladders is obtained by sandwiching rohacell with two carbon fiber sheets in an omega-shaped structure. An additional thin carbon fiber layer integrating a pipe for the circulation of a coolant liquid serves as a cold plate in direct thermal contact with a raw of sensors. These chips are electrically connected by aluminum flex circuits, for powering and data output. The material budget of each oVTX layer is expected to be less than 0.45% X/X0.
Results from the mechanical and thermal characterization of the prototype ladders will be reported.

Sensing materials & Radiaiton tolerance / **58**

First generation 4H-SiC LGAD production and its performance evaluation

Auteurs: Adam Klimsza[1]; Adam Kozelsky[1]; David Novák[1]; Jan Chochol[1]; Jiří Kroll[2]; Marcela Mikeštíková[2]; Michal Marčišovský[3]; Mária Marčišovská[3]; Peter Slovák[1]; Peter Švihra[3]; Radek Novotný[3]; Radim Špetík[1]; Roman Malousek[1]; Vladimír Kafka[3]

[1] *OnSemi*

[2] *FZU*

[3] *CVUT*

Auteur correspondant radek.novotny@cern.ch

This contribution will delve into the design and performance of the newly produced Silicon Carbide Low Gain Avalanche Detectors (4H-SiC LGADs) and provide a comprehensive summary of their

measured characterizations. This includes an analysis of the detector's performance, temperature stability, and the effectiveness of the internal gain layer in improving signal generation.

The 4H-SiC is re-emerging as a strong candidate for the next generation of semiconductor detectors. This material offers several advantages, including high radiation tolerance and the ability to operate over a wide range of temperatures without significant annealing effects. However, the signals generated by 4H-SiC detectors are lower than those produced by standard silicon detectors due to their higher bandgap energy. This is addressed by implementing a charge multiplication layer, which results in intrinsic gain of the device.

The presented 4H-SiC LGADs, produced by OnSemi, are specifically designed and optimized for fabrication on N type substrate/epi wafer with the gain layer implanted approximately 1 μm below the surface. The first iteration of these LGAD structures has already been manufactured early in 2023 and since then has been subjected to laboratory evaluation. The measured properties of these detectors align well with the predictions made by performed TCAD simulations.

Posters / **60**

Topmetal-M3: a position and time sensitive MAPS with delay line readout

Auteurs: Chaosong Gao[1]; Qianjun Chen[1]

[1] *Central China Normal University*

Auteur correspondant chaosonggao@ccnu.edu.cn

Monolithic active pixel sensors (MAPS) integrating sensitive element and readout circuits into one silicon chip have proven their good performance as high spatial resolution particle trackers in the past years. The MAPS provides high granularity with low material budget and has been applicated in high energy physical experiments, such as MIMOSA sensors for the STAR HFT at RICH, ALPIDE sensors for the ALICE ITS upgrade at LHC and so on. MIMOSA sensors use a rolling shutter technology to read out the data. While a priority readout technology is adopted in ALPIDE to read out the data. Compared to the rolling shutter readout scheme, the priority readout scheme can significantly reduce the integration time, power consumption and data volume. But both MIMOSA and ALPIDE are position-sensitive MAPS but the time of arrival cannot be measured.

Topmetal-M3 is a position- and time-sensitive MAPS which is developing at Central China Normal University in China. A delay-line readout scheme with column-level Time-to-Digital Converter (TDC) is adopted in Topmetal-M3. The Topmetal-M3 is composed of a pixel array arranged in 256 (row) x 96 (column), column-level TDCs, a digital readout module and a configuration module. A bidirectional inverted "U"-shaped delay line which is composed of inverters is inserted in each double column and shared by all pixels in the double column. When a pixel is hit, the signal is amplified and converted into a digital signal. And then the leading edge is converted into a narrow digital pulse with a pulse width of less than 1 ns. The narrow digital pulse is fed into the bidirectional inverted "U"-shaped delay line and transmits in opposite directions. The arrival time of the leading edge in the end of each column is measured by the column-level TDC. By calculating the time difference of the arrival time on each double column, the hit position can be located. The TDC architecture mainly consists of a coarse counter and a delay-line-based analog-digital hybrid interpolator. The outputs of the TDCs are fed into the digital readout module. The data are framed in the digital readout module and transmitted off-chip in parallel.

The Topmetal-M3 sensor has been designed and taped out in a 180 nm standard process. The pixel size is 32 μm x 26 μm. The detailed simulations have been done. The delay time of the delay unit of the inverted "U"-shaped delay line is about 90 ps. The time resolution of the TDC is better than 10 ps. Each hit pixel can be located by the time information. The chip has come back to the lab and the test work is ongoing. We will present the test results in the conference.

Monolithic sensors / **62**

Development of monolithic pixel sensor prototypes for the first CEPC vertex detector prototype

Auteur: Ying Zhang[1]

Co-auteurs: Wei Wei [2]; Zhijun Liang [1]; Jun Hu [1]; Ziyue Yan [3]; Shuqi Li [2]; Tianya Wu [4]; Xiaoxu Zhang [5]; Xiaomin Wei [6]; Xiaoting Li [7]; Liang Zhang [8]; Xinghui Huang [1]; Jia Wang [6]; Ming Qi [5]; Sebastian Grinstein [9]; Joao Guimaraes da Costa [2]

[1] *Institute of High Energy Physics, CAS*

[2] *IHEP*

[3] *Institute of High Energy Physics*

[4] *Nanchang University*

[5] *Nanjing University*

[6] *NWPU*

[7] *Institue of High Energy Physics, CAS*

[8] *Shandong University*

[9] *IFAE*

Auteur correspondant zhangying83@ihep.ac.cn

The TaichuPix chip is a dedicated monolithic CMOS pixel sensor developed for the first 6-layer silicon vertex detector prototype for the Circular Electron Positron Collider (CEPC) vertex detector R&D. Two small-scale demonstrator chips (25 mm^2) had been designed to optimize the in-pixel circuit and readout architecture, and to verify the radiation hardness. The promising test results of the small-scale prototypes led to a submission of the first full-scale (~ 4 cm^2) TaichuPix prototype in 2022. Figure 1 shows the architecture of a full-scale TaichuPix chip, including a matrix of 512 × 1024 pixels with a size of 25 × 25 μm^2. The full-scale sensor chip was characterized at the DESY test beam facility. The preliminary results indicate that the best spatial resolution of the individual TaichuPix-3 sensor is better than 5 μm combined with a detection efficiency better than 99% (see Fig. 2). The TaichuPix-3 chip also fulfills the TID tolerance requirement. This talk will report the design and test of TaichuPix prototypes and the readout electronics of the ladder for vertex detector. The design of the first vertex detector prototype and its beam test results will also be presented.

Posters / **64**

Synchronous and Asynchronous Data Quality Control of the ALICE Inner Tracking System in the LHC Run 3

Auteur: Svetlana Kushpil[1]

[1] *Nuclear Physics Institute of the CAS*

Auteur correspondant skushpil@ujf.cas.cz

The Inner Tracking System (ITS) of the ALICE experiment at the CERN Large Hadron Collider (LHC) is the largest Monolithic Active Pixel Sensor technology application in high-energy physics.
The updated version of the tracking system, called ITS2, consists of seven concentric layers of ALPIDE monolithic active pixel sensors produced in the 180 nm CMOS process, covering a total sensitive area of about 10 m^2.
The sensor features a pixel pitch of 27 μm × 29 μm and a position resolution of about
5 μm. The very low material budget, 0.36\% X_0/layer for the three innermost layers and 1.10\% X_0/layer for the outer layers, in combination with the small radial distance of only 23 mm from the beam,
leads to an excellent impact parameter resolution at low transverse momentum. This

makes the detector well suited for experimentally challeging physics measurements such as the reconstruction of low transverse momentum heavy-flavor particles in the heavy-ion collision environment.

The contribution provides an overview of the ITS2 data Quality Control system (QC),
a framework designed to synchronously monitor the detector operating parameters and provide asynchronous reconstruction of the collected data, with the goal of guaranteeing a stable and efficient data taking.
The monitoring for fake-hit rate, front-end electronics status, data integrity, cluster and track distributions,
will be presented, together with a preview of the ITS2 performance during the recent Run 3 pp and Pb-Pb data taking campaigns, as extracted from the QC asynchronous reconstruction.

Monolithic sensors / **66**

Impact of the circuit layout on the charge collection in a monolithic pixel sensor

Auteurs: Adriana Simancas[None]; Ana Dorda[None]; Anastasiia Velyka[None]; Christian Reckleben[None]; Corentin Lemoine[1]; Dominik Dannheim[None]; Eric Buschmann[None]; Finn Feindt[None]; Gianpiero Vignola[None]; Håkan Wennlöf[2]; Ingrid-Maria Gregor[None]; Iraklis Kremastiotis[None]; Judith Schlaadt[None]; Karsten Hansen[None]; Larissa Mendes[None]; Lennart Huth[None]; Manuel Alejandro Del Rio Viera[None]; Michael Campbell[None]; Philipp Gadow[None]; Rafael Ballabriga[3]; Raimon Casanova Mohr[None]; Sara Ruiz Daza[4]; Sebastien Rettie[None]; Simon Spannagel[None]; Stefano Maffessanti[None]; Tomas Vanat[None]; Walter Snoeys[None]; Yajun He[None]; Younes Otarid[3]

[1] *IPHC/CERN*

[2] *University of Birmingham (GB)*

[3] *CERN*

[4] *DESY*

Auteur correspondant corentin.lemoine@cern.ch

Monolithic CMOS sensors combine the sensing volume and the processing electronics in the same die, leading to complex shapes of doped regions with various concentrations. As a consequence, the electric field in such sensors cannot be accurately expressed analytically. Considering the importance of the charge propagation process on the signal formation in the pixels, the electric field is usually simulated with Technology Computer Aided Design (TCAD) prior to any further study.
While in most circumstances the sensor can be considered independent of the CMOS electronics thanks to an implant separating the two parts, measurement results of the Hybrid to Monolithic (H2M) chip feature a clearly asymmetric efficiency pattern at high threshold. This pattern was not expected since the sensitive volume is designed symmetric, it is however correlated with the asymmetric layout of the circuitry.
This contribution details the simulation method including TCAD and Monte Carlo deployed to better understand this effect. The simulation procedure highlighting the differences compared to the case where the circuit is not considered will be presented first, before focusing on the results obtained with the TPSCo 65nm technology used by the CERN Experimental Physics R&D and for the H2M.
Simulations qualitatively reproduce the efficiency pattern observed in the H2M only when taking into account the layout of the CMOS part, and allowed to clarify its origin: an interplay between the relatively large pixel pitch of 35um, the fast front end and the specific layout of the circuit. The same simulation flow was used on other prototypes in the same technology, confirming that this effect is marginal for smaller pitch, in agreement with previous measurements.

HEP experiments / **67**

Design and performance of the prototype gaseous beam monitor with GEM and pixel sensors for the CSR external-target experiment

Auteurs: Hulin Wang[1]; Chaosong Gao[1]; Jun Liu[1]; Xiangming Sun[1]; Kai Chen[1]; Xianglun Wei[2]; Chengxin Zhao[2]; Zhen Wang[3]

[1] *Central China Normal University*

[2] *Institute of Modern Physics, Chinese Academy of Sciences*

[3] *Guizhou Normal University*

Auteur correspondant hulin.wang@ccnu.edu.cn

A gaseous beam monitor utilizing gas electron multiplier (GEM) and pixel sensors is being developed for the Cooling Storage Ring (CSR) external-target experiment (CEE) at Heavy Ion Research Facility in Lanzhou (HIRFL). The beam monitor is mainly used to track each beam particle, providing an accurate reconstruction of the primary vertex of the collision. Two generations of the pixel sensors (named Topmetal-CEE) were produced, with the second generation having much-improved noise performance over the first one. The readout electronics includes two chip carrier cards, two front-end cards, and a readout and control unit. This talk presents the design and performance of two prototype detectors, featuring two generations of the pixel sensors, respectively.
In particular, the results of the tests with heavy-ion beams and laser beams are presented, showing a spatial resolution of better than 50 μm and a time resolution of better than 15 ns.

Sensing materials & Radiaiton tolerance / **68**

A lightweight algorithm to model radiation damage effects in Monte Carlo events for High-Luminosity LHC experiments

Auteurs: Keerthi Nakkalil[1]; Marco Bomben[2]

[1] *APC Paris*

[2] *APC*

Auteur correspondant marco.bomben@apc.in2p3.fr

Radiation damage significantly impacts the performance of silicon tracking detectors in Large Hadron Collider (LHC) experiments such as ATLAS and CMS, with signal reduction being the most critical effect. While adjusting sensor bias voltage and detection thresholds can help mitigating these effects, generating simulated data that accurately mirrors the performance evolution with the accumulation of luminosity, hence fluence, is crucial.
The ATLAS and CMS collaborations have developed and implemented algorithms to correct simulated Monte Carlo (MC) events for radiation damage effects, achieving impressive agreement between collision data and simulated events.
In preparation for the high-luminosity phase (HL-LHC), the demand for a faster ATLAS MC production algorithm becomes imperative due to escalating collision, events, tracks, and particle hit rates, imposing stringent constraints on available computing resources. This article outlines the philosophy behind the new algorithm, its implementation strategy, and the essential components involved. The results from closure tests will be presented for different sensor's geometry; some preliminary results on computing performance will be commented too.

Posters / **69**

Integration Concept of the CBM Micro Vertex Detector

Auteur: Franz Matejcek[1]

Co-auteur: Christian Muentz [2]

[1] *Goethe-University Frankfurt*

[2] *Goethe-University Frankfurt, Germany*

Auteurs correspondants: c.muentz@physik.uni-frankfurt.de, matejcek@physik.uni-frankfurt.de

The Micro Vertex Detector (MVD) is the first downstream detector of the fixed-target CBM experiment at the future Facility for Antiproton and Ion Research (FAIR). It enables high-precision tracking of low-momentum particles in direct proximity of the target, e.g., the first out of four planar stations is placed only 8 cm downstream the interaction point. Thus, minimizing the material budget while operating the dedicated CMOS (MAPS) pixel sensors called MIMOSIS in the moderate target chamber vacuum is challenging. Each detector plane will feature a material budget x/X0 ranging between 0.3 and 0.5%. The harsh radiation environment of up to 7 • 1013 neq/cm2 and 5 Mrad per CBM running year poses challenging constraints on the choice of technology and materials, and in particular on the sensors. Stable sub-0° C operation to maintain high detection efficiency and low fake rate is mandatory.

The baseline integration technique relies on integrating the large-area (31.15×17.25 mm2) thinned (50 µm) pixel sensors onto planar carriers of Thermal Pyrolytic Graphite (TPG, 380 µm, ~ 1500 W/m • K). The carriers provide both mechanical support and superior thermal conductivity inside the geometrical acceptance. They are mounted to actively cooled aluminum heat sinks outside the acceptance. The sensors are wire-bonded to dedicated thin flex cables which are fed into front-end boards mounted on the heat sinks inside the vacuum. Providing seamless active pixel coverage inside the geometrical acceptance per MVD plane calls for the - vacuum-compatible - integration of sensors on both sides of each TPG carrier. With up to 28 individual sensors per carrier the mechanical integration yield of the sensors is, accordingly, of concern and challenging.

This contribution will present the detector and sensor integration concept, elaborating on the selection and preparation of materials, dedicated assembly procedures and quality assessment steps. Carriers made of TPG feature pros (outstanding heat conductivity and price) as well as cons (surface quality and softness) and we will present solutions developed during prototyping recommending employing this material in high-precision vertex trackers operated in vacuum.

HEP experiments / **70**

The new two-layer Belle II PiXel Detector (PXD)

Auteur: Fabian Becherer[1]

Co-auteur: Botho Paschen [2]

[1] *DESY*

[2] *University of Bonn*

Auteur correspondant fabian.becherer@desy.de

The Belle~II experiment at the SuperKEKB super B-factory collects data from asymmetric-energy e^+e^- collisions at the $\Upsilon(4S)$ resonance since 2019.
Its goal is to collect a $B\bar{B}$ data set 50 times larger than that of the predecessor experiments Belle and Babar enabling new levels of accuracy in measurement of standard model processes and search for new physics at the luminosity/precision frontier.

A vertex resolution of O(10) μm is required for the precise discrimination of decay vertices and lifetime measurements of short-lived particles.
This is made possible by the Belle~II VerteX Detector (VXD). It consists of the ultra low-mass PiXel Detector (PXD) based on the DEpleted P-channel Field Effect Transistor (DEPFET) sensor technology surrounded by a double sided silicon strip detector (SVD).

The PXD features self supported all-silicon modules with 75 μm thin sensor areas bringing down the material budget to an average of $\sim 0.21\%\ X_0$ per layer inside the physics acceptance.
This constitutes the lowest mass tracking detector in a running high energy physics experiment to date.

It features ladders of up to 17 cm length with pixel sizes of 50×55 to 50×85~$\mu\mathrm{m}^2$.
Cooling of the low power matrix is provided by N_2 gas flow while the readout Application Specific Integrated Circuits (ASICs) are cooled by closed two-phase CO_2 loops.

During Run 1 (2019-2022), a single-layer of PXD was installed and delivered the expected performance. In 2023, during the first long shutdown (LS1) a new, fully populated two-layer PXD (PXD2) has been installed.
The production and pre-commissioning of PXD2 took several years and culminated in its installation into the Belle~II detector in summer 2023.
Since February 2024, Belle II has restarted data-taking of Run 2 and PXD2 performs within its specifications.

Due to its large thin ladder design, PXD is subject to small scale mechanical deformation caused by varying temperatures depending on its operation and beam conditions.
Ensuring mechanical stability of the system has been a significant effort during the commissioning of the detector and the monitoring of its condition is an ongoing task.
In order to avoid damage from severe sudden beam losses, as experienced when tuning SuperKEKB for higher luminosities, the PXD was switched off for part of the current run.

This presentation will highlight challenges from the construction and commissioning of PXD2 as well as its performance during the first months of Run 2.

Photon science applications / **72**

Development of 20.2 Mpixel CITIUS detector for the XFEL facility SACLA

Auteur: Takaki Hatsui[1]

Co-auteurs: Haruki Nishino [2]; Kyosuke Ozaki ; Yoshiaki Honjo ; Toshiyuki Nishiyama Hiraki ; Kazuo Kobayashi ; Koji Motomura ; Takashi Sugimoto ; Mitsuhiro Yamaga ; Yasumasa Joti

[1] *RIKEN*

[2] *JASRI/RIKEN*

Auteur correspondant hatsui@spring8.or.jp

CITIUS is an integrating-type detector developed for synchrotron and XFEL applications. CITIUS operates at the maximum frame rate of 26.1 kframes/s for full image recording in a spectro-imaging mode, and the associated data rate is 140 Gbps at the physical layer from a single chip. In this talk, we report recent progress in the development of 20.2M CITIUS detector for Serial Femtosecond Crystallography (SFX) at the X-ray free electron laser (XFEL) facility, SACLA. The detector operates in an XFEL mode of CITIUS and runs at a maximum frame rate of 5 kHz. At SACLA operating at 60 pulses/s, the detector is configured to run at 960 frames per second, where 16 frames are recorded for each pulse at 60 Hz (multi-sampling). This mode reduces the noise floor down to 25 e-rms, which is equivalent to 0.015 photons (rms) at 6 keV, while the detector's peak signal is 17,000 photons. The detector generates 107 GB/s of data. We have developed a dedicated set of servers to record, calibrate, transfer, and compress the data. Data-framing boards (DFBs) with three Arria10 FPGAs for each were installed in the servers. DFBs reduce the data rate to 15 GB/s by accumulating the 16 frames. The detector was placed in an experimental hutch of SACLA in April 2024. In July 2024, we will conduct the first experiment using XFEL beams. This talk outlines the results obtained in the first experiment and future plans of CITIUS for the other applications, where some have a maximum data rate of 10 Tbps.

Timing with pixels / **73**

Timing performance of a digital SiPM prototype

Auteurs: Daniil Rastorguev[1]; Finn Feindt[1]; Gianpiero Vignola[1]; Inge Diehl[1]; Karsten Hansen[1]; Simon Spannagel[1]; Stephan Lachnit[1]; Tomas Vanat[1]

[1] *DESY*

Auteur correspondant daniil.rastorguev@desy.de

Single Photon Avalanche Diodes (SPADs) have been recently introduced in process design kits of several CMOS foundries. This opens up possibilities to embed SPADs into custom CMOS ASICs, thus allowing for novel designs of monolithic silicon avalanche photo-detectors. A digital silicon photomultiplier (dSiPM) prototype with integrated readout was designed at DESY in the LFoundry 150 nm process node, featuring a matrix of 32x32 SPAD pixels, each including four 25 µm SPADs and signal processing circuits. This device combines the intrinsically fast rise time and single-photon detection capability of SPADs with features typical for pixel detectors, such as full hitmap readout and individual pixel masking. To match the fast rise time, the dSiPM provides fine hit timestamping (bin size of 95 ps) with on-chip time-to-digital converters.
The dSiPM, simultaneously offering excellent timing resolution due to the use of SPADs as sensitive elements, and also good spatial resolution thanks to the high-granularity readout, is an interesting candidate for a 4D-tracking detector in future collider experiments. As a 4D-tracking device needs to provide time and position information for each individual particle interaction, uniformity of timing characteristics across the sensitive matrix is of particular interest.
This contribution focuses on the characterization of the temporal resolution of the dSiPM prototype, performed by the means of charge injection with a pulsed laser and by the direct detection of charged particles at the DESY-II test beam facility. Measured timing characteristics match the design expectations, and their variations as a function of the interaction position can be correlated to intrinsic SPAD properties, and to the layout of the digitization circuits.

Sensing materials & Radiaiton tolerance / **74**

Development of high radiation tolerance detector with CIGS

Auteur: Kosuke Itabashi[1]

Co-auteurs: Jiro Nishinaga [2]; Manabu Togawa [1]; Miyahara Masaya [1]; Okumura Hironori [3]; Tadaaki Isobe [4]

[1] *High Energy Accelerator Research Organization*

[2] *National Institute of Advanced Industrial Science and Technology*

[3] *University of Tsukuba Faculty of Pure and Applied Sceinces*

[4] *Physical and Chemical Research*

Auteur correspondant itaba@post.kek.jp

In the hadron collider experiments, many silicon detectors have been used for the tracking detection. When these semiconductor detectors are exposed to high radiation level, their detector performances are degraded by the radiation damage. It becomes a serious problem for the future collier experiment expected higher radiation levels. Therefore, new semiconductors in place of silicon with high radiation tolerance have been widely developing in the world.
A $\mathrm{Cu(In_{1-x}, Ga_x)Se_2}$ (CIGS), which is an alloy semiconductor of $\mathrm{CuInSe_2}$ and $\mathrm{CuGaSe_2}$, is one of the candidates for radiation hard detector. It has been confirmed that CIGS solar cells can recover from radiation damage through thermal annealing, and CIGS is expected to become a new detector with high radiation tolerance for using in future hadron colliders ($O(10^{17})\ \mathrm{n_eq/cm^2}$). We developed the prototype of CIGS detectors with 2 $\mu\mathrm{m}$ thickness which composed of a pn (CIGS-CdS) junction, investigating radiation tolerance of them with two irradiation experiments.
In the first experiment at Heavy Ion Medical Accelerator in Chiba (HIMAC), the heavy ion ($^{132}\mathrm{Xe}^{54+}$) beam with the energy of 400 $\mathrm{MeV/u}$ was irradiated to the CIGS detectors, and amount of collected charge from $^{132}\mathrm{Xe}^{54+}$ signals and the leakage current were measured during the $^{132}\mathrm{Xe}^{54+}$ irradiation.
The collected charge after exposure to a radiation dose of 0.6 MGy was degraded to a half of before irradiation, but recovered to 97% of the pre-irradiation level after 2-hours thermal annealing at 130 °C. We also confirmed second recovery of collected charge to 94% by 50-minutes thermal annealing at 130 °C after more irradiation with radiation dose of 0.2 MGy. We observed the continuously

recovery from radiation damage and found the possibility of long-term operation in high radiation environments with periodic thermal treatments.
In the second experiment at Cyclotron and Radioisotope Center (CYRIC), the fluence with 7.5×10^{15} $\mathrm{n_{eq}/cm^2}$ by 70 MeV/c proton beam irradiated to CIGS solar cells. We investigated recovery mechanism in the CIGS. In this study, we treated the samples by thermal annealing after proton irradiation samples under various temperature conditions, investigating temperature dependence of recovery rates and a behavior of defect levels using Deep Level Transient Spectroscopy (DLTS) measurement.
I will introduce the progress of CIGS detector development and the recovery mechanism from radiation damage with two irradiation experimental results.

Posters / **75**

Qualification and Characterization of Mupix11 sensor modules for the Mu3e Vertex Detector

Auteur: Thomas Senger[1]

[1] *University of Zurich*

Auteur correspondant thomas.senger@physik.uzh.ch

The Mu3e experiment aims to detect charged lepton flavor violation through the decay channel μ ⟶ e e e. With sensitivities of 10^−15 in its initial phase and 10^−16 in the final phase, it improves upon prior experiments by four orders of magnitude. The innovative experimental concept is based on a tracking detector built from novel ultra-thin silicon pixel sensors and scintillating fibres and tiles. In this talk, I will present the qualification procedure and test results of Mupix11 pixel sensor modules. Additionally, I will delve into the challenges associated with data transmission, particularly concerning connections via micro-twisted pair cables

Monolithic sensors / **76**

Recent results from the R&D on the MIMOSIS CMOS MAPS

Auteur: Michael Deveaux[1]

[1] *GSI/FAIR Darmstadt*

Auteur correspondant m.deveaux@gsi.de

The CMOS Sensor MIMOSIS is being developed to equip the Micro Vertex Detector (MVD) of the CBM experiment at FAIR in Darmstadt, Germany. It will feature 1024 × 504 pixels and combine a time resolution of 5 µs with a spatial resolution of ~ 5 µm. Moreover, it will have to handle a peak rate of 80 MHz/cm² and radiation doses of 5 MRad and up to 1e14 neq/cm² per year. It is being developed within a joined R&D program of IPHC Strasbourg, Goethe University Frankfurt and GSI. Prototypes of MIMOSIS have been tested in an intense test program among others on their response to minimum ionizing particles, their radiation tolerance and their tolerance to direct heavy ion impacts. We discuss about the sensor requirements and report about the status of the R&D program. Moreover, we report the results of multiple beam tests obtained with close to final full-feature full-size prototypes.

HEP experiments / **77**

ALICE ITS2: overview and performance

Auteur: Artem Isakov[1]

[1] *Nikhef*

Auteur correspondant aisakov@nikhef.nl

The upgraded Inner Tracking System (ITS2) is instrumental for tracking and vertex reconstruction in the ALICE experiment. The new tracker consists of seven cylindrical layers equipped with silicon Monolithic Active Pixel Sensors (MAPS) with a pixel size of 27 by 29 μm. The sensors are thinned down to a thickness of 50 μm and 100 μm for the three innermost layers and for the four outer layers, respectively. The material budget of the innermost layers is as low as 0.36% X_0/layer compared to 1.14% X_0/layer of the previous ITS1. In combination with a radius of 23 mm for the innermost layer and a position resolution of about 5 μm, the low material budget greatly enhances the reconstruction capabilities of heavy-flavour and low-pT particles compared to Run 2.

ITS2 has been in operation since the beginning of Run 3 and has already recorded more than 42 pb^-1 proton-proton events at √s = 13.6 TeV and more than 2 nb^-1 PbPb events at √s_NN = 5.36 TeV, operating stably during these operations at interaction rate up to 4 MHz in pp and about 50 kHz in Pb-Pb collisions. This contribution will review the detector performance during LHC Run 3 and give an overview on the calibration methods and running experience.

System integration / **78**

First experience with the Mu3e Vertex detector construction

Auteur: Luigi Vigani[1]

[1] *University of Heidelberg*

Auteur correspondant vigani@physi.uni-heidelberg.de

The Mu3e experiment searches for the lepton flavour violating decay μ⟶ eee with an ultimate aimed sensitivity of 1 event in 10^16 decays in phase 2. This goal can only be achieved by reducing the material budget per tracking layer to X/X0 ≈ 0.1 %. For this purpose, gaseous helium is chosen as coolant, while High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) thinned to 50 μm constitute the baseline for the Vertex detector.
As the Phase 1 detector is in production, this talk will focus on the first achievements and solutions adopted for the construction of the Vertex detector. Located around the muon stopping target, the Vertex detector is designed to reconstruct the tracks of low energetic electrons coming from the muon decays. The light and compact experimental design poses unique challenges to its construction, from the characterization of the sensors to the implementation of the services. Several of these aspects will be discussed in this talk, along with the integration of the final system.

Posters / **80**

Charge Collection Properties of a CMOS Sensor Produced in a 55 nm Process

Auteur: le xiao[1]

[1] *Central China Normal University*

Auteur correspondant lexiao@mails.ccnu.edu.cn

The vertex detector in high-energy physics experiments demands high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) stands out as the most promising technology to fulfill all these requirements. A 55nm CMOS imaging sensor process has been selected because it allows for full CMOS utilization within the pixel, facilitated by the availability of a deep p-well. In this context, we developed the MAPS sensor MIC6_Explorer0 in the 55nm process to investigate the charge collection properties with various MAPS design parameters.
The MIC6_Explorer0 chip measures 3980μm×2145μm and comprises three matrices designed for various purposes. Matrix-1 features 18 sub-matrices of 16*16 pixels with serial analog output for studying pixel pitch, diode geometry, reset method and readout circuit structure. The pixel pitch of sub-matrices A1~A6, A7~A12, A13~A18 is 8 μm, 16 μm and 24 μm, respectively. A1~A6 are readout using a typical two-stage source follower method, while A7~A18 utilize the dual correlated double sampling readout method implemented by two capacitors within each pixel. The A1/A3/A5 sub-matrices are reset using diodes, while other sub-matrices are reset using MOS transistors. Matrix-2 consists of 21 mini-matrices of 4×4 pixels with parallel analog output for the studying pixel pitch, diode geometry, reset method, readout circuit structure and charge collection time within a cluster. The pixel pitch of mini-matrices B1~B9, B10~B15, B16~B21 are 24 μm, 16 μm and 8 μm, respectively. B1~B3 are readout using ALPIDE front-end circuit, while B4~B21 are readout using a two-stage source follower circuit. The B1~B6, B10~B12, B16~B18 mini-matrices are reset using diodes, while other mini-matrices are reset using MOS transistors. Matrix-3 includes 3 diode matrices without readout electronics for direct measurement of leakage current and sensing diode capacitance. These diode matrices are actually a certain number of diodes connected in parallel. The pixel size, N-well size, and spacing of the three types of diode test structures correspond to sub-matrices A4, A8, and A14, respectively.
The testing system comprises multi-channel, high-speed ADCs, DACs, an FPGA, and DAQ firmware to assess the performance of each matrix. The digital I/O of the chip is controlled by the FPGA. The chip's analog signals are sampled by the ADC, then processed by the FPGA and buffered in DDR3 memory before being transmitted to a PC via a 1 Gbps Ethernet interface. Test commands from the control software on the PC are received by the TCP/IP module. Subsequently, the ADCs, DACs and MIC6_Explorer0 controller module are configured by the FPGA according to the commands. Preliminary test results indicate that the pixel with a 24 μm×24 μm pixel pitch in mini-matrix B4 achieved a 95% charge collection efficiency when exposed to a 55Fe source.

Posters / **81**

A Monolithic Active Pixel Sensor with a Novel Readout Architecture for Vertex Detector in particle physics Experiments

Auteurs: Kai Chen[None]; Le Xiao[1]; Qiming Liang[1]; Weigang Yin[2]; le xiao[3]

[1] *CCNU*

[2] *IHEP*

[3] *Central China Normal University*

Auteurs correspondants: chenkai@ccnu.edu.cn, lexiao@mails.ccnu.edu.cn

The vertex detector in high energy physics experiment requires high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) is the most promising candidate technology to satisfy all those requirements. We have developed the MAPS sensor MIC6_V1 in a 55 nm quad-well CMOS image sensor process with a node-based data-driven readout scheme.
MIC6_V1 contains a pixel matrix of 64 rows by 64 columns with a pixel size of 23.6 μm 20 μm. Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a node-based sparse readout circuitry. Every double-column of pixels share a readout circuit, and 4x2 pixels form a super pixel group. The 8 pixels in each super pixel share a VCO for hit arrival time measurement. The VCO oscillates only when the super pixel group is hit to reduce power consumption. The oscillation frequency of VCO can be configured between 100 ~ 200 MHz. Each super pixel also includes a node of sparse readout logic circuit, and the hit information will be asynchronously transmitted to the bottom of the double-column through the readout nodes. Readout nodes transmit data based on request-acknowledge handshake protocol. When a super pixel group is hit, 20 bit data will be generated, including 4-bit super pixel group address, 8-bit time counter and 8-bit hit shape.
In the bottom of MIC6_V1, a periphery readout module also based on asynchronous readout node has been implemented to readout 20-bit data and 5-bit column address from each double-column.

Then, a synchronizer module is connected to the peripheral readout module, which is responsible for processing handshake, data synchronization, data bit-width conversion, and finally outputting the data. In addition, an asynchronous handshake multiplexer module is implemented, through which any double-column can be tested independently.
We first individually tested each double-column readout link. The data port at the top of each double-column readout link was configured with a test pattern. By sending a request signal to the top of the double-column, the chip would output the correct response signal at the top, completing the handshake and writing the test pattern data into the double-column. After transmission through 16 nodes within the double-column, a request signal was output at the bottom, and the test pattern was observed at the data port at the bottom. The entire process took approximately 25ns, indicating that the hit information of a super pixel group could be output every 1.56 ns. In addition to testing the double-column readout link through the top, we further evaluated the functionality of the double-column readout link by using test signals within the pixels. By activating test pulse enable switches inside certain pixels and combining them with the test Pulse signal and Strobe signal, we simulated situations where pixels are hit. As a result, we observed the expected 20-bit data and request signal at the bottom of the double-column. Based on this, we tested the readout of the entire chip array through the peripheral asynchronous readout module and synchronizer module.

Timing with pixels / **82**

Design and optimisation of radiation resistant AC- and DC-coupled resistive LGADs

Auteurs: Alessandro Fondacci[1]; Tommaso Croci[2]; Daniele Passeri[3]; Roberta Arcidiacono[4]; Nicolo' Cartiglia[5]; Maurizio Boscardin[6]; Matteo Centis Vignali[7]; Giovanni Paternoster[7]; Omar Hammad Ali[7]; Leonardo Lanteri[8]; Luca Menzio[9]; Federico Siviero[5]; Vincenzo Monaco[10]; Marco Ferrero[5]; Valentina Sola[8]; Arianna Morozzi[11]; Francesco Moscatelli[2]

[1] *CNR-IOM and INFN, Perugia*

[2] *INFN Sezione di Perugia, Perugia, Italy*

[3] *University and INFN Perugia*

[4] *INFN Sezione di Torino, Torino, Italy*

[5] *INFN*

[6] *FBK Trento*

[7] *Fondazione Bruno Kessler*

[8] *Univ. of Torino - INFN*

[9] *UPO - INFN*

[10] *University and INFN Torino*

[11] *Istituto Nazionale di Fisica Nucleare (INFN)*

Auteur correspondant alessandro.fondacci@pg.infn.it

High Energy Physics at future colliders demands a new generation of particle detectors with capabilities exceeding those of current silicon technology. For example, at the various e^+e^- machines (CEPC, CLIC, FCC-ee, and ILC), the key requests are low material budget and excellent spatial resolution, with modest requests for radiation resistance or precise timing ($\sigma_t < 50$ ps). On the other hand, at hadron machines (FCC-hh, HE-LHC, and SppC), the most challenging requests are the radiation resistance (fluences above 10^{17} 1 MeV n_{eq}/cm^2) and the spatial and time precision (pileup $\sim$ 1000 events/bunch crossing, $\sigma_t \sim 5$ ps/hit, $\sigma_x \sim 5$ μm/hit).

Among different ongoing R&D activities, thin silicon sensors that combine resistive read-out and internal gain, known as low gain avalanche diode Resistive Silicon Detectors (RSDs), represent a very promising technology solution. For example, excellent position and temporal resolutions (in the order of 10 μm and below 50 ps, respectively) have been observed at the DESY test beam facility on 450 μm-pitch prototypes with AC-coupled cross-shaped electrodes coming from the second batch of RSD sensors produced by FBK (RSD2). Moreover, their large pixel size will allow for a reduction

in the number of read-out channels and thus help build 4D silicon telescopes with minimised power consumption.

However, using AC-coupled electrodes shows that, on average, 30% of the signal leaks outside the hit pixel, thus limiting the use of AC-RSDs in high occupancy environments. DC-coupled electrodes were investigated as a potential solution to improve signal containment within the pixel area. The concept of DC-coupled RSD (DC-RSD) has been finalised using an innovative mixed-mode approach to simulation (SPICE-based fast modelling and full 3D TCAD simulations of the sensor behaviour) that guided the design of their first production, presently in progress at Fondazione Bruno Kessler.

In this contribution, the design guidelines for DC-RSDs, as well as new strategies for signal confinement in AC-RSDs, will be shown. The impact of different sensor components (e.g. the coupling oxide and the resistive layer) is evaluated in the latter case. Moreover, a predictive analysis of both AC- and DC-RSD performance after irradiation carried out with state-of-the-art Technology CAD tools coupled with the last release of the Perugia radiation damage numerical model will be presented.

System integration / **83**

ATLAS High Granularity Timing Detector: mechanics, services, integration and assemly

Auteur: Sergei Malyukov[1]

Co-auteur: Irena Nikolic [2]

[1] *JINR*

[2] *LPNHE Université Paris Cité CNRS*

Auteur correspondant sergei.malyukov@cern.ch

The High-Granularity Timing Detector (HGTD), a novel detector based on Low Gain Avalanche Detector (LGAD) technology, being bult for ATLAS Phase 2 upgrade to help mitigate the effects of increased pileup at the HL-LHC by providing high-precision timing information, measuring charged-particle trajectories in time as well as space. In addition, it will provide an instantaneous measurement of the luminosity, reading this information at 40 MHz.
The HGTD consist of two end caps, which will be installed in the gaps between barrel and end cap calorimeters at approximately ± 3.5m from the interaction point, covering the pseudorapidity region between 2.4 and 4.0. With an average of 2.5 hits per track, the target time resolution per track for a minimum-ionising particle is 30 ps at the start of lifetime, increasing to 50 ps at the end of HL-LHC operation (total integrated luminosity of 4000 fb−1).
The HGTD includes 8032 front-end modules. Each module is constructed of two hybrids, each composed of Low Gain Avalanche Sensor (LGAD) of approximately 2×2cm2 in size, bump-bonded to ATLAS LGAD Timing Integrated Read-Out Chip (ALTIROC). The hybrids are held together by a short flexible PCB and connected to Peripheral Electronics Boards (PEB) by another flexible PCB. The LGAD sensor has 225 pixels of 1.3x1.3 mm2, which gives 3.61 million reading channels in total. Each HGTD end cap comprises 4016 such modules installed on either side of four identical half-disc cooling supports, which make up two double-sided instrumented disks. The disks are rotated by 15° relative to each other to maximize the hit efficiency. The detector will operate at -35 Co using CO2 cooling, which requires encapsulation of the instrumented disks in a hermetic vessel, the vessel also includes a neutron moderator layer. To prevent condensation on the detector components, the interior volume of the vessel is flushed with dry nitrogen gas.
The HGTD envelope is limited by the space available in the gap region between the barrel and end cap calorimeters, making it very compact. The detector vessel has a radial extent of 110 mm to 1050 mm. The envelope in the beam direction (z) is 125 mm, including the front and rear covers and the internal moderator, resulting in only 75 mm in z for the detector components.
Such a tight envelope makes it very challenging the integration of the detector modules, on-detector electronics and connection of services. The construction of the detector requires construction of dedicated tools for assembling the instrumented half-disks and their integration into the vessel.

Timing with pixels / 84

The MiniCactus CMOS timing sensor development line: towards HV-CMOS monolithic timing sensors with 20 ps resolution

Auteurs: Eva Vilella[1]; Fabrice Guilloux[None]; Jean-Pierre MEYER[2]; Philippe Schwemling[3]; Raimon Casanova Mohr[4]; Sebastian Grinstein[5]; Yavuz Degerli[None]; Yujing Gan[6]

[1] *University of Liverpool*

[2] *CEA-SACLAY*

[3] *Université Paris Cité and CEA/Irfu/DPhP*

[4] *IFAE Barcelona and Department of Microelectronics and Electronics Systems of the Autonomous University of Barcelona*

[5] *IFAE*

[6] *IFAE Barcelona*

Auteur correspondant philippe.schwemling@cea.fr

I. Introduction

The v1 and v2 MiniCACTUS sensors are monolithic CMOS sensors in LF15A technology, designed to investigate the possiblity of tagging time of arrival of Minimum Ionizing Particles with a resolution better than 100 ps. These sensors are a first step towards an ultimate time resolution of 20 ps, needed for future projects like FCC-ee. MiniCactus v1 and v2 feature arrays of diodes without internal amplification, with an analog front-end and discriminator per pixel. A time resolution of 65 ps has been measured on a 0.5 mm² pixel from a 200 µm-thick sensor MiniCactus v1 sensor tested at CERN.

II. MiniCactus Sensors Description
The MiniCACTUS v1 and v2 sensors have the front-end electronics for each pixel at the column level, avoiding large power rails and the associated parasitic capacitance in the active area. The v1 front-end electronics comprises an AC-coupled charge sensitive amplifier, a discriminator and a 4-bit DAC for threshold tuning.

Standard MiniCactus v1 HR wafers have been thinned (100, 200 and 300 µm) and post processed for backside polarization. MiniCactus v1 substrates can be safely biased to at least -300V. All pixels from MiniCactus v1 have been calibrated with 55Fe and 241Am sources. MiniCactus v2 is an improved version of MiniCactus v1, with corrections of couplings between analog and digital electronics, an improved discriminator with programmable hysteresis and twice as many pixels. MiniCactus v2 also features new flavours of analog front-end : an improved CSA, and a VPA inspired from the Altiroc ASIC developed for the ATLAS HGTD. These new front-ends have much faster return to baseline than the original CSA of MiniCactus v1, making them better suited for an environment with high pileup.

III. Test-beam results
MiniCactus v1 sensors with 200 µm and 100 µm thickness, as well as MiniCactus v2 with thicknesses of 200, 175 and 150 µm have been tested with muons at CERN SPS (H4, in parallel with RD51/DRD1). The best timing results so far have been obtained with a 200 µm MiniCactus thick sensor, for a pixel 500 by 1000 microns, with a timing resolution of 65 ps at nominal FE settings and –450 V bias voltage, after time walk effect corrections. First test beam measurements done in June-July 2024 with MiniCactus v2 confirm the shortcomings of MiniCactus v1 have been corrected, and time resolution is comparable for similar high voltage and front-end settings.

IV Future prospects
Time resolution for non amplified sensors is limited by Landau fluctuations, since the charge collection region has to be thick, about 200 microns, to ensure sufficient signal over noise ratio. A way to overcome this difficulty is to add intrinsic amplification to the sensor, produced by a buried PN junction. TCAD simulations performed with Sentaurus have shown the concept to allow for a charge gain of about 10, provided the structure of the pixel edge is carefully optimized to avoid early breakdown. Passive test structures in LF15A technology have been designed to test this idea, and will be available by end of 2024.

Monolithic sensors / **85**

TelePix2: A HVCMOS pixel sensor for Fast Timing and Region of Interest Triggering

Auteur: Arianna Wintle[1]

Co-auteurs: Andre Schöning [2]; David Immig [2]; Felix Sefkow [3]; Heiko Augustin [2]; Ivan Peric [4]; Lennart Huth [1]; Lucas Dittmann [2]; Marcel Stanitzki [1]; Ruben Kolb [2]

[1] *Deutsches Elektronen-Synchrotron (DE)*

[2] *Heidelberg University (DE)*

[3] *Deutsches Elektronen-Synchrotron*

[4] *The Karlsruhe Institute of Technology*

Auteur correspondant arianna.wintle@desy.de

The DESY II Test Beam Facility offers electrons with a user selectable momentum ranging from 1-6 GeV alongside beam telescopes as precise reference tracking systems. Whilst providing a very high spatial resolution, they provide no timestamps for individual hits within the readout frame. The length of this readout frame means the telescopes frequently read out hits from multiple electrons together, without an additional segmented timing layer, it becomes impossible to assign tracks to specific triggers. Additionally a size mismatch between the trigger of the telescope and the test device leads to inefficient data taking. To overcome this, a configurable region of interest trigger is needed.

TelePix2 is a High Voltage Monolithic Active Pixel Sensor (HV-MAPS); it provides both fast timing with a timestamp of 4 ns and a fast digital single ended trigger output with a configurable region of interest down to the level of individual pixels.

The sensor, implemented in the 180 nm HV-CMOS process of TSI, has a pixel matrix of 120 columns by 400 rows with a pixel size of 165 x 25 µm leading to an active area of size 19.8 x 10 mm^2. Both an amplifier and comparator are housed within the pixel electrode. Three tune bits can be set on a per pixel basis to apply an offset to the comparator threshold for trimming purposes. The range of the offset these tune bits apply is controlled by a separate global DAC parameter.

The discriminated hit signal is transferred to the periphery. Here timestamps are assigned to the rising and falling edge, allowing for offline timewalk and delay corrections. The readout of hits is executed in a data driven column drain scheme via a 1.25 GBit/s link. The DAQ of TelePix2 is based on the HV-MAPS DAQ developed in Heidelberg and is fully integrated with EUDAQ2 and the AIDA-TLU.

Here, characterisation results of TelePix2 are presented based on the latest test beam measurements. A time resolution, without additional corrections for time-walk and pixel to pixel fluctuations, below 4 ns was found at an efficiency above 99% at a depletion voltage of -85 V. The time resolution of the trigger output from TelePix2 is around 2.5 ns. TelePix2 is utilised by users successfully and is currently transitioning to regular user infrastructure at the DESY II Test Beam Facility.

HEP experiments / **86**

Status and Performance of CMS Pixel Tracker during Run 3

Auteur: Steffi Bower[1]

[1] *CMS/FSU*

Auteur correspondant nb19o@fsu.edu

The CMS pixel detector is the innermost part of the CMS tracking system. The performance of the detector is monitored closely with frequent calibrations to measure expected degradation due to radiation damage. The pixel tracker provides high quality data for physics despite the ongoing challenges of Run 3. The operational experience and performance of the pixel tracker during 2022, 2023, and 2024 data-taking periods is presented.

Medical imaging applications / **87**

AlphaBeast: a CMOS-based neutron counter for radiation protection

Auteurs: Jean-Michel Horodynski[1]; Nicolas Arbor[2]; The-Duc Lê[3]; stephane higueret[3]

[1] *CNRS-iRSD*

[2] *IPHC-Strasbourg*

[3] *IPHC*

Auteur correspondant nicolas.arbor@iphc.cnrs.fr

Neutrons are one of the main secondary radiations produced by particle accelerators. They are therefore a key element in the radiation protection of facilities used for fundamental research or medical and industrial applications (production of radionuclides, hadrontherapy, sterilization). The main risks relate both to the radiation dose received by people exposed to neutrons (workers, patients) and to the neutron activation. Whatever the field of application, reducing risks and optimizing processes requires a better understanding of the neutron fields produced by the operation of particle accelerators. However, the spatio-temporal characterization of secondary neutrons produced during irradiation is still very difficult to implement systematically. The current reference methods (activation foil, Bonner spheres systems, solid nuclear track detectors) have economic and human costs that severely limit the quantity and quality of the available data, which are essential for better neutron risk management.

In this context, the IPHC-DeSIs team works on the development of a CMOS-based counter for real-time monitoring of thermal and fast neutrons. The *AlphaBeast* CMOS sensor (XFAB technology 0.35 mum) was designed in 2022 (Figure 1), as an improved version of the *AlphaRad* prototype developed in 2017 [1,2]. This sensor is completely integrated, highly transparent to photons and optimized for low power consumption. Neutrons are detected from their conversion into protons (fast neutrons, PE converter) and alpha particles (thermal neutrons, 10B converter). Internal thresholds are used to separate the two populations, giving a distinct indication of the fluxes of thermal and fast neutrons. Several configurations of diodes and apertures in the top oxide layer were tested in order to determine which offered the best compromise between detection efficiency and alpha/proton signal separation.

Accurate measurements of neutrons in mixed fields requires a precise evaluation of the CMOS sensor response to photons, electrons, protons and alpha particles. We present a full experimental characterization of the *AlphaBeast*, based on several test beam experiments done in research (cyclotron), medical (linear accelerator) and industrial (rhodotron) facilities. A Geant4/GATE Monte Carlo simulation of the sensor is also carried out, incorporating 2D charge collection efficiency maps obtained from the AIFIRA (IP2I-Bordeaux) proton-alpha microbeam line. The Monte Carlo modelling is used to determine the efficiency and purity of the selection cuts for thermal (alpha) and fast (proton) neutron separation. We also discuss the various sources of background, such as direct interactions of neutrons in silicon, and the corresponding correction factors to be applied.

The *AlphaBeast* sensor is the central component of a future real-time neutron mapping system, dedicated to the radiation protection of particle accelerators and associated applications. This system will be designed as a network of connected autonomous CMOS sensors, strategically positioned in the irradiation room to enable real-time measurement of the spatial and energy distributions of neutron fluxes.

[1] N. Arbor et al., "Real-time detection of fast and thermal neutrons in radiotherapy with CMOS sensors", PMB, 62(5) (2018)
[2] N. Arbor, S. Higueret, D. Husson, « Micro-scale characterization of a CMOS-based neutron detector for in- phantom measurements in radiation therapy », NIM A 888 (2018)

Monolithic sensors / **88**

Design and measurement of a large CMOS pixel with nanosecond collection time

Auteur: Sven Boulanger[1]

Co-auteurs: Ajit Kumar Kalgi [1]; Bart Dierickx [1]; Jens De Vroe [1]; Nicolas Van Opstal [1]; Shirly Regev [2]

[1] *Caeleste*

[2] *Ethesian*

Auteur correspondant sven.boulanger@caeleste.be

For particle counting detectors with high repetition rate, low latency and low jitter using direct detection of incident electrons, a short transit time of the secondary generated electrons and holes within the pixel structure is required. Additionally, for a pixel array that spans a large area, we wish to minimize the overall power consumption by minimizing the number of pixels, implying larger pixel areas. The conversion of electron-hole pairs generated by the incident electrons to a useful signal, requires a dedicated per-pixel circuit with a high SNR. Modeling and simulations show that this circuit requires a small input capacitance. Reducing the transit time can primarily be achieved through application of a (negative) backside voltage.

In this paper, we explore the trade-off of a short transit time in combination with a low junction capacitance and pixel area. We make a brief survey of different pixel topologies (SPADs, APDs, scintillators, resistive-feedback and capacitive-feedback transimpedance amplifiers) and compare their theoretical noise performance for high repetition rate counting applications.

We present TCAD simulations and measurements for an implementation of such a pixel in a mixed CMOS process. In TCAD, we attempt to extract a worst-case transit time. We observe a double peak in the current waveform.

We attempt to confirm these TCAD findings with measurements using a short pulsed laser using a wavelength of 640nm that exhibits a similar penetration depth as the Continuous Slowing Down Approximation (CSDA) of the incident electron.

Monolithic sensors / **89**

Particam: A fully digital sensor for sub micron resolution

Auteurs: Gianluigi Casse[1]; Jan Hammerich[1]; Luca Parmesan[2]; Massimo Gottardi[2]; Nicola Massari[2]

[1] *University of Liverpool (UK)*

[2] *Fondazione Bruno Kessler*

Auteur correspondant j.hammerich@cern.ch

While silicon industry advances to smaller and smaller feature sizes, silicon particle detectors struggle to follow that miniaturisation. One of the main bottlenecks are the relatively large transistors required for the optimal performance of the analogue frontend. Particam instead uses a digital only approach which is focused on digital storage cells switching due to transient radiation (Single Event Upset (SEU)). Normally, great effort is expended to prevent SEUs from affecting the registers of any

ASIC, designs can also be optimised in the opposite way. With a pixel being little more than a memory cell it can be designed with close to minimum feature size with very few transistors allowing pixel pitches of a few microns.
A proof of principle demonstrator with different pixel flavours with pitches ranging from 6.5um to 2um has been produced in the UMC 65nm process. Test pulse measurements show the circuits work as intended, the charge collection was found to be insufficient for most types of ionising radiation besides alpha particles. Samples coated with a neutron converter are under investigation as demonstrator for precision measurements. Results of this prototype are to be presented.
A second prototype fabricated in the LFoundry 110nm node exploring if the charge collection in a thin epi-layer process is sufficient for this concept. First measurements of this prototype will be shown.
In addition, plans for further developments and possible applications will be discussed.

Timing with pixels / **90**

Design and production of timing optimised 3D silicon sensors for future LHC experiments and beyond

Auteurs: Adriano Lai[1]; Angelo Loi[2]; Gian-Franco Dalla Betta[3]; Jixing Ye[4]; Maurizio Boscardin[5]; Sabina Ronchin[6]

[1] *INFN*

[2] *INFN Cagliari*

[3] *University of Trento and TIFPA INFN*

[4] *Università di Trento e TIFPA*

[5] *FBK Trento*

[6] *FBK*

Auteur correspondant jixing.ye@unitn.it

During the last years, the need for innovative technologies that allows to enhance performance of particle tracking detectors has become a very important point. New sensor technologies play a key role in detector R&D, focusing the development on increased radiation hardness, improved timing and space resolution.
Among the currently developed sensor technologies, the 3D silicon sensor has already demonstrated its validity in terms of optimum space resolution and large field coverage within large scale LHC experiments, such as the ATLAS experiment within the IBL and current ITK tracking detector. Using the 3D silicon technology also for 4D tracking with intrinsic time resolution below 20 ps has been already investigated within different research groups, especially related to the LHCb collaboration. The R&D achieved over the last 8 years has brought to the development of a timing optimised sensor based on a trenched-shaped electrode instead on the more classical columnar shape pixel like the ones used within the IBL and ITK. R&D projects such as TimeSPOT and, successive, AIDAinnova developed and produced already 3 prototype production batches at FBK, two of them already demonstrating intrinsic time resolution of less than 20 ps and the possibility to operate after an integrated damage of $1*10^{17}$ 1 MeV n_eq /cm^2.
This study aims to present a current design and evaluation process for a new, 3D silicon sensor batch that aims to achieve timing close to the TimeSPOT/AIDAinnova 3D trench geometry by using a simplified geometry using columnar electrodes in specific organised setting and with a reduced pixel size.
The design approach is based on Synopsys TCAD with the support of the TCoDe GPU-Multy Thread transient simulator that allows to simulate very large statistic of events over a very short simulation time compared to similar tools available in HEP. Different sensor geometries with different pixel sizes have been designed and analysed, in terms of intrinsic charge collection time and intrinsic capacitance. Among the simulated geometries, 3 have been chosen to be explored more deeply by simulating the behaviour of the single pixel within a 3x3 pixel matrix. From the collected data, a trend is evident that also columnar electrode-based 3D pixel geometries are suitable for being implemented within 4D tracking detectors with ps time resolution.
This design study is also propaedeutic towards future beam test campaigns that will include timing optimised 3D silicon sensor based on trench electrodes from the AIDAinnova project, as well as a

newer sensor batch, with production beginning scheduled for the third quarter of 2024, based on columnar electrodes with smaller pitch and pixel matrices, with a more refined production process for easier and higher yield hybridisation that will be compatible with future INFN IGNITE-1 and INFN-IGNITE-X readout chips respectively.

Timing with pixels / **91**

Design and characterization of Low-Gain Avalanche MAPS in 110nm CMOS

Auteur: Lucio Pancheri[1]

Co-auteurs: Fabiola Caso [1]; Jacopo Endrizzi [1]; Stefano Durando [2]; Umberto Follo [2]; Giulia Gioachin [3]; Chiara Ferrero [2]; Marco Mandurrino [4]; Manuel Rolo [4]; Angelo Rivetti [4]; Stefania Bufalino [3]

[1] *University of Trento and TIFPA-INFN, Italy*

[2] *INFN Sezione di Torino and DET Politecnico di Torino, Italy*

[3] *INFN Sezione di Torino and DISAT Politecnico di Torino, Italy*

[4] *INFN Sezione di Torino, Italy*

Auteur correspondant lucio.pancheri@unitn.it

Charged Particle detection in High-Energy Physics (HEP) applications increasingly asks for sensors with improved timing resolution and low power. A trade-off between these two requirements is typically necessary and strongly linked to the design and technology of front-end readout electronics. Low-Gain Avalanche Detectors (LGADs), which have become an established technology in HEP experiments, offer significant improvements in this respect. However, advanced packaging techniques are required to fully exploit the potential of large-area pixelated detectors based on LGADs, thus substantially increasing system costs and reducing the yield.

To address these limitations, several research groups are beginning to explore the feasibility and performance of CMOS-integrated LGADs. This work presents the ongoing activities towards customizing the fully depleted monolithic sensor technology developed at INFN project ARCADIA by adding a gain layer to the readout electrodes. In this way, the electrons generated in the active volume of the sensors by the absorbed radiation and drifting towards the collection electrodes need to cross a high-field region, resulting in a net signal improvement. The sensors' active region is a high-resistivity n-type epitaxial layer grown on a standard p+-doped silicon substrate, and its thickness can thus be easily modified by changing the thickness of the epitaxial layer. The gain layer is depleted by applying a sufficiently high voltage at the top electrode, which requires a bias resistor and needs to be AC-coupled to the readout electronics. The substrate has to be biased at a negative voltage to deplete the full active substrate and generate the required drift field in all the device's active regions.

Several test pixel layouts have been included in the first design, exploring large pixels for improved timing resolution and smaller pixel test structures suitable for simultaneous tracking and timing (4D detection). Large test pixels, designed for the requirements of ALICE 3 Time of Flight layers, have an active area of 250µm x 70µm and 250µm x 250µm, while smaller square pixels feature a pitch of 25 and 50µm. A sensor array with integrated readout electronics was also designed for the 250µm x 70µm pixels.

Different sensor terminations have been explored in the design. For large pixels, a termination similar to the one used in standard LGADs, where the edges of the sensor provide charge collection with unit gain is acceptable, since a small amount of generated charges is collected at the periphery. However, in small pixels, the fraction of electrons collected by the gain-less termination region would be unacceptably large and spoil the pixel performance. To this end, another termination type exploiting deep p-well implantations, capable of conveying all the collected charges to the gain region, was also included in the design.

A preliminary characterization campaign, exploring electrical device characteristics, and functional measurements with optical sources and charged particles is underway. A summary of updated simulation results and experimental data obtained on the different pixel configurations will be presented.

Electronics / **92**

Testing the Limits of ITKPixV2: the ATLAS Inner Tracker Pixel Detector Readout Chip

Auteurs: Liam Foster[1]; Luc Le Pottier[1]; Maria Mironova[1]; Maurice Garcia-Sciveres[1]; Timon Heim[1]

[1] *Lawrence Berkeley National Laboratory*

Auteur correspondant luclepot@lbl.gov

The ITkPixV2 readout chip is the production readout chip for the ATLAS Phase 2 upgrade for the High-Luminosity LHC of the ATLAS inner detector, scheduled for commissioning at the start of 2029. The innermost layers of the ATLAS ITk pixel detector are expected to reach maximum hit rates of 3GHz/cm^2, a total radiation dose of 1 GRad, and data readout rates of 5Gbps, with an operational lifetime of over a decade.
In order to ensure continuous operation of the ATLAS pixel detector, it is critical to perform rigorous testing of the ITkPixV2 readout chip and the accompanying Data Acquisition (DAQ) system. To perform this testing, we utilize the YARR DAQ system, which is designed to support the readout of ATLAS ITk Pixel and Strip detector modules on a variety of hardware platforms. For readout hardware, we use the YARR PCIe firmware, which employs Simple PCIe Carrier (SPEC) cards to readout Pixel detector modules.
In this talk, we present the development towards and results of several such tests done in the past year in test beam campaigns, Single Event Effect (SEE) facilities, X-ray irradiation machines, and simple bench testing, as well as the DAQ development done concurrently in YARR software and firmware to facilitate these tests. These results present the closest test yet of ITkPixV2 chips to their target nominal operational conditions in the upgraded ATLAS detector at the HL-LHC. This includes reaching the highest hit rates and trigger frequencies measured to date, along with simultaneous development of the YARR DAQ software and firmware to be able to handle continuous stable operation, automatic chip error handling, and online data processing at these rates.

Posters / **93**

Performance studies of the CE-65v2 MAPS prototype structure

Auteur: Alessandra Lorenzetti[1]

Co-auteurs: Ajit Kumar [2]; Alex Kluge [3]; Andrei DOROKHOV [4]; Anna Macchiolo [1]; Armin Ilg [1]; Christine HUGUO [4]; Claude Colledani [5]; Daito Shibata [6]; Felix Reidt [3]; Hitoshi Baba [7]; Jerome Baudot [4]; Jonghan Park [6]; Kimmo JAASKELAINEN [8]; Lukas Tomasek [9]; Magnus Mager [3]; Mathieu Goffe [10]; Miljenko Sulic [3]; Pavel Stanek [9]; Serhiy SENYUKOV [11]; Shingo Sakai [6]; Szymon Bugiel [4]; T. Chujo [12]; Taku Gunji [7]; Towa Katsuno [13]; Walter Snoeys [3]; Yitao WU [14]; Yorito Yamaguchi [13]; Ziad El Bitar [4]; auguste besson [15]; hasan shamas ; isabelle valin [4]

[1] *University of Zürich*

[2] *IPHC Strasbourg*

[3] *CERN*

[4] *IPHC*

[5] *IPHC - IN2P3*

[6] *University of Tsukuba*

[7] *University of Tokyo*

[8] *CNRS/IN2P3/IPHC*

[9] *CTU Prague*

[10] *IPHC IN2P3 CNRS CERN*

[11] *Institut Pluridisciplinaire Hubert CURIEN (IPHC)*

[12] *Tsukuba Univ.*

[13] *Hiroshima University*

[14] *USTC & IPHC*

[15] *Institut Pluridisciplinaire Hubert Curien*

Auteur correspondant alessandra.lorenzetti@cern.ch

With the next upgrade of the ALICE inner tracking system (ITS3) as its primary focus, a set of small MAPS test chips have been developed in the 65 nm TPSCo CMOS process. The Circuit Exploratoire 65 nm (CE-65) focuses on the important characterisation of the analogue charge collection properties of this technology. The latest iteration of sensor design in this line of development is CE-65v2, which was produced in different processes (standard, with a low-dose n-type blanket, and blanket with gap between pixel) and pixel pitches (15, 18, 22.5μm). The comparatively large pixel array size of 48×24 pixels in CE-65v2 allows, among other benefits, to study the uniformity of the pixel response.
This year, the CE-65v2 chip was characterised in a test beam at the CERN SPS. A first analysis showed that hit efficiencies of $\geq 99\%$ and spatial resolution better than 5μm can be achieved for all pitches and process variants. For the standard process, with a pitch of 15μm, spatial resolutions below 3μm are achieved, thanks to larger charge sharing between the pixels, in line with the requirements of FCC-ee vertex detectors.
This contribution further investigates the data collected at the SPS test beam. The large amount of statistics collected, thanks to the large sensor size and efficient data taking, allow for detailed in-pixel studies to see the efficiency and spatial resolution as a function of the hit position within the pixels, again comparing different pitches and process variants.

Timing with pixels / **94**

4D tracking results with the Timepix4 telescope

Auteurs: Kevin Heijhoff[1]; Martin Van Beuzekom[1]

Co-auteur: Kazu Akiba [1]

[1] *Nikhef*

Auteur correspondant k.heijhoff@nikhef.nl

A high rate beam telescope based on the Timepix4 ASIC has been built to evaluate novel pixel sensors with high spatial and temporal resolution. Moreover, the telescope can also be used for tests of synchronous multiple-detector readout and track reconstruction with fast timing capability (i.e. 4D tracking demonstrator).
The telescope consists of eight planes with n-on-p silicon sensors, each bump bonded to a Timepix4 ASIC. Four of these planes are instrumented with 300 µm thick planar sensors, which are tilted with respect to the beam to improve the track pointing resolution. The other four planes have 100 µm thick sensors and are perpendicular to the beam to provide the best track time resolution.
The Timepix4 is designed to record both the time of arrival (ToA) and the time over threshold (ToT) for each discriminated signal. It has a 448 × 512 pixel matrix with square pixels at a 55 µm pitch. Each superpixel, a group of two by four pixels, has a 640 MHz voltage controlled oscillator (VCO). The VCO provides four phase shifted copies of the 640 MHz clock, which results in a ToA digitisation with time bins of 195 ps. The ToT is proportional to the charge collected by the silicon sensor, and is used to improve spatial resolution based on charge sharing. The ToT is also used to correct for timewalk and thereby improve the ToA resolution. After VCO and timewalk corrections a time resolution of 160-180 ps is achieved for each of the thin planes. The measurements are combined to achieve a more precise time stamp of a track of about 90 ps. In this presentation an overview of the telescope capabilities is given, and the most recent results of the temporal and spatial resolutions obtained by the telescope will be shown.

Posters / **95**

Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations

Auteurs: Giulio Borghello[1]; Corentin Lemoine[2]; Walter Snoeys[None]

[1] *CERN*

[2] *IPHC/CERN*

Auteur correspondant giulio.borghello@cern.ch

Monolithic Active Pixel Sensors (MAPS) offer the possibility to integrate sensors and readout electronics on the same chip in a standard CMOS process. This significantly reduces the material budget while maintaining good spatial resolution, making MAPS an attractive solution for High Energy Physics (HEP) applications. A prominent example of MAPS in HEP applications is the new ITS3 vertex detector of the ALICE experiment at the Large Hadron Collider (LHC) at CERN [1]. This chip will be located at less than 20 mm from the interaction point and is planned to be installed in 2026, during the LHC Long Shutdown 3 period.
This work focuses on the optimization of the pixel sensor for the new ITS3 vertex detector and future monolithic chips for HEP applications. In the framework of the CERN Experimental Physics Research & Development Work-Package on monolithic sensor (EP-R&D WP1.2) and in synergy with the ALICE experiment and the ITS3 upgrade, an extensive 3D TCAD simulation campaign was conducted to optimize the sensor for both higher performance and better radiation tolerance.
Performance of the sensor is evaluated based on the sensor capacitance CS, the total charge collected, and the collection time in both cases where a particle crosses either the center or the corner of the pixel.
Given the proximity of the sensor to the interaction point, ensuring its radiation tolerance is essential. While sensors in ITS3 must endure a fluence of 1×10^13 1MeVneq/cm2, fluences in other applications can be significantly higher, sometimes exceeding 1×10^16 1MeVneq/cm2.
This optimization acts on the implants of the TPSCo 65nm CMOS commercial imaging process used to realize the sensor. The TPSCo 65nm technology has been qualified for HEP and this further optimization aims at reducing CS. Smaller CS result in a higher signal for the same charge, increasing the operating margin for a given power consumption or reducing the power consumption for a given operating margin. A large part of simulations focused on the relevant practical situation of a sensor biased at only VB=-1.2V, a requirement for ITS3. This work is a continuation and further improvement of the work presented in [2].
The optimized version of the process presented in this work demonstrates a reduction in sensor capacitance of more than two orders of magnitude in comparison to the standard process. Compared to the work in [2], CS was reduced by more than a factor of 4, maintaining very similar timing and radiation hardness. This result is extremely relevant for the design of the front-end circuit. The extensive simulations (more than 300GB) are used to explore the limits of the sensor operating point to ensure sufficient operating margin.
The simulations were extended to higher reverse-bias voltages to explore the possibility of improving the radiation tolerance of the sensors for applications operating at fluences higher than ITS3. The data presented here contribute to demonstrate that higher reverse-biases are necessary for designing sensors capable of withstanding fluences above 1×10^15 1MeVneq/cm2.
[1] TDR ALICE-ITS3. No. CERN-LHCC-2024-003. 2024
[2] C. Lemoine et al 2024 JINST 19 C02033

System integration / **96**

Pixel detector hybridization with anisotropic conductive adhesives

Auteur: Ahmet Lale[1]

Co-auteurs: Alexander Volker [1]; Debora Magalhaes Suarez ; Dominik Dannheim [1]; Giovanni Calderini [2]; Haripriya Bangaru [1]; Helge Kristiansen [3]; Janis Viktor Schmidt [4]; Justus Braach [1]; Marie Ruat [5]; Mateus Vicente Barreto Pinto [6]; Matteo Centis Vignali [7]; Peter Švihra [1]; Rui De Oliveira [1]; Xiao Yang [1]

[1] *CERN*

[2] *LPNHE Paris*

[3] *Conpart AS*

[4] *KIT - Karlsruhe Institute of Technology (DE)*

[5] *ESRF*

[6] *Universite de Geneve (CH)*

[7] *Fondazione Bruno Kessler*

Auteur correspondant ahmet.lale@cern.ch

In the development of hybrid pixel detectors, a reliable and cost-effective interconnect technology is paramount. This technology must be tailored to the specific pitch and die sizes of the applications at hand. Particularly crucial during the ASIC and sensor development phases, these interconnection technologies must also accommodate the assembly of single dies, commonly available from Multi-Project-Wafers.

Within the CERN EP R&D program and the AIDAinnova collaboration, innovative and scalable hybridization concepts are pursued for pixel-detector applications in future colliders. The recent focus has been on developing a reliable single-die interconnection process based on Anisotropic Conductive Adhesives (ACA). Two different approaches are studied: Anisotropic Conductive Paste (ACP) and Anisotropic Conductive Film (ACF). These ACA technologies replace solder bumps with conductive micro-particles embedded in an adhesive layer, applied either as film or paste. The electro-mechanical connection between the sensor and ASIC is achieved through thermo-compression of the ACA using a flip-chip device bonder. The ACA technology demonstrates versatility by also facilitating ASIC-PCB/FPC integration, offering a viable alternative to wire bonding or large-pitch solder bumping techniques.

A critical aspect of the ACA approach is the necessity for a specific pixel-pad topology, enabling connection via micro-particles and creating cavities for excess adhesive flow. This pixel-pad topology is achieved through an in-house Electroless Nickel Gold (ENIG) process, which is concurrently under development within the project.

The ENIG and ACA processes are rigorously qualified with various ASICs, sensors, and dedicated interconnect test structures, featuring pad diameters ranging from 10 µm to 140 µm and pitches between 20 µm and 1.3 mm. Thanks to recent process optimizations, an excellent ENIG plating yield has been achieved, with nearly 99% of pads correctly plated. For flip-chip assemblies using ACF and ACP, the rate of correctly connected pads is close to 98% for chips with large pad dimensions and pitches (80µm pads with a 200µm pitch). Current efforts focus on chips with pad dimensions around 10µm with a 25µm pitch, aiming to achieve similar connection rates for these smaller dimensions. Several projects participate with readout ASICs and sensors in the qualification of the assembly process, including Timepix3 with 12-14µm exposed pad diameter, 55 µm pitch on a 2cm² bonding surface, ESRF SPHIRD with 15µm exposed pad diameter, 50 µm pitch on a 5mm² surface, ALTIROC2/3 with 90µm exposed pad diameter, 1.3mm pitch on a 4 cm² surface, and CLICpix2 with 12µm exposed pad diameter, 25µm pitch on a 2.6mm² surface. The assemblies produced undergo comprehensive electrical characterization, including tests with radioactive-source exposures and high-momentum particle beams. Additionally, thermal cycling is conducted to study the robustness and potential aging of the assemblies. Initial results show good resistance of the interconnections to temperatures ranging from -40℃ to 120℃.

In summary, this contribution serves to introduce the developed interconnect and plating processes, highlighting several types of hybrid assemblies produced and tested using the aforementioned methods. Notably, recent optimizations in plating and interconnect processes have led to improved plating uniformity and interconnect yield, enhancing the overall reliability and performance of hybrid pixel detectors.

System integration / **97**

A Packaging Method for ALPIDE Integration Enabling Flexible and Low-Material-Budget Designs

Auteurs: David Novel[1]; Pierluigi Bellutti[1]; Roberto Iuppa[2]; Stefania Beole'[3]; Tiziano Facchinelli[1]; alessandro lega[4]

[1] *Fondazione Bruno Kessler*

[2] *University and INFN of Trento*

[3] *Universita' di Torino*

[4] *Universita' di Trento*

Auteurs correspondants: novel@fbk.eu, alessandro.lega@unitn.it

This work presents a novel, patent-pending solution for the packaging of ALPIDE chips that facilitates non-planar assembly with a minimal material budget. This solution represents an advancement based on methodologies developed for the ALICE ITS1 and the STAR tracker two decades ago. The core of this approach involves the use of flexible cables composed of aluminum and polyimide, with thicknesses on the order of tens of micrometers. These cables are connected to the sensors using single-point Tape Automated Bonding (spTAB), which replaces the traditional wire bonding technique that is suboptimal for curved integrations. The spTAB bonding is achieved by creating openings in the polyimide layer, allowing aluminum wires to remain free-standing, which are then connected to the sensor using pressure and ultrasonic energy. Extending this concept, we have applied this approach to entire printed circuit boards (PCBs), resulting in a fully flexible packaging solution maintaining an ultra-low material budget. This work introduces a prototype utilizing this method to bond an ALPIDE chip, proposing it as a viable option for future designs necessitating flexible packaging for both the chip and associated electronics. The overall workflow, comprising microfabrication and assembly, is carried out in the Fondazione Bruno Kessler laboratories and will be detailed to elucidate our procedures and demonstrate the applicability of our solution in future experimental setups. The proposed packaging features a flexible PCB constructed from three stacked layers, each containing 20 µm thick aluminum features and a 25 µm thick polyimide substrate. These layers include a ground layer, a signal layer (encompassing both digital and analog signals), and a bonding layer (which substitutes wire bonding). The spTAB technique is employed for inter-layer connections within the PCB and for sensor bonding. We will discuss the performance of transferring both digital and analog electrical information through the flexible PCBs. SEM and PFIB optical characterizations, along with pull-test measurements to qualify the bonding, will be reported. Furthermore, we will quantitatively assess the flexibility of the entire assembly (ALPIDE and flexible PCB) and describe the behavior of the spTAB connections when the device is bent to a curvature radius of a few millimeters.

Posters / **98**

DC resistive read-out silicon sensors for future 4D tracking: recent advancements and first prototypes characterization.

Auteurs: Roberta Arcidiacono[1]; et al.[None]

[1] *Università del Piemonte Orientale e INFN Torino (IT)*

Auteur correspondant roberta.arcidiacono@uniupo.it

Recent advancements in silicon sensor technology have paved the way for the development of high-resolution 4D-tracking detectors capable of simultaneously measuring the position and time of passage of charged particles within a single sensitive device. A key approach is the use of resistive read-out in thin Low Gain Avalanche Diode (LGAD) sensors, which introduces combined intrinsic signal sharing and internal gain within a single detector element.
This contribution focuses on the developments of a thin LGAD with a resistive DC-coupled read-out (DC-coupled Resistive Silicon Detector - DC-RSD).
The aim of the DC-RSD sensors is to achieve a spatial resolution of a few micrometers and an excellent time resolution of approximately 30 ps, using relatively large pixels (150-200 micrometers), which enables detectors with low channel density and low power consumption.
This contribution describes the development path and the design strategy of the first DC-RSD production, presently in progress at Fondazione Bruno Kessler. The strategy includes signal containment within a pre-determined number of electrodes, using isolating trenches (TI technology). Several test

structures and application-oriented devices have been implemented in the wafer layout.
This first, proof-of-concept, prototype run will enable detailed studies of the charge sharing and charge containment mechanism in a large phase-space of all key parameters.
The production will be completed in September 2024.
Preliminary results from static characterization performed in the laboratory will be presented, along with initial studies of signal propagation and signal sharing properties, performed employing a Transient Current Technique laser setup.
The characterization of this first prototype production will provide us with immediate feedback on the soundness of the DC-RSD concepts.

HEP experiments / **99**

Upgrade of the Belle II Vertex Detector with depleted monolithic active pixel sensors

Auteurs: Alice Gabrielli[1]; The Belle II VTX collaboration[None]

[1] *INFN Pisa*

Auteur correspondant alice.gabrielli@pi.infn.it

The Belle II experiment currently records data at the SuperKEKB e+e- collider, which holds the world luminosity record of 4.7x10^34 cm-2.s-1 and plans to push up to 6x10^35 cm-2 s-1. In such luminosity range for e+e- collisions, the inner detection layers should both cope with a hit rate dominated by beam-induced parasitic particles and provide minute tracking precision. A R&D program has been established to develop a new pixelated vertex detector (VTX), based on the most recent pixel detection technologies. The VTX strategy entails higher space-time granularity, lighter overall structure and services compared to the current operating VXD based on two different technologies.
The expected gains include more robustness against the machine background as well as higher vertexing and tracking performance.

The VTX design matches the current vertex detector radial acceptance, from 14 mm up to 140 mm. It includes 5 to 6 layers for an overall material budget lower than 3 % of X0. All layers are equipped with the same depleted monolithic active pixel sensors, OBELIX This contribution focuses mainly on the latest expected performances after the sensor design finalisation.

The first OBELIX sensor version is designed in the Tower 180 nm technology, which pixel matrix is derived from the TJ-Monopix2 sensor originally developed for the ATLAS experiment. Featuring a 33 μm pitch and a time over threshold digitisation over 7 bits, OBELIX time-stamps hits with a 50 ns binning. The digital trigger logic matches the required 30 kHz average Belle II trigger rate with 10 μs trigger delay and a maximum hit rate of 120 MHz/cm2.
Two switchable additional features are intended for the outer layers coping with hit rates below 10 MHz/cm2. One corresponds to time stamping hits outside the matrix with 3 ns precision. The other provides continuous hit-information with 30 ns binning but with degraded position-precision for track-triggering. Recent simulations showing that the degraded spatial granularity can still lead to excellent track reconstruction efficiency will be discussed.

The radiation environment requires a tolerance to 5x10^14 1 MeV n_eq/cm2 and 1 MGy. In addition, the minimal material budget limits the cooling power and hence necessarily mean warm operation of the sensor, considering that its power dissipation is estimated to 200 mW/cm2 at the average hit rate of the inner layer.
We will review the latest characterisation of the TJ-Monopix2 forerunner sensor in beam after irradiation to assess the expected performance of the pixels and decide the tuning range of the OBELIX matrix.

Posters / **100**

Early evaluation of the triggering capacity of an upgrade Vertex Detector for the of the Belle II experiment

Auteurs: Matteo MAUSHART[1]; The Belle II VTX collaboration[None]

[1] *IPHC*

Auteur correspondant matteo.maushart@iphc.cnrs.fr

An upgraded vertex detector (or VTX) is in development for the Belle II experiment. A central concept of the VTX is the usage of a new CMOS monolithic pixel sensor, OBELIX. The design of this sensor offers new possibilities for specific read-out modes, such as a fast output for track-triggering purpose with degraded spatial granularity.
That means the nearly 400 000 pixels of OBELIX are reduced to only 8 macro-pixels, shaped as strips.
This contribution reports the first study investigating the tracking performance with such macro-pixels and simulations reproducing the VTX geometry.
A track reconstruction algorithm is developped based on a large look-up table containing simulated single track hit pattern over three VTX outer layers. The algorithm is then applied to various simulated data sets as test samples to evaluate figures of merit.
The reconstruction efficiency exceeds 98 % in average but features a clear decrease at low momentum below 500 MeV/c. The sensitivity to tracks drops very rapidly with the distance along the beam axis between the track origin and the collission point. After a few centimers, no more tracks can be reconstructed.
These early results show that the low granularity mode is a promising solution for building a trigger decision based on tracks reconstructed with the OBELIX sensor.

Photon science applications / **102**

Developments of a 25 µm pitch hybrid pixel detector for photon science

Auteurs: Anna Bergamaschi[1]; Julian Heymes[1]; Roberto Dinapoli[1]

Co-auteurs: Aldo Mozzanica [1]; Bechir Braham [1]; Bernd Schmitt [1]; Carlos Lopez-Cuenca [1]; Christian Ruder [1]; Davide Mezza [1]; Dhanya Thattil [1]; Dominic Greiffenberg [1]; Erik Fröjhd [1]; Filippo Baruffaldi [1]; Jiaguo Zhang [1]; Khalil Ferjaoui [1]; Kirsty Anne Paton [1]; Konstantinos Moustakas [1]; Maria Carulla-Areste [1]; Martin Brückner [1]; Patrick Sieberer [1]; Pawel Kozłowski [1]; Rebecca Barten [1]; Shqipe Hasanaj [1]; Simon Ebner [1]; Thomas King [1]; Viktoria Hinger [1]; Xiangyu Xie [1]

[1] *Paul Scherrer Institut*

Auteur correspondant julian.heymes@psi.ch

The MÖNCH detector is a charge integrating prototype Hybrid Pixel Sensor with 25 µm pixel pitch. With low noise pixel architectures and the charge sharing effect, the position of the impinging photon can be interpolated into virtual sub-pixels enabling high spatial resolution. The small pixel pitch also offers excellent native resolution with high frame-rates. The MÖNCH detector has already demonstrated its capabilities in several pilot experiments with various types of sensors (*i.e.* LGADs, standard Si sensors, High-Z materials) covering a very broad range of photon energies.

Using the characterisation results of 19 different pixel designs in MÖNCH0.4 (1cm²), and from the performance of MÖNCH0.3 (single design, 1cm²), we have designed a new prototype: MÖNCH0.5 (4x4 mm²) featuring 6 pixel designs and an optimised analogue readout chain.

We will present the path towards the design of our current prototype accompanied with the first test results in preparation to future pilot experiments. The obtained results will support the scaling-up towards a full-size MÖNCH1.0 detector (~3 x 2 cm²).

Sensing materials & Radiaiton tolerance / **103**

Compensated LGAD –An innovative design of thin silicon sensors for very high fluences

Auteurs: Valentina Sola[1]; Giovanni Paternoster[2]; Arianna Morozzi[3]; Anna Rita Altamura[4]; Roberta Arcidiacono[5]; Giacomo Borghi[6]; Maurizio Boscardin[7]; Nicolo' Cartiglia[8]; Matteo Centis Vignali[2]; Marco Costa[4]; Tommaso Croci[9]; Matteo Durando[4]; Marco Ferrero[8]; Alessandro Fondacci[10]; Leonardo Lanteri[11]; Luca Menzio[5]; Francesco Moscatelli[9]; Daniele Passeri[12]; Nadia Pastrone[8]; Federico Siviero[8]; Robert White[11]

[1] *INFN Torino (IT)*

[2] *Fondazione Bruno Kessler*

[3] *Istituto Nazionale di Fisica Nucleare (INFN)*

[4] *Torino University and INFN*

[5] *UPO - INFN*

[6] *Politecnico di Milano*

[7] *FBK Trento*

[8] *INFN*

[9] *INFN Sezione di Perugia, Perugia, Italy*

[10] *CNR-IOM and INFN, Perugia*

[11] *Univ. of Torino - INFN*

[12] *University and INFN Perugia*

Auteur correspondant marco.ferrero@to.infn.it

Future high-energy and high-intensity colliders, such as the Muon Collider or the FCC-hh, require precise particle tracking in space and time up to very high fluences, above 10^{16} 1 MeV equivalent n/cm^2 or even an order of magnitude higher.

To design future tracker detectors able to operate in very harsh radiation conditions, it is necessary to manufacture new sensors which provide excellent tracking and timing performances.

We will present an innovative silicon sensor concept which profits from the saturation of the radiation effects observed at high fluences, uses thins sensors, which are intrinsically less affected by irradiation, and internal multiplication of the signal up to the target fluences.

This breakthrough is possible thanks to a new concept of the implant responsible for signal multiplication in Low-Gain Avalanche Diodes (LGADs) obtained through the compensation of p- and n-type dopants. This new strategy is more resilient to radiation, as both acceptor and donor atoms will undergo deactivation with irradiation, but if properly engineered, their difference will remain constant. Therefore, the compensated LGADs will empower the 4D tracking ability to a fluence of 10^{17} 1 MeV equivalent n/cm^2 and above.

To achieve our target, a close interconnection with the modelling of the radiation effects is straightforward and state-of-the-art Technology CAD tools will be exploited. Present models need to be extended to unexplored regions of fluences to drive the detector engineering for the experiments of the future.

The first batch of compensated LGADs was released by FBK at the end of 2022. Sensor characterisation and signal analysis before and after irradiation will be presented and discussed. Possible improvements to the present design will be envisaged, and the next steps, guided by the modelling, will be introduced. The path to extend the validity of the present models to very high fluences will be enlighted.

Posters / **104**

Thin LGADs as radiation-resilient sensors for 4D tracking

Auteurs: Marco Ferrero[1]; Lucio Anderlini[1]; Anna Rita Altamura[2]; Roberta Arcidiacono[3]; Giacomo Borghi[4]; Maurizio Boscardin[5]; Nicolo' Cartiglia[1]; Matteo Centis Vignali[6]; Tommaso Croci[7]; Fabio Davolio[1]; Matteo Durando[2]; Alessandro Fondacci[8]; Simone Galletto[9]; Leonardo Lanteri[10]; Luca Menzio[3]; Francesco Moscatelli[7]; Daniele Passeri[11]; Nadia Pastrone[1]; Federico Siviero[1]; Robert White[10]; Valentina Sola[12]; Giovanni Paternoster[6]; Arianna Morozzi[13]

[1] *INFN*

[2] *Torino University and INFN*

[3] *UPO - INFN*

[4] *Politecnico di Milano*

[5] *FBK Trento*

[6] *Fondazione Bruno Kessler*

[7] *INFN Sezione di Perugia, Perugia, Italy*

[8] *CNR-IOM and INFN, Perugia*

[9] *Torino University*

[10] *Univ. of Torino - INFN*

[11] *University and INFN Perugia*

[12] *INFN Torino (IT)*

[13] *Istituto Nazionale di Fisica Nucleare (INFN)*

Auteur correspondant matteo.durando@edu.unito.it

Precise tracking in space and time is becoming a more and more pivotal ingredient in designing high-energy physics experiments. Low-Gain Avalanche Diodes (LGADs) with an active thickness of $\sim$ 50 µm have proved the ability of silicon sensors to provide precise timing down to about 30 ps. At present, this timing performance is maintained almost unchanged up to a fluence of $2.5{\cdot}10^{15}$ 1 MeV equivalent n/cm^2. Thinner substrates can further improve the timing resolution and the radiation tolerance of the LGAD sensors.

At the end of 2022, FBK released a batch of thin LGAD sensors with an active thickness between 15 and 45 μm to investigate the effect of the thickness in improving sensor performances.

A new design of the sensor layout and periphery has been studied and realised, optimised for the sensor thickness and the requirement to withstand high electric fields up to very high fluences.

The state-of-the-art design of the LGAD gain implant from FBK has been used on thin substrates, exploiting the concurrent implantation of boron and carbon atoms in the multiplication region typical of LGAD sensors. This resulted in the most radiation-tolerant LGADs ever produced by FBK.

The electrical characterisation of sensors before and after irradiation, together with the analysis of the signals from laser stimulus and charged particles, will be presented. The impact of the sensor thickness on the collected charge and the timing resolution will be explored and discussed.

Posters / **105**

TCAD and charge transport simulations of MAPS in 65nm for the ALICE ITS3

Auteur: Isabella Sanna[1]

[1] *CERN*

Auteur correspondant isabella.sanna@cern.ch

The Inner Tracking System 3 (ITS3) is the new vertex detector proposed for the upgrade of the ALICE experiment at CERN planned for the LHC long shutdown 3. It will consist of bent, wafer-scale monolithic pixel sensors manufactured in the TPSCo 65 nm process, reducing the material budget to an average of 0.9%X0 and the innermost layer's radius to 19 mm. These improvements will double the impact parameter resolution at 1 GeV/c transverse momentum. In the context of this upgrade, several sensor prototypes designed in a 65nm technology were produced and tested. A significant aspect of this characterization involved laboratory measurements using radioactive sources, with the 55Fe source being extensively employed. The study of these spectra enabled the evaluation of the charge collection performance of these chips, playing a crucial role in validating this technology for ITS3.

While the radiation hardness requirement for ITS3 (1013 1 MeV neq cm−2) has been fully met, higher levels of irradiation result in a degradation on the 55Fe spectra which remain to be not entirely understood. Irradiation can have various counteracting effects on silicon sensors, such as carrier trapping and doping reduction. In view of future designs, it is crucial to understand the role these effects play in the performance degradation.

To comprehensively understand this, simulating the charge transport mechanisms within these sensors is of fundamental importance. The 55Fe X-ray spectrum is used as reference for these simulations because its precise reproduction is very sensitive since it is not affected by large Landau fluctuations that are inherent to MIPs.

To achieve this kind of simulation, TCAD tools were utilized to model the electric field within the sensor, and Garfield++ was employed to simulate the charge transport and collection mechanisms.

This presentation will highlight the importance of these simulations and the tools employed. It will showcase the algorithms used to simulate the x-rays response and present comparisons with data for both non irradiated and highly irradiated chips.

Timing with pixels / **106**

New developments in 3D-trench electrode sensors

Auteurs: Jixing Ye[1]; Maurizio Boscardin[2]; Matteo Centis Vignali[3]; Francesco Ficorella[3]; Omar Hammad Ali[3]; Adriano Lai[4]; Angelo Loi[5]; Francesca Mattedi[6]; Laurea Parellada Monreal[6]; Sabina Ronchin[6]; Gian-Franco Dalla Betta[7]

[1] *Università di Trento e TIFPA*

[2] *FBK Trento*

[3] *Fondazione Bruno Kessler*

[4] *INFN*

[5] *INFN Cagliari*

[6] *FBK*

[7] *University of Trento and TIFPA INFN*

Auteur correspondant jixing.ye@unitn.it

Future experiments at high-luminosity hadron colliders will involve unprecedent levels of pile up, calling for precise time information at the pixel level to ease distinguishing between particle tracks. The unique geometry of 3D sensors enables to achieve very good timing performance, besides high radiation hardness. Remarkable results in terms of timing resolution have so far been reported for 3D sensors with columnar electrodes (~30 ps) [1] and even better with trenched electrodes from the INFN TIMESPOT project (~10 ps) [2], owing to a more uniform distribution of the electric field and weighting field. However, 3D-trench technology is more complex, and has still to be optimized. To this purpose, a new batch of sensors was designed at the University of Trento and fabricated at FBK

within the AIDA Innova project.
Figure 1(a) shows the reticle layout, including pixel sensors and test structures (top right corner). The baseline pixel size is 55x55 μm^2, whereas a smaller version of 42x42 μm^2 has been introduced in test structures. Pixels come with two design variants for the ohmic trenches, either continuous (STD) or dashed (DSH). The former was already tested in the TIMESPOT batches, whereas the latter is new and aims at improving the fabrication yield. The performance of the two designs has been investigated by TCAD and AllPix2 simulations and found to be comparable [3]. Three different array sizes are present: 128x128, 64x64, and 32x32. The larger sensors are intended for future Read-Out Chips (ROCs) of the IGNITE (INFN) and Picopix (CERN) types, whereas the smaller ones are compatible with existing ROCs from the TIMESPOT project. Compared to previous productions at FBK, the batch has been processed with an improved technology aimed at increasing the yield and the number of devices on wafer. Figures 1(b) and 1(c) show the two reticle exposure plans used in the batch, featuring 18 and 29 printed blocks, respectively. Compared to just 11 blocks printed in the TIMESPOT2 batch, the device density is now much larger. Through the process, the wafer warp has been continuosly monitored, and a sufficiently low warp of ~80 μm has been measured at the end of the process also in case of the very dense wafer layout.
The batch was completed in June 2024 and initial electrical tests were performed on automatic probe station using a temporary metal layer. As an example, Figure 2 shows the total leakage current vs. reverse voltage curves measured on the larger pixel sensors of wafer 13 (18 reticle blocks). Most sensors have low leakage current, in the range of a few nA, and breakdown voltage higher than the measurement limit of 100 V, that is promising in view of functional tests.

[1] L Diehl et al., J. Instrum 17 (2022), C12003
[2] F Borgato et al., Front. Phys. 12 (2024) 1393019
[3] J Ye et al., J. Instrum 18 (2023), C11021

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Monolithic sensors / 108

Development of a high gain and high MTF CMOS electron detector for transmission electron microscope (TEM)

Auteur: olivier Marcelot[1]

Co-auteur: Cécile Marcelot [2]

[1] *ISAE-SUPAERO*

[2] *CEMES-CNRS*

Auteur correspondant o.marcelot@isae.fr

Last advanced TEM techniques are dedicated to the observation of sensitive materials which can be damaged with the electron dose, such as biological specimen. In this situation it is mandatory to use a low dose and conventional beam energies (200keV). Consequently, electron detectors need to have a gain as high as possible while maintaining high spatial resolution performances. Nowadays, camera providers propose CMOS image sensors for the direct detection of electrons with optimizations focused on the improvement of spatial resolution, only demonstrated at 300kV [McMullan2009]. Indeed, one big issue with TEM detectors is the large spread of the electron distribution in the silicon substrate, greater than the pixel size, which induces a bad spatial resolution. Thus, one solution chosen by camera providers is to back-thin the substrate. However, the drawback is a strong reduction of the gain. One other big issue is the strong ionizing dose imposed by the experiment, which require to use specific hardening by design pixels, based on 3T (3 transistors) architectures.

In this study, Technology Computed Aided Design (TCAD) simulations are used to determine the best substrate characteristics (thickness, doping concentration) leading to a high detector gain and a high detector spatial resolution estimated by means of the MTF, for beam energies equal or lower to 200keV. Actually, state of the art cameras have a gain in the range of 50. The goal is therefore to

develop a detector with a gain higher than 100 while keeping similar MTF performances compared to state of the art detectors.

TCAD simulations are performed with the Synopsys software with a special method based on two optical illuminations demonstrated in a previous work [Marcelot2023] (see the Fig.1). Then, several substrates are used and the gain is simulated in 3 dimensions (3D), while the MTF is extracted from a 2D simulation of the line spread function acquired on 11 pixels. Substrates are defined by:
- doping concentration ranging from 10^12B/cm2 to 10^15B/cm3
- epitaxy thicknesses ranging from 7µm to 30µm on un-thinned substrates and back-thinned substrates.

With un-thinned substrates, the simulations are showing a gain 3 times higher compared to state of the art camera for most of the substrate doping concentration. The drawback is a weak MTF, but it is shown that it can be improved by using low doped 7µm epitaxies, because of a better lateral collection of electrons induced by a larger depleted region. Therefore, at 200kV, a higher gain and MTF is demonstrated compared to state of the art cameras.
With back-thinned substrates, the gain is strongly reduced due a the reduction of the sensitive volume. In addition, and in contrary to a previous study performed at 300kV [McMullan2009], it is shown that the MTF is degraded with 200kV and 150kV electron beams. This unexpected result is due to the fact that a lower beam energy induces much more electrons in the epitaxy and the reduced volume of silicon cannot efficiently recombined the electron excess which diffuses to adjacent pixels and reduce the MTF.

Posters / **111**

A Column-level ADC designed to CMOS image sensors

Auteurs: Guangming Huang[1]; Haowei Xiong[1]; Kai Jin[1]; Ping Yang[1]; Xiangming Sun[1]; Xianzhen Wang[1]; Yifan Wang[1]; Yunqi Deng[1]

[1] *Central China Normal University*

Auteur correspondant pingyang@ccnu.edu.cn

Due to their advantages of fast readout rate, high integration and low power consumption of CMOS image sensors, they have been widely used in medical imaging, security monitoring, and space X-ray detection. As an important part of CMOS image sensors, the performance of analog-to-digital converters (ADCs) directly affects the quality of imaging. In large-area and high-speed CMOS image sensors, ADCs are usually arranged in a column-level readout mode. The traditional structure is a single or dual slope ADC, which is not fast enough. This work is to research and design a 12-bit 5MS/s low-power Cyclic ADC using 180nm process.
The ADC adopts a SHA-less front-end sample-and-hold structure, which reduces sampling time, saves power consumption and area. Each working cycle adopts 1.5bit MDAC, where 1 bit is the effective bit and 0.5bit is the redundant correction bit.
In order to reduce the impact of the offset voltage of the comparator, the sub-ADC uses a pre-amplified large latched dynamic comparator, embeds an automatic zeroing technology.
The overall post-simulation results show that, when the sampling rate is 5MS/s, the input signal frequency is 300KHz, the input range is 0.4V~1.4V, the SNR of the Cyclic ADC is 70.4dB, the SFDR is 79.3dB, the THD is -77.8dB, and the ENOB is 11.28bit. The chip is under testing now, test results will be presented then as well.

Electronics / **112**

Rapid prototyping platform for highly segmented detectors

Auteurs: Dominik Gorni[1]; Giovanni Pinaroli[1]; Grzegorz Deptuch[2]; Piotr Maj[1]; Timothy Kersten[1]

[1] *Brookhaven National Laboratory*

[2] *BNL*

Auteur correspondant pmaj@bnl.gov

We present the design and implementation of a comprehensive testing setup for validating pixelated detectors, emphasizing rapid prototyping and minimizing printed circuit board design and debugging efforts. The system features an off-the-shelf embedded controller with an Intel CPU running under LinuxRT, paired with an Artix 7 FPGA. This FPGA supports both VHDL and LabVIEW code, enhancing setup preparation and testing efficiency, particularly for pixelated structures. We will present results obtained with the presented circuits to demonstrate developments of the integrated circuits, interfaces and external readout and processing hardware.

We discuss the overall concept and the realization of three distinct systems: an asynchronous event-based readout interface (EDWARD), the hexagonal-shaped pixelated detector readout IC (HEXID), and a Full Field Fluorescence Imaging (3FI) pixelated hybrid detector readout IC. The proposed systems consist of programmable voltage reference sources, power supply stages, and high-speed, 16-channel, 14-bit ADCs sampled at 65MHz. These systems are optimized for low noise and high sampling rates, resulting in over a 10Gbps data stream processed in the FPGA for feature extraction.

All presented solutions are pixelated structures. The EDWARD IC enables the verification of an event-driven readout, controlled by an I2C interface, with data generated inside each channel streamed out using an encoded digital protocol. Similar methods are further utilized in HEXID and 3FI—pixelated CZT hybrid detector readout integrated circuits. The setup is designed to facilitate fast prototyping, significantly enhancing performance, development speed, and the efficiency of validating various pixelated detector technologies.

In addition to the technical components, the setup incorporates modular design principles, allowing for easy reconfiguration and scalability. This flexibility ensures that the system can be adapted for a wide range of testing scenarios, from initial prototyping to final validation stages. By leveraging these innovative components and design strategies, our testing setup stands out as a crucial tool for advancing the development and validation of next-generation pixelated detectors.

Astrophysics applications / **114**

AstroPix: Low power high voltage CMOS active pixel sensors for space and collider experiments

Auteur: Manoj Jadhav[1]

[1] *Argonne National Laboratory*

Auteur correspondant mjadhav@anl.gov

High voltage CMOS (HV-CMOS) sensors are novel monolithic CMOS active pixel sensors designed for future particle tracking detectors satisfying exceptional performance requirements. These sensors have the advantages of a fully monolithic structure, low manufacturing cost, low material budget, fast charge collection, and high radiation tolerance. Derived from ATLASPix3 (for High-Luminosity Large Hadron Collider), AstroPix is an HV-CMOS monolithic silicon sensor designed using a 180 nm CMOS process for NASA's AMEGO-X (All-sky Medium-Energy Gamma-ray Observatory eXplorer) mission concept, a low-orbit medium energy gamma-ray observatory for multi-messenger astrophysics.\\
\noindent To ensure high precision and sensitivity, a next-generation Pair/Compton telescope (ComPair2 prototype for AMEGO-X) targeting a medium-energy (MeV) γ-ray from extreme explosions and accelerators requires detectors with good energy and position resolution in three dimensions with a low energy threshold. AstroPix provides low-power operation with large sensitive areas, low noise, wide dynamic range, and good energy/spatial resolution. These features synergies with an electromagnetic shower environment. Consequently, AstroPix is the baseline silicon sensor for the imaging part in the barrel imaging calorimeter (BIC) for the Electron-Proton/Ion Collider experiment (ePIC) at the Electron-Ion Collider (EIC). At AMEGO-X, 40 tracking layers with a total area of 40 m^2

are designed with AstroPix sensors. The prototype tracker detector, ComPair2, comprising 10 layers of AstroPix, will be integrated next year. Whereas imaging layers in the BIC at ePIC cover an area of over 100 m^2. The speaker will describe the integration of the AstroPix MAPS sensor in the ComPair2 prototype for AMEGO-X and BIC at ePIC. The presentation will highlight the characterization and performance evaluation results of the AstroPix sensor.

Posters / **115**

Ghosts as self-sustained avalanches in Ti-LGADs with different self-quenching times: Linking experimental data, hypotheses and simulations

Auteurs: Gordana Lastovicka Medin[1]; Vagelis. Gkougkousis[None]; Gregor Kramberger[2]; Mateusz Rebarz[3]

[1] *University of Montenegro*

[2] *Jozef Stefan Institute*

[3] *ELI ERIC, ELI Beamlines*

Auteur correspondant gordana.lastovicka.medin@cern.ch

In this presentation we will show results from our comprehensive study on inter-pixel region in trench-isolated Low Gain Avalanche Detectors. The focus will be on recently observed atypical self-induced signals with extremely large amplitude that are also very extended in time. We will be comparing the results from study on Trenched LGADs with results from study on Trenched PINs. We will be also showing the results obtained on irradiated samples. We will offer some hypotheses that will be tested using simulation tools.

HEP experiments / **116**

Entering a New Era of Innovation in Semiconductor Technologies with Increased Interdisciplinary Synergies for Advanced Compute Scaling

Auteur: Anabela Veloso[1]

[1] *IMEC, Leuven*

Auteur correspondant anabela.veloso@imec.be

The need for increased computing keeps growing at ultra high speed, required to support an ever larger and wider range of applications, with generative AI significantly accelerating this trend. Logic standard cell shrinkage remains at the core of the compute roadmap. Its momentum is expected to carry on, even as 2D scaling has become increasingly challenging, by introducing novel device architectures, new materials, scaling boosters like backside (BS) power delivery (PD) with its significant benefits for power integrity, and an overall increased use of design-technology co-optimization (DTCO)-driven design improvements.
A key support pillar of the roadmap remains continued dimensional scaling, enabled by progressive advances in holistic patterning which increasingly rely on the use of extreme ultraviolet (EUV) lithography (evolving into high numerical aperture (NA) EUV lithography) to obtain cost-effective scaling and considerably lower energy consumption. At transistor level, nanosheet (NS)-based FETs are taking the central stage, first as single-level devices consisting of several vertically stacked NS per structure, and potentially evolving into 3D stacked configurations like the so-called complementary FET (CFET) for which several options may be possible regarding the materials and crystal orientations of the stacked channels. Moreover, changes in how the devices are connected, as they become sandwiched and accessed from levels above and below them, also allow interesting new opportunities for device engineering and circuit design. Exploring further the third (vertical) dimension is,

in fact, a common current trend of both logic and memory roadmaps, with new options feasible to envision thanks to the recent advances in bonding, 3D and photonic technologies which are allowing new connectivity possibilities besides the typical on-chip interconnects at system-on-chip (SoC) level. That is enabling a system (r)evolution towards smart partitioning, wherein, looking ahead, compute systems have the potential to be assembled in ways enabling much more versatile, hybridized platforms for enhanced system performance. Such scenario is becoming possible thanks largely to an increased embrace of the use of both wafer sides, 3D stacking and sequential integration, together with an overall leveraging of the unique capabilities of different technologies like logic, memory, and 3D under the umbrella of system-technology co-optimization (STCO). The latter' s adoption is instrumental in driving the proposal and evaluation of new technology options tailored to the specific requirements of different applications such as mobile, GPU, server or wearables.
This presentation aims to highlight and discuss some of these key advances, including challenges and opportunities, occurring in the area of advanced compute/logic scaling, wherein exciting, sustainability-aware innovations with increased interdisciplinary synergies are shaping the roadmap ahead.

Posters / 117

Recent test beams results of ATLAS ITk pixel modules

Auteurs: Martina Resegotti[1]; Md Arif Abdulla Samy[2]

[1] *INFN, Genoa*

[2] *University of Glasgow*

Auteur correspondant md.arif.abdulla.samy@cern.ch

The ATLAS inner detector will be completely replaced to cope with the increased occupancy, bandwidth and radiation damage that will be posed by the High Luminosity phase of the Large Hadron Collider. The new all-silicon Inner Tracker (ITk) will be equipped with pixel detectors in the innermost part, using several silicon sensor technologies equipped with novel ASICs connected by bump-bonding technique.
n-in-p planar hybrid modules 100 μm and 150 μm thick will instrument the four outer layers of the pixel detector. Due to their radiation hardness, 3D sensors will be installed in the innermost layer, where a fluence up to 2 e16 neq/cm2 is expected. Their production is distributed among different vendors, and the pre-production sensors from each vendor are progressively being tested before and after irradiation with test beams. The most recent results will be presented.

Posters / 118

X-ray Irradiation Campaigns of the Monopix depleted monolithic active pixel sensors

Auteurs: Lars Schall[1]; Lars Schall[1]

[1] *University of Bonn*

Auteurs correspondants: lars.schall@uni-bonn.de, lschall@uni-bonn.de

Monolithic active pixel sensors with depleted substrates present a promising option for pixel detectors in high-radiation environments. Leveraging high-resistivity silicon substrates and high bias voltages in commercial CMOS technologies facilitates depletion of the charge sensitive volume. This enhances the radiation tolerance and charge collection capabilities to meet the demands of such environments. TJ-Monopix2 and LF-Monopix2 are the most recent large-scale chips in their respective development line, originally designed for the ATLAS Inner Tracker outer layer environment.
LF-Monopix2 is designed in 150 nm LFoundry CMOS technology and integrates all in-pixel electronics within a large charge collection electrode relative to the pixel pitch of 50x150 μm2. This approach

facilitates short drift distances and a homogeneous electric field across the sensor. The resulting sensor capacitance of approximately 250 fF compromises the noise performance requiring more analog power for optimal operation. The pixel layout has been optimized to minimize potential cross-talk from digital circuitry to the sensor node. LF-Monopix2 wafers have successfully been thinned-down to 100 um and backside processed.
TJ-Monopix2 is designed in 180 nm TowerJazz CMOS technology and features a small charge collection electrode, which requires the separation of the in-pixel electronics into p-wells. Process modifications in form of an additional n-type implant minimize regions with low electric field and improve the charge collection efficiency impaired by the long drift distances. The small pixel size of 33x33 μm2 reduces the detector capacitance to approximately 3 fF enhancing noise and power performance.
This contribution focuses on the performance of both Monopix2 chips after X-ray irradiation. Latest laboratory and beam test measurements are presented.

Sensing materials & Radiaiton tolerance / **119**

Wide band-gap material sensors for applications in high energy physics experiments

Auteur: Alexander Oh[1]

[1] *University of Manchester*

Auteur correspondant alexander.oh@cern.ch

In this presentation the latest developments on detectors made of wide-band-gap materials for applications in high energy physics experiments will be discussed. In particular the status of SiC, GaN and Diamond based detector developments will be reviewed and the plans of the newly formed DRD3 collaboration with it's focus on wide-bandgap materials in working group 6 will be presented.

Silicon Carbide (SiC) is a wide bandgap semiconductor known for its exceptional properties, making it a promising material for radiation particle detection. The presentation will give an overview of the advantages of SiC detectors and the current research progress in this area, with emphasis on the latest experimental results on SiC diodes for detecting ionising radiation and the status of developing LGAD structures to increase the signal yield. The status of radiation damage on detector performance and simulation effort will be also discussed.

GaN is wide-bandgap semiconductor which is overcoming Si in high-power, high-temperature switching applications and thus is of great interest to industry. It offers a large bandgap and high atomic bond energy which makes it an attractive candidate for a sensor material at extreme fluences. First studies with GaN Schottky diodes in the framework of the RD50 collaboration have been undertaken and are presented.

Diamond has the largest band-gap with about 5.5eV of the wide-bandgap materials discussed here. There is no need to create a depletion zone by doping and reverse-biasing as in the case for e.g. Silicon. Diamond as sensor material is well established and used in the experiments at Tevatron and LHC, and the LHC itself primarily for beam monitoring applications. The radiation tolerance was tested with protons, pions and neutrons, and a radiation damage model was developed. The radiation studies indicate that the 3D diamond detector shows superior radiation hardness compared to planar diamond detectors. The recent progress in planar diamond and 3D diamond detectors and future applications will be discussed, primarily based on the effort of the RD42 collaboration.

Acknowledgements: The majority of the work presented has been conducted within the context of the CERN Detector R&D collaboration RD42 and RD50.

Sensing materials & Radiaiton tolerance / **120**

Realistic Monte Carlo simulation of silicon particle detectors for timing and tracking with Garfield++

Auteur: Marco Mandurrino[1]

[1] *INFN Torino*

Auteur correspondant marco.mandurrino@to.infn.it

Simulation-guided design represents a fundamental contribution towards the development of modern semiconductor devices aiming to reach high-performance particle detection, identification and tracking, and constitutes a strategic element of the new detector R&D roadmap.
At the same time, the complexity of microelectronic structures and the related detection systems is drastically increasing, also thanks to the progressive scaling down of the design rules with the process technology.
Owing to the capability to embed a detailed description of the ionisation mechanism into a device-level framework, as well as capture the stochastic nature of signal formation, the Monte Carlo (MC) approach has become the most recommended strategy to achieve reliable predictions of the dynamic properties of particle detectors in realistic settings such as in-beam experiments.
In my contribution I will give an overview of the key aspects characterizing MC tools, with special mention to the Garfield++ simulation toolkit.
To this aim, I will go through the analysis of some specific case studies concerning the design of silicon particle detectors for timing and 4D-tracking in present and future high-energy physics experiments, presenting the comparison between measured and simulated figures of merit and highlighting strengths and open challenges of such approach.
The examples are intentionally chosen among the family of Monolithic Active Pixel Sensors because it represents one of the most promising and topical frontiers in particle detection and because the CMOS monolithic integration offers the widest workbench possible to test the robustness of the numerical design.

Timing with pixels / **121**

Time-stamping photons with sub-nanosecond resolution for quantum-enhanced imaging and telescopy

Auteur: Andrei Nomerotski[1]

[1] *Czech Technical University in Prague*

Auteur correspondant andrei.nomerotski@cvut.cz

Correlations of photons from entangled quantum sources offer advantages and provide additional opportunities such as low light imaging or new sensing approaches. In general, strong spectro-temporal correlations inherent for entangled photons make those sensing techniques much more precise and resource efficient. To take advantage of the correlations one would need efficient single photon imagers with excellent timing resolution. In the presentation I will review the existing detector options focussing on the time-stamping CMOS and SPAD cameras, which have been used recently in a variety of quantum imaging experiments, in particular the Tpx3Cam and LinoSPAD2 cameras, both based on data-driven readouts. As a motivation for fast imaging in astrophysics I will also review the standard techniques of single-photon amplitude (Michelson) interferometry and two-photon (Hanbury Brown & Twiss) intensity interferometry, and then visit recent ideas for how they can be improved in the optical through the use of entanglement distribution. A proposed new technique of two-photon amplitude interferometry requires precise spectral binning and 10 picosecond scale time-stamping of single optical photons with a product of resolutions close to the Heisenberg Uncertainty Principle limit. Another prominent example of multi-dimensional quantum correlations is the parametric down-conversion of x-rays in diamond. In this case all three types of correlations, in momentum, energy and time, can be measured simultaneously. In all cases I will illustrate the concepts with recent results and will discuss future directions for the technology.

[1] A. Nomerotski, "Imaging and time stamping of photons with nanosecond resolution in Timepix based optical cameras,"Nuclear Instruments and Methods A: 937, 26 (2019).
[2] Y Zhang, D England, A Nomerotski, B Sussman, "High speed imaging of spectral-temporal correlations in Hong-Ou-Mandel interference," Opt. Express 29, 28217 (2021).
[3] P Stankus, A Nomerotski, A Slosar, S Vintskevich, "Two-photon amplitude interferometry for precision astrometry"; Open Journal of Astrophysics 5 (2023).

[4] T. Milanese et al. "LinoSPAD2: an FPGA-based, hardware-reconfigurable 512×1 single-photon camera system." Optics Express 31.26 (2023): 44295.
[5] J.Jirsa et al. "Fast spectrometer near the Heisenberg limit with direct measurement of time and frequency for multiple single photons." arXiv:2304.11999 (2023).
[6] J.Goodrich et al, "Imaging of X-ray Pairs in a Spontaneous Parametric Down-Conversion Process,"arXiv:2310.13078 (2023).

Monolithic sensors / **122**

Enhancing Sensor Readout Efficiency: Innovations and Challenges

Auteur: Grzegorz Deptuch[1]

[1] *BNL*

Auteur correspondant gdeptuch@bnl.gov

The increasing segmentation of sensors, especially in tracking and vertexing applications, along with the drive to reduce the material budget, necessitates that processing of charge signals from sensors through amplification, filtering, extraction of amplitude, time of occurrence, as well as of additional features, such as particle trajectory direction and type identification, be confined to ever-smaller areas on readout integrated circuits. The circuit networks that transmit information about detected events from radiation interactions with the sensor material to an external data acquisition system compete for the space needed for implementing relevant circuit networks. Both signal processing from radiation interaction events and information extraction aims at minimization of power dissipation, reduction of interference-causing activities, and ensuring low latency.
The human eye is the most efficient biological system operating in the mentioned manner. Optic nerves extending from the retina in parallel transmit highly efficiently encoded data from each light sensitive element to the brain for parallel processing. How the eye achieves its biological efficiency is not understood, and the eye remains an unattainable model for human-built readout detector systems. However, numerous efforts aim to bring readout methods closer to this ideal.
Over the years, technological miniaturization, reflected in node dimensions decreasing from 1 micron in the early nineties to 28 nm today, could have enabled fitting parallel readouts by increasing the density of readout electronics. However, this technological gain has been largely consumed by the miniaturization of individual channel sizes and implementations of additional advanced functionalities, primarily enhancing the performance of front-end blocks through digital assistance in correcting process variabilities, rather than easing the readout.
In radiation detector systems, sensor matrix data are typically transmitted to the periphery before being sent to the data acquisition system. This periphery-oriented approach applies regardless of whether all data or only trigger-confirmed data are read, whether empty data are removed or compressed in the readout circuits, or whether data are read continuously or selectively. The main difficulty is ensuring that the data transmission link, with its bandwidth optimized to match the combined event information generation from the channels it serves, transmits data without losing time slots (which would otherwise carry empty data). This must be done without collisions and, most importantly, by allocating transmission rights to individual channels based on their need for service.
Upon closer examination, all the readout methods to be presented fall into the category of Address-Event Representation, differing in address generation, address information coding, latency, and whether readout is framed or frameless. The presentation will start with simple x-y readouts like Delphi pixel, then move to polling methods such as token passing/token rings used in current LHC detector systems and similar setups. It will then cover framed methods with self-identification of channels for readout using various priority encoder schemes, and finally address frameless methods within neuromorphic engineering. In the latter, the discussion will start with globally asyn-

chronous, locally synchronous systems, including arbitration issues, and provide examples of fully event-driven, collision-free readouts. This comprehensive review will enable a broader discussion based on collected material.

Astrophysics applications / **123**

Pixel sensors for ground and space astronomical observatories

Auteur: Claire JURAMY-GILLES[1]

[1] *{CNRS}UMR7585*

Auteur correspondant claire.juramy@lpnhe.in2p3.fr

Pixel sensors will face new challenges to provide the enhanced performances required by the next generation of ground and space astronomical observatories. Dedicated pixel CMOS sensors are now competing with the traditional CCD designs, offering opportunities for new readout methods. On the other hand, the study of CCD sensor characteristics allows to reach the precision required by surveys like the Legacy Survey of Space and Time, and new developments in CCD designs promise improvements in both readout noise and readout speed. In the near infra-red, several high-profile current and next-generation projects rely on hybrid detectors, a technology which still presents significant challenges for precision measurements.

Medical imaging applications / **124**

CMOS image sensors for scientific, medical and life science applications

Auteur: Renato Turchetta[1]

[1] *IMASENIC Advanced Imaging S.L.*

Auteur correspondant renato.turchetta@imasenic.com

CMOS image sensors nowadays the dominant imaging technology, are being deployed in many applications, from consumer to machine vision, from industrial to automotive. They are now also used in scientific as well as medical and life science. In these fields, the requirements can be as varied as very low noise for scientific applications, or area coverage for medical and speed for life science. In this talk we will review the status of the CMOS technology in general, before focusing on the requirements on the applications listed in the title. The status of scientific CMOS image sensors, often referred to as sCMOS, will be reviewed. For medical and life science, we will focus on the state of the art for wafer-scale sensors, reviewing the performance of existing sensors and going beyond what exists today to look at future trends of these type of sensors.

Welcome / **126**

Welcome address

Auteur correspondant luc.hebrard@unistra.fr

Welcome / **127**

Practical info

Auteur correspondant baudot@in2p3.fr

Farewell / **128**

Proceeding instructions & Acknowledgement

Auteur correspondant baudot@in2p3.fr

Farewell / **129**

Announncement for Pixel 2026

130

Info for excursion

Auteur correspondant baudot@in2p3.fr