NEGMA- Demonstrator

An RFSoC FPGA Development

A. BOUJRAD

PHY/GTA/GANIL

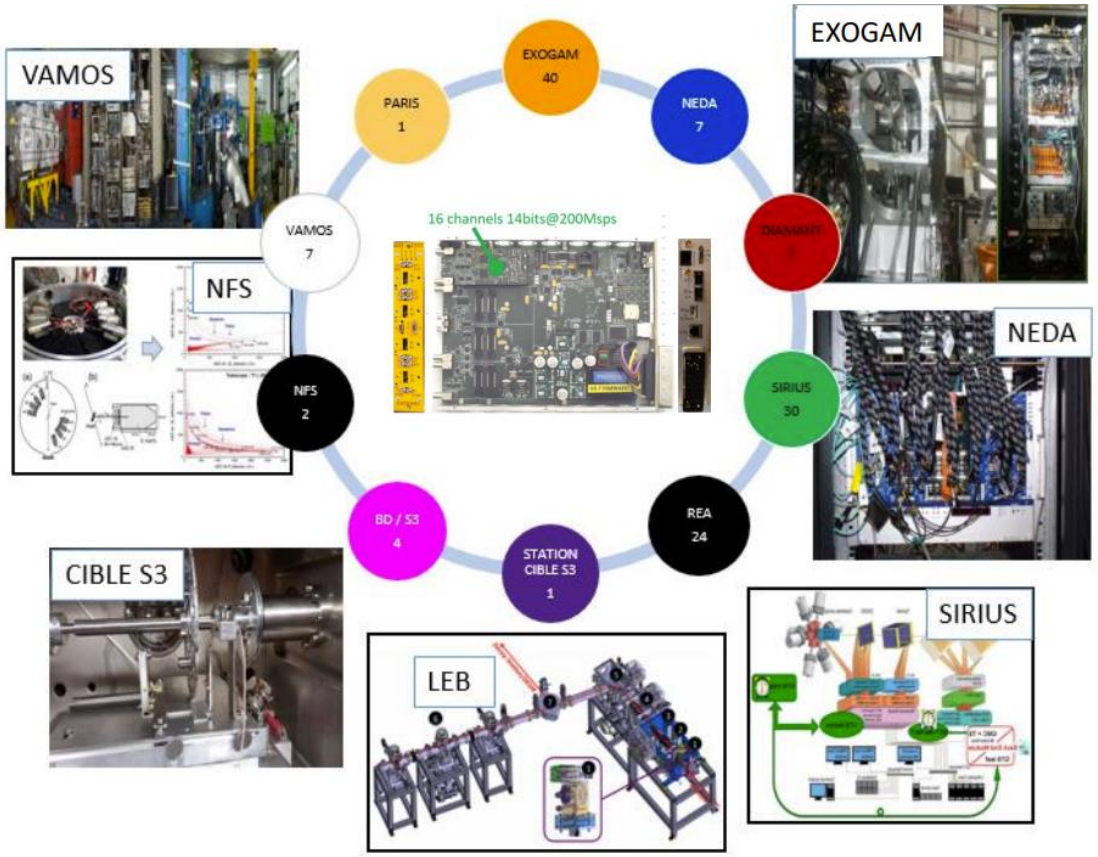
Demonstrator Local Team

Hardwre : *A. Boujrad, C. Houarner, M. Blaizot, P. Bourgault, M. Bezard*

Software : *L. Legeard, S. Coudert, S. Rabahia(apprentice)*

- Introduction
- ZCU216 Evaluation Kit as a demonstrator
- NEGMA General Overview
- Conclusion

Present Digitizer: NUMEXO2



- Dedicate to EXOGAM => Extended to Other detection systems
  - *NEDA, DIAMANT, SIRIUS, VAMOS NFS…*
  - *128 Modules manufactured*
  - *Used on several experiments : VAMOS, Lise2022/2023, NFS….*
- Status
  - *Icreased needs (Expeiments and Setup)*
  - *No possibility to re-manufacture => components and tools obsolescences*
  - *No more possible Evolution => Firmware limitation Ressources*

Futur Digitizer : NEGMA + REActif

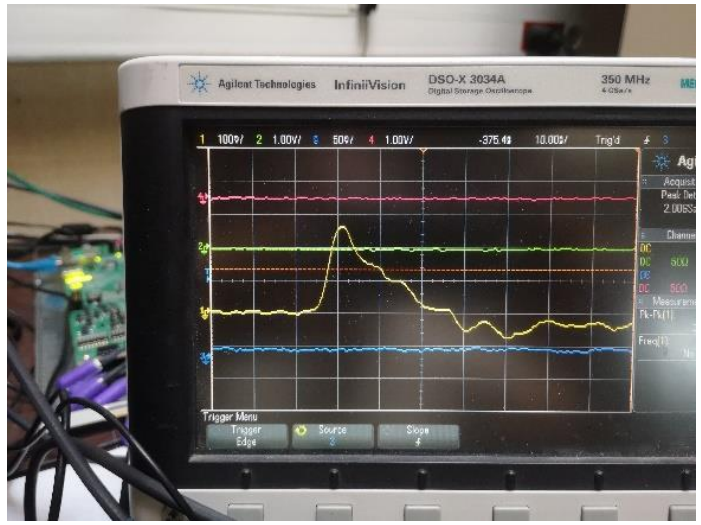
NEGMA

NEw **G**eneration of **M**ultifunction **A**dcs

REActif

- New Generation of RFSoC/FPGA
  - 16 Channels (14bits @2.5 Gsps), *Integrated ADCs & DACs*
- High resolution Scope & More complex algorithms
  - *Deported Digital Signal Processing with GPUs on REActif*
- Gb Ethernet data transmission

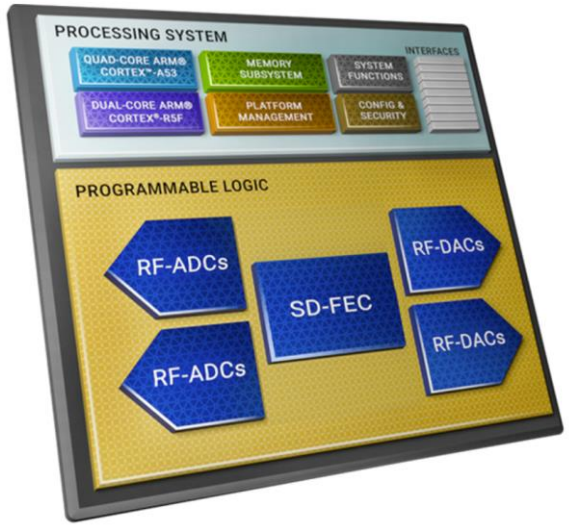
Introduction



NEEDS

1- Fast signal measurements ***(ns)***
2- Fast data transmission ***(1 à 10 GEth)***
3- Complex algorithms in remote location
4- SMART TimeStamping integration

ZYNQ RFSoC



Our Proposal

1- *14bits @ 2.5 GHz* ADCs & *14bits @ 9.85 GHz DACs*
2- Optical data links (up to *10 Gbits per link*)
3- Massively parallel computing via external GPU *(REACTif)*

Kits & Commercial modules

PENTEK
Now Part of Mercury

vadatech
THE POWER OF VISION

HITECH GLOBAL

Abaco SYSTEMS

TELEDYNE
SP DEVICES
Everywhereyoulook

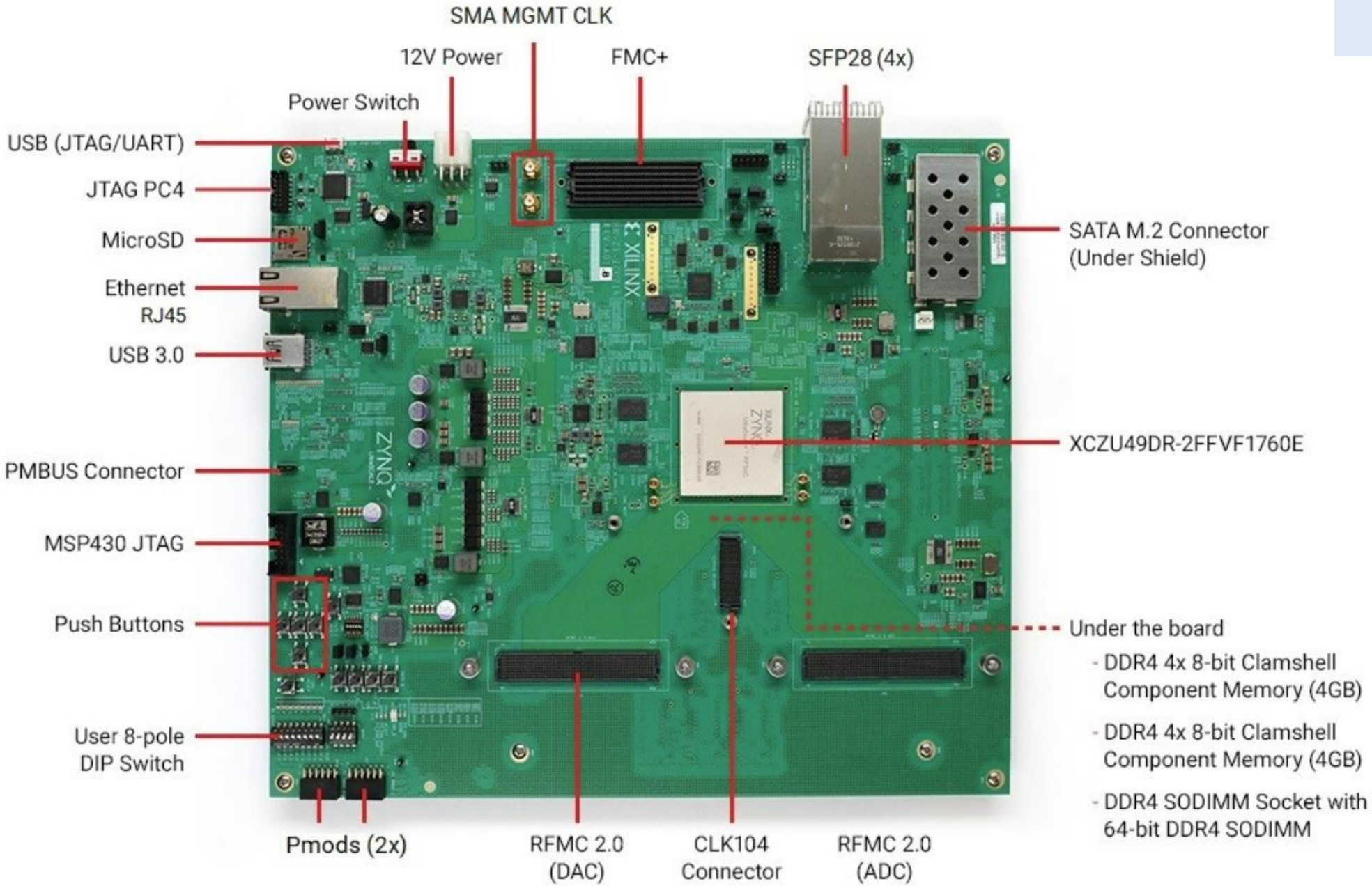
Zynq® UltraScale+™ RFSoC Boards & Kits Portfolio

Gen 1 4GHz			Gen 2 5GHz	Gen 3 6GHz	
ZCU111 Evaluation Kit	Avnet RFSoC Kit Development Kit	ZCU1275 Characterization Kit	ZCU1285 Characterization Kit	ZCU208 Evaluation Kit	ZCU216 Evaluation Kit
					
ZU28DR	ZU28DR	ZU29DR	ZU39DR	ZU48DR	ZU49DR
Application Development and Performance Evaluation of: **ADCs**: 8x 12-bit 4.096GSPS **DACs**: 8x 14-bit 6.554GSPS **SD-FEC**: 8	**Wireless Application Development Leveraging:** **Xilinx** ZCU111 Evaluation Kit **Avnet** Qorvo 2x2 Small Cell RF Front End 1.8GHz Card **Avnet** RFSoC Explorer with MATLAB and Simulink	**Ideal for Tone Testing and Data Sheet Verification of:** **ADCs**: 16x 12-bit 2.058GSPS **DACs**: 16x 14-bit 6.554GSPS	**Ideal for Tone Testing and Data Sheet Verification of:** **ADCs**: 16x 12-bit 2.220GSPS **DACs**: 16x 14-bit 6.554GSPS	**Application Development and Performance Evaluation of:** **ADCs**: 8x 14-bit 5.0GSPS **DACs**: 8x 14-bit 10.0GSPS **SD-FEC**: 8	**Application Development and Performance Evaluation of:** **ADCs**: 16x 14-bit 2.5GSPS **DACs**: 16x 14-bit 10.0GSPS
XILINX	AVNET	XILINX	XILINX	XILINX	XILINX

AVNET

KNOWLEDGE RESOURCES
Switzerland GmbH

ZCU216 Description



FPGA_RFSOC Familly

Zynq® UltraScale+™ RFSoCs

Section	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	ZU65DR	ZU67DR
		Gen 1					Gen 2	Gen 3						DFE	
PS		**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz													
RF Data Converter	12-bit RF-ADC w/DDC # of ADCs	0	8	8	8	16	16	–	–	–	–	–	–	–	–
RF Data Converter	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–	–	–
RF Data Converter	14-bit RF-ADC w/DDC # of ADCs	–	–	–	–	–	–	8 / 2	4	8 / 4	8	8	16	6	8 / 2
RF Data Converter	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	2.5 / 5.0	5.0	2.5 / 5.0	5.0	5.0	2.5	5.9	2.95 / 5.9
RF Data Converter	14-bit RF-DAC w/DUC # of DACs	0	8	8	8	16	16	8	4	12	8	8	16	6	8
RF Data Converter	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85(3)	9.85(3)	9.85(3)	9.85(3)	9.85(3)	9.85(3)	10.0(4)	10.0(4)
RF Data Converter	SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0	0	0
RF Data Converter	Digital Front-End (DFE)	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓
RF Data Converter	Number of DDCs per RF-ADC(1)	0	1	1	1	1	1	1	2	1	1	1	1	1	1
RF Data Converter	RF input Freq max. GHz	4					5	6						7.125	
RF Data Converter	Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x						1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x	
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930	489	489
Programmable Logic (PL)	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425	224	224
Programmable Logic (PL)	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0	6.8	6.8
Programmable Logic (PL)	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0	22.8	22.8
Programmable Logic (PL)	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5	45.0	45.0
Programmable Logic (PL)	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272	1,872	1,872
Programmable Logic (PL)	GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16	8	8
Programmable Logic (PL)	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–	–	–
Programmable Logic (PL)	PCIeGen3 x16/Gen4 x8 / CCIX(2)	–	–	–	–	–	–	0	2	2	2	2	2	0	0
Programmable Logic (PL)	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1	0	0
Programmable Logic (PL)	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2	1	1
Programmable Logic (PL)	System Monitor	2	2	2	2	2	2	2	2	2 / 2	2	2	2	2	2
Programmable Logic (PL)	Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
D1156	35x35	214, 72, 208 4, 16 0, 0													
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8		214, 24, 130 4, 8 6, 6	214, 24, 130 4, 8 10, 8
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8			
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16		
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12					

1. This value applies when all RF I/O of an RF-ADC tile are used. 2. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213. 3. For operation up to 10GSPS, contact your local Xilinx Sales Representative. 4. 10GSPS RF-DAC operation is available in -2I speed grade.

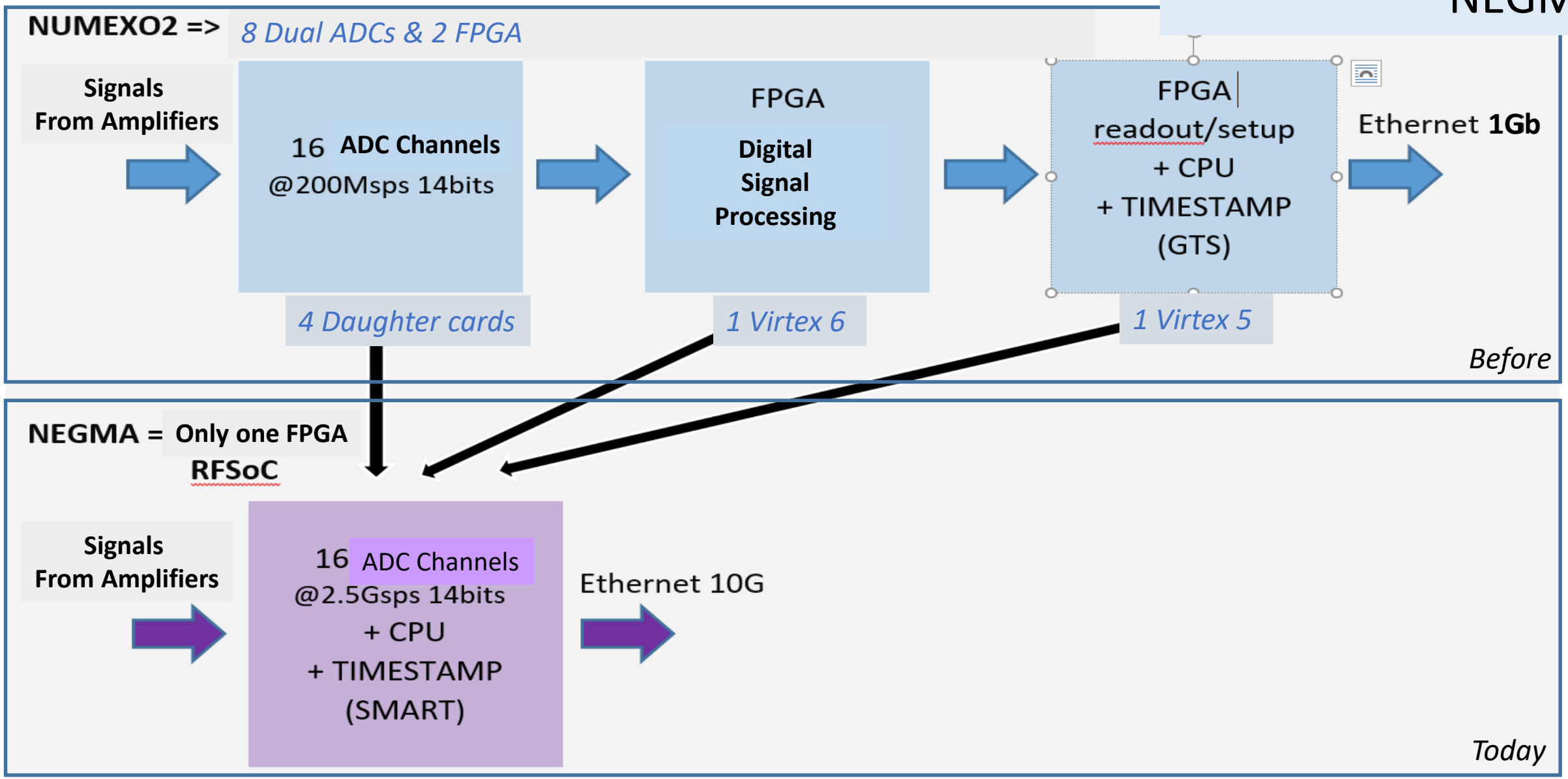
FPGA Features
XCZU49DR

Featured Xilinx Devices

Featuring the Zynq UltraScale+ **XCZU49DR-2FFVF1760** RFSoC

14-bit, 2.5GSPS RF-ADC	16
14-bit, 9.85GSPS RF-DAC	16
Max. RF input Frequency (GHz)	6
System Logic Cells (K)	930
Memory (Mb)	60.5
DSP Slices	4,272
33G Transceivers	16
Maximum I/O Pins	408

Our Proposal NEGMA



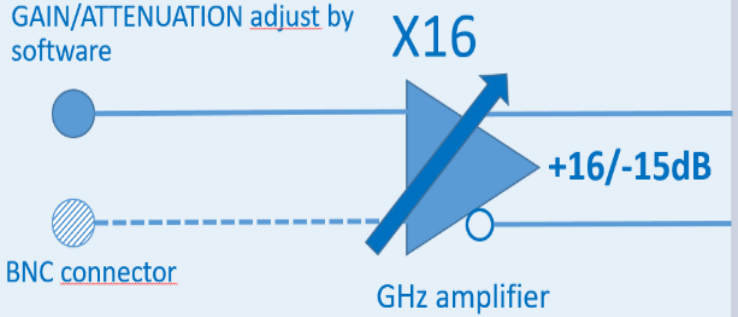
(Charles Houarner)

NEGMA
Front End Electronics

FRONT END 16 channels GHz bandwidth

ALL signal detectors input

- ✓ +/- or bipolar
- ✓ Mono or differential
- ✓ GAIN/ATTENUATION adjust by software



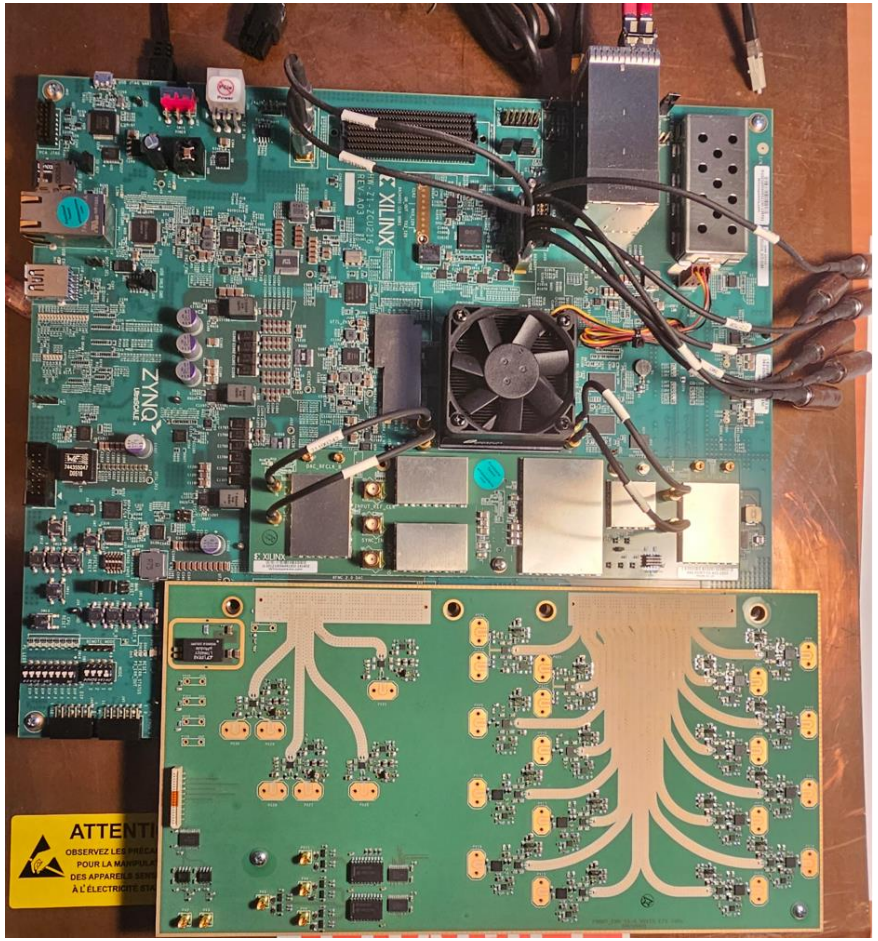
FPGA RFSoC 3rd generation

Highest level of integration

- ✓ 16 ADC GHz & DAC
- ✓ Multi CPU and GPU
- ✓ FPGA logic ressources
- ✓ GIGA Transceivers

16 ADC 14bits@2.5GHz inside FPGA

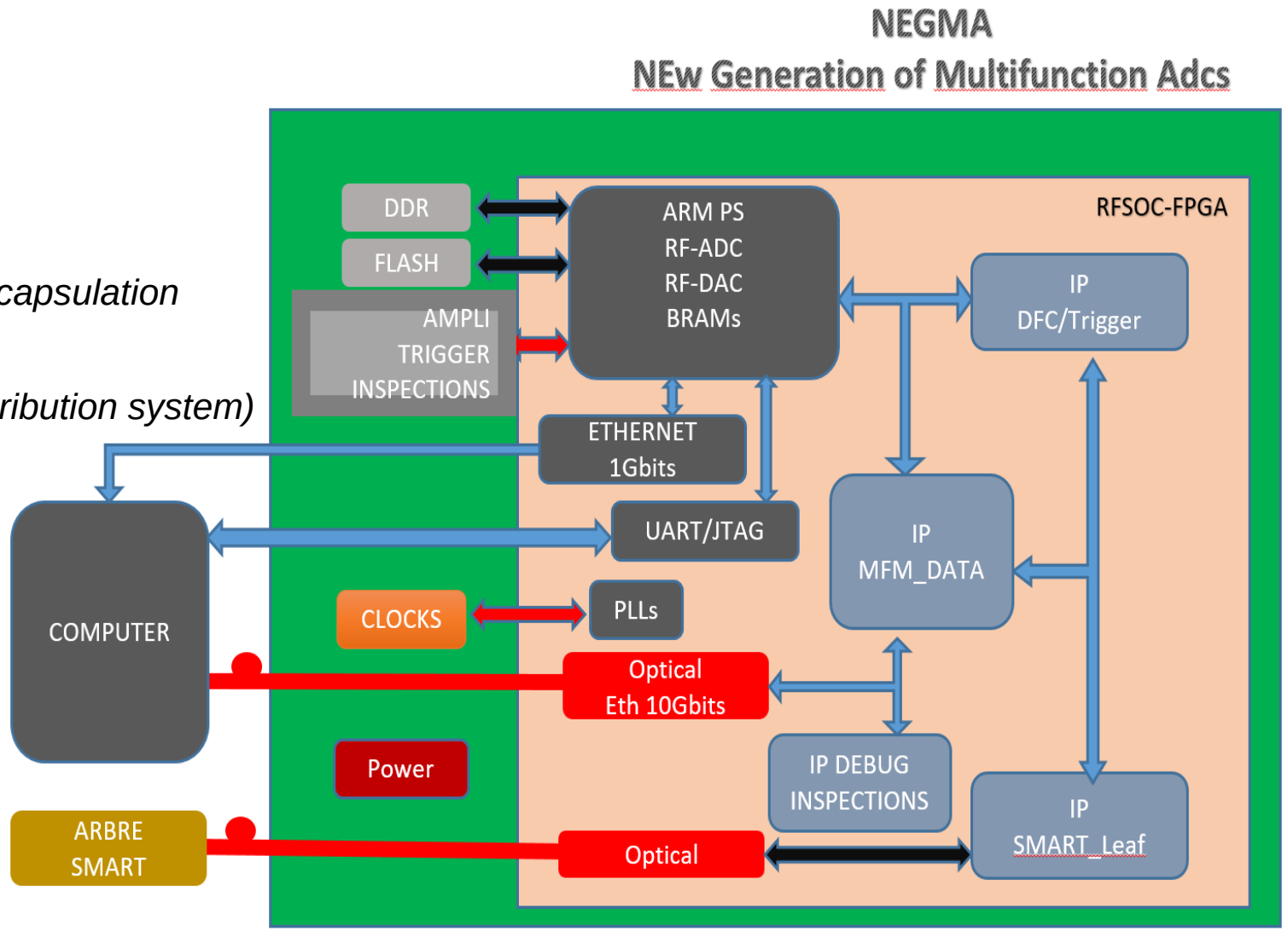
4 DAC 14bits@2.5GHz



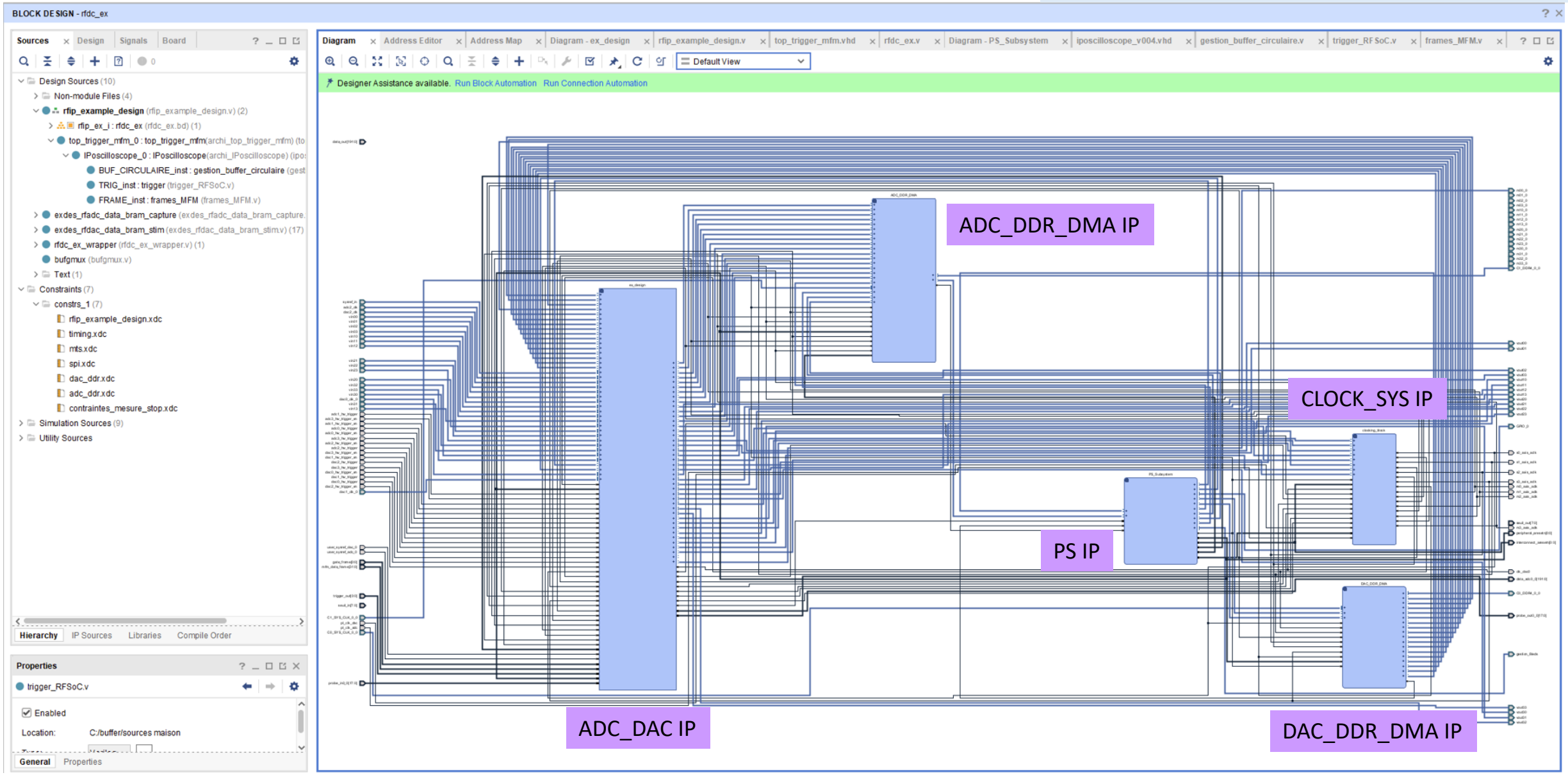
(from Charles Houarner)

NEGMA
General overview

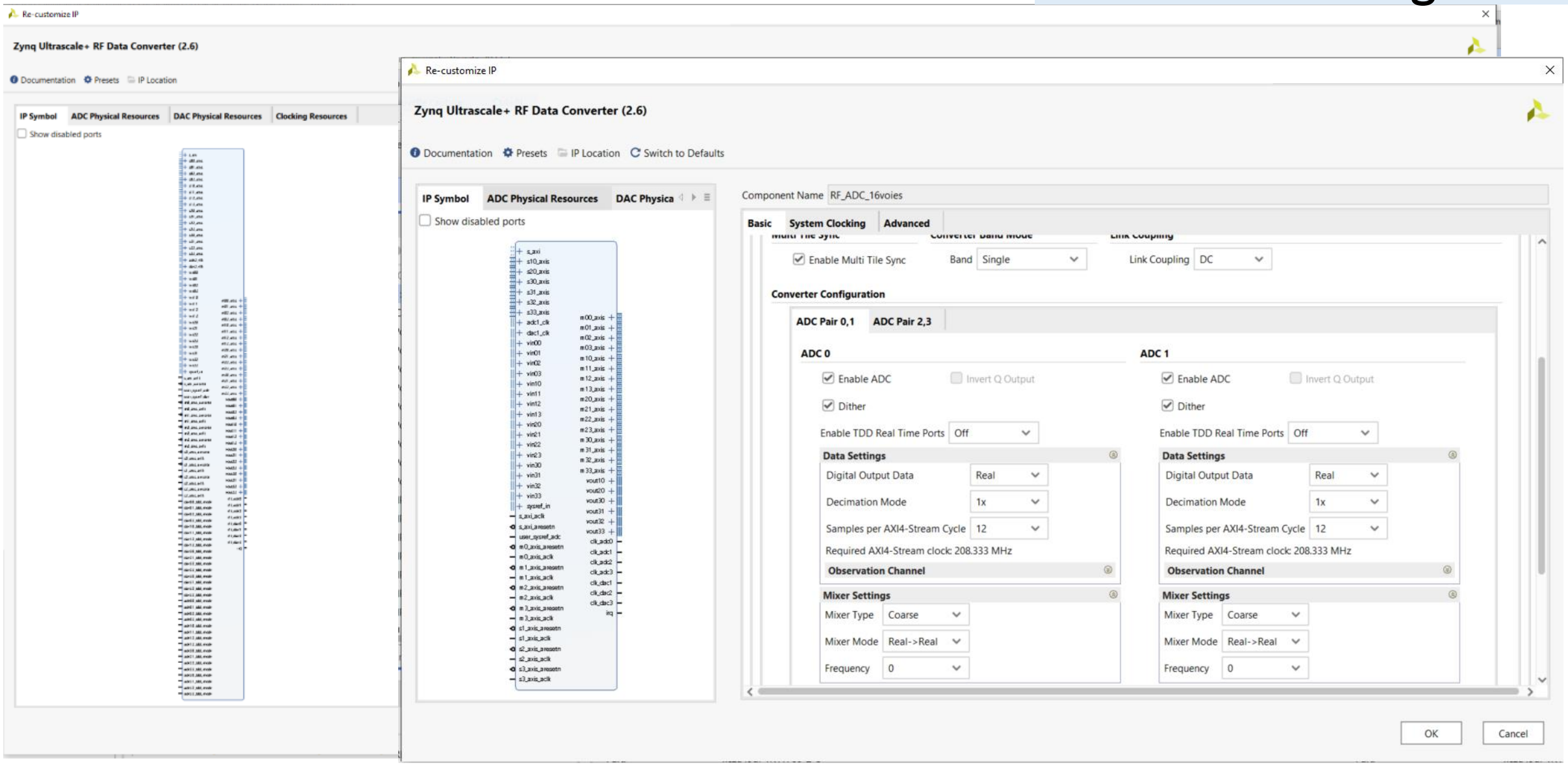
- **Processing System Area** :
  - **ARM PS** :
    - *Linux, Slow Control, Data debug...*
- **Programmable Logic Area**:
  - ***TRIGGER & MFM_DATA IP***
    - *Trigger, Data generation and MFM encapsulation*
  - ***SMART_ENDPOINT IP***
    - *SMART (Time stamping and clock distribution system)*
  - ***Eth 1 à 10Gbits IP***
    - *High Gb data transmission Interface*
  - ***DEBUG & INSPECTION IPs***
    - Signal inspection & debug



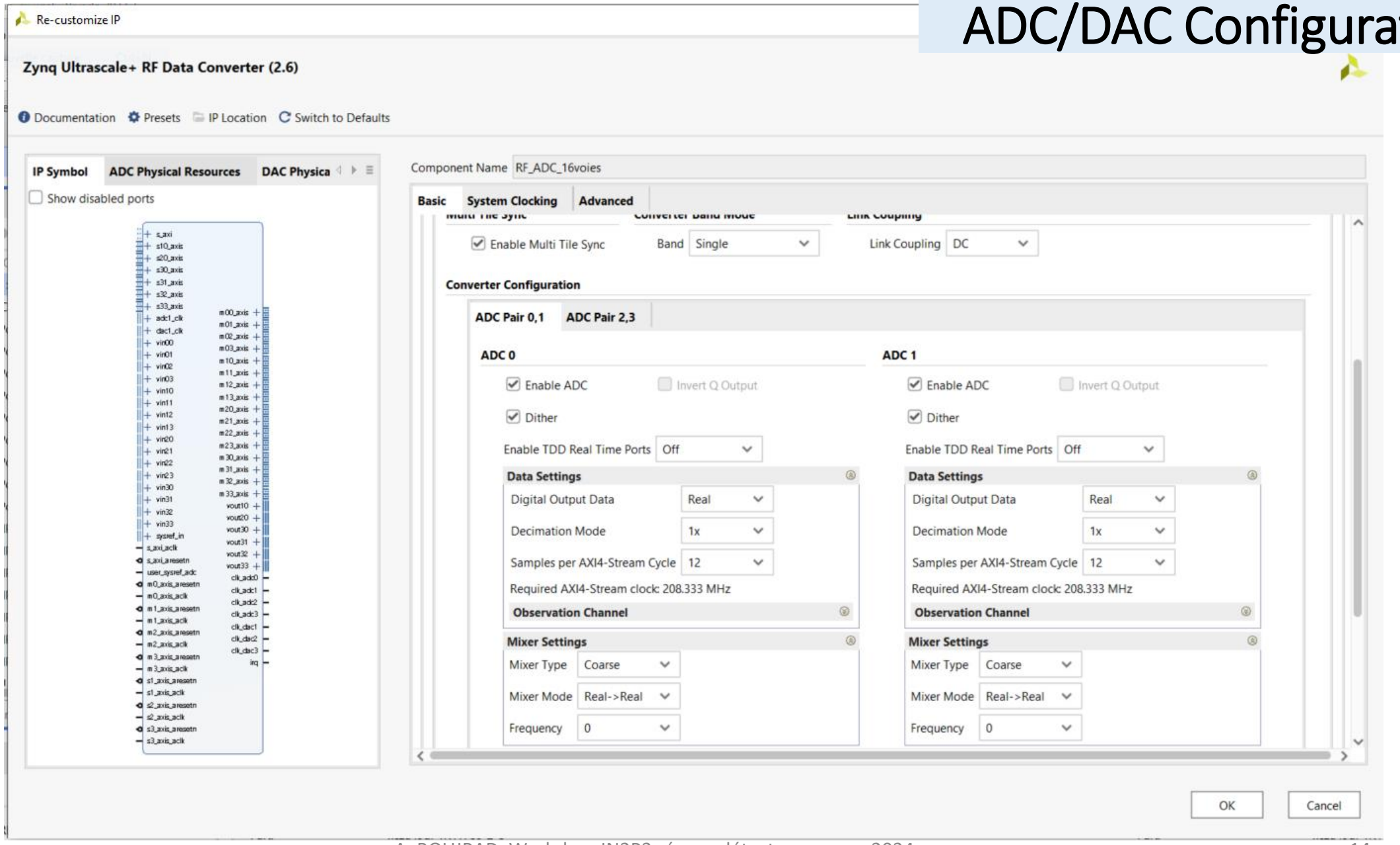
Block diagram in Vivado



Vivado
Clock Configuration



Vivado
ADC/DAC Configuration



PC/xubuntu

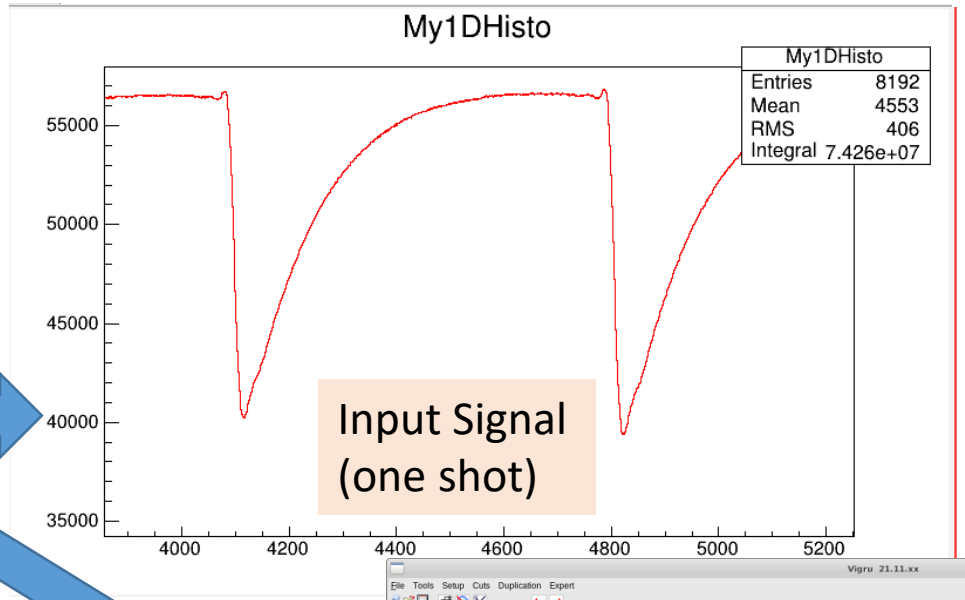
GetMFM
GRU
Client

PC/Win10

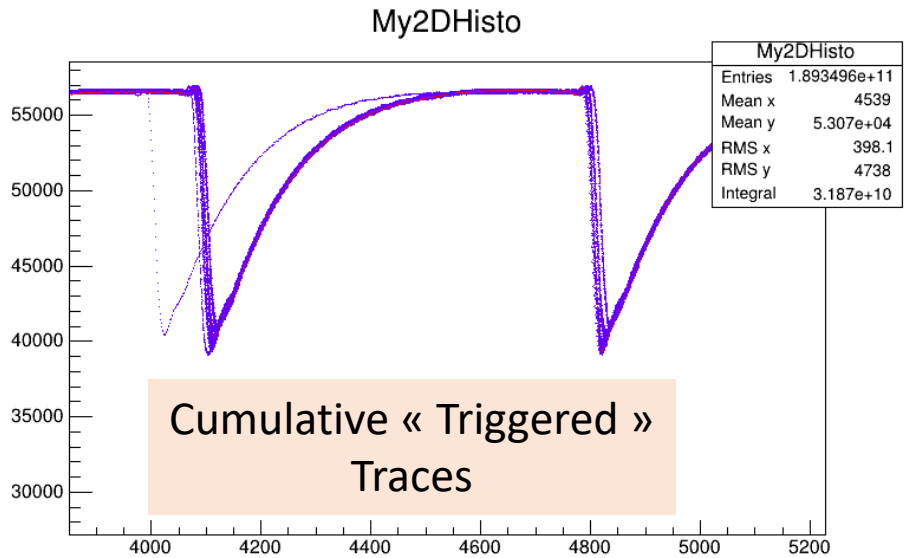
EUI
Client

Ethernet

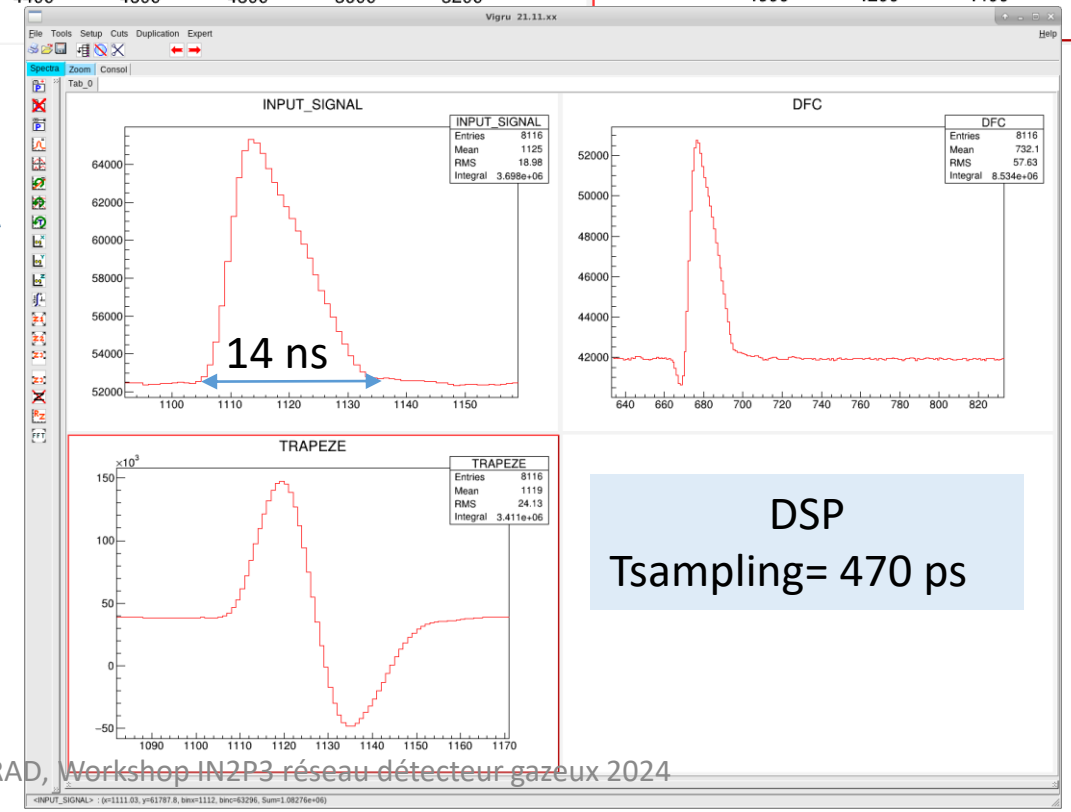
ZCU216
RFTOOL
(Server)



Input Signal
(one shot)



Cumulative « Triggered »
Traces



DSP
Tsampling= 470 ps

Conclusion

- **Phase 1 (Demonstrator)**
  - Software Program : *to be finalized*
  - Fimware :
    - Time Stamp IP : *To be tested with SMART Three*
    - Trace IP : *We are validating the 16 channels version*
    - Gb Ethernet IP : *Host software under development (REACTif)*
  - Front End Card : *Under test*
  - ZCU216 Mecanics : *To be designed*
  - *Ongoing collaboration : NEEL Institut/ Grenoble*
  - Demonstrator validation : *The end of 2024*

- **Demonstrator Local Team**
- **Hard :** *A. Boujrad, C. Houarner, M. Blaizot, P. Bourgault, M. Bezard*
- **Soft :** *L. Legeard, S. Coudert*

Thank you for your listening