

NEGMA- Demonstrator

An RFSoc FPGA Development

A. BOUJRAD

PHY/GTA/GANIL

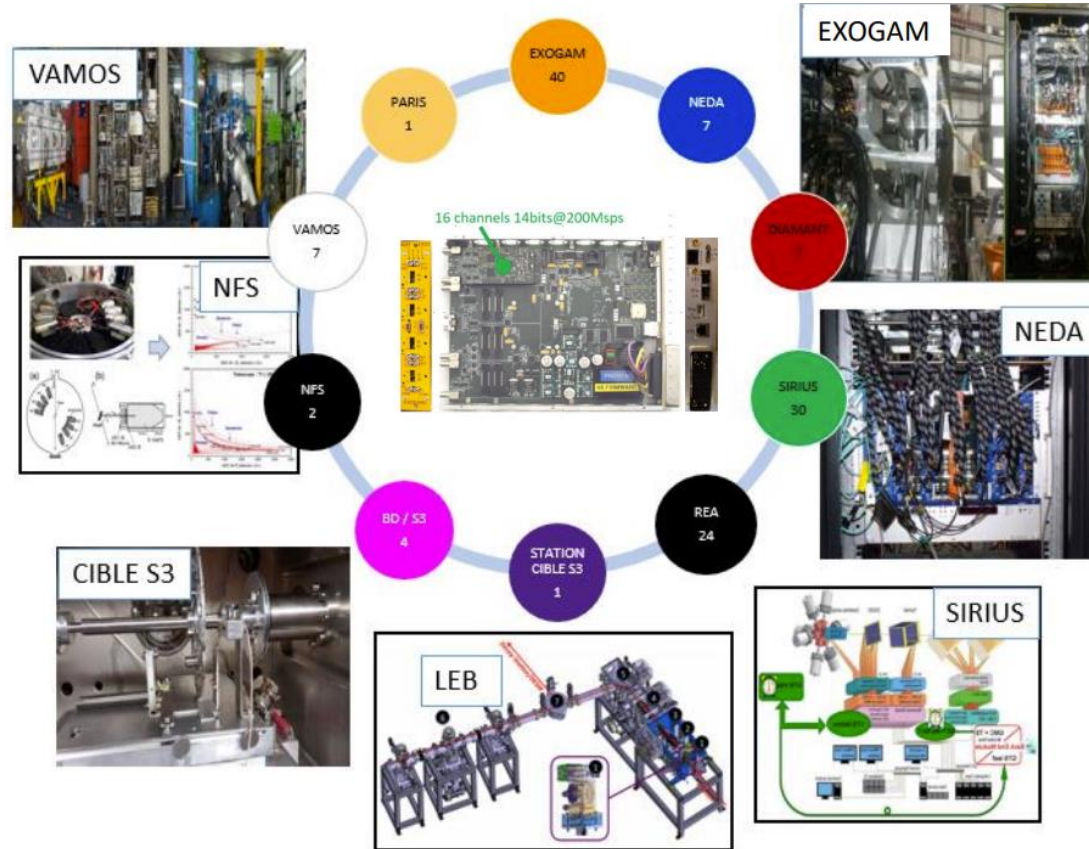
Demonstrator Local Team

Hardware : *A. Boujrad, C. Houarner, M. Blaizot, P. Bourgault, M. Bezard*

Software : *L. Legeard, S. Coudert, S. Rabahia(apprentice)*

- Introduction
- ZCU216 Evaluation Kit as a demonstrator
- NEGMA General Overview
- Conclusion

Present Digitizer: NUMEXO2



- Dedicate to EXOGAM => Extended to Other detection systems
 - *NEDA, DIAMANT, SIRIUS, VAMOS NFS...*
 - *128 Modules manufactured*
 - *Used on several experiments : VAMOS, Lise2022/2023, NFS....*
- Status
 - *Icreased needs (Expeiments and Setup)*
 - *No possibility to re-manufacture => components and tools obsolences*
 - *No more possible Evolution => Firmware limitation Ressources*

Futur Digitizer : NEGMA + REActif



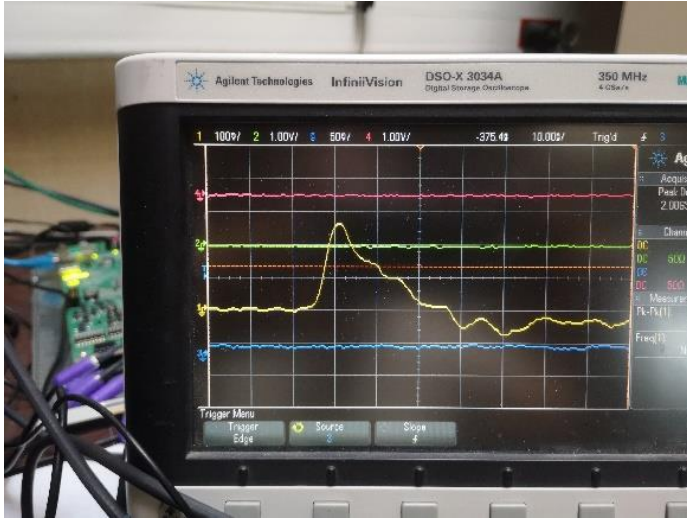
NEGMA

New Generation of Multifunction Adcs



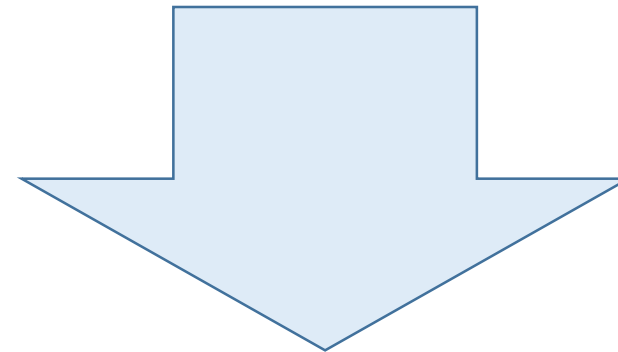
REActif

- New Generation of RFSoc/FPGA
 - *16 Channels (14bits @2.5 Gps), Integrated ADCs & DACs*
- High resolution Scope & More complex algorithms
 - *Deported Digital Signal Processing with GPUs on REActif*
- Gb Ethernet data transmission

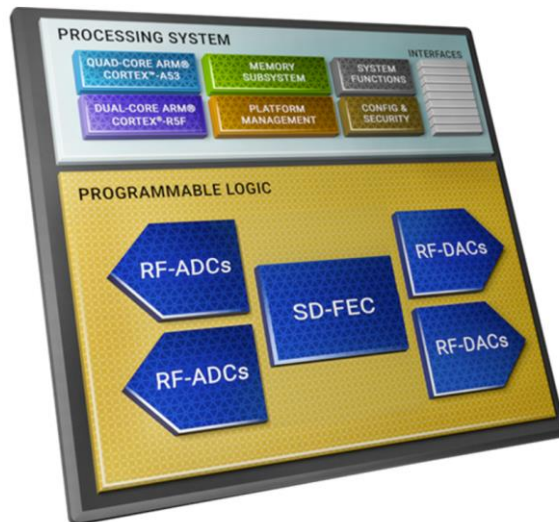


NEEDS

- 1- Fast signal measurements (*ns*)
- 2- Fast data transmission (**1 à 10 GEth**)
- 3- Complex algorithms in remote location
- 4- SMART TimeStamping integration



ZYNQ[®]
RFSoc



Our Proposal

- 1- *14bits @ 2.5 GHz ADCs & 14bits @ 9.85 GHz DACs*
- 2- Optical data links (up to *10 Gbits per link*)
- 3- Massively parallel computing via external GPU (*REACTif*)

Kits & Commercial modules

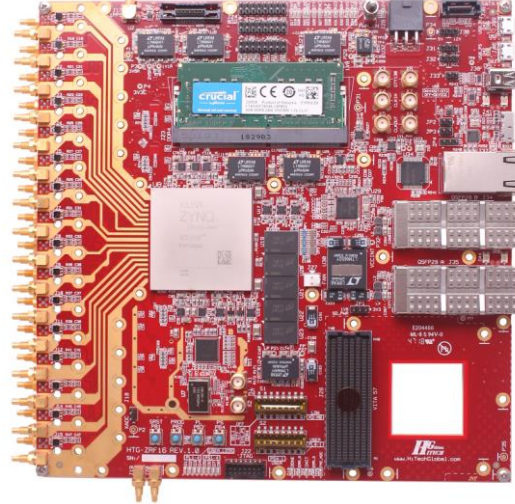
PENTEK
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vadatech
THE POWER OF VISION



**H GLOBAL
HITECH**



**Abaco
SYSTEMS**



**TELEDYNE
SP DEVICES**
Everywhere you look



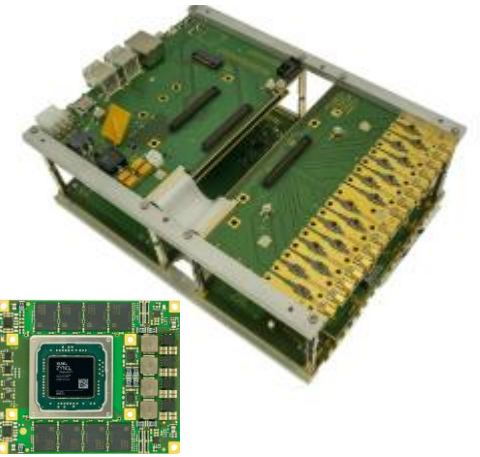
Zynq® UltraScale+™ RFSoc Boards & Kits Portfolio

Gen 1 4GHz		Gen 2 5GHz		Gen 3 6GHz	
ZCU111 Evaluation Kit	Avnet RFSoc Kit Development Kit	ZCU1275 Characterization Kit	ZCU1285 Characterization Kit	ZCU208 Evaluation Kit	ZCU216 Evaluation Kit
					
ZU28DR Application Development and Performance Evaluation of: ADCs: 8x 12-bit 4.096GSPS DACs: 8x 14-bit 6.554GSPS SD-FEC: 8	ZU28DR Wireless Application Development Leveraging: Xilinx ZCU111 Evaluation Kit Avnet Qorvo 2x2 Small Cell RF Front End 1.8GHz Card Avnet RFSoc Explorer with MATLAB and Simulink	ZU29DR Ideal for Tone Testing and Data Sheet Verification of: ADCs: 16x 12-bit 2.058GSPS DACs: 16x 14-bit 6.554GSPS	ZU39DR Ideal for Tone Testing and Data Sheet Verification of: ADCs: 16x 12-bit 2.220GSPS DACs: 16x 14-bit 6.554GSPS	ZU48DR Application Development and Performance Evaluation of: ADCs: 8x 14-bit 5.0GSPS DACs: 8x 14-bit 10.0GSPS SD-FEC: 8	ZU49DR Application Development and Performance Evaluation of: ADCs: 16x 14-bit 2.5GSPS DACs: 16x 14-bit 10.0GSPS SD-FEC: 8
					

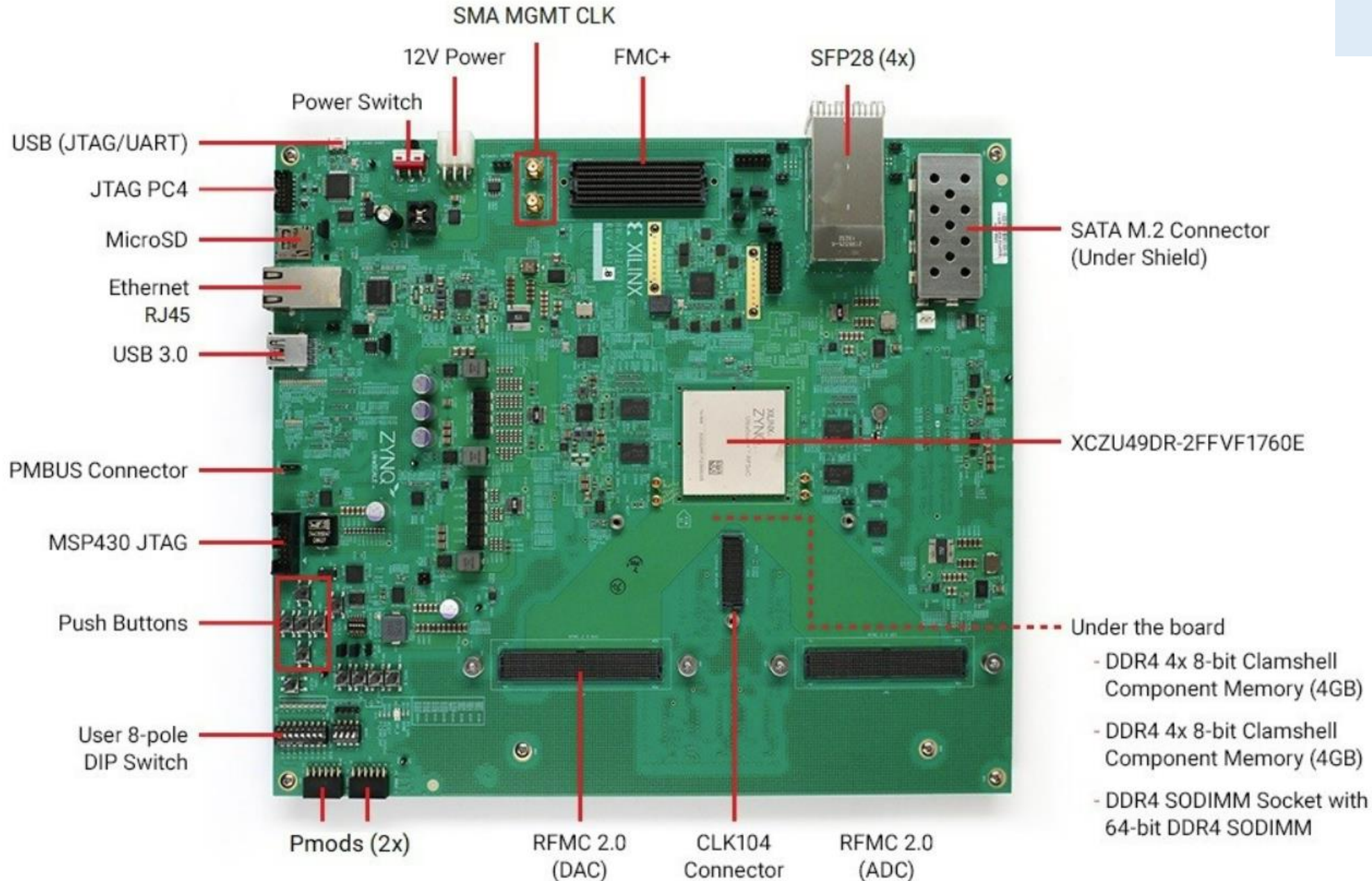
AVNET®



KR KNOWLEDGE RESOURCES
Switzerland GmbH



ZCU216 Description



FPGA_RFSOC Family

Device Name		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	ZU65DR	ZU67DR	
		Gen 1					Gen 2	Gen 3					DFE			
		Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5F MPCore up to 533MHz														
RF Data Converter	12-bit RF-ADC	# of ADCs	0	8	8	8	16	16	-	-	-	-	-	-	-	
	w/DDC	Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	-	-	-	-	-	-	-	
	14-bit RF-ADC	# of ADCs	-	-	-	-	-	-	8	2	4	8	4	8	8	
	w/DDC	Max Rate (GSPS)	-	-	-	-	-	-	2.5	5.0	5.0	2.5	5.0	5.0	5.0	
	14-bit RF-DAC	# of DACs	0	8	8	8	16	16	8	4	12	8	8	16	6	
	w/DUC	Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	10.0 ⁽⁴⁾	10.0 ⁽⁴⁾
		SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0	0	0
		Digital Front-End (DFE)	-	-	-	-	-	-	-	-	-	-	-	-	✓	✓
		Number of DDCs per RF-ADC ⁽¹⁾	0	1	1	1	1	1	1	2	1	1	1	1	1	1
		RF input Freq max. GHz			4			5			6				7.125	
Programmable Logic (PL)		Decimation / Interpolation	1x, 2x, 4x, 8x				1x, 2x, 4x, 8x		1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x		
		System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930	489	489
		CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425	224	224
		Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0	6.8	6.8
		Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0	22.8	22.8
		UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5	45.0	45.0
		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272	1,872	1,872
		GTy Transceivers	16	8	16	16	16	16	8	16	16	16	16	16	8	8
		PCIe® Gen3 x16	2	1	2	2	2	2	-	-	-	-	-	-	-	-
		PCIeGen3 x16/Gen4 x8 / CCIX ⁽²⁾	-	-	-	-	-	-	0	2	2	2	2	2	0	0
	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1	0	0	
	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2	1	1	
	System Monitor	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
	Speed Grades	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	
D1156	35x35	214, 72, 208 4, 16 0, 0														
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8		214, 24, 130 4, 8 6, 6	214, 24, 130 4, 8 10, 8	
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16			
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12						

Zynq® UltraScale+™ RFSOCs

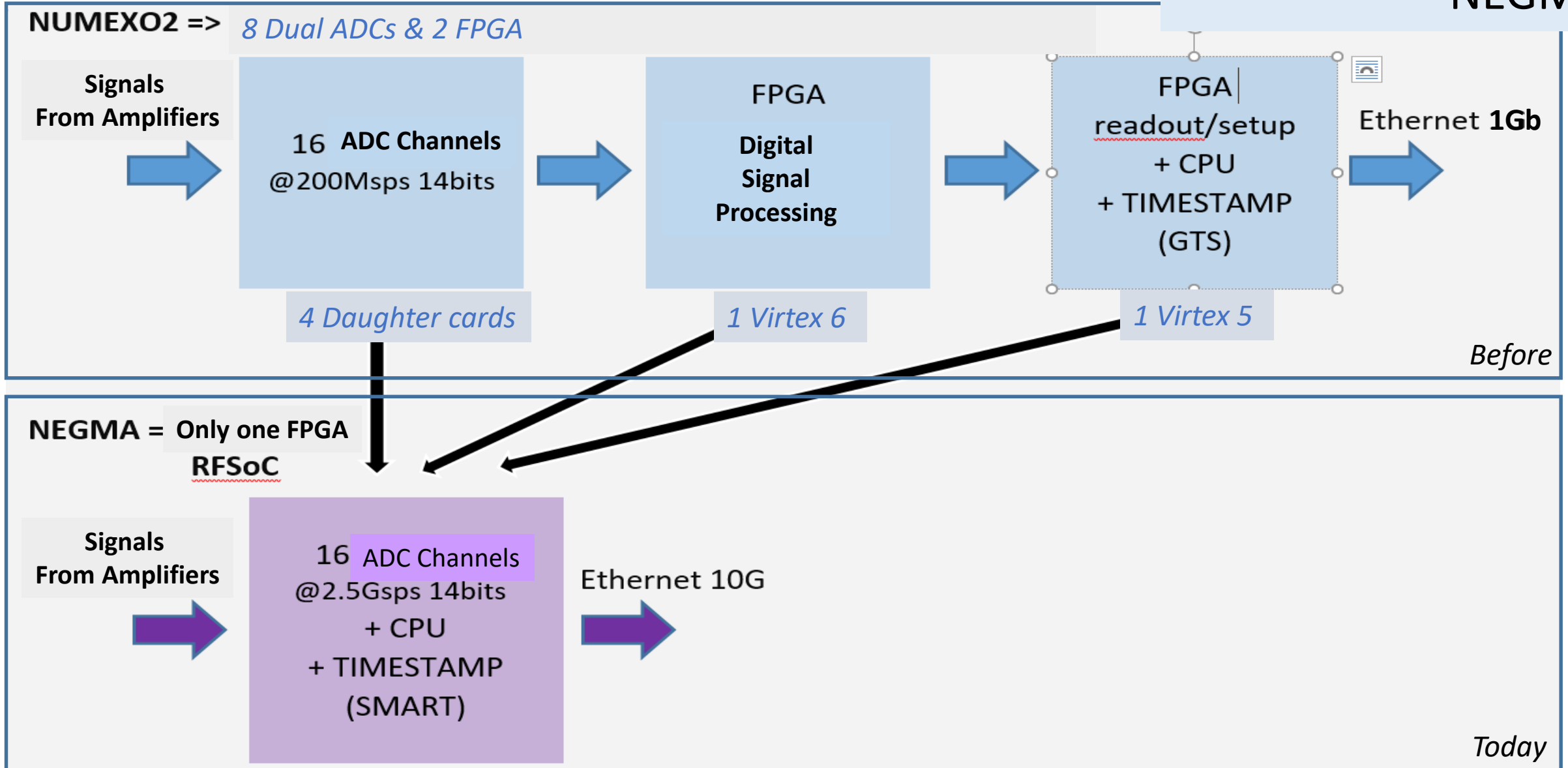
1. This value applies when all RF I/O of an RF-ADC tile are used. 2. This block operates in compatibility mode for PCIe, Gen4, and Gen5. 3. Resonance detectors are not available for all devices. 4. 10GSPS RF-DAC operation is available in -2I speed grade.

Featured Xilinx Devices

Featuring the Zynq UltraScale+ **XCZU49DR-2FFVF1760** RFSoc

14-bit, 2.5GSPS RF-ADC	16
14-bit, 9.85GSPS RF-DAC	16
Max. RF input Frequency (GHz)	6
System Logic Cells (K)	930
Memory (Mb)	60.5
DSP Slices	4,272
33G Transceivers	16
Maximum I/O Pins	408

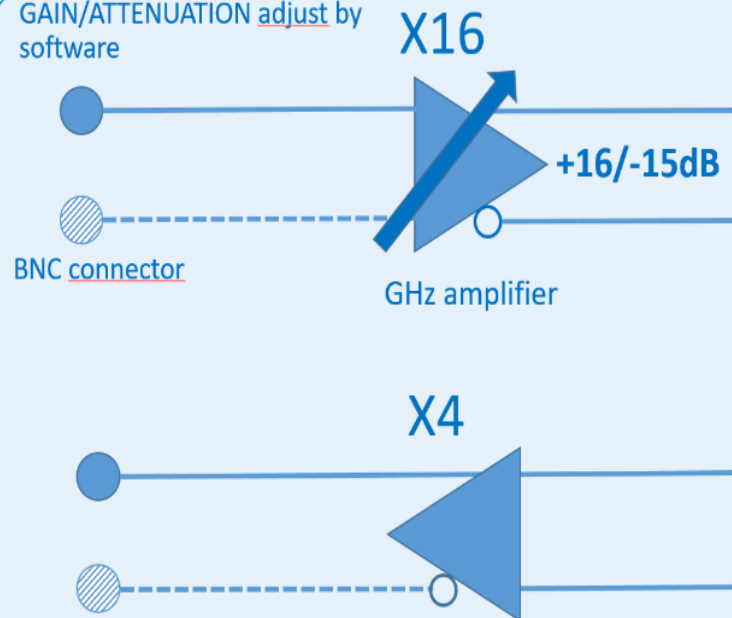




FRONT END 16 channels GHz bandwidth

ALL signal detectors input

- ✓ +/- or bipolar
- ✓ Mono or differential
- ✓ GAIN/ATTENUATION adjust by software



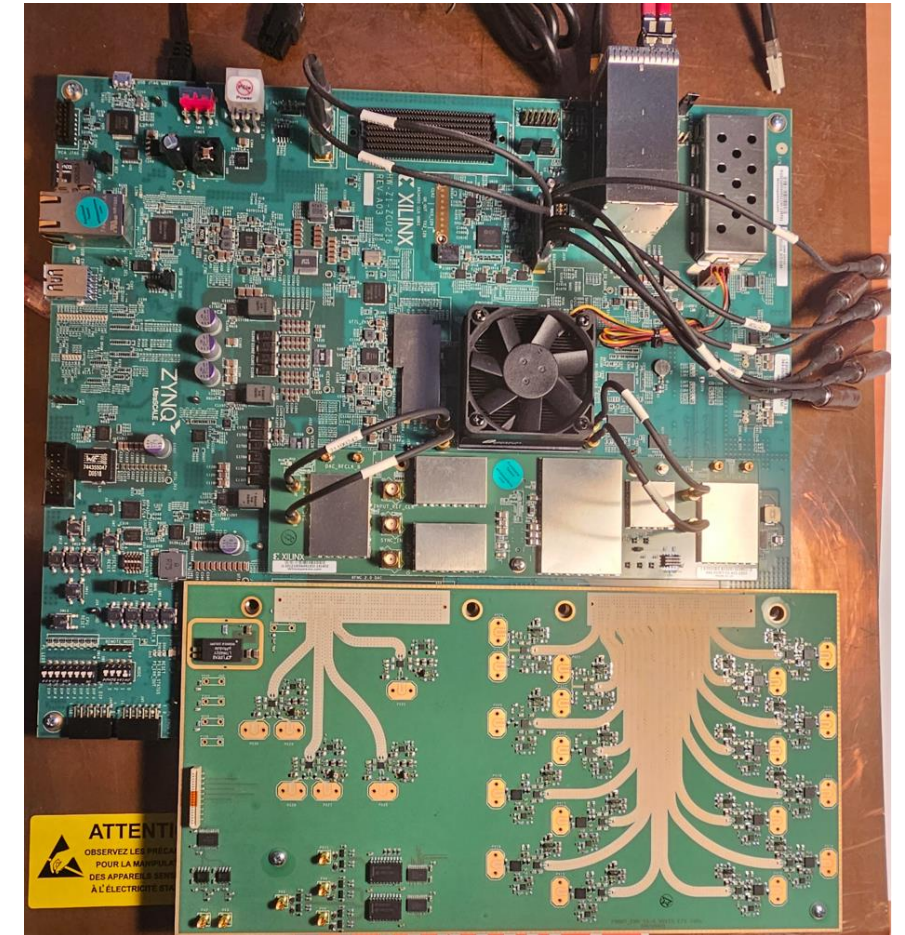
FPGA RFSoc 3rd generation

Highest level of integration

- ✓ 16 ADC GHz & DAC
- ✓ Multi CPU and GPU
- ✓ FPGA logic resources
- ✓ GIGA Transceivers

16 ADC 14bits@2.5GHz inside FPGA

4 DAC 14bits@2.5GHz



(from Charles Houarner)

- Processing System Area :

- ARM PS :

- Linux, Slow Control, Data debug...*

- Programmable Logic Area:

- TRIGGER & MFM_DATA IP**

- Trigger, Data generation and MFM encapsulation*

- SMART_ENDPOINT IP**

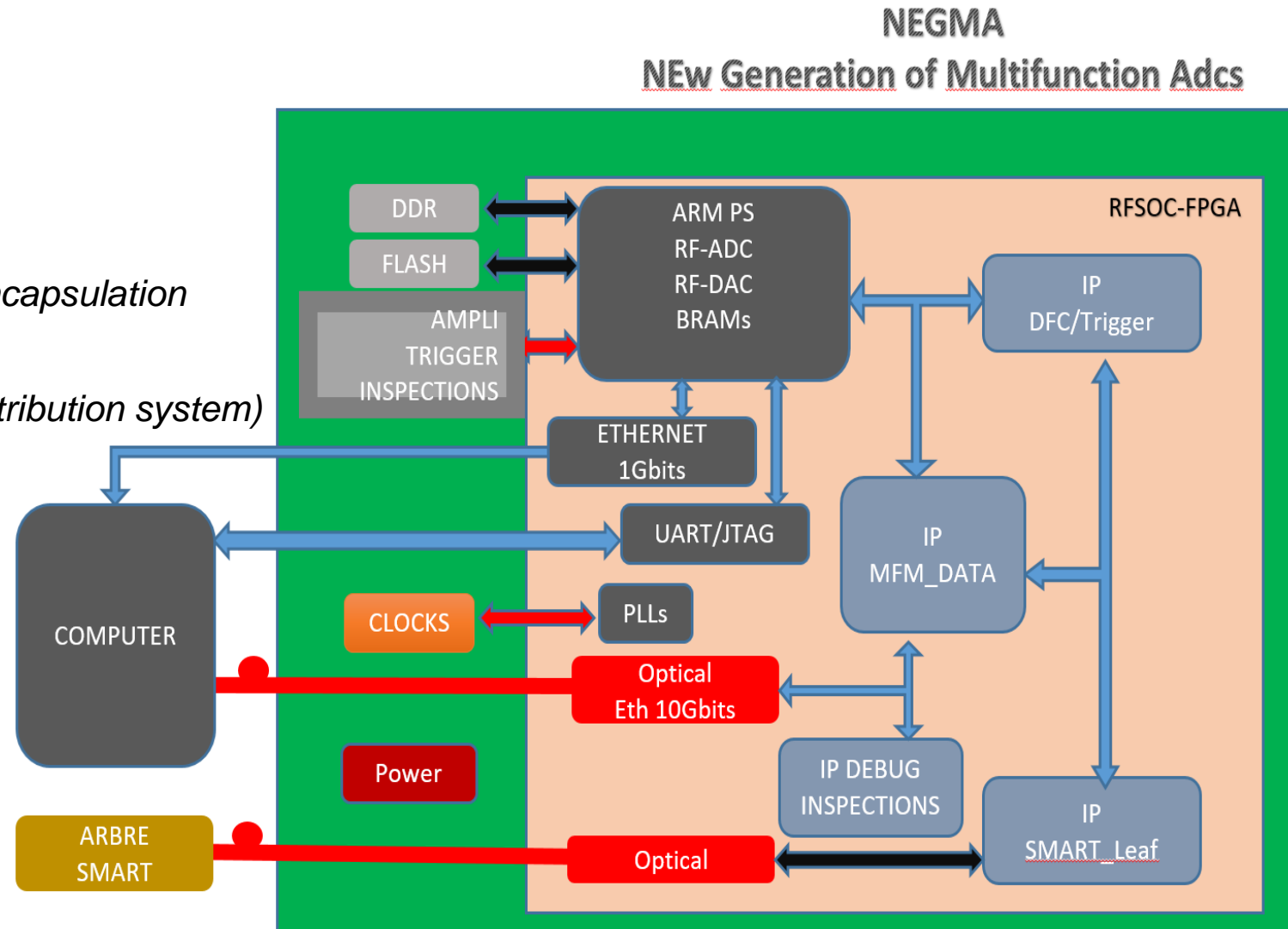
- SMART (Time stamping and clock distribution system)*

- Eth 1 à 10Gbits IP**

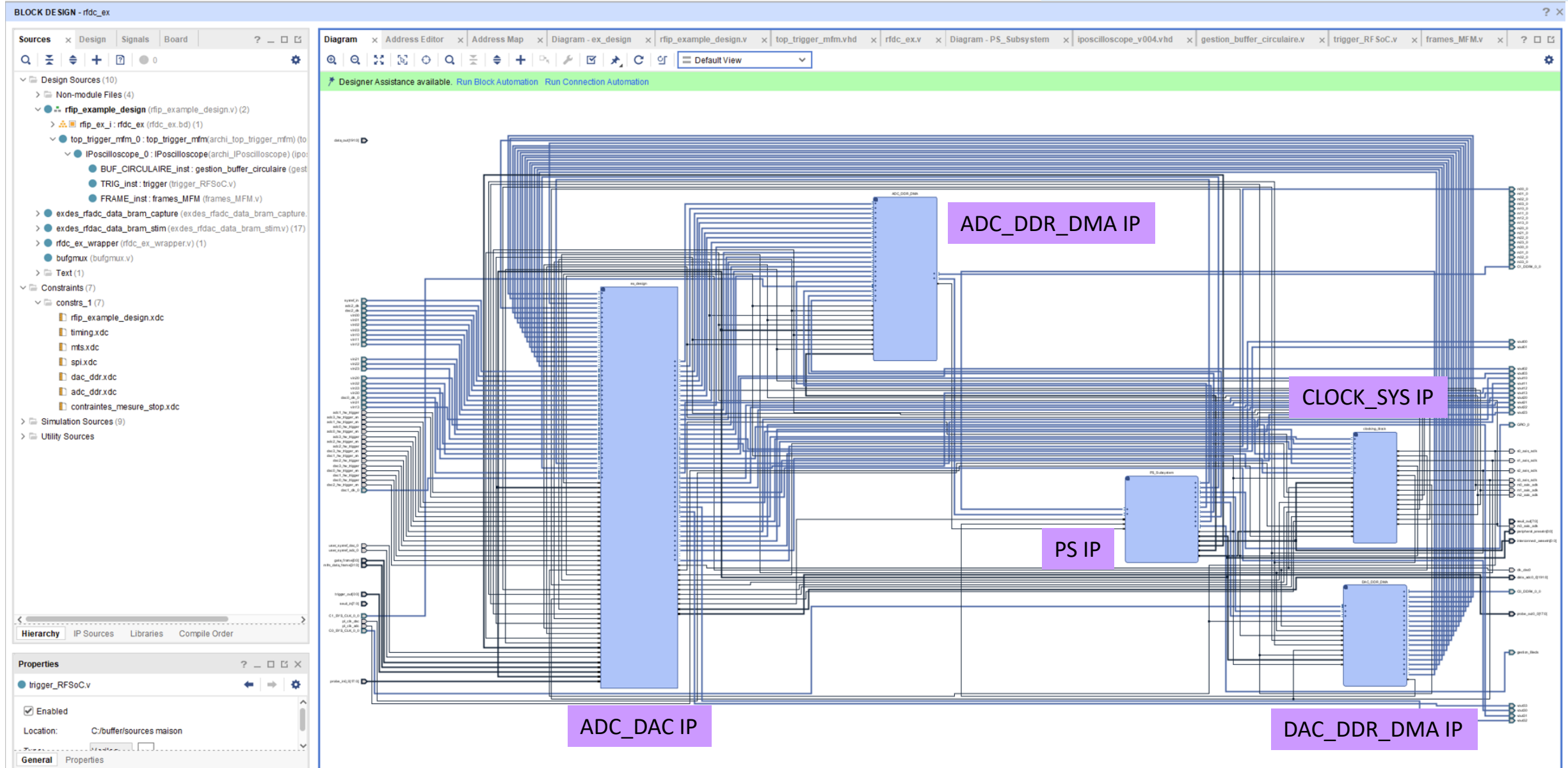
- High Gb data transmission Interface*

- DEBUG & INSPECTION IPs**

- Signal inspection & debug*



Block diagram in Vivado



Vivado Clock Configuration

The image displays two overlapping Vivado configuration windows for the Zynq Ultrascale+ RF Data Converter (2.6) IP.

Left Window (IP Symbol Tab): Shows the 'ADC Physical Resources' tab with a list of resources including s_axi, s10_axis, s20_axis, s30_axis, s31_axis, s32_axis, s33_axis, s_axi_jack, s_axi_jack0, s_axi_jack1, s_axi_jack2, s_axi_jack3, s_axi_jack4, s_axi_jack5, s_axi_jack6, s_axi_jack7, s_axi_jack8, s_axi_jack9, s_axi_jack10, s_axi_jack11, s_axi_jack12, s_axi_jack13, s_axi_jack14, s_axi_jack15, s_axi_jack16, s_axi_jack17, s_axi_jack18, s_axi_jack19, s_axi_jack20, s_axi_jack21, s_axi_jack22, s_axi_jack23, s_axi_jack24, s_axi_jack25, s_axi_jack26, s_axi_jack27, s_axi_jack28, s_axi_jack29, s_axi_jack30, s_axi_jack31, s_axi_jack32, s_axi_jack33, s_axi_jack34, s_axi_jack35, s_axi_jack36, s_axi_jack37, s_axi_jack38, s_axi_jack39, s_axi_jack40, s_axi_jack41, s_axi_jack42, s_axi_jack43, s_axi_jack44, s_axi_jack45, s_axi_jack46, s_axi_jack47, s_axi_jack48, s_axi_jack49, s_axi_jack50, s_axi_jack51, s_axi_jack52, s_axi_jack53, s_axi_jack54, s_axi_jack55, s_axi_jack56, s_axi_jack57, s_axi_jack58, s_axi_jack59, s_axi_jack60, s_axi_jack61, s_axi_jack62, s_axi_jack63, s_axi_jack64, s_axi_jack65, s_axi_jack66, s_axi_jack67, s_axi_jack68, s_axi_jack69, s_axi_jack70, s_axi_jack71, s_axi_jack72, s_axi_jack73, s_axi_jack74, s_axi_jack75, s_axi_jack76, s_axi_jack77, s_axi_jack78, s_axi_jack79, s_axi_jack80, s_axi_jack81, s_axi_jack82, s_axi_jack83, s_axi_jack84, s_axi_jack85, s_axi_jack86, s_axi_jack87, s_axi_jack88, s_axi_jack89, s_axi_jack90, s_axi_jack91, s_axi_jack92, s_axi_jack93, s_axi_jack94, s_axi_jack95, s_axi_jack96, s_axi_jack97, s_axi_jack98, s_axi_jack99.

Right Window (Advanced Tab): Shows the configuration for the 'RF_ADC_16voies' component. The 'Converter Configuration' section is expanded to show settings for 'ADC Pair 0,1' and 'ADC Pair 2,3'. The 'ADC 0' and 'ADC 1' settings are as follows:

ADC 0	ADC 1
<input checked="" type="checkbox"/> Enable ADC	<input checked="" type="checkbox"/> Enable ADC
<input type="checkbox"/> Invert Q Output	<input type="checkbox"/> Invert Q Output
<input checked="" type="checkbox"/> Dither	<input checked="" type="checkbox"/> Dither
Enable TDD Real Time Ports: Off	Enable TDD Real Time Ports: Off
Data Settings	Data Settings
Digital Output Data: Real	Digital Output Data: Real
Decimation Mode: 1x	Decimation Mode: 1x
Samples per AXI4-Stream Cycle: 12	Samples per AXI4-Stream Cycle: 12
Required AXI4-Stream clock: 208.333 MHz	Required AXI4-Stream clock: 208.333 MHz
Mixer Settings	Mixer Settings
Mixer Type: Coarse	Mixer Type: Coarse
Mixer Mode: Real->Real	Mixer Mode: Real->Real
Frequency: 0	Frequency: 0

Re-customize IP

Zynq Ultrascale+ RF Data Converter (2.6)

Documentation Presets IP Location Switch to Defaults

IP Symbol ADC Physical Resources DAC Physical Resources

Show disabled ports

Component Name RF_ADC_16voices

Basic System Clocking Advanced

Multi Tile Sync Band Single Link Coupling DC

Converter Configuration

ADC Pair 0,1 ADC Pair 2,3

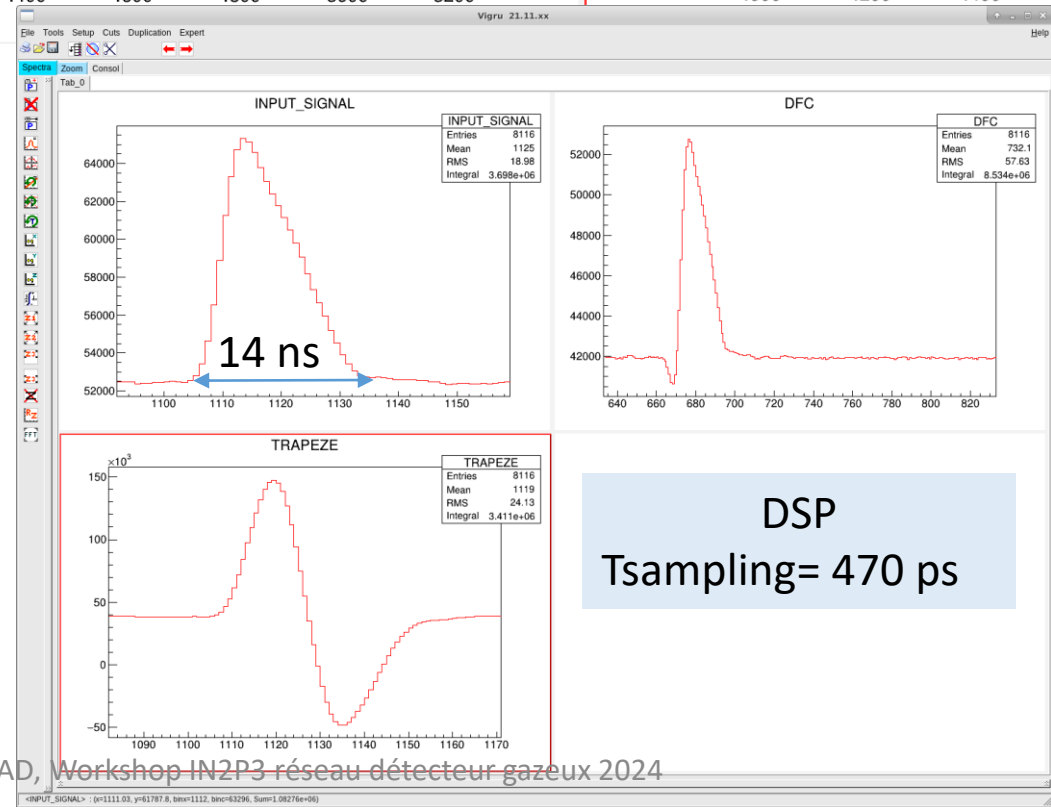
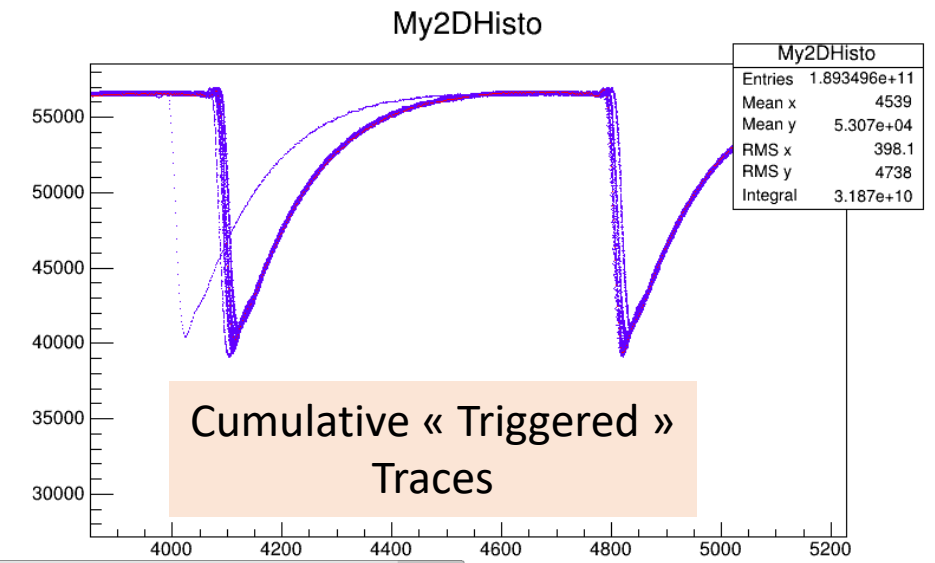
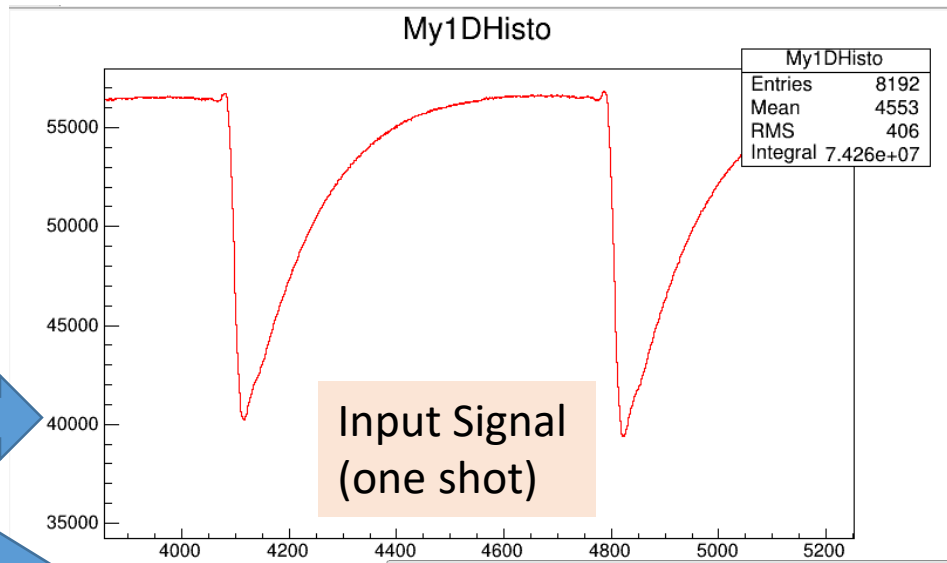
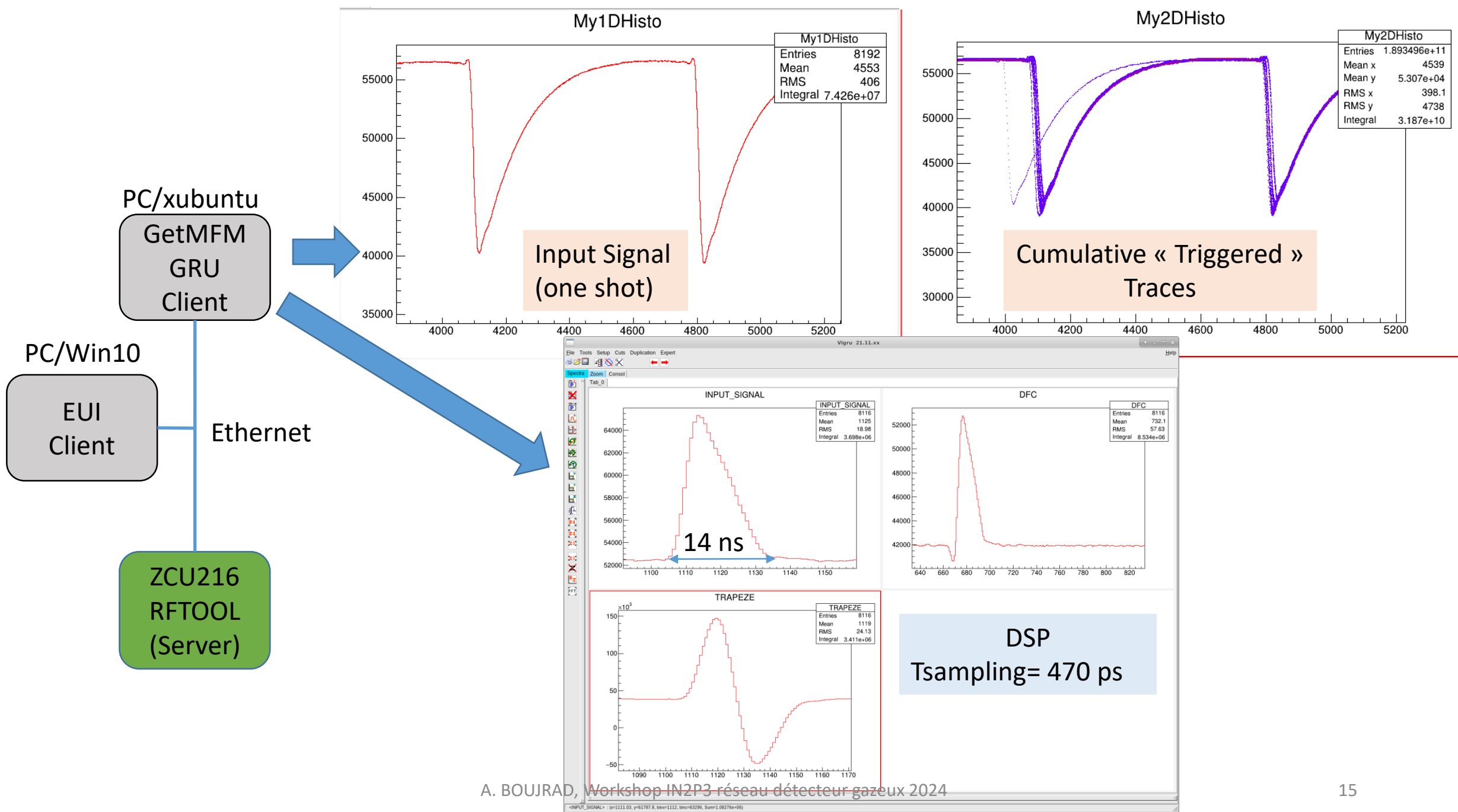
ADC 0

- Enable ADC Invert Q Output
- Dither
- Enable TDD Real Time Ports Off
- Data Settings**
 - Digital Output Data Real
 - Decimation Mode 1x
 - Samples per AXI4-Stream Cycle 12
 - Required AXI4-Stream clock: 208.333 MHz
- Observation Channel**
- Mixer Settings**
 - Mixer Type Coarse
 - Mixer Mode Real->Real
 - Frequency 0

ADC 1

- Enable ADC Invert Q Output
- Dither
- Enable TDD Real Time Ports Off
- Data Settings**
 - Digital Output Data Real
 - Decimation Mode 1x
 - Samples per AXI4-Stream Cycle 12
 - Required AXI4-Stream clock: 208.333 MHz
- Observation Channel**
- Mixer Settings**
 - Mixer Type Coarse
 - Mixer Mode Real->Real
 - Frequency 0

OK Cancel



- **Phase 1 (Demonstrator)**

- Software Program : *to be finalized*
- Firmware :
 - Time Stamp IP : *To be tested with SMART Three*
 - Trace IP : *We are validating the 16 channels version*
 - Gb Ethernet IP : *Host software under development (REACTif)*
- Front End Card : *Under test*
- ZCU216 Mechanics : *To be designed*
- *Ongoing collaboration : NEEL Institut/ Grenoble*
- Demonstrator validation : *The end of 2024*

- **Demonstrator Local Team**

- **Hard** : *A. Boujrad, C. Houarner, M. Blaizot, P. Bourgault, M. Bezard*
- **Soft** : *L. Legeard, S. Coudert*

Thank you for your listening