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SALSA chip: a new electronics to read MPGD

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Atelier détecteurs gazeux

21/03/2024

Introduction

SALSA project and specifications

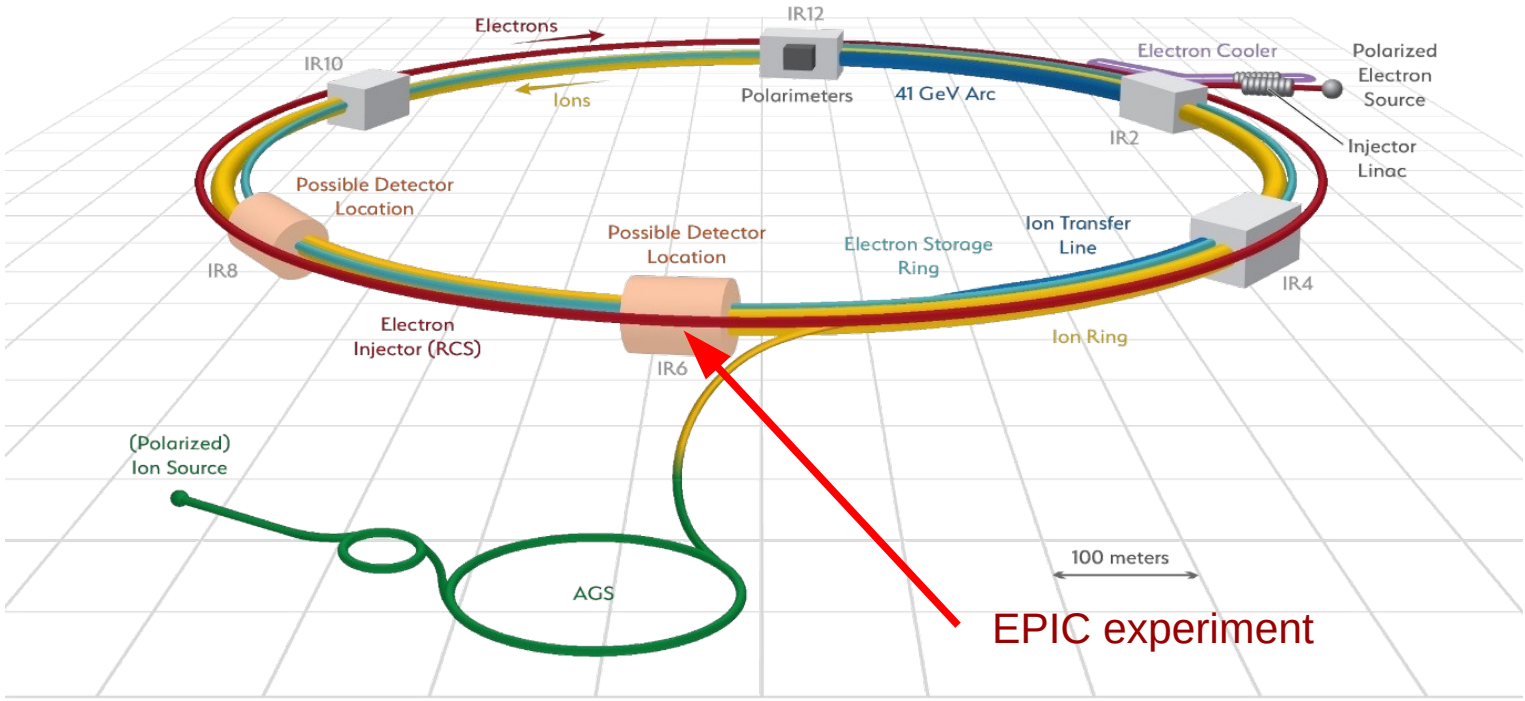
First prototype results

Prospects

THE EIC PROJECT

EIC collider

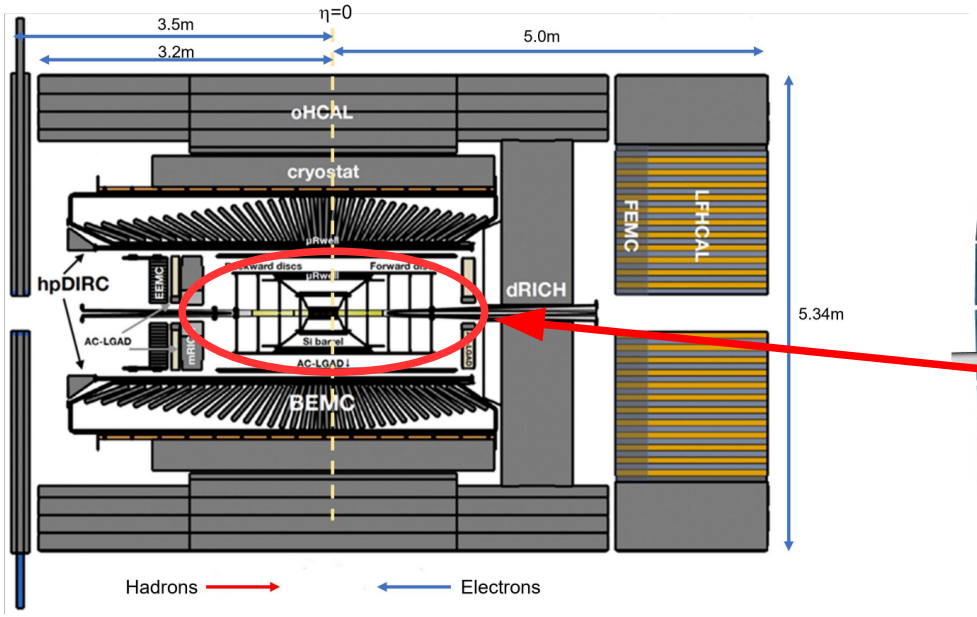
- Hadron physics: nucleon structure, quarks and gluons spins, gluon saturation, etc...
- High luminosity electron-ion collider (all nuclei from p to U) at BNL (USA), also with polarized beams: e, p, d, ^{3}He
- 5-18 GeV e^- vs 40-275 GeV p, 20-100 GeV in CoM
- First beam ~ 2032
- 2 experiments: EPIC (already financed) and "Detector 2"

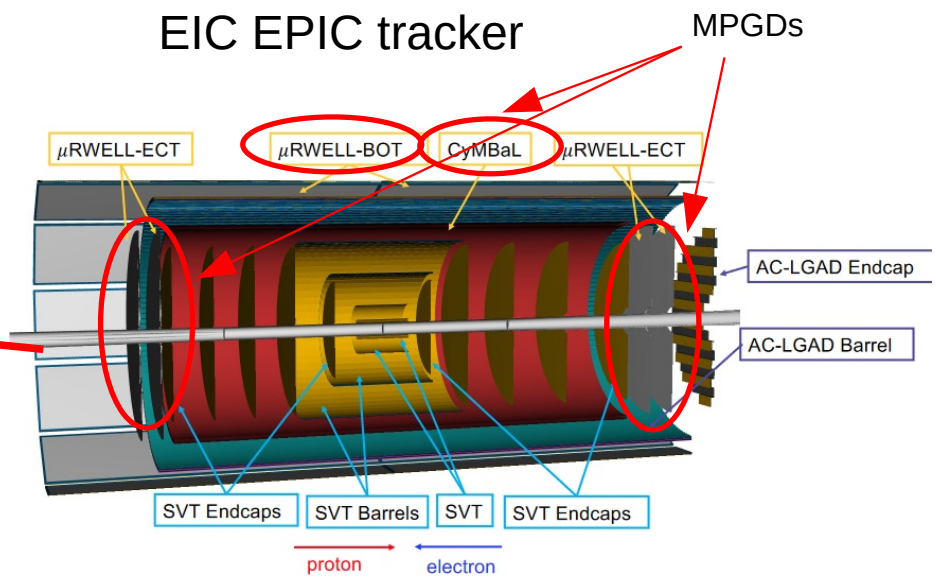


THE EPIC EXPERIMENT

EPIC detector

- 1.7 T solenoid with trackers, particle ID, calorimetry, far-forward/backward detectors
- Tracking: Silicon, MPGDs
- pID: hpDIRC, RICH, TOF (AC-LGAD 30 ps resolution)
- Tracker expected resolution: 150 μm, 10-20 ns
- MPGD trackers: cylindrical Micromegas + μRWell endcap disks (or GEM) + flat μRwell outside of TOF barrel
- DAQ with triggerless streaming readout
- SALSA ASIC: foreseen for readout of all MPGDs





SALSA : VERSATILE READOUT CHIP FOR MPGD

Motivations of the project

- To develop a new versatile multi-channel readout chip in the framework of the EIC project and beyond
  - adapted to streaming readout DAQs
  - for MPGD trackers but not only, also TPC, photon detectors,...
  - with possible future developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints (ps-level time resolutions ?)
- Integrated per-channel ADC and digital processing
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times, signal rates
- TSMC 65nm technology for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University (USP) + associated institutes designed the SAMPA chip (ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC and HGCROC TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences to collaborate on a common versatile front-end chip including digitization and digital processing
- Service blocks developed by CERN in TSMC 65nm technology are also reused

SALSA CHIP DESIRED SPECIFICATIONS

Versatile front-end characteristics

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (EPIC is limited to 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

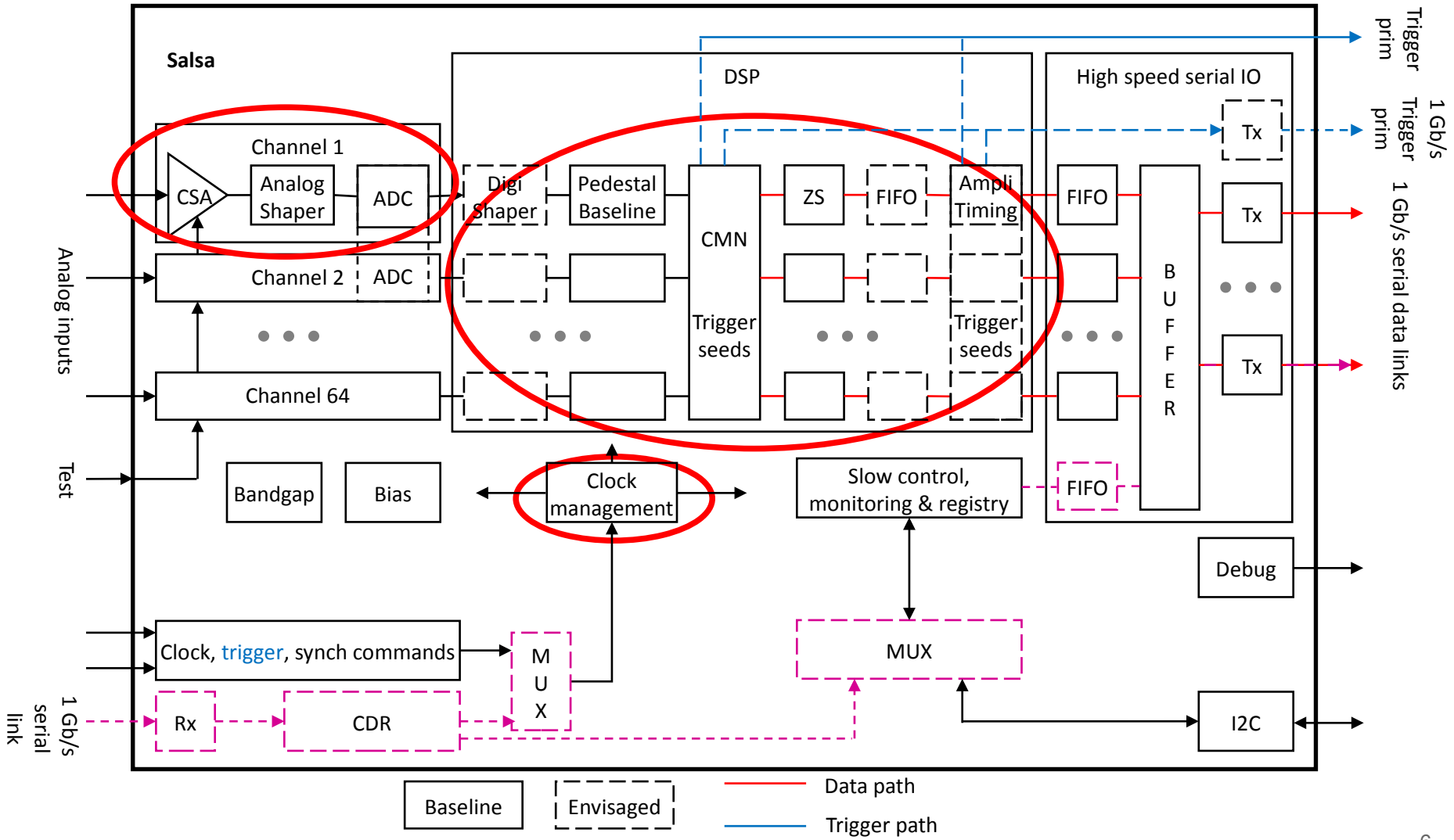
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- Input clock, fast commands and slow control to be fed both from unique signal, or from standard separated ones
- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

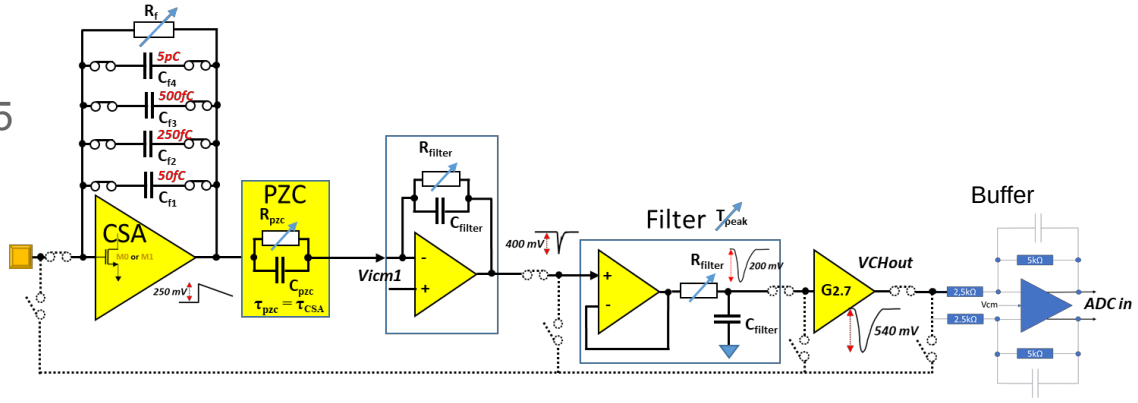
Preliminary design of SALSA



SIGNAL AMPLIFICATION AND DIGITIZATION

Front-end stage

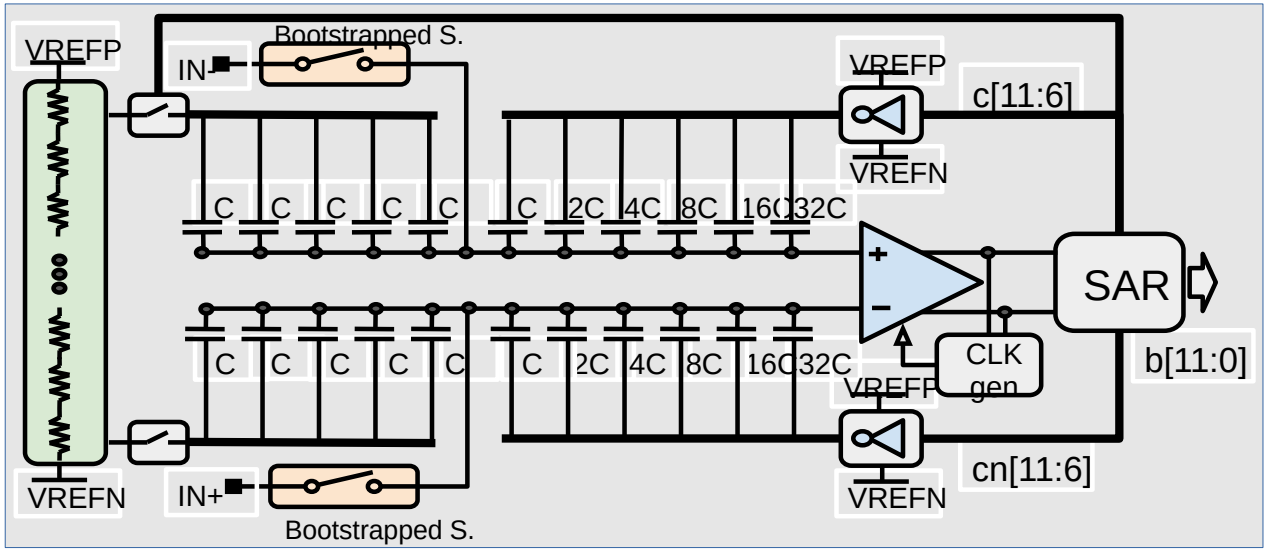
- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges from 0-50 fC to 0-5 pC
- 8 peaking times 50 to 500ns
- 2 input transistor sizes
- 2 polarities
- Integrated anti-saturation circuit
- Integrated test pulses



Scheme from P. Baron

ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits



Scheme from H. Hernandez

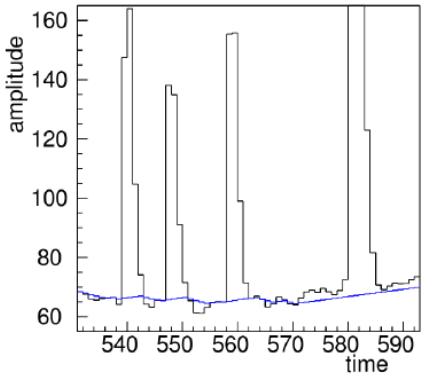
DSP DATA PROCESSING, PRELIMINARY VERSION

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Considered processes still under study, suggestions welcome !

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail if necessary

Zero suppression

- Keeping samples above fixed thresholds, possibly neighbor ones
- Possibility to keep non-ZS samples in some cases, calibrations for instance

DSP DATA PROCESSING

Feature reconstruction

- To further reduce data flux, only a few values extracted instead of a bunch of samples, possibility to keep them from time to time
- For instance peak finding algorithm: amplitude + time + TOT extraction

Trigger management

- Trigger in: Samples kept when trigger signals received
- Trigger out: primitive generation when samples above threshold
- Nature of trigger out primitives to be defined (logic signal, data on fast link, etc...)

Calibration and monitoring data, generated on demand

- Calibration data: non-ZS samples, with test pulses, etc...
- Informations on chip: configuration, status, environment, channel occupancy, etc...

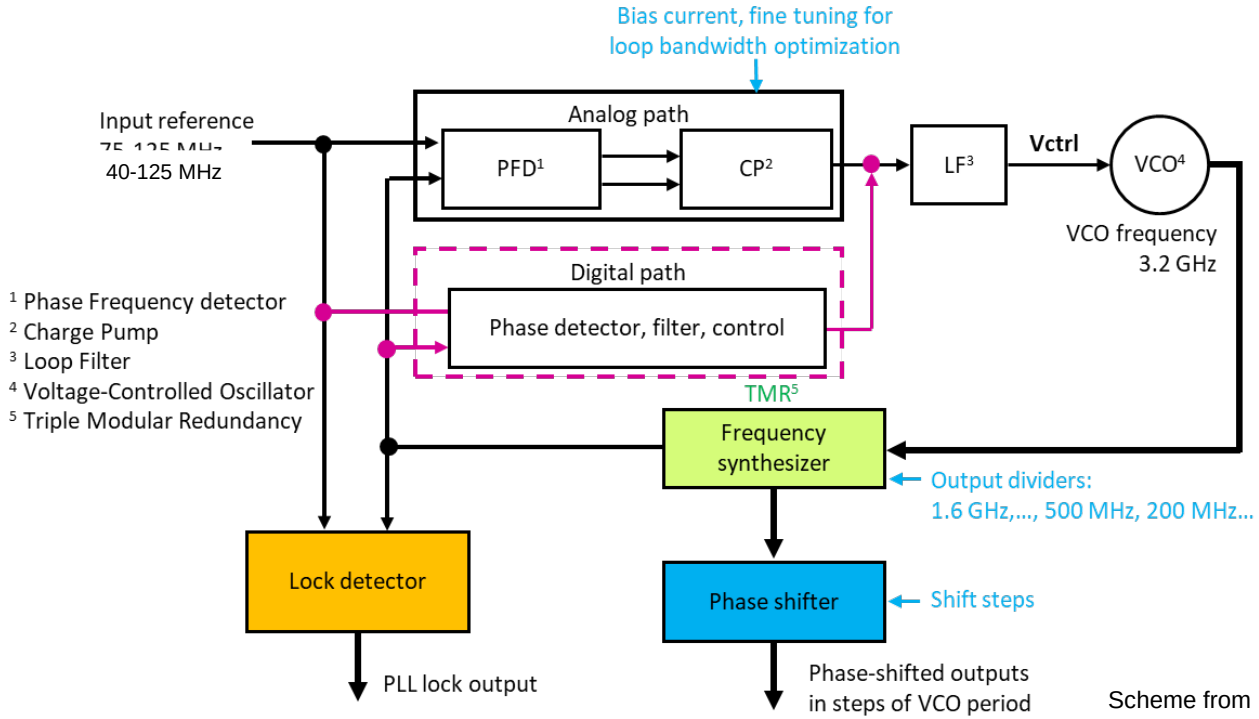
Data formatting and buffering

- Formats for ZS and non-ZS sample data, reconstructed data, monitoring data
- Output data flux segmented in packets which may contain all kinds of data
- Packet identification by numbering and timestamps
- Packet buffering and transmission over 1 or several Gbit/s links
- Generation of error packets in case of troubles

SALSA CLOCK MANAGEMENT

Development of the PRISME 65nm PLL IP block

- Motivation: no 65nm PLL block already existing meeting SALSA requirements
- Large frequency ranges for input (40-125 MHz) and outputs (up to 1.6 GHz)
- Low power and radiation hardness capability
- Hybrid PLL mixing analog and digital paths, with 3.2 GHz VCO frequency
- Very low internal time jitter: ~3 ps RMS for up to 1 GHz
- 4 clock outputs each with programmable frequency and phase
- This block will be available for HEP community



Scheme from F. Bouyjou

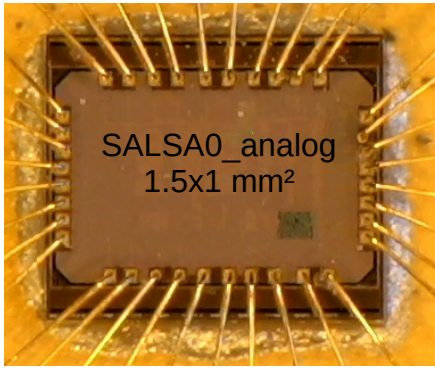
TIMELINE OF THE SALSA PROJECT

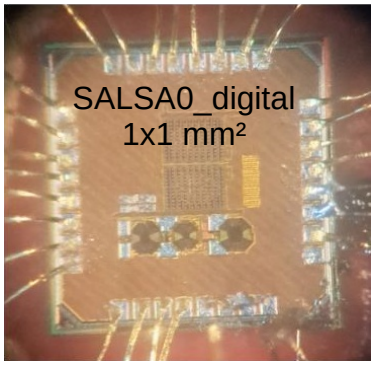
The different steps

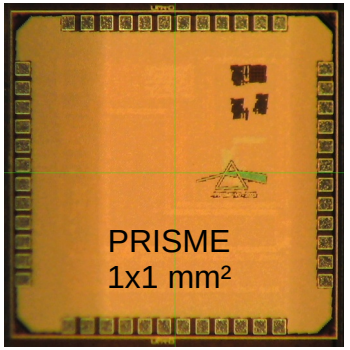
- 2020-22: Discussions and reflections on the project
- 2022-23: SALSA0 prototypes to study first designs
  - SALSA0_analog featuring 4 front-end channels
  - SALSA0_digital featuring an ADC block
- 2023: PRISME prototype for PLL block + first version of general services
- 2023-24: SALSA1 prototype to test full front-end + ADC chains
- 2023-25: SALSA2 prototype to test fully featured ASIC including DSP, but with low number of channels
- 2025-26: SALSAf as pre-serial prototype with nominal number of channels

Status of prototypes

- SALSA0 prototypes submitted in November 2022 and January 2023, tests of analog proto done, tests of digital ones in progress
- PRISME prototype dies received in December 2023, tests started end of February
- SALSA1 design ongoing, submission foreseen in April 2024
- Reflections on SALSA2 architecture and DSP data processing ongoing, submission foreseen beginning of 2025







Pictures from P. Baron, B. Sanches and F. Bouyjou

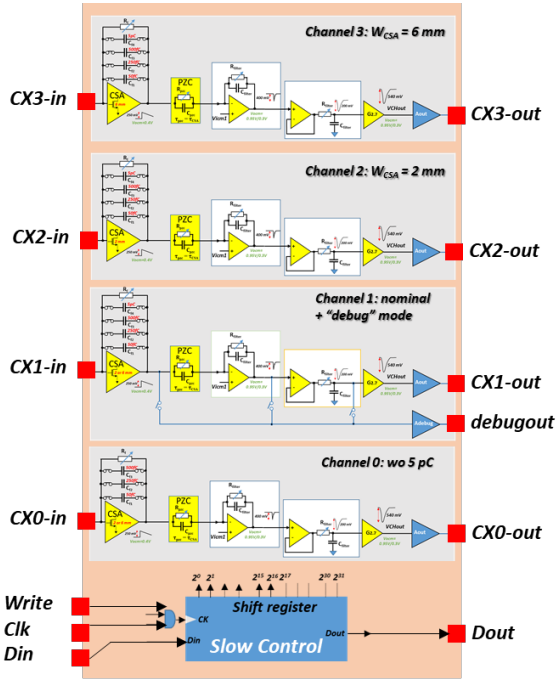
TESTS ON SALSA0 FRONT-END STAGE

SALSA0_analog prototype

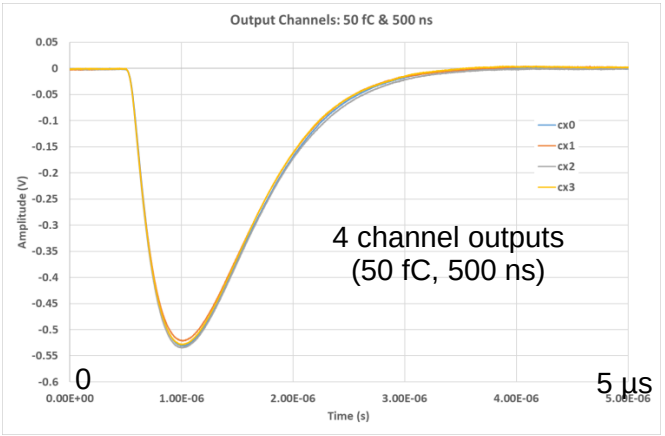
- 4 front-end channels with slight differences between them
- CX1 channel with debug output for monitoring
- CX0-2-3 with different input transistors, CX0 without 5 pC gain range

General results

- Test-bench: selectable input capacitance, input signal generation with configurable amplitude and rate, programmable oscilloscope, etc...
- Almost all configuration parameters (gains, peaking times, anti-saturation,...) were tested and work well
- Measurements in agreement with simulations: bias currents, power consumption, DC values, etc...
- Some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range
- Origin due to parasitic resistances in the chip. Now understood and reproduced in simulations. Already corrected in the charge-sensitive amplifier design
- Updated front-end stage already implemented in SALSA1 prototype design

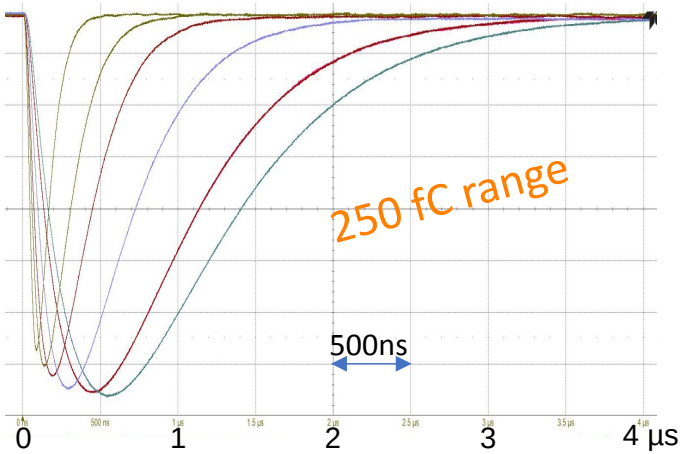


Scheme from P. Baron

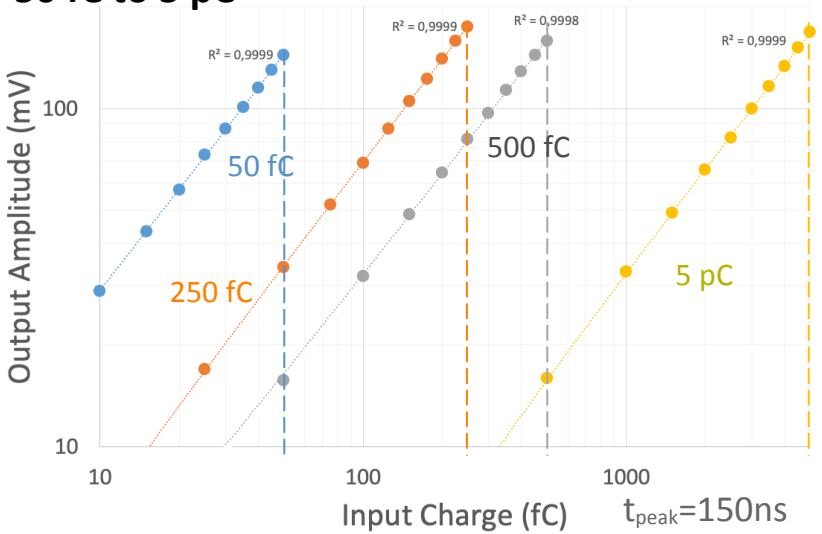


MAIN RESULTS WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

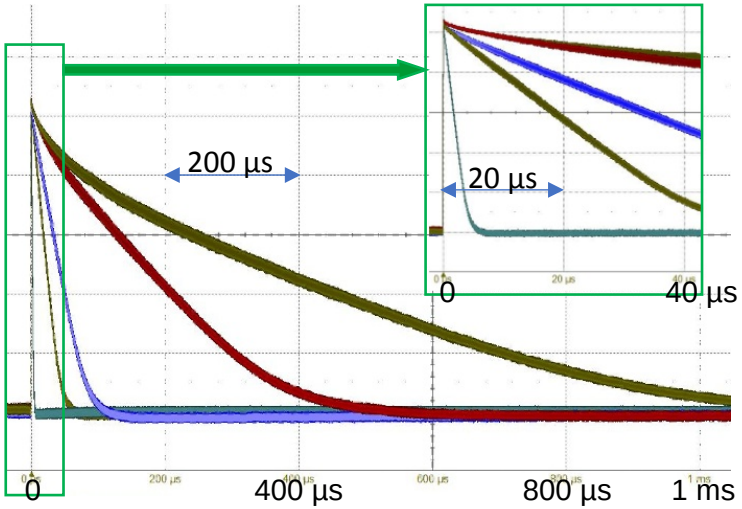


Gain programmable => dynamic range from **50 fC to 5 pC**

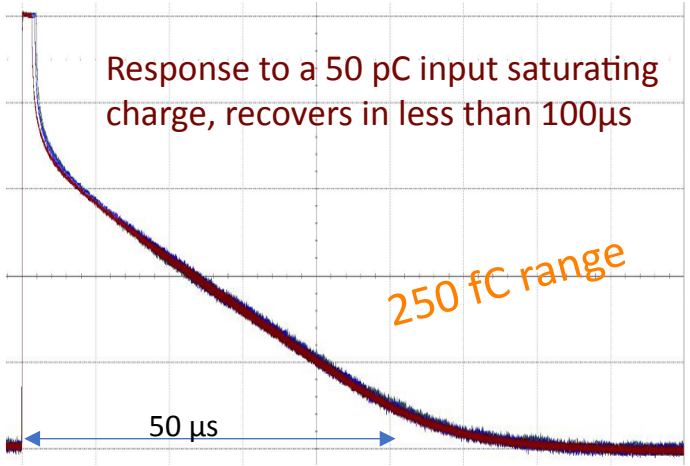


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



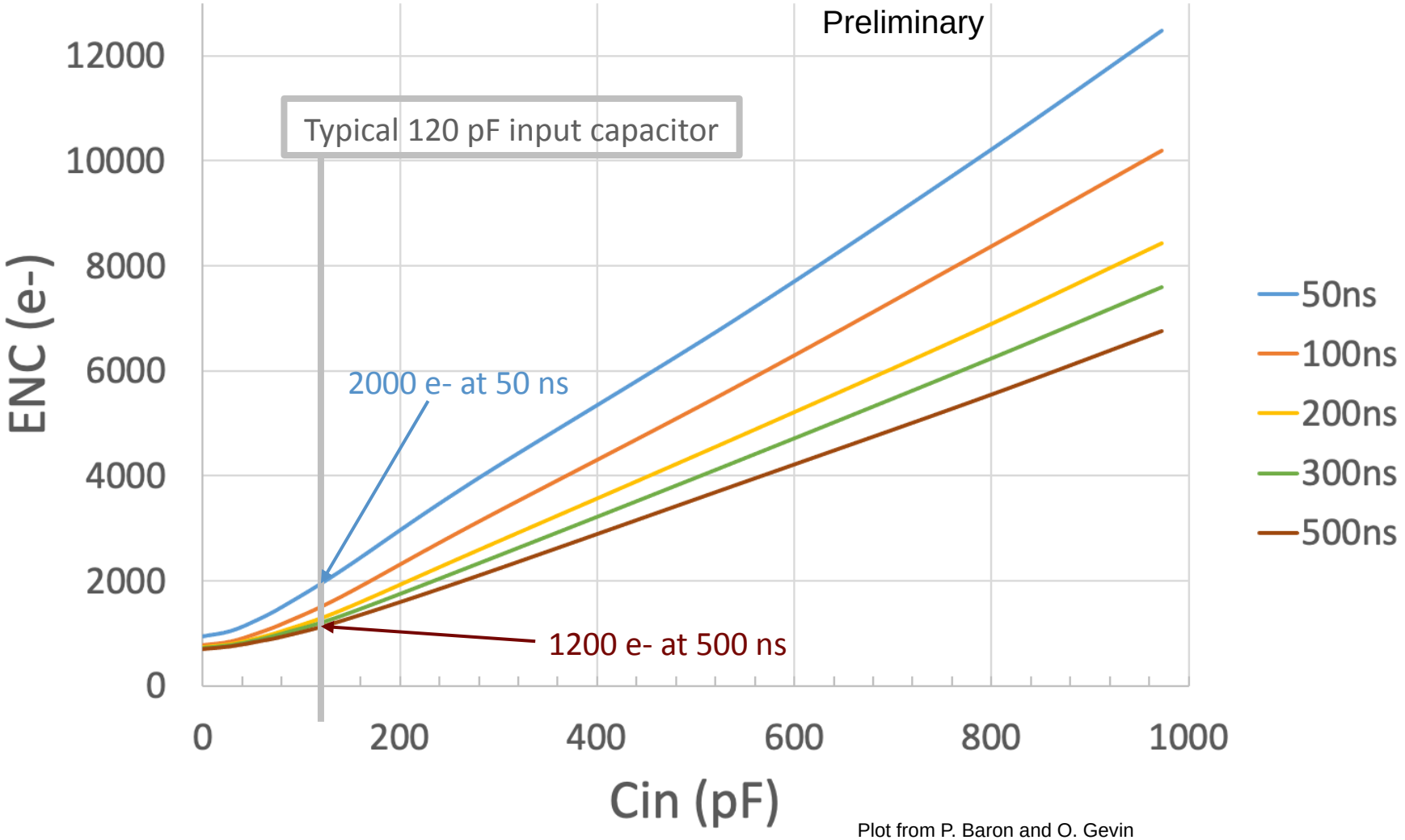
CSA anti-saturation circuit => **fast recovering**



Plots from P. Baron and O. Gevin

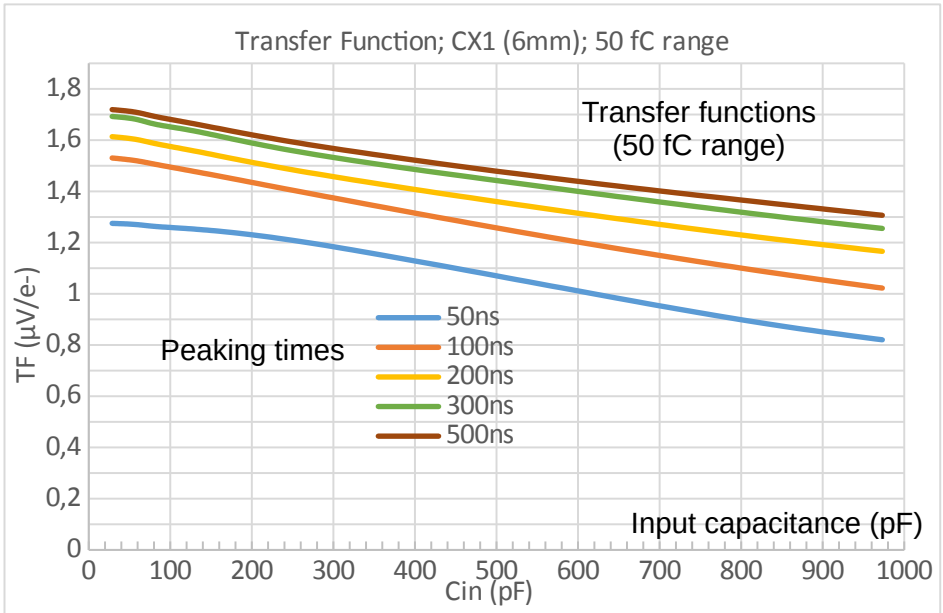
MAIN NOISE RESULTS: TYPICAL CASE

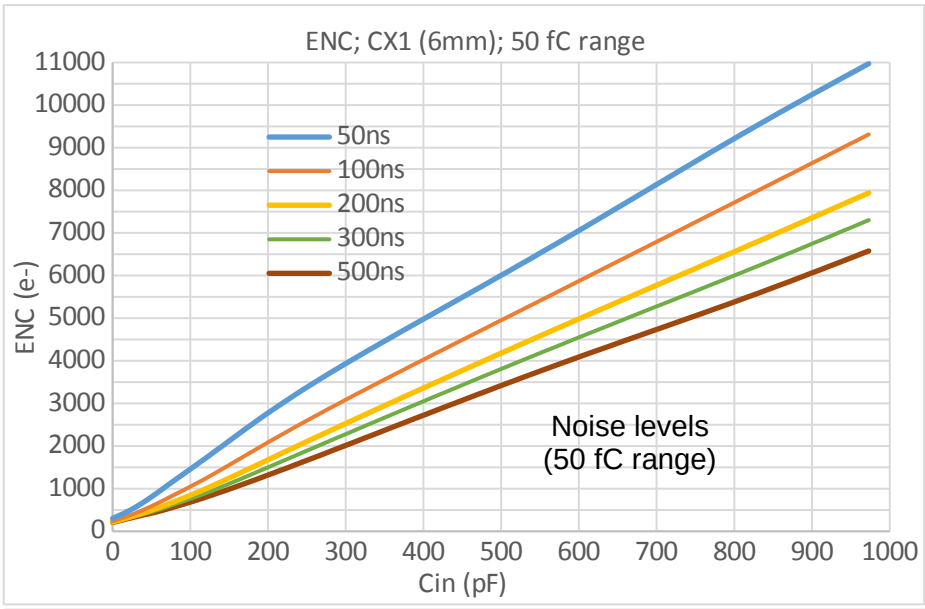
Equivalent Noise Charge in the **250 fC range** at different peaking times



Plot from P. Baron and O. Gevin

TRANSFER FUNCTIONS AND ENC FOR EXTREME GAIN RANGES





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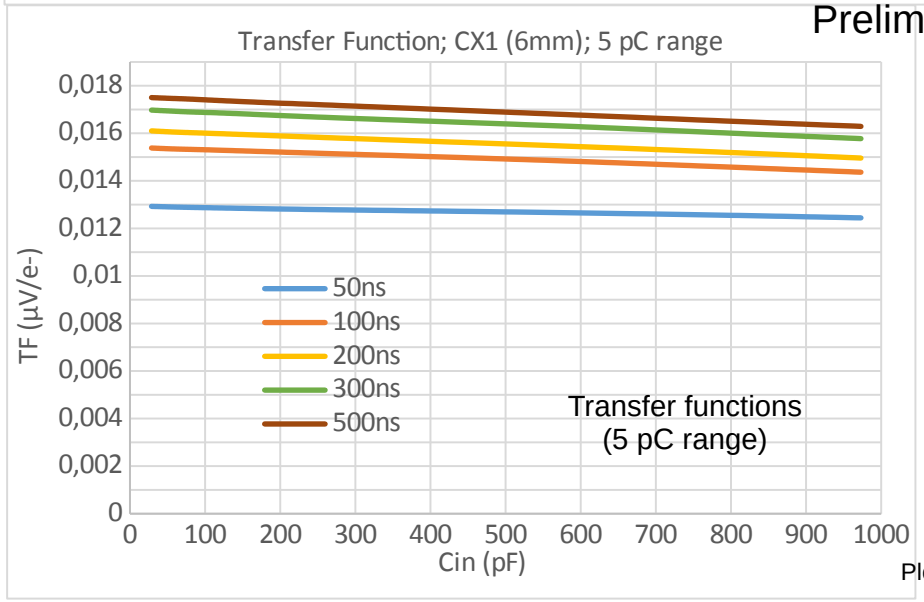
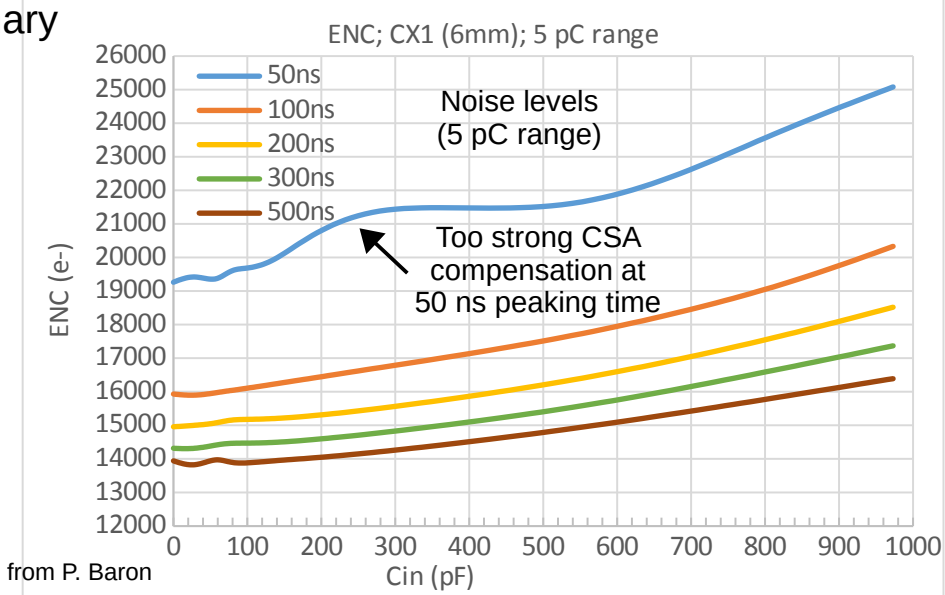




Plots from P. Baron

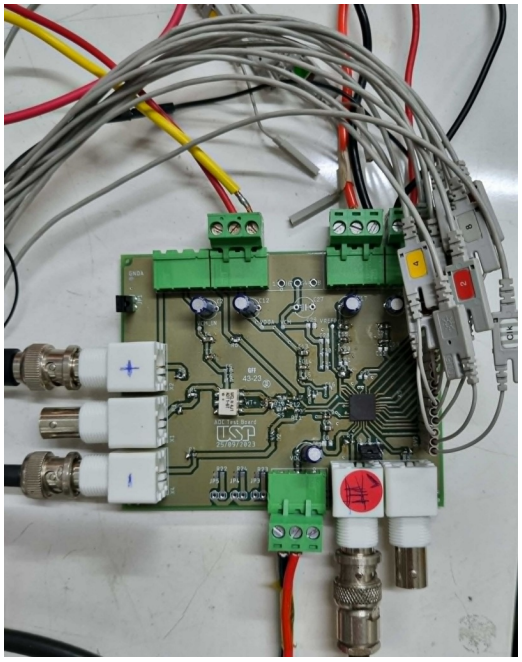
TESTS ON SALSA0 ADC BLOCK

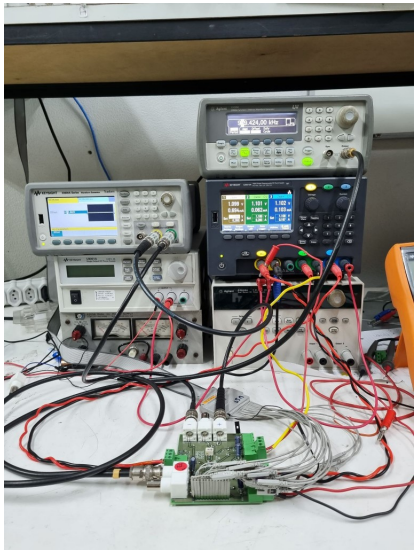
SALSA0_digital prototype

- 1 ADC block
- Test board to feed LV and clocks (sampling and conversion)
- Digital analyzer to read ADC output
- Tests started from end of November

Preliminary outcomes

- Resolution OK but max sampling rate too low, fixed in present ADC design
- Problem of offset of the digital 0, with reduced dynamic range leading to lower ENOB
- Also lower power consumption compared to simulation
- 10 more chips were packaged, but they are also affected with the same problems
- Studies ongoing in simulations, but can't reproduce these behaviors yet, to be continued





Pictures from B. Sanches

STATUS OF PRISME PROTOTYPE

Test bench

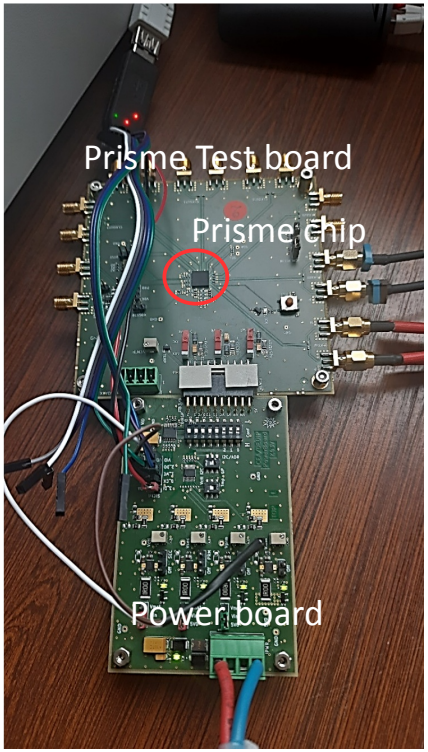
- Test of new hybrid 65nm PLL block with 4 clock outputs
- Power boards + PRISME test boards arrived February 19th and are working
- Test bench completed with low jitter clock generator from CERN + high precision signal generator, 80GS/s scope and phase noise analyzer

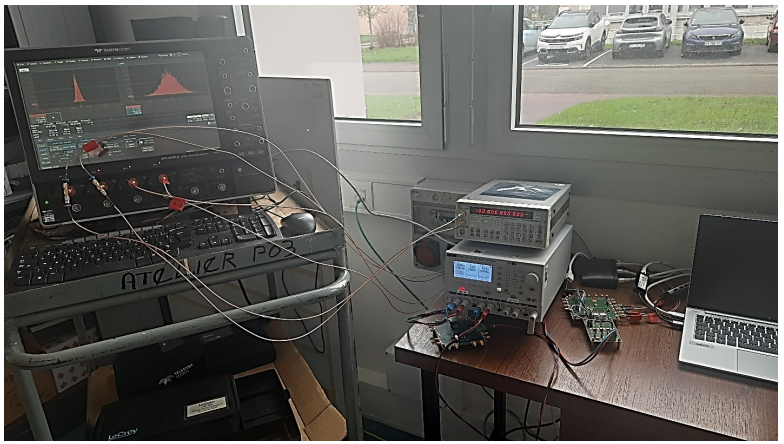
Preliminary results

- Power consumption nominal
- I2C working to read and write registers
- Low voltage differential clock signals going in and out the chip

Tests on PLL block

- Digital branch of PLL operational (allows to find the right frequency range for the analog branch)
- Oscillator driven by analog branch reaches the 3.2 GHz nominal frequency from 40 and 100 MHz input clocks, divider working properly
- 4 configurable outputs tested → deliver right requested frequencies
- Ongoing tests on jitter characterization and optimization





PRESENT STATUS AND PROSPECTS

Present status

- Development of SALSA readout ASIC for MPGD ongoing
- Performance specifications finalized, could be adapted in function of chip block study results. Still open to suggestions !
- Tests done on SALSA0 and PRISME prototypes, helpful to fix bugs, verify simulations, and evaluate performances
- Design of SALSA1 prototype (front-end + ADC) in progress, submission foreseen in April
- Studies ongoing on logic architecture and DSP data processing for SALSA2 prototype

Next steps

- Completion of tests on present prototypes
- Production and tests of SALSA1 in 2024
- Production and tests of SALSA2 in 2025
- Design of SALSAf pre-serial ASIC in 2025, production and tests in 2026
- Large scale production foreseen in 2027, expression of interest welcome !
- Compatible with the EIC project timeline