S fp connectivity and M icrotca for A dvanced R emote T rigger

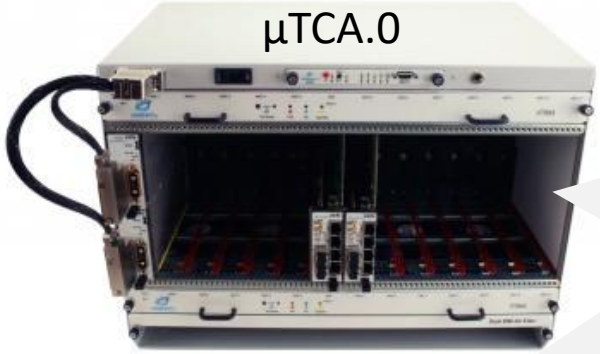
Project Status

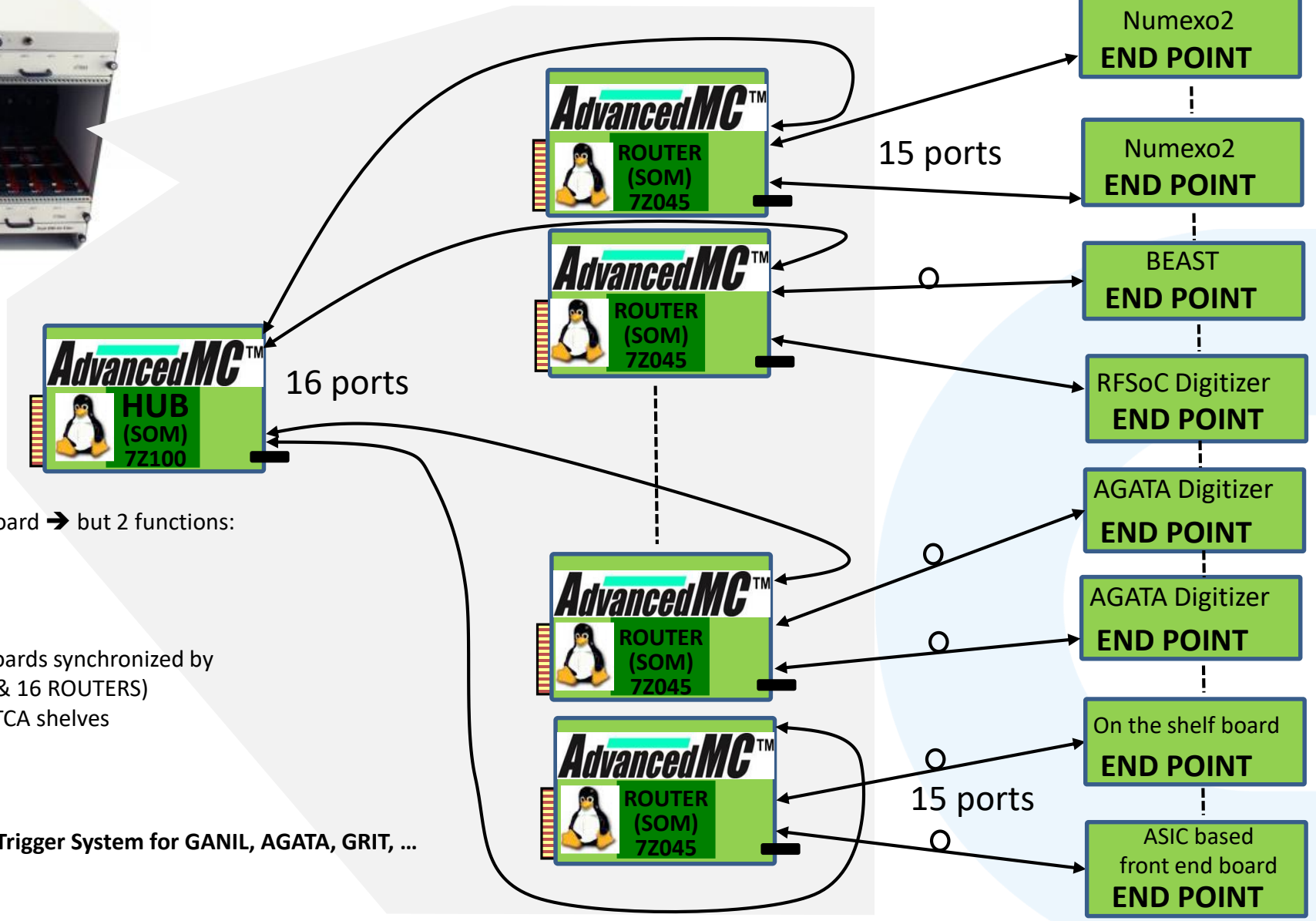
Phase 1: SMART AMC
Phase 2: SMART MCH

© O. Naves/Drakodrone

Gilles Wittwer

SMART_AMC Architecture (Phase 1)





Only one AMC carrier board ➔ but 2 functions:
- HUB
- ROUTER

Up to 240 digitizers or boards synchronized by
17 AMC's (1 HUB & 16 ROUTERS)
housed in 2 µTCA shelves

A new Timestamping and Trigger System for GANIL, AGATA, GRIT, … and available for any Lab

A - Main characteristics (Phase 1)

COMMUNICATION RATES

- **HUB ↔ ROUTER**: Line Rate = 4 Gb/s; Payload Data Rate = 400 MB/s; Reference Clock = 100 MHz

- **ROUTER ↔ EP's**: Line Rate = 2 Gb/s; Payload Data Rate = 200 MB/s; Reference Clock = 100 MHz

CLOCK & TIMESTAMPING

- **HUB to ROUTER (to EP's)** : 8B/10B encoding/decoding with Recovered Clock = 100 MHz;
  TS on 48 bits/10ns (more than 1 month of experiment)

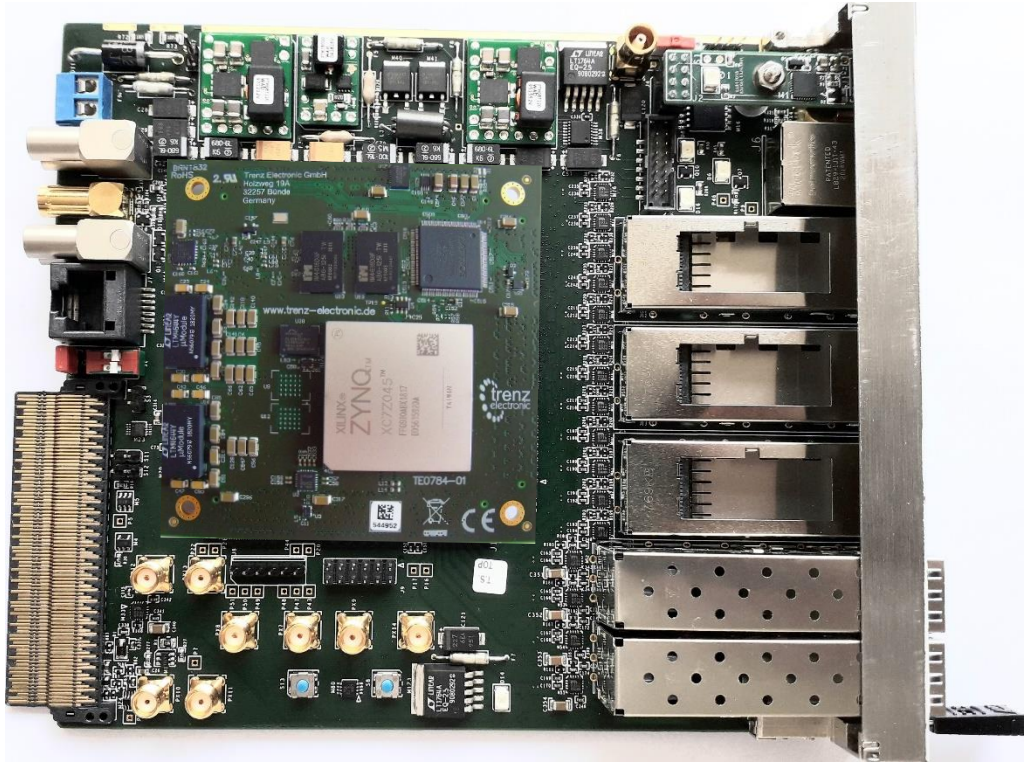
AUTOMATIC ALIGNMENT

- **HUB to EP's** : with external TDC chip

TRIGGER @ HUB LEVEL

- **Trigger req./val.** : based on uplink and downlink frames (build with EP ID recognition/digitizer type)
- **Multi-partitions** : 240, 480, up to 720 digitizer channels (typically 45x16ch-NUMEXO2 boards)
- **Multiplicity** : threshold by partition
- **Acceptance window**: for late channels arriving during a trigger cycle
- **Logic Equation** : (OR/AND/NOT) between partitions for the final decision (ACCEPT/REJECT)
- **32 bit Event Number** : for accepted returned frames
- **Max 208 KHz/channel – Total trigger rate @HUB level: 800 Mtrig_req/s**

SMART AMC status in terms of Hardware and Production



SOM and SOC USED on SMART AMC BOARD (Phase 1)

- **HUB**: TE0784-01 from TRENZ Company with Xilinx XC7Z100-2FFG900I
- **ROUTER** : TE0784-01 from TRENZ Company with Xilinx XC7Z045-2FFG900I

Production: 26 SOM ordered in 2023 for GANIL (2H/10R) and AGATA (14R)
26 SMART_AMC boards will be assembled in 2024

New communication media qualified for SMART
(all them remotely identified by “SFP_QSFP_device_checker”

SFP+ to SFP+
(10Gb/s passive cables)

2 Finisar SFP transceivers
One 6.1 Gb/s and one 8.5 Gb/s
(more than 150 m with OM3 fiber)

- Four-channel full-duplex transceiver module
- Hot Pluggable QSFP+ form factor
- Maximum link length of 100m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel

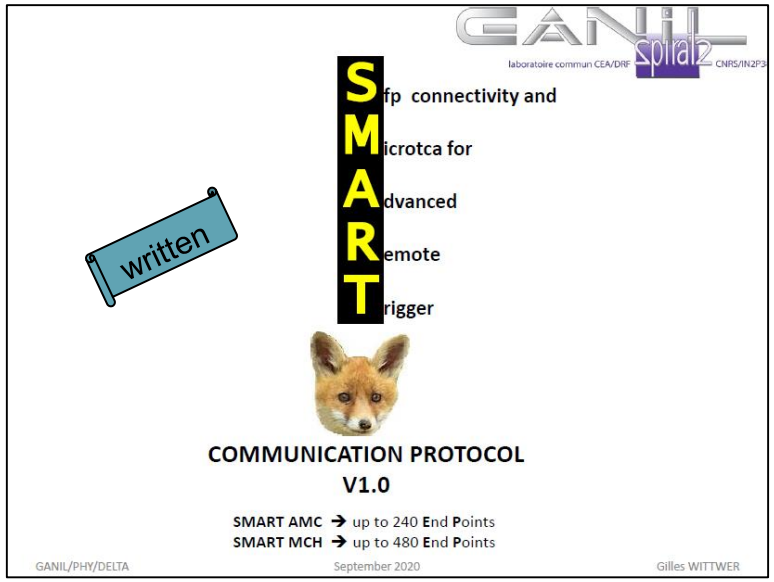
QSFP to MPO
(Finisar FTL410 series)

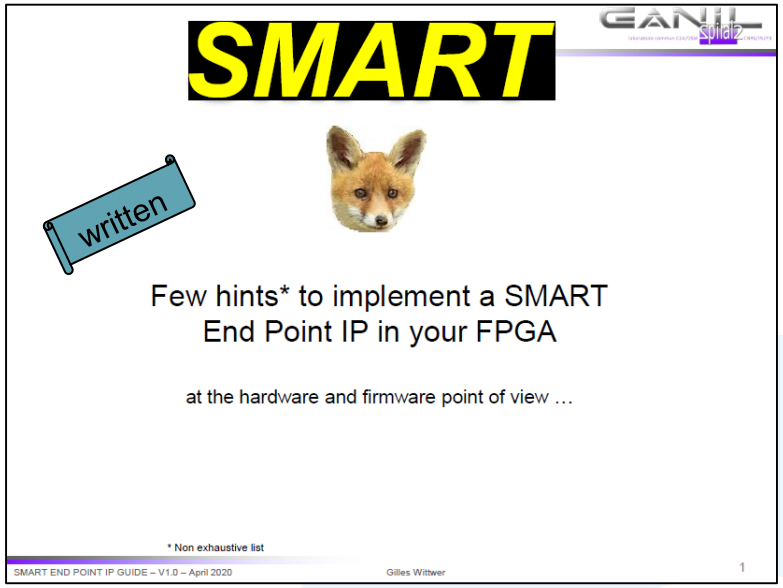
QSFP to 4xSFP+
(40G breakout passive cables)

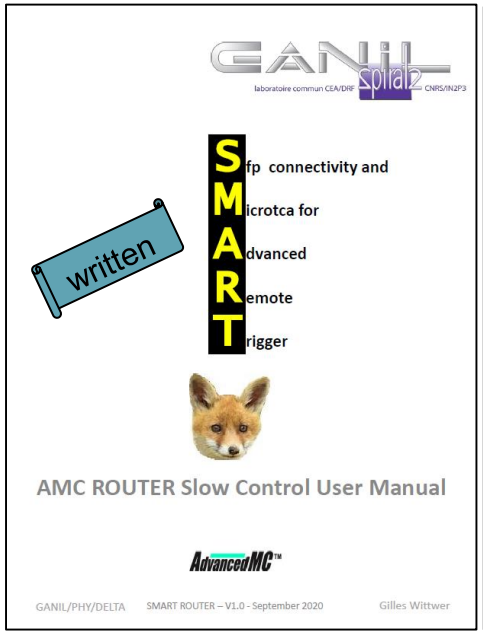
Fiber MPO to 4 x 2 Fiber MPO Duplex LCs

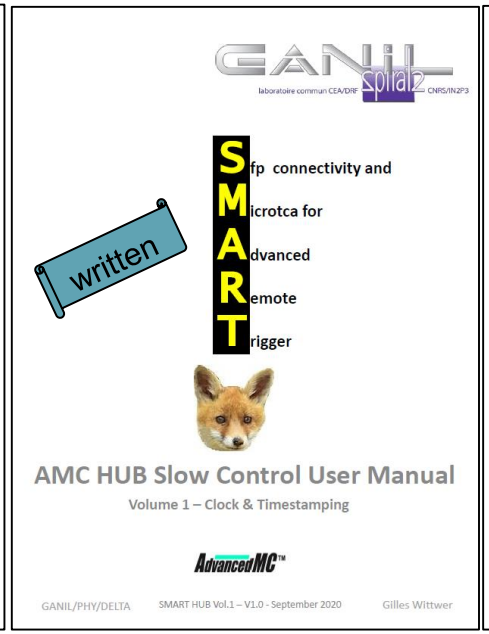
QSFP(ch.1) to SFP adapter
(Useful with passive cables
or transceivers)

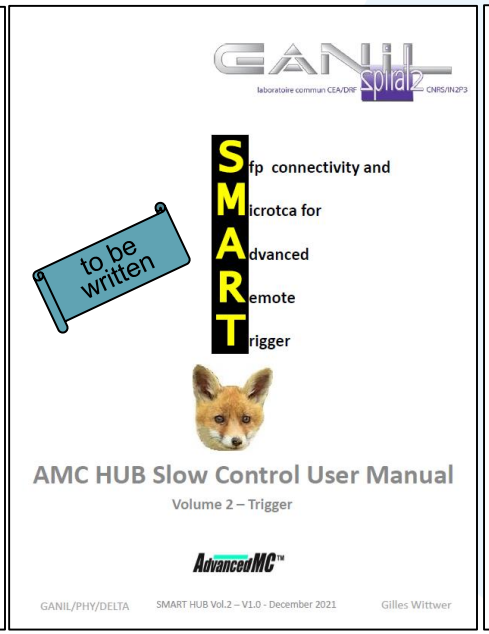
SMART - Phase 1 Documentation

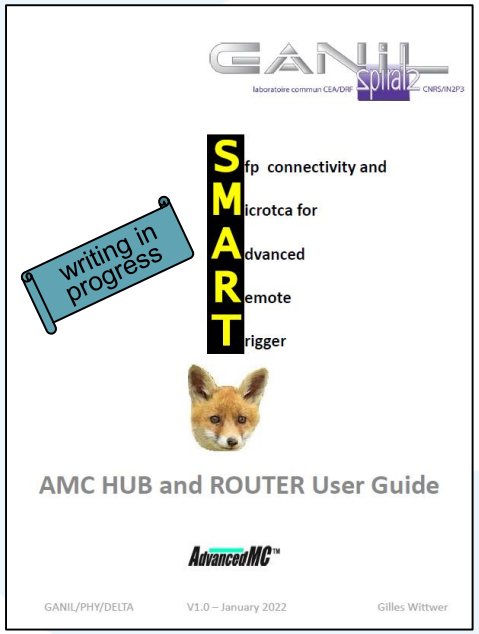












SMART AMC delay measurement results 1/2

SMART HUB - ttyUSB2

Fichier Éditer Affichage Terminal Onglets Aide

```
*** Delay results port by port for the current SMART HUB (delay in ps) ***


HUB port: 0 not connected ...

HUB port: 1 not connected ...

HUB port: 2
ROUTER port: 0 Min Delay:       0  Mean Delay:       0  Max Delay:       0  D=       0
ROUTER port: 1 Min Delay:       0  Mean Delay:       0  Max Delay:       0  D=       0
ROUTER port: 2 Min Delay:       0  Mean Delay:       0  Max Delay:       0  D=       0
ROUTER port: 3 Min Delay:       0  Mean Delay:       0  Max Delay:       0  D=       0
ROUTER port: 4 Min Delay:       0  Mean Delay:       0  Max Delay:       0  D=       0
ROUTER port: 5 Min Delay:       0  Mean D
ROUTER port: 6 Min Delay:       0  Mean D
ROUTER port: 7 Min Delay:       0  Mean D
ROUTER port: 8 Min Delay:       0  Mean D
ROUTER port: 9 Min Delay:       0  Mean D
ROUTER port:10 Min Delay:       0  Mean D
ROUTER port:11 Min Delay:       0  Mean D
ROUTER port:12 Min Delay:       0  Mean D
ROUTER port:13 Min Delay:  190080  Mean D
ROUTER port:14 Min Delay:       0  Mean D

HUB port: 3
ROUTER port: 0 Min Delay:       0  Mean D
ROUTER port: 1 Min Delay:  158166  Mean D
ROUTER port: 2 Min Delay:       0  Mean D
ROUTER port: 3 Min Delay:       0  Mean D
ROUTER port: 4 Min Delay:       0  Mean D
ROUTER port: 5 Min Delay:       0  Mean D
ROUTER port: 6 Min Delay:       0  Mean D
ROUTER port: 7 Min Delay:       0  Mean D
ROUTER port: 8 Min Delay: 1113102  Mean D
ROUTER port: 9 Min Delay:       0  Mean D
ROUTER port:10 Min Delay:       0  Mean D
ROUTER port:11 Min Delay:       0  Mean D
ROUTER port:12 Min Delay:       0  Mean D
ROUTER port:13 Min Delay:       0  Mean D
ROUTER port:14 Min Delay:       0  Mean D

HUB port: 4 not connected ...

HUB port: 5 not connected ...

HUB port: 6 not connected ...

HUB port: 7 not connected ...

HUB port: 8 not connected ...

HUB port: 9 not connected ...

HUB port:10 not connected ...

HUB port:11 not connected ...

HUB port:12 not connected ...

HUB port:13 not connected ...

HUB port:14 not connected ...

HUB port:15 not connected ...

For this SMART HUB, the most delayed port is EP: 53  HUB PORT: 3  ROUTER PORT: 8
                and the least delayed port is EP: 46  HUB PORT: 3  ROUTER PORT: 1
```

HUB CH.	ROUTER CHANNEL (fine delays are in ps)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
2	X	X	X	X	X	X	X	X	X	X	X	X	X	95081	X	
3	X	79109	X	X	X	X	X	X	556669	X	X	X	X	X	X	
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
8	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
9	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
11	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
13	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

A total of 3 end-point fine delay(s) have been measured (half loop)

SMART AMC delay measurement results 2/2

*** Coarse delay results port by port for the current SMART HUB (delay in ps) ***

HUB port: 0 not connected

HUB port: 1 not connected

HUB port: 2
ROUTER port: 0 Min Delay:
ROUTER port: 1 Min Delay:
ROUTER port: 2 Min Delay:
ROUTER port: 3 Min Delay:
ROUTER port: 4 Min Delay:
ROUTER port: 5 Min Delay:
ROUTER port: 6 Min Delay:
ROUTER port: 7 Min Delay:
ROUTER port: 8 Min Delay:
ROUTER port: 9 Min Delay:
ROUTER port:10 Min Delay:
ROUTER port:11 Min Delay:
ROUTER port:12 Min Delay:
ROUTER port:13 Min Delay:
ROUTER port:14 Min Delay:

HUB port: 3
ROUTER port: 0 Min Delay:
ROUTER port: 1 Min Delay:
ROUTER port: 2 Min Delay:
ROUTER port: 3 Min Delay:
ROUTER port: 4 Min Delay:
ROUTER port: 5 Min Delay:
ROUTER port: 6 Min Delay:
ROUTER port: 7 Min Delay:
ROUTER port: 8 Min Delay:
ROUTER port: 9 Min Delay:
ROUTER port:10 Min Delay:
ROUTER port:11 Min Delay:
ROUTER port:12 Min Delay:
ROUTER port:13 Min Delay:
ROUTER port:14 Min Delay:

HUB port: 4 not connected

HUB port: 5 not connected

HUB port: 6 not connected

HUB port: 7 not connected

HUB port: 8 not connected

HUB port: 9 not connected

HUB port:10 not connected ...

HUB port:11 not connected ...

HUB port:12 not connected ...

HUB port:13 not connected ...

HUB port:14 not connected ...

HUB port:15 not connected ...

HUB CH.	ROUTER CHANNEL (coarse + fine) delays are in ps)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X	X	X	X	X	X	594688	X	X
3	X	760442	X	X	X	X	X	X	1061963	X	X	X	X	X	X	X
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
8	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
9	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
11	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
13	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

A total of 3 end-point coarse delay(s) have been measured most del. Hport 3, Rport 8, - least del. Hport 2, Rport 13

SMART AMC – End Point delay setup

-- True End Point coarse/fine delays are the following ...

HUB CH.	ROUTER CHANNEL (delays to set in registers)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
2	X	X	X	X	X	X	X	X	X	X	X	X	X	0/ 0	X	
3	X	10/23F	X	X	X	X	X	X	2E/2D7	X	X	X	X	X	X	
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
8	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
9	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
11	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
13	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

3 Sets of HEXADECIMAL end-point delay values are now available for correction ...

June 2023 – One month of test

Fichier Édition Affichage Reche

```
connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd5f268879fd
beast-2: 0xcd5f268879fe
beast-3: 0xcd5f268879fe
diffs: -1 -1 0
current out of limits=0
pulse counter = 1009959

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd5f6d95627e
beast-2: 0xcd5f6d95627e
beast-3: 0xcd5f6d95627e
diffs: 0 0 0
current out of limits=0
pulse counter = 1009960

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd5fb4bd8cc7
beast-2: 0xcd5fb4bd8cc7
beast-3: 0xcd5fb4bd8cc7
diffs: 0 0 0
current out of limits=0
pulse counter = 1009961

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd5ffbf60a7b
beast-2: 0xcd5ffbf60a7b
beast-3: 0xcd5ffbf60a7b
diffs: 0 0 0
current out of limits=0
pulse counter = 1009962

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd6043c86cdf
beast-2: 0xcd6043c86cdf
beast-3: 0xcd6043c86cdf
diffs: 0 0 0
current out of limits=0
pulse counter = 1009963

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd608b096d64
beast-2: 0xcd608b096d65
beast-3: 0xcd608b096d65
diffs: -1 -1 0
current out of limits=0
pulse counter = 1009964

connected BEASTs are: 1 2 3.
pulse on beast-1
beast-1: 0xcd60d27e5d2f
beast-2: 0xcd60d27e5d2f
beast-3: 0xcd60d27e5d30
diffs: 0 -1 -1
current out of limits=0
pulse counter = 1009965
```

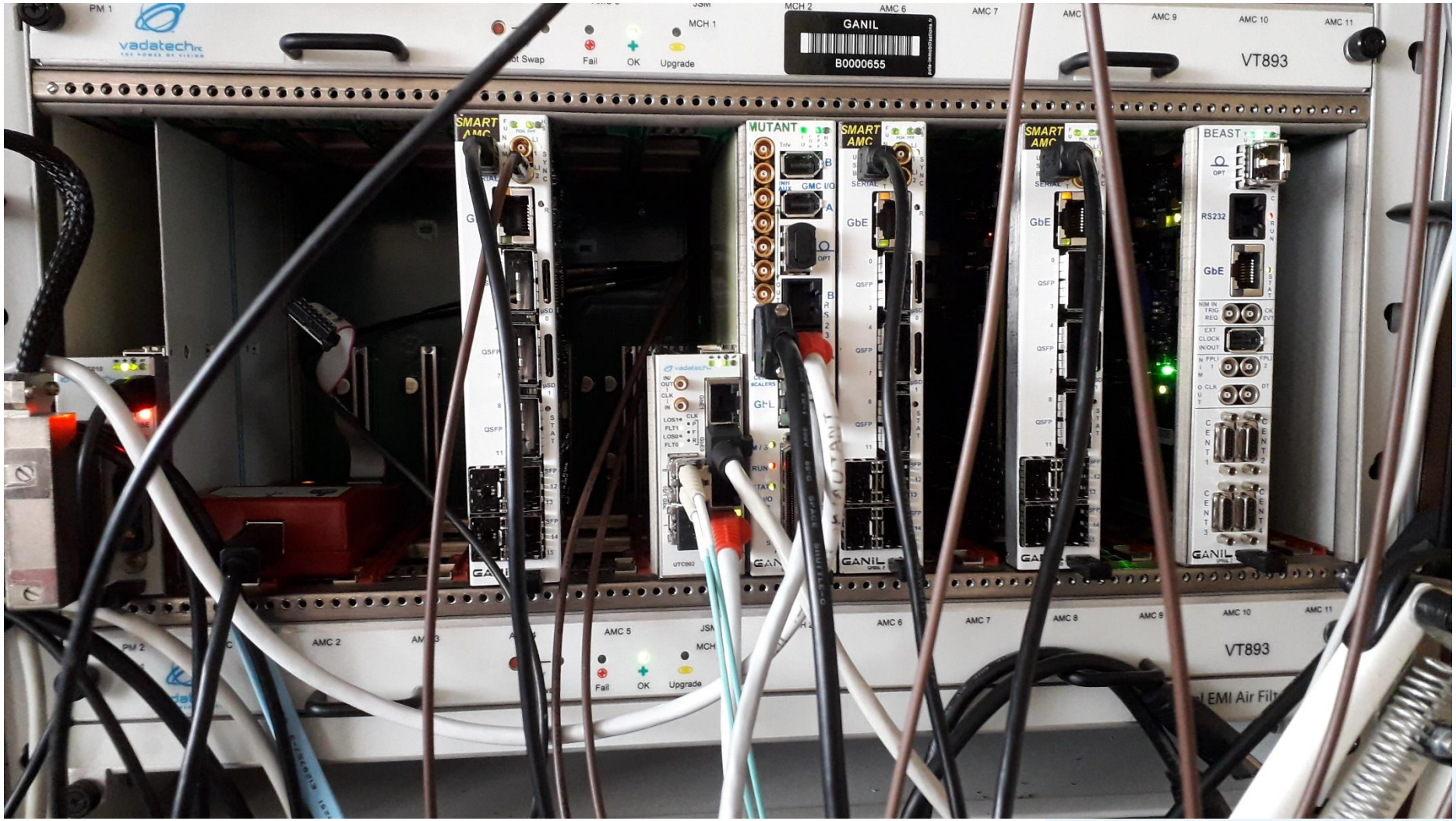
Involved manpower in SMART project and Updated schedule for SMART AMC (Phase 1)

A minimum of 7 people involved in the project:

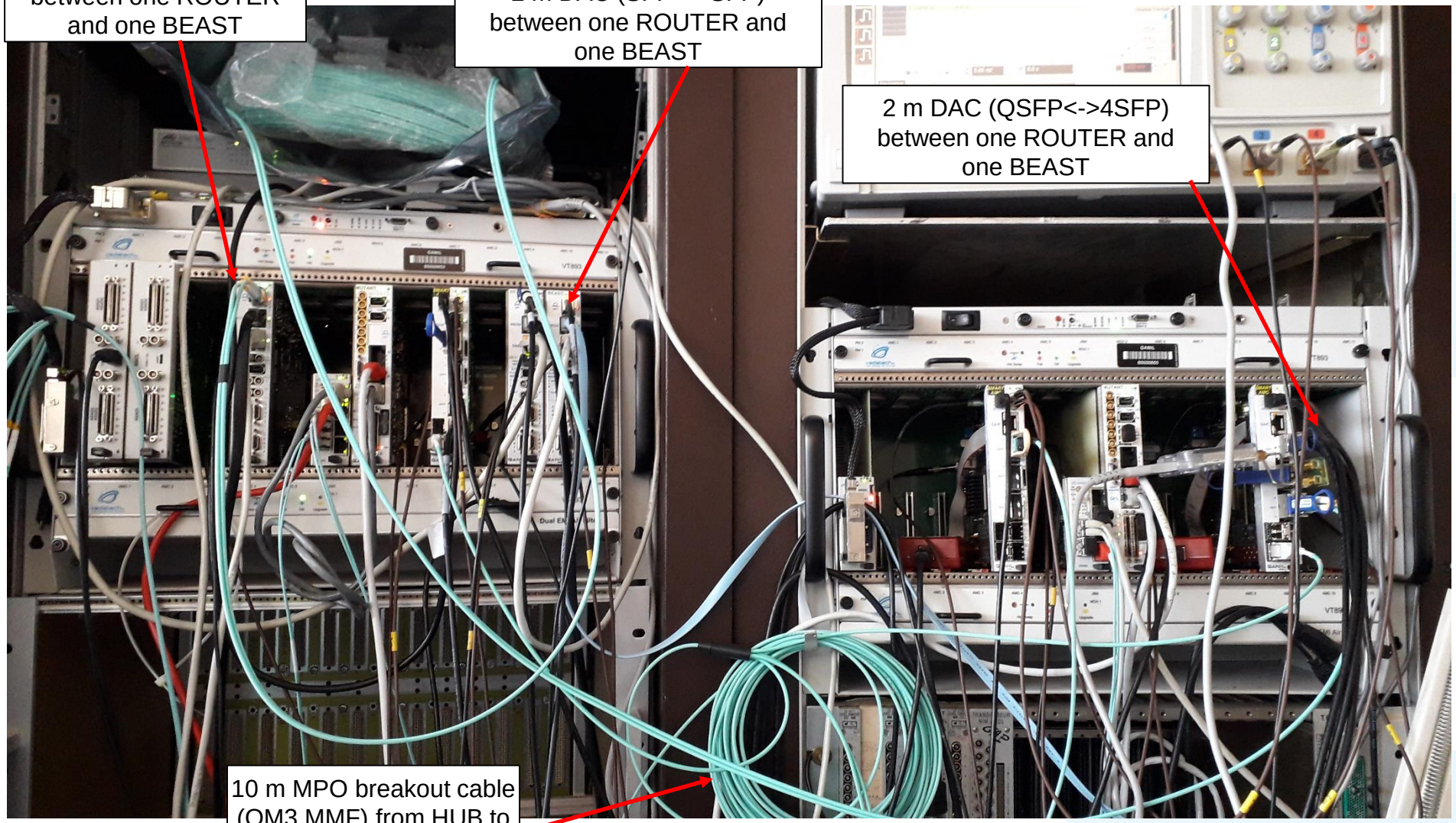
- Project leader, global architecture, firmware, software, CAD:……Gilles Wittwer
- PCB Routing, component ordering, manufacturing follow-up: .....Maria Blaizot
- Embedded software (Linux OS, slow control): ……Sébastien Coudert/Frédéric Saillant
- CPLD firmware: ……Patrice Bourgault
- SMART IP in NUMEXO2, Production Tests and Trigger features.....**Matthieu Bezard**
- SMART GUI: ……..Blandine Duclos

Main tasks	Main key dates
• 6 SMART AMC prototypes tested and SMART concept validated	• June 2022
• Annual GANIL project review	• July 2022
• Final firmware versions ready for HUB and ROUTER (CLK & TS)	• July 2023
• Green light for SMART AMC production over 2 years (SOM, active components and µTCA FP mechanics purchase)	• April -> October 2023
• Embedded Linux with automatic alignment included	• June 2024
• Specifications ready for “French public market” production	• April 2024
• Subcontractor selected for assembly of 26 SMART AMC boards	• May 2024
• Delivery of SMART AMC production	• Summer 2024

Tests of SMART AMC in one µTCA

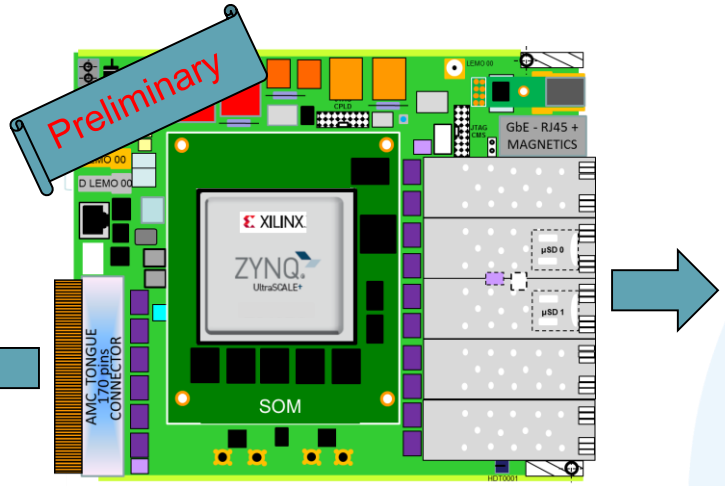


Few pictures of SMART AMC test bench



AGATA week 2022, my last slide was:

Main requirement: Increasing the number of EP's (digitizers) from 240 to 480 !



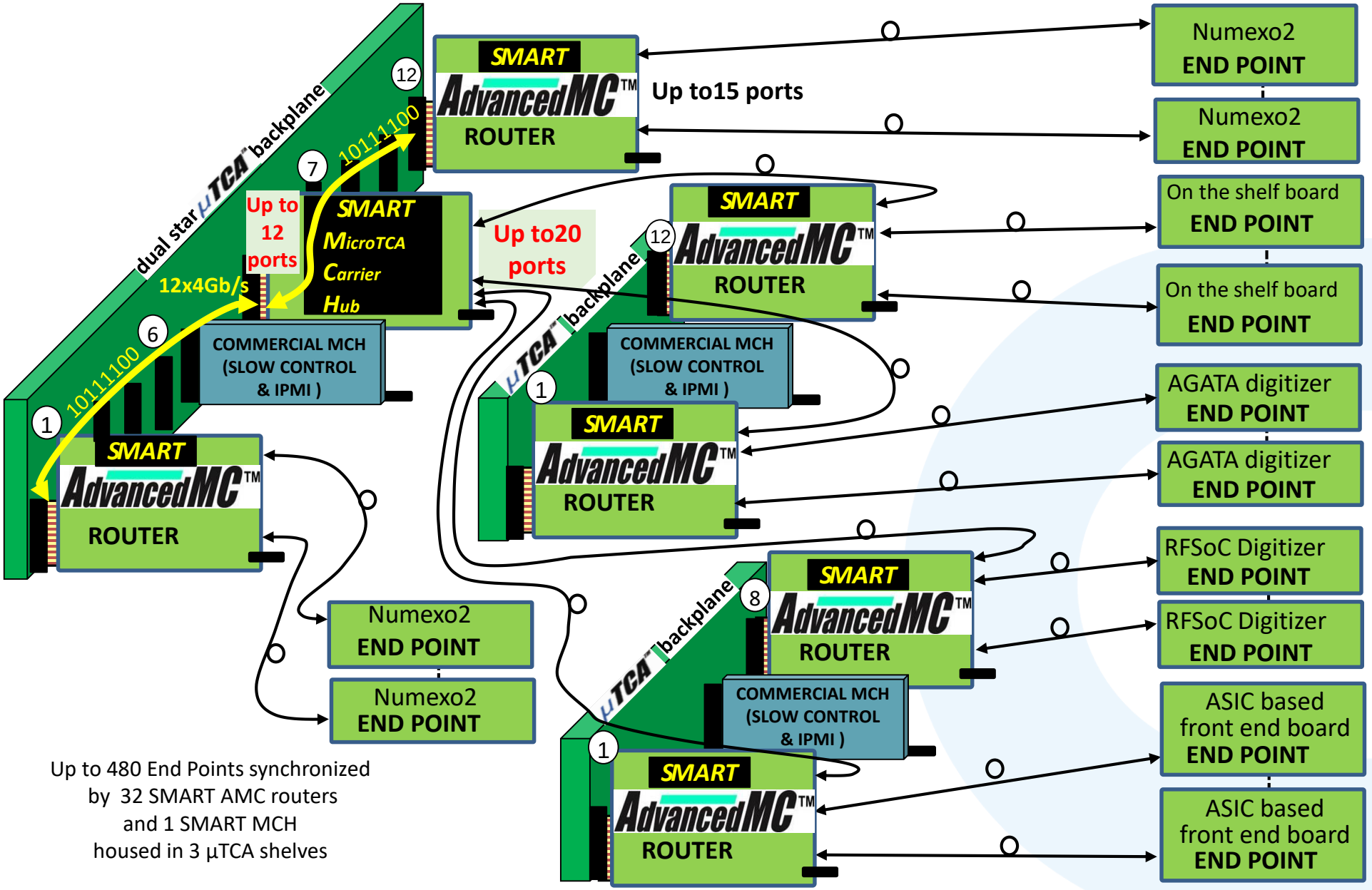
To 12 Routers

5 QSFP - To 20 Routers

A total of 32 transceivers is required

Conclusion, strong demand for SMART MCH construction ⇨ Phase 2

SMART (Phase 2) Full Architecture



Up to 480 End Points synchronized
by 32 SMART AMC routers
and 1 SMART MCH
housed in 3 µTCA shelves

Zynq-7000 vs Zynq UltraSCALE+ ZU19 vs latest Kintex UltraSCALE+ KU19P

Zynq-7000 SoCs

	Device Name	Z-7045	Z-7100
	Part Number	XC7Z045	XC7Z100
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	350K	444K
	Look-Up Tables (LUTs)	218,600	277,400
	Flip-Flops	437,200	554,800
	Block RAM (# 36 Kb Blocks)	19.2 Mb (545)	26.5 Mb (755)
	DSP Slices (18x25 MACCs)	900	2,020
	Peak DSP Performance (Symmetric FIR)	1,334 GMACs	2,622 GMACs
		16 x GTX |	16 x GTX

SMART AMC
ROUTER | HUB

Zynq® UltraScale+™ MPSoCs

Device Name	ZU19EG	
System Logic Cells (K)	1,143	
CLB Flip-Flops (K)	1,045	
CLB LUTs (K)	523	
Max. Distributed RAM (Mb)	9.8	
Total Block RAM (Mb)	34.6	(984)
UltraRAM (Mb)	36.0	128
Clock Management Tiles (CMTs)	11	
DSP Slices	1,968	
PCI Express® Gen 3x16 / Gen4x8	5	
150G Interlaken	4	
100G Ethernet MAC/PCS w/RS-FEC	4	
AMS - System Monitor	1	
GTH 16.3Gb/s Transceivers	44	
GTY 32.75Gb/s Transceivers	28	

SMART MCH 1st candidate

KINTEX UltraSCALE+

Kintex® UltraScale+™ FPGA

Device Name	KU19P	
System Logic Cells (K)	1,843	
CLB Flip-Flops (K)	1,685	
CLB LUTs (K)	842	
Max. Distributed RAM (Mb)	11.6	
Total Block RAM (Mb)	60.8	1728
UltraRAM (Mb)	81.0	288
Clock Mgmt Tiles (CMTs)	9	
DSP Slices	1,080	
PCIE4 (PCIe® Gen3 x16)	0	
PCIE4C (PCIe® Gen3 x16 / Gen4 x8 /CCIX)	3	
150G Interlaken	0	
100G Ethernet w/ KR4 RS-FEC	1	
Max. Single-Ended HD I/Os	72	
Max. Single-Ended HP I/Os	468	
GTH 16.3Gb/s Transceivers	0	
GTY 32.75Gb/s Transceivers	32	

SMART MCH 2nd candidate

Up to 2016 FIFO's ready to use

SOM provider for SMART MCH

AMD XILINX

XILINX® PREFERRED SOM PARTNERS

Robust Ecosystem of SoC and FPGA based System-on-Modules

ALINX®

AVNET Reach Further™

ENCLUSTRA FPGA SOLUTIONS

iWave Embedding Intelligence

MYiR

trenz electronic GmbH

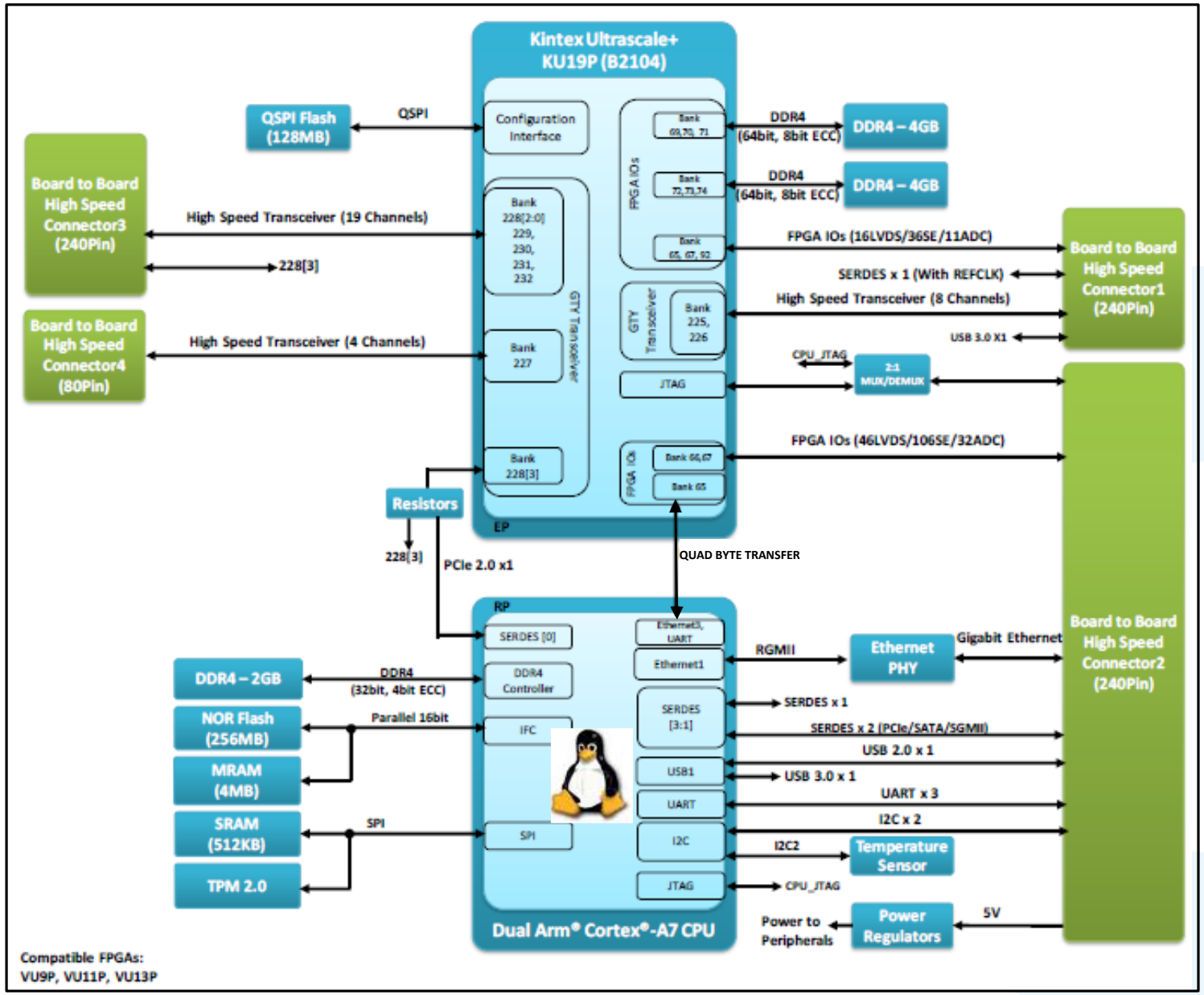
iWave Systems Tech. Pvt. Ltd.,
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore-560076, India.
Ph:+91-80-26683700, 26786245
Email: mktg@iwavesystems.com
www.iwavesystems.com

iWave Europe
Venkelbaan 55 2908KE
Capelle aan den IJssel
The Netherlands
Ph: +31 10 28403383
Email: info@iwavesystems.eu

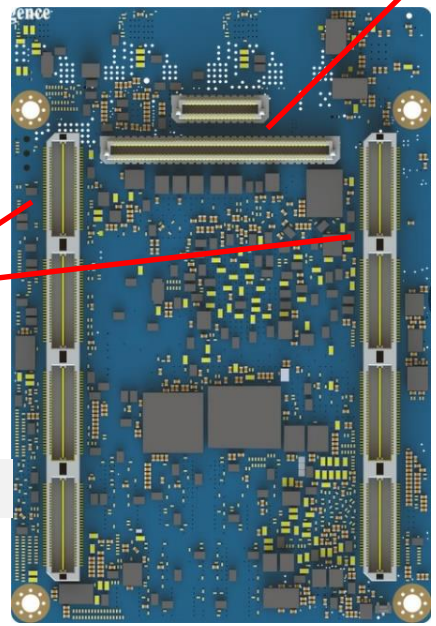
iW-RainboW-G47M

Kintex Ultrascale+ FPGA SOM

SMART MCH - SOM block diagram



SMART MCH - SOM top & bottom



NRZ 25 Gbps

2 x 240 pin SAMTEC QTH/QSH connectors

(4 banks x 2 rows of 30 pins)

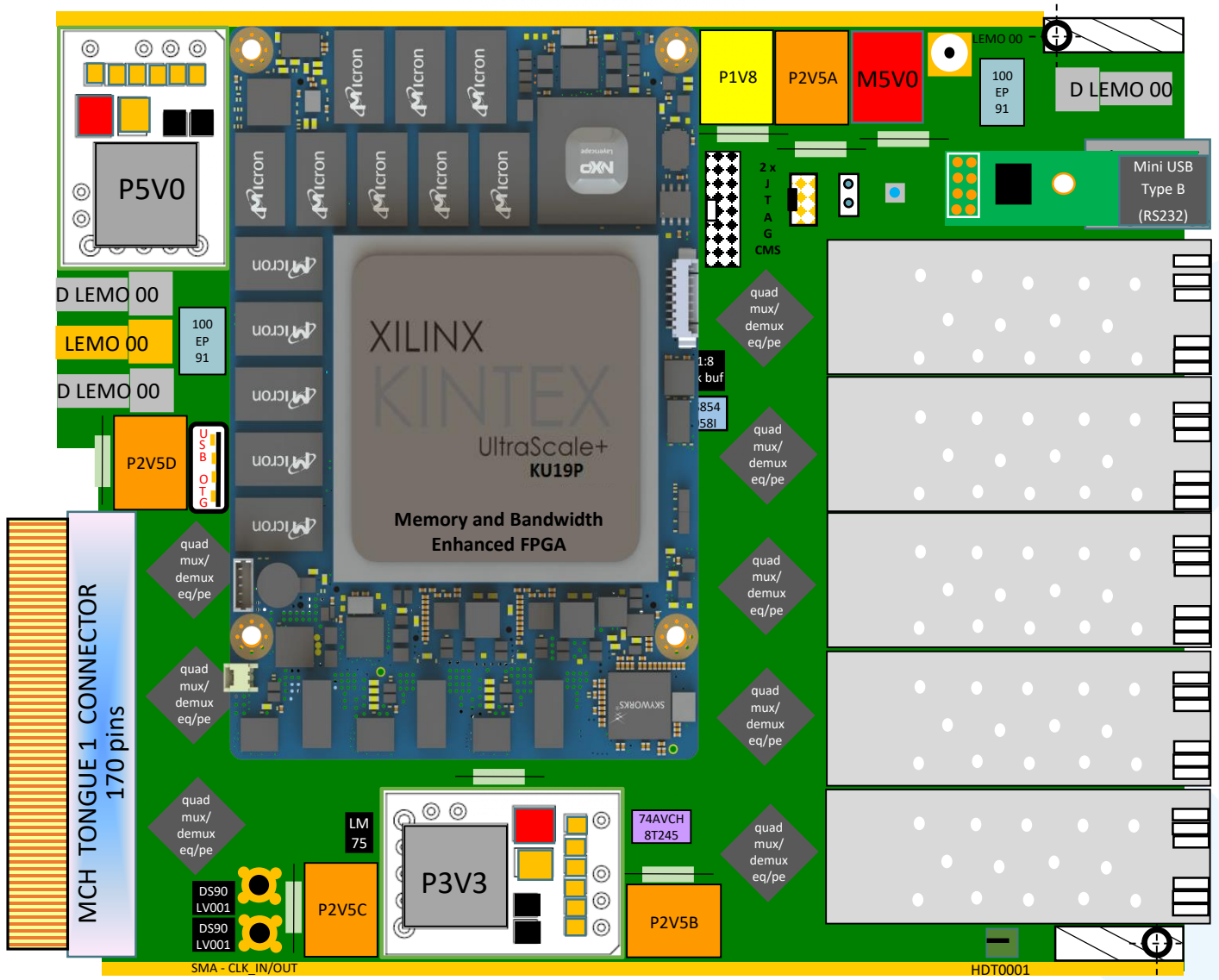
samtec ACCELERATE®HD

NRZ 28 Gbps | PAM4 56 Gbps

2 connectors

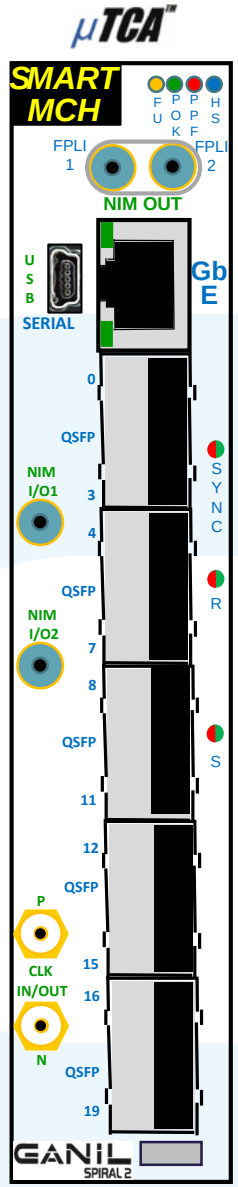
(4 rows x 60 balls & 4 rows x 20 balls)

SMART MCH implantation



12 HUB ports (via backplane)

5 QSFP - 20 HUB ports



SMART MCH project schedule

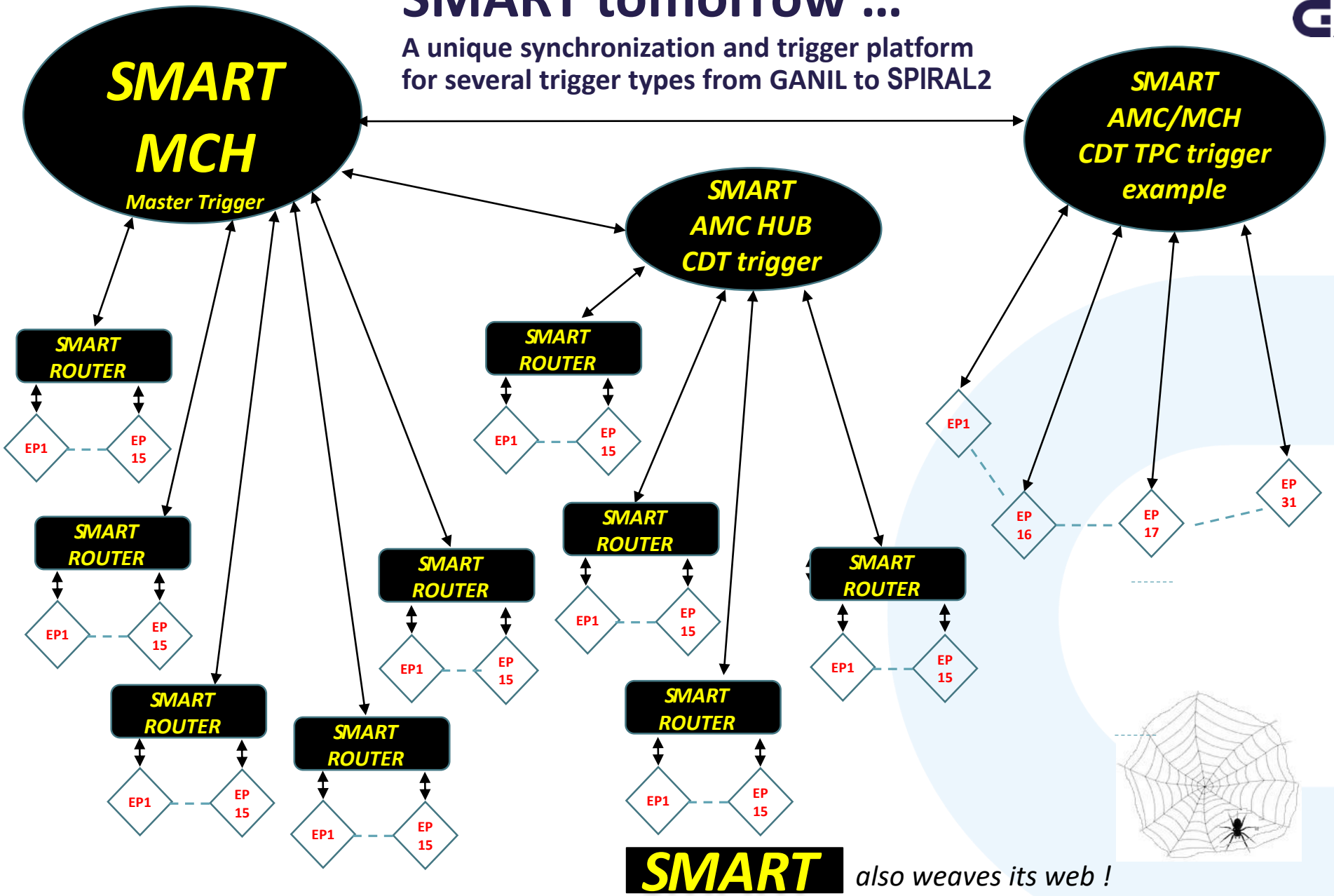
Main tasks	Main key dates
• Global architecture defined	• September 2022
• SOM Iwave iW-Rainbow-G47M chosen and ordered	• October 2022
• 1st SOM + Development platform delivered	• January 2023
• Embedded bare metal C code developed and tested on kit for required peripherals (LS1021A processor – Code Warrior suite)	• Mai 2023
• 19 new symbols developed for CAD tools (Cadence-Concept)	• July 2023
• 2 Iwave SOM ordered for AGATA	• August 2023
• 1st firmware developed for KU19P FPGA (Xilinx-Vivado 2022.1)	• September 2023
• 19 new footprints prepared for CAD tools (Cadence-Allegro)	• January 2024
• SMART MCH schematics	• January 2024
⇨ • SMART MCH board routing	• April 2024
• SMART MCH prototype assembly	• June 2024
• SMART MCH prototype tests (hardware, firmware, software)	• September 2024
• SMART MCH Production (4 units –> 2 for AGATA & 2 for GANIL)	• March 2025

SMART
Production costs summary
(last update: August 2023)

	SMART AMC ROUTER	SMART AMC HUB	SMART MCH
PCB (14 layers)	640+150(VAT)	640+150(VAT)	~1000(estimation)
Front panel kit + Drilling + Silkscreen	20 50 70	20 50 70	20 50 70
Assembly + Passive components	850	850	900
Active components (provided)	600	600	700
SOM	2300	2600	9000
UART2USB board	120	120	120
Price/Unit (€)	**4800**	**5100**	**11860**

SMART tomorrow …

A unique synchronization and trigger platform for several trigger types from GANIL to SPIRAL2



SMART *also weaves its web !*

Merci de votre attention

questions