



SOIPIX Telescope System

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SOIPIX Group for HEP

Tokyo Metropolitan College

Miho Yamada

KEK

Akimasa Ishikawa, Tristan Fillinger, Yasuo Arai, Toru Tsuboyama, Junji Haba

University of Tsukuba

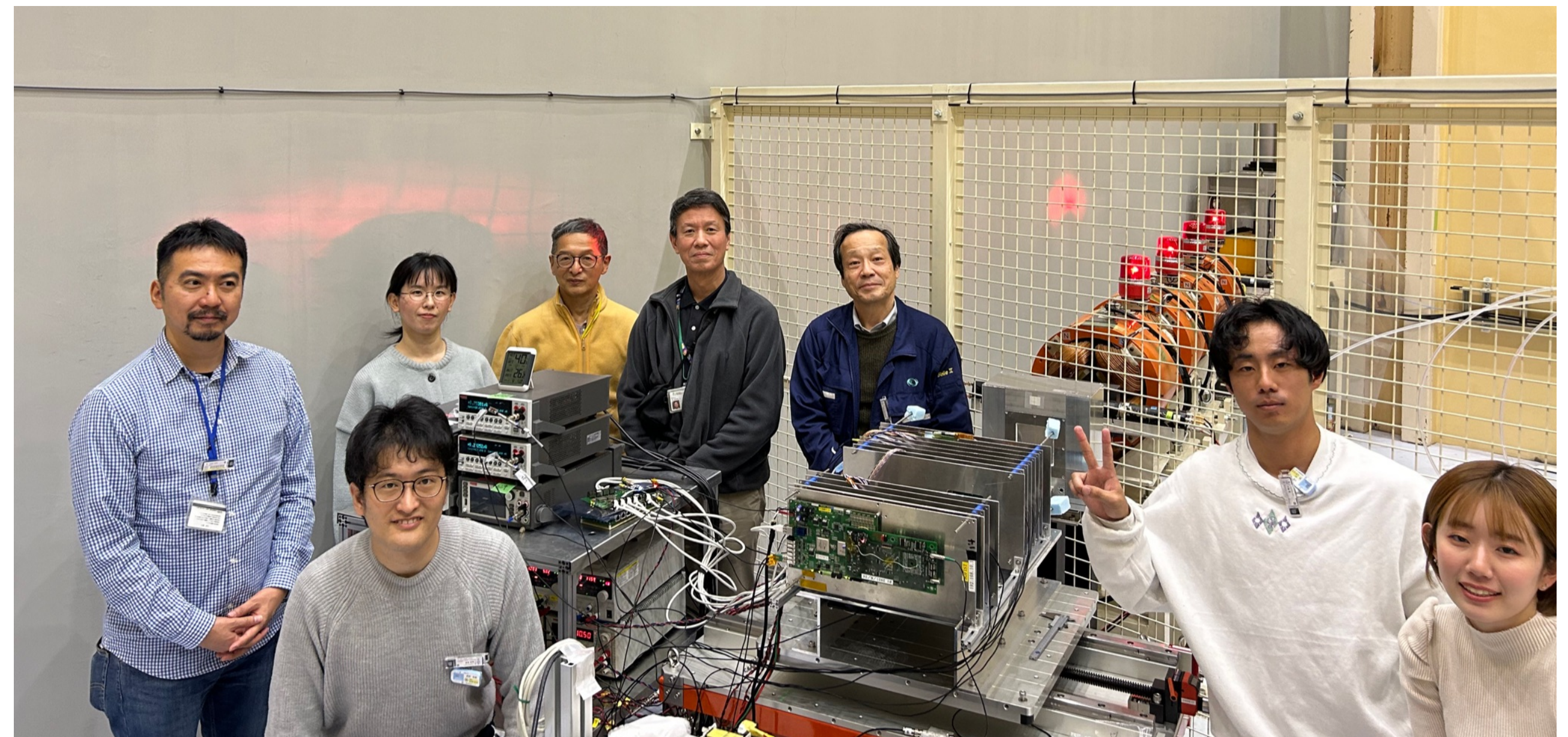
Kazuhiko Hara, Takumi Omori (M2)

University of Miyazaki

Ayaki Takeda

Nara Women's University Newcomers

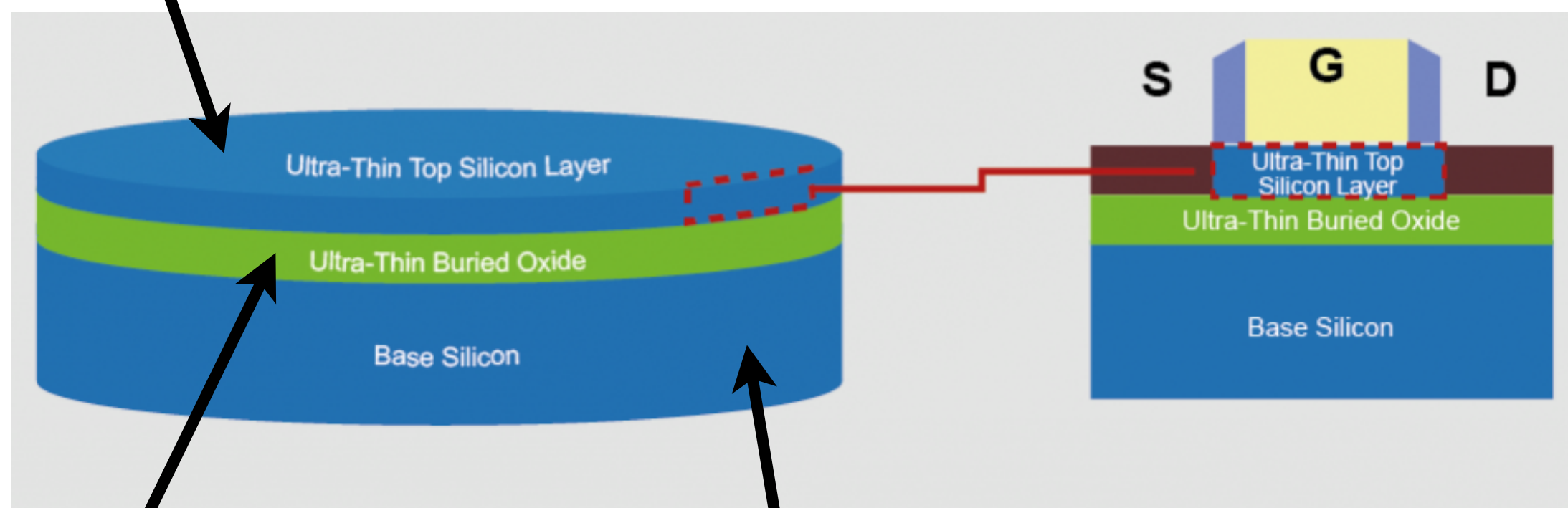
Kenkichi Miyabayashi, Hina Tagashira (M2)



SOI Pixel Sensor (SOIPIX)

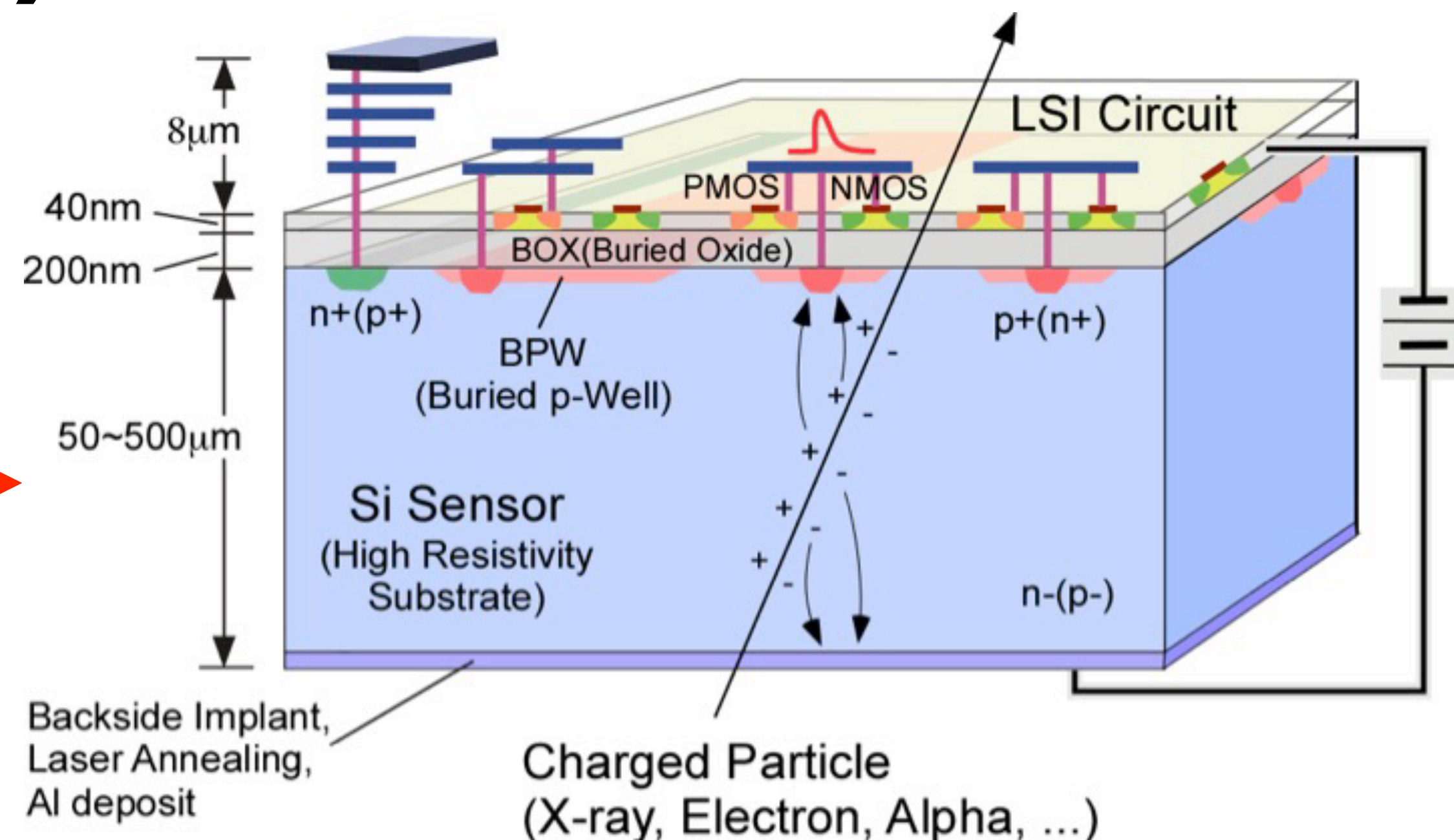
Low-Resistance Silicon Layer for CMOS circuit

SOI Wafer



Buried Oxide Layer (Insulator)

High-Resistance Support Base Silicon Layer



SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by Lapis Semiconductor Co. Ltd.

SOI Pixel Detector: Monolithic type detector

- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- Less single event effects (SEE) probability
- Sensor thickness: 50 - 500 μm
- Sensor Resistivity: > 1 kΩ·cm

Sensors

SOFIST for ILC
 PIXOR for Belle II
 XRPIX for X-ray astronomy
 INTPIX for general purpose
 FPIX, the highest granularity pixel

KEK PF-AR Test Beam Line

KEK ITDC, PF-AR Test Beam Line

<https://itdc.kek.jp/testBeamLine/index.html>

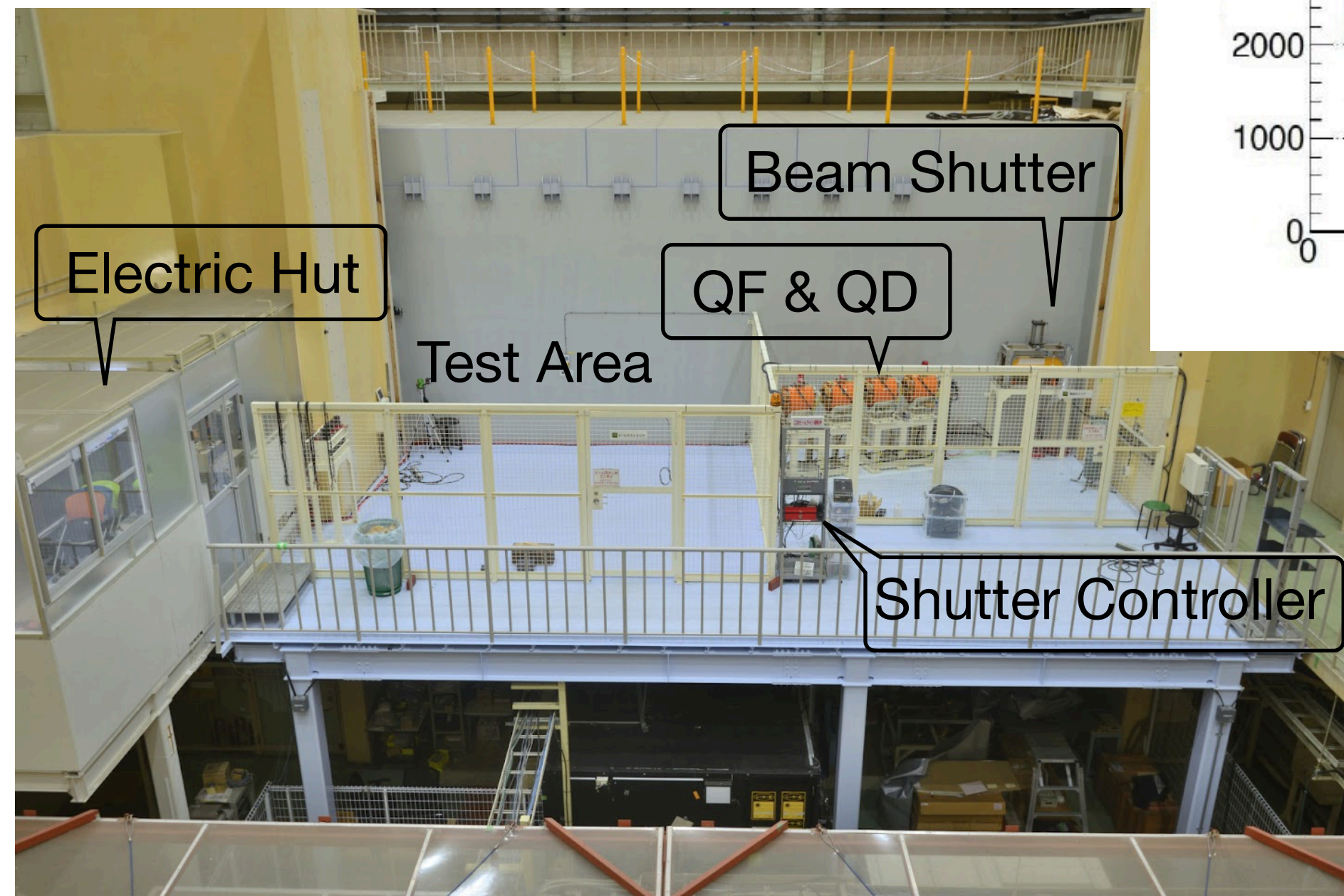
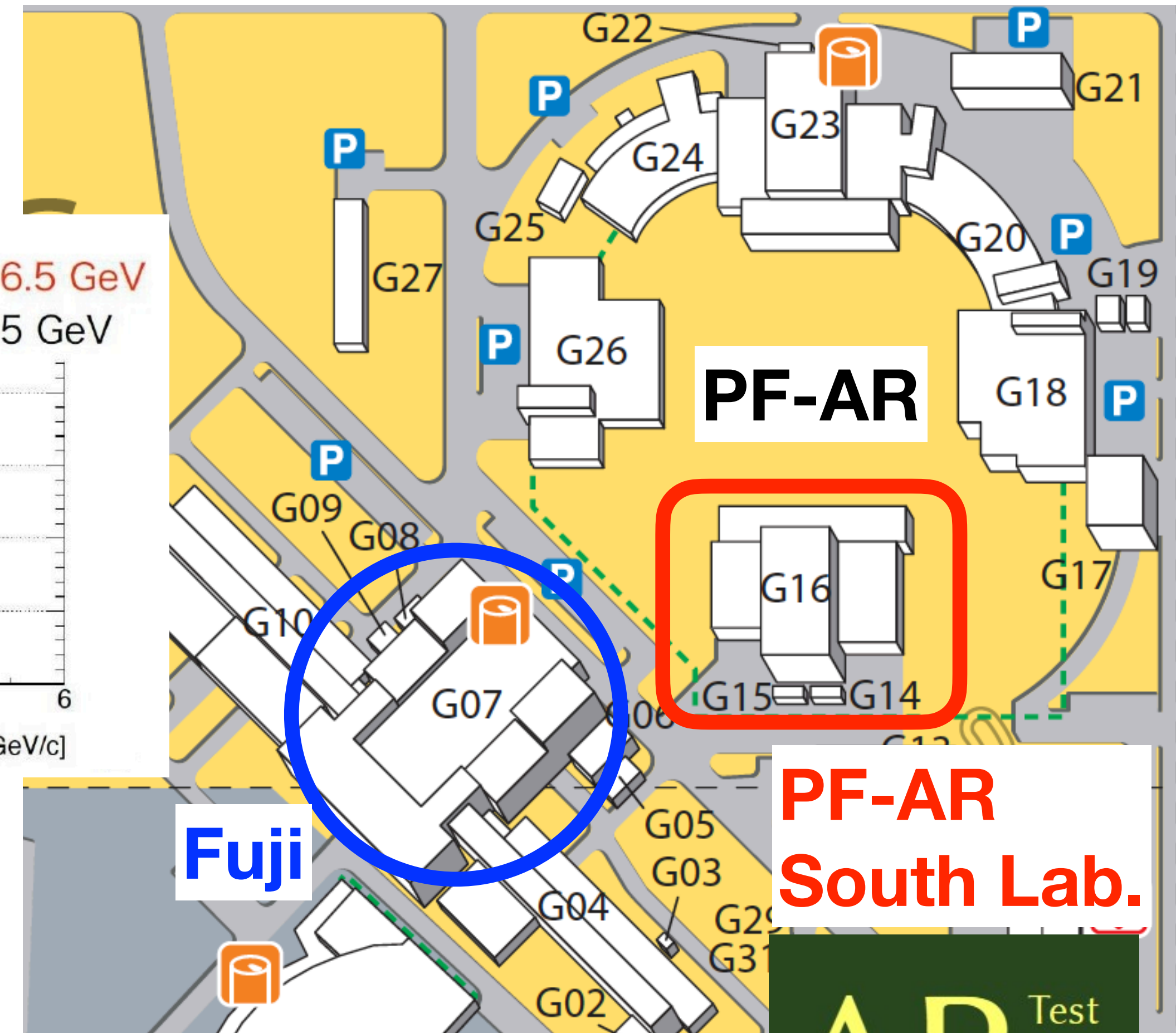
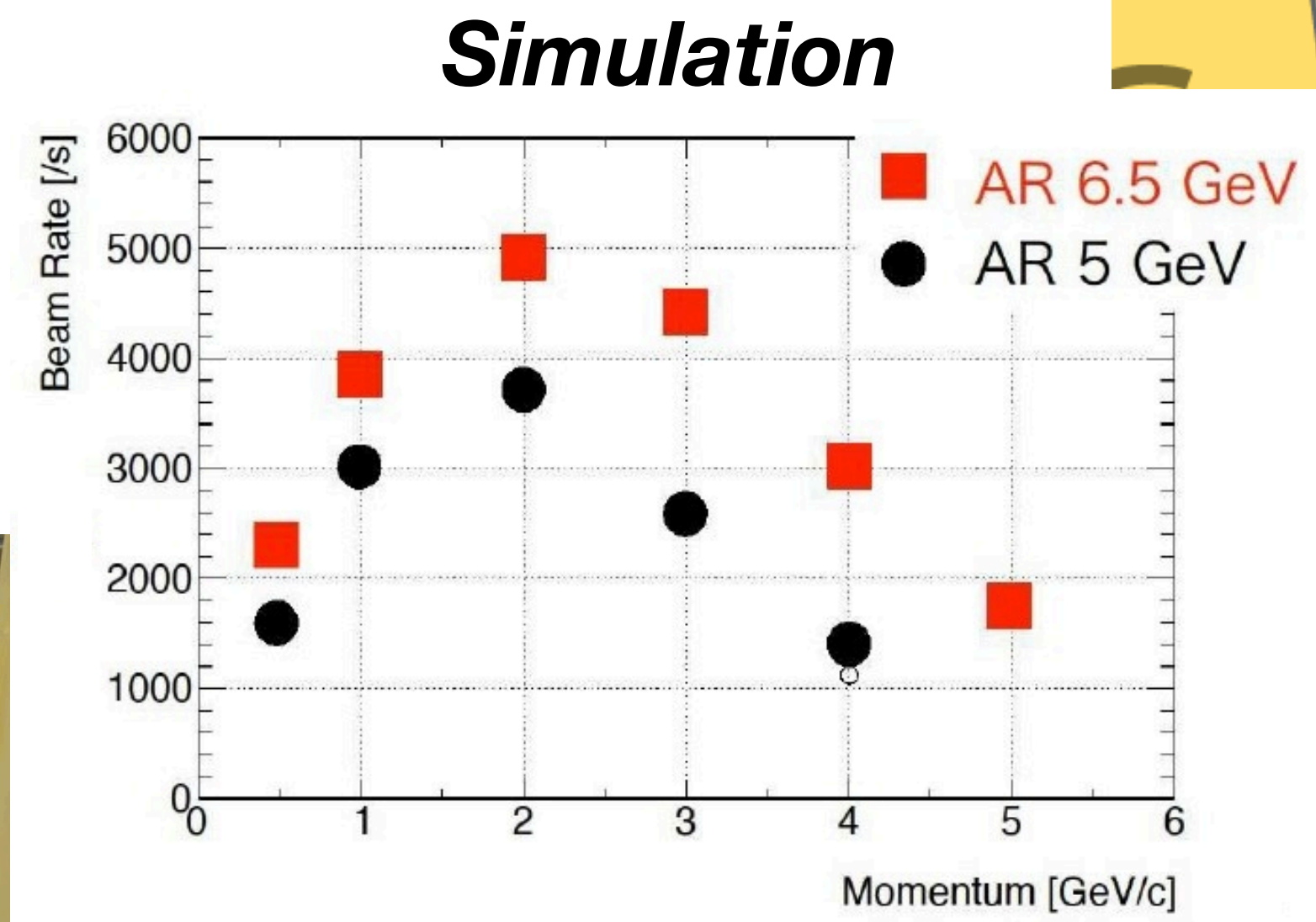
K. Hanagaki, JPS 2020 Autumn Meeting

<https://kds.kek.jp/event/35569/>

Beam rate is maximum at 2 GeV/c

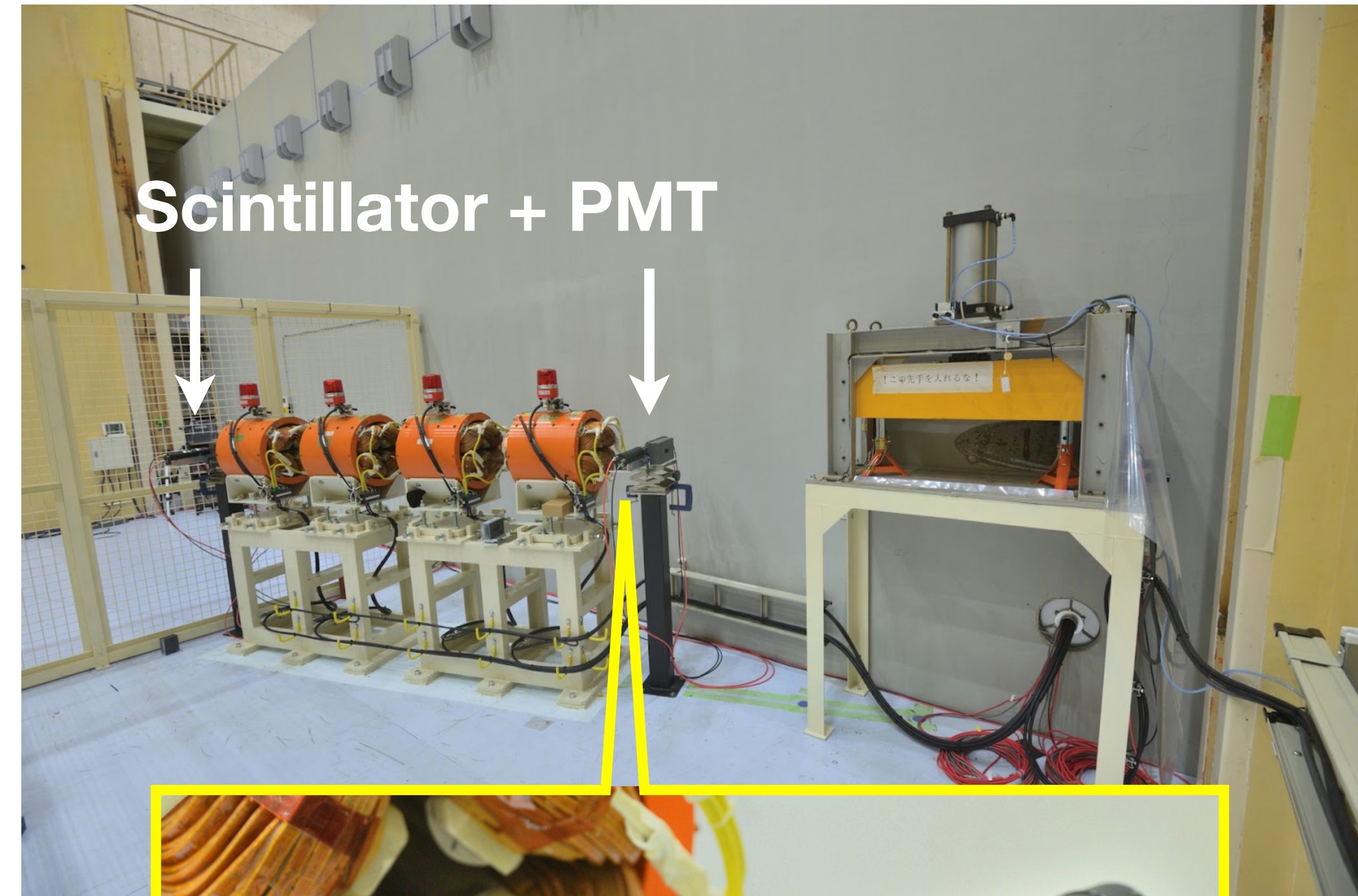
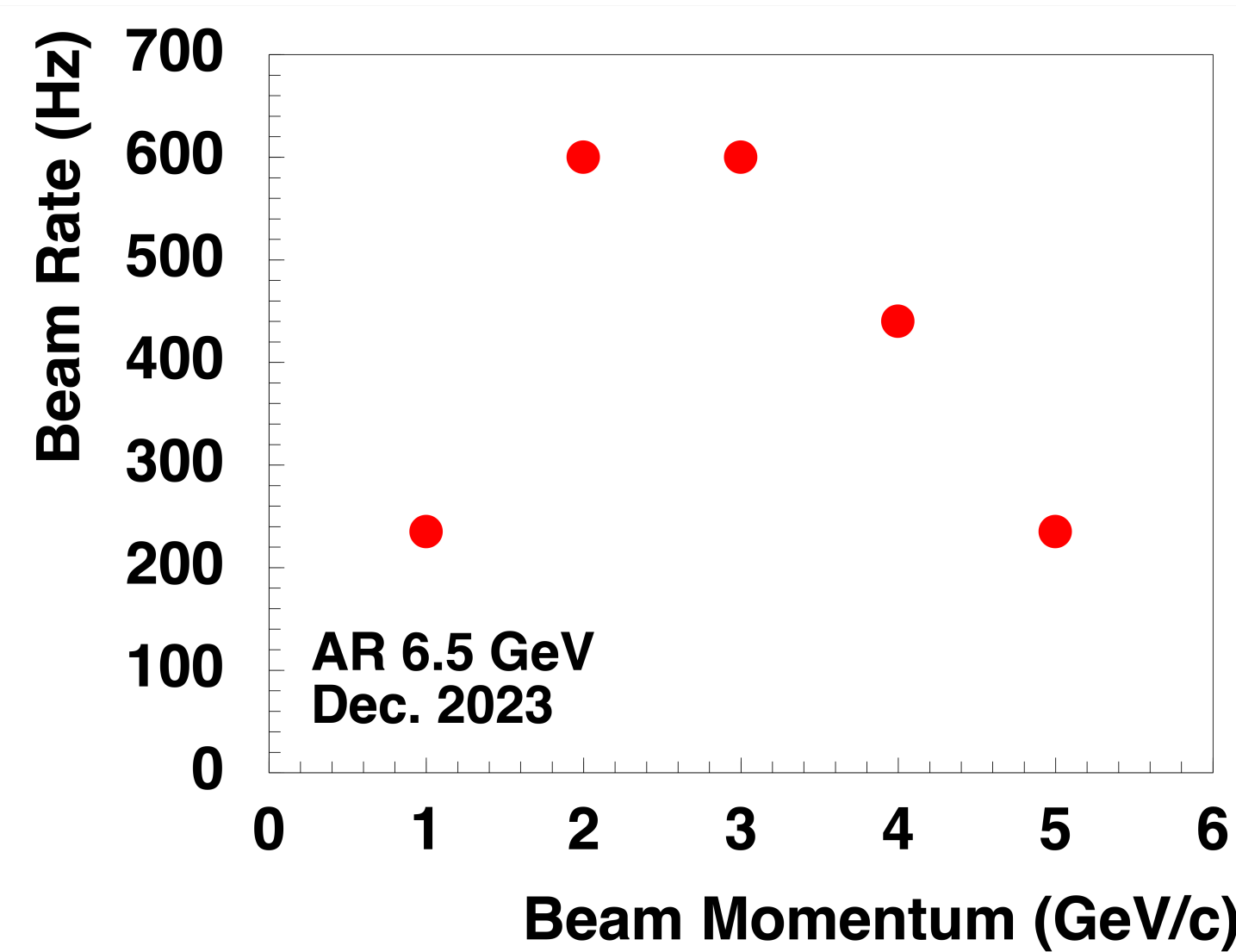
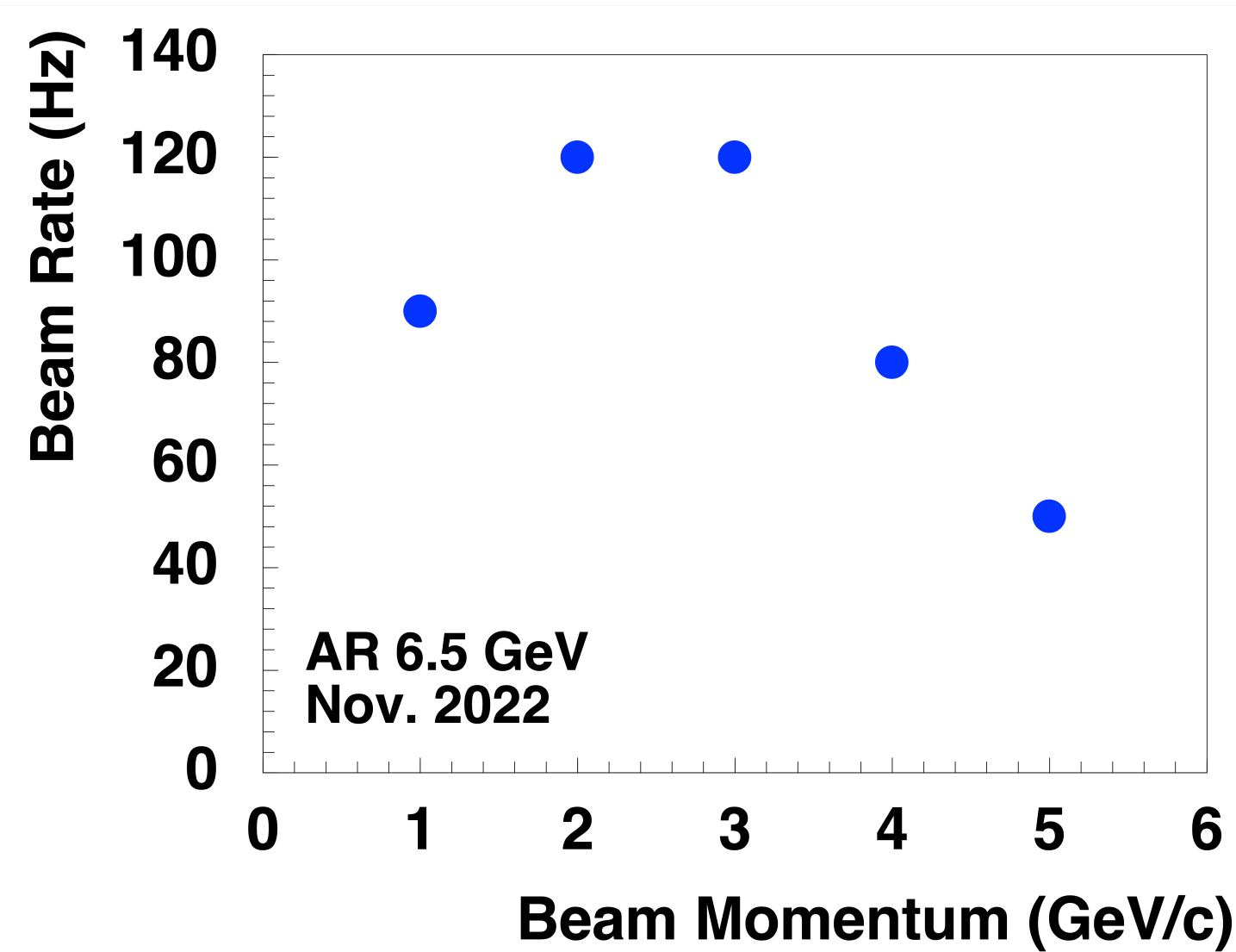
Currently ~1kHz

Depends on the target position



KEK PF-AR Test Beam Line

Beam Rate (4 fold)



The current for the bending magnet can be changed by the user.

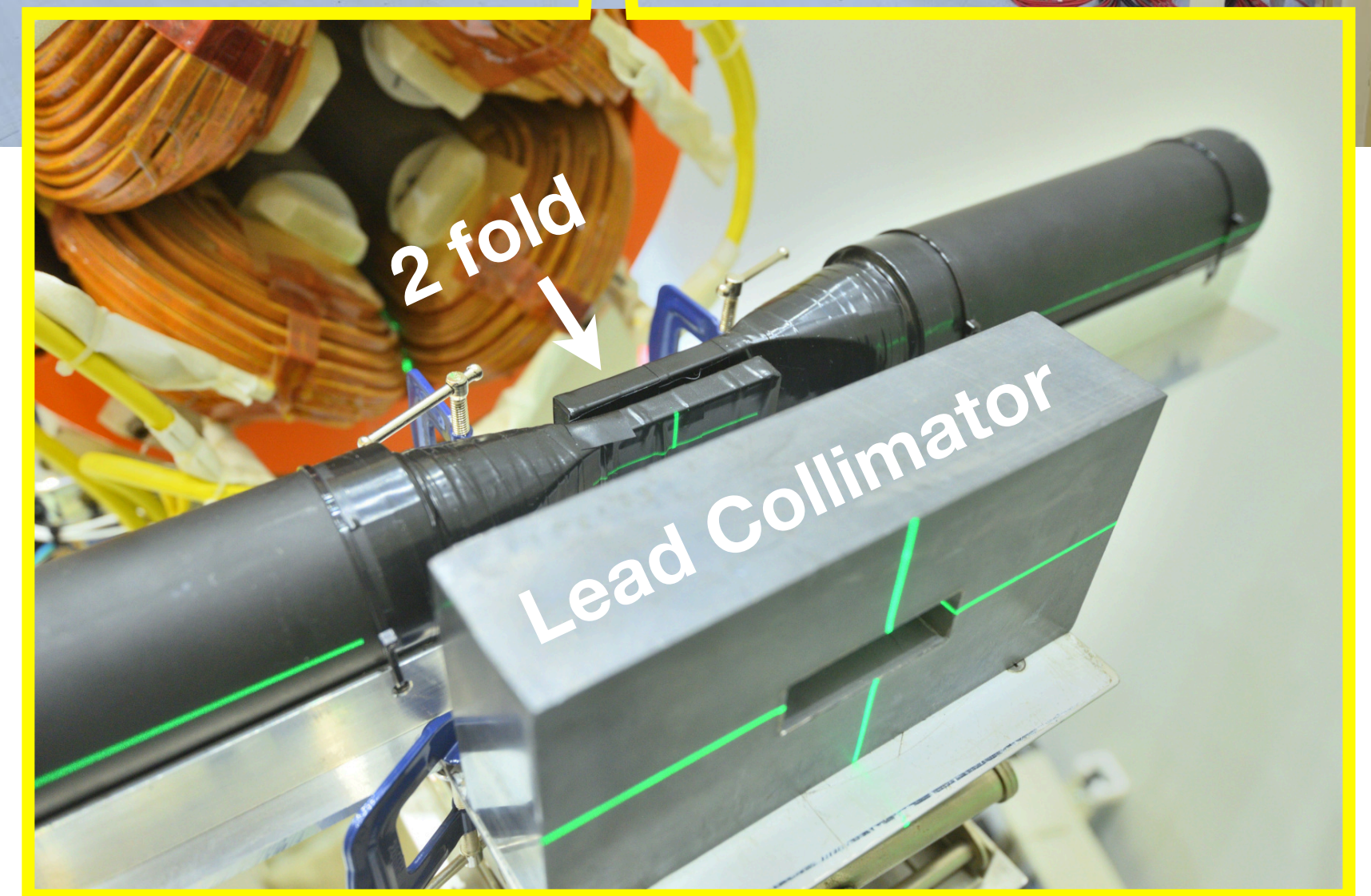
In 2023

The beam rate was more than 1kHz at AR 5 GeV.

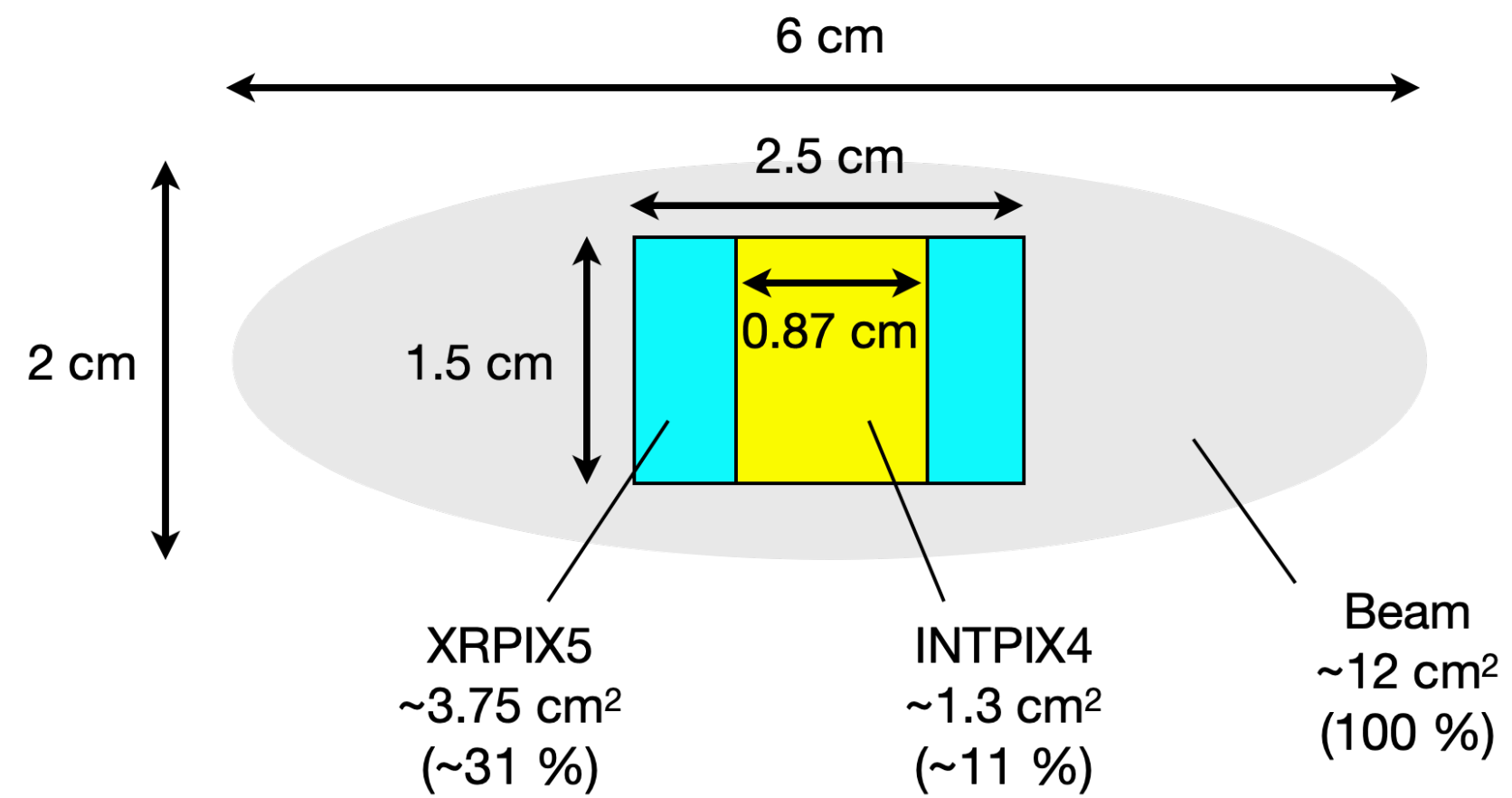
The target position was more inside than AR 6.5 GeV.

AR 5 GeV: 11/17 - 12/6

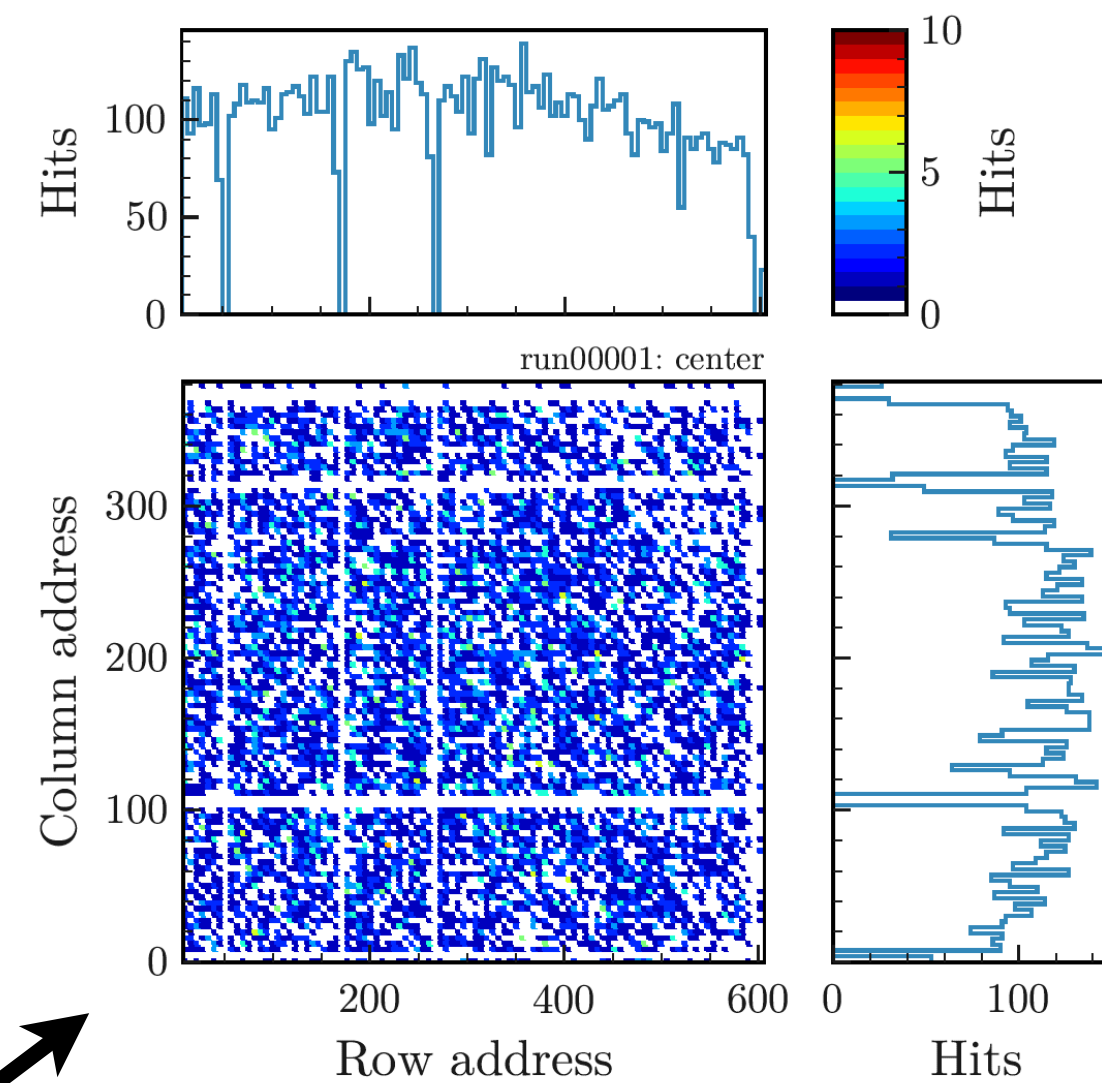
AR 6.5 GeV: 12/8 - 12/28 (our beam time: 12/13 - 12/20)



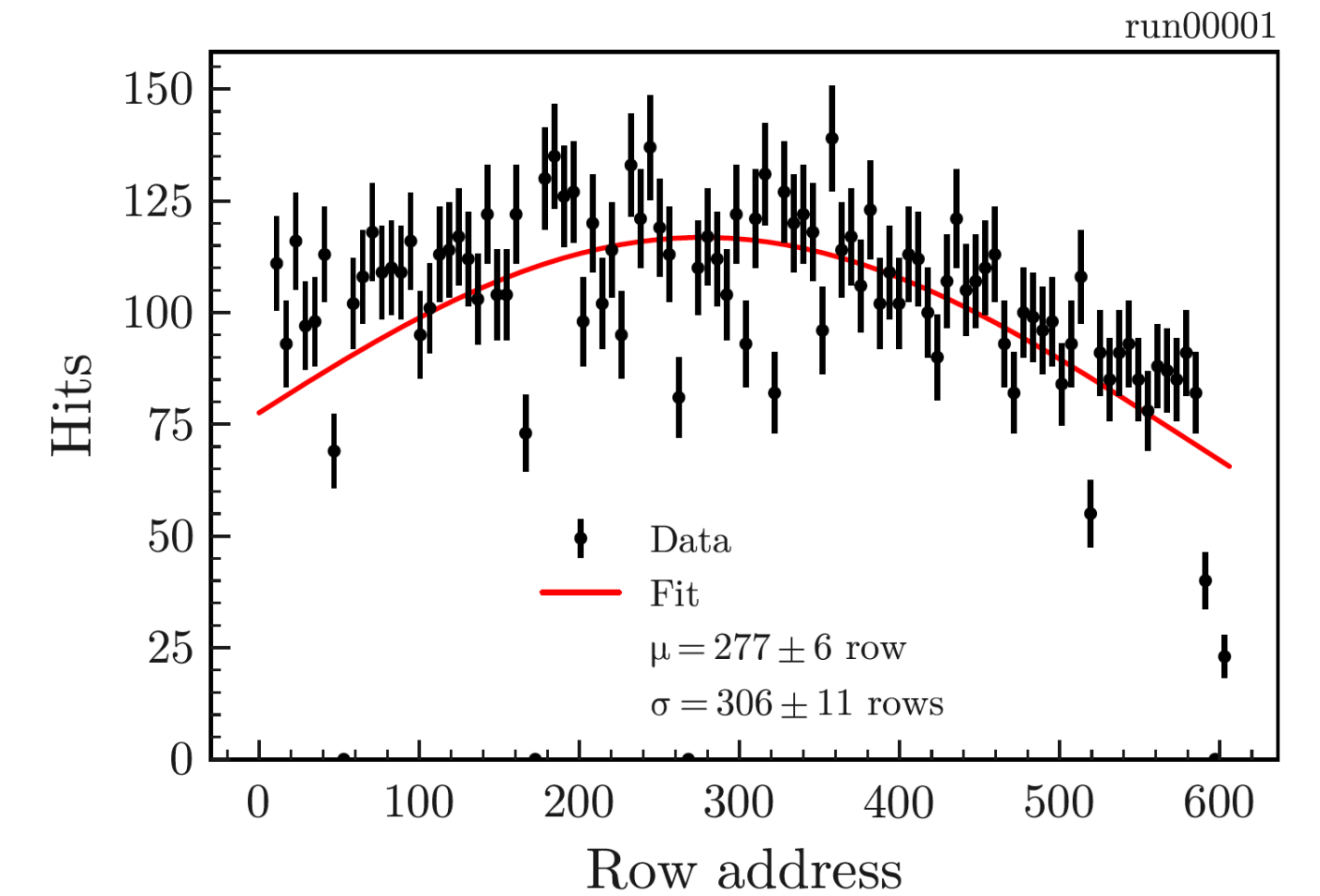
Beam Profile



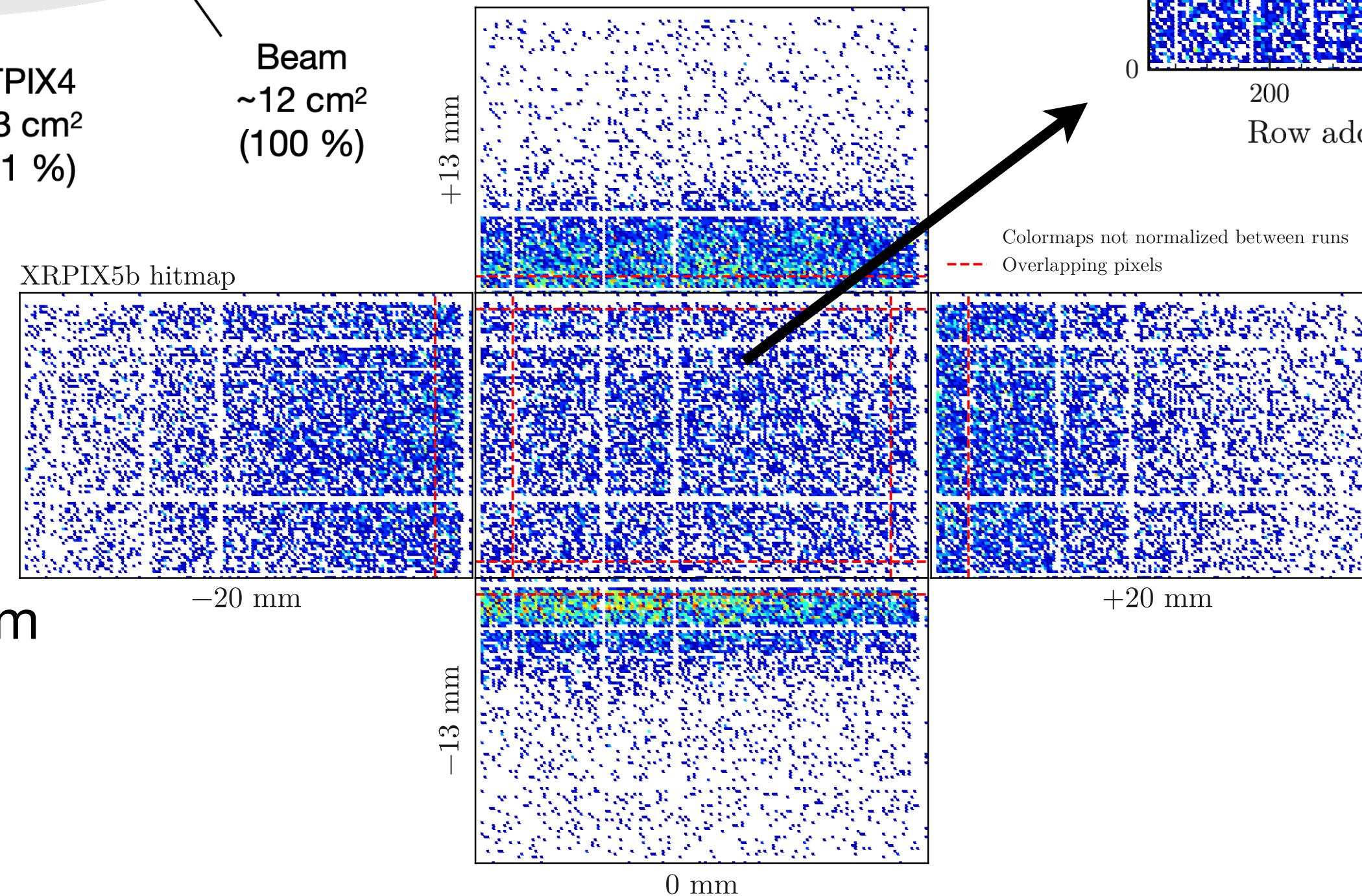
Projection



Horizontal



$$\sigma = 306 \text{ pixels} \times 36 \mu\text{m} = 1.1 \text{ cm}$$



XRPIX5 (SOIPIX)

Trigger and beam profile monitor system

Pixel size: $36 \mu\text{m} \times 36 \mu\text{m}$

Active are: $2.5 \text{ cm} \times 1.5 \text{ cm}$

The beam profile is obtained by stitching the hit map with five positions. These hit maps are not normalized between runs.

Telescope for KEK PF-AR Test Beam Line

Position Resolution for Pixel Detector

LHC ATLAS: 12 μm

KEKB Belle II: 10 μm

ILC: 3 μm

High-energy beams are available at CERN and Fermilab.

Coulomb multiple scattering of the beam is negligibly small.

In general, a tracker consists of multiple sensors that perform precise spatial resolution.

Japanese Facility

ELPH (Tohoku University) : ~820 MeV/c Positron Beam

KEK AR-TB: 1- 5 GeV/c Electron Beam

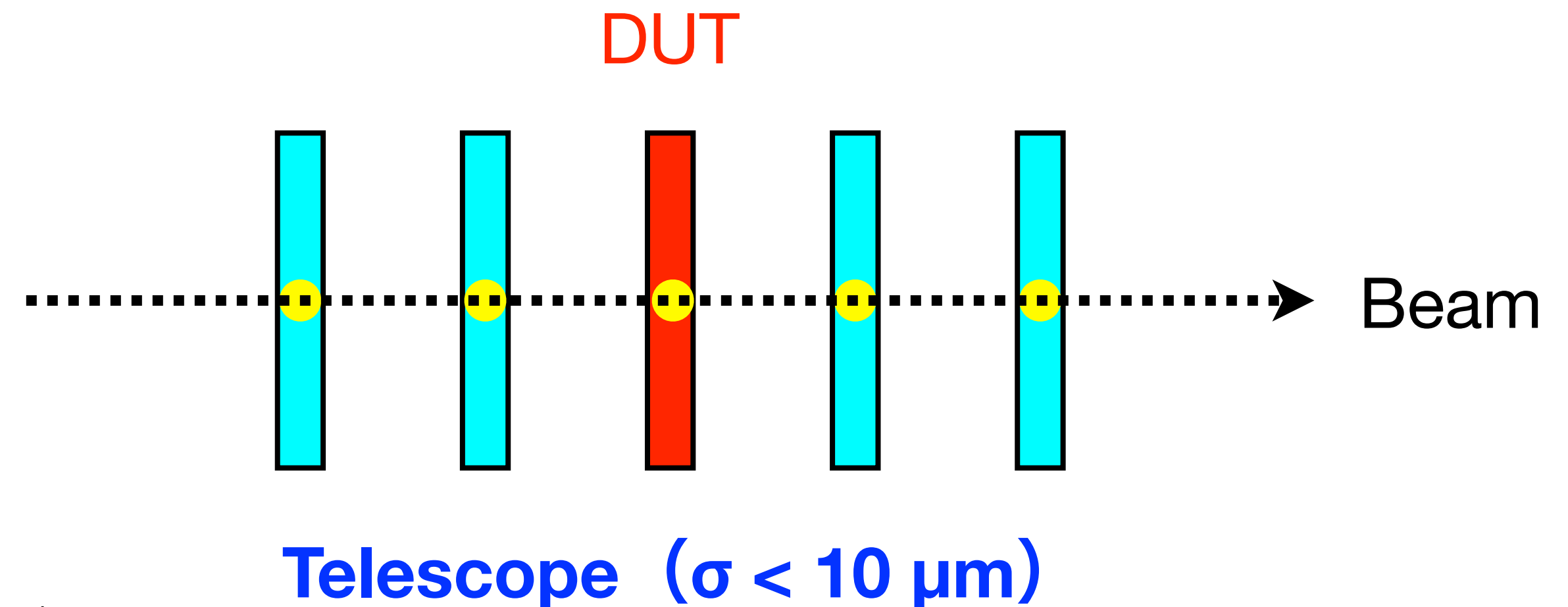


Development of a precision beam telescope system at the sub-GeV to GeV energy range.

→ Better than 10 μm of position resolution at GeV order electron beam

Need to be optimized

- Number of Sensors for Tracking
- Sensor Thickness
- Tracking Method

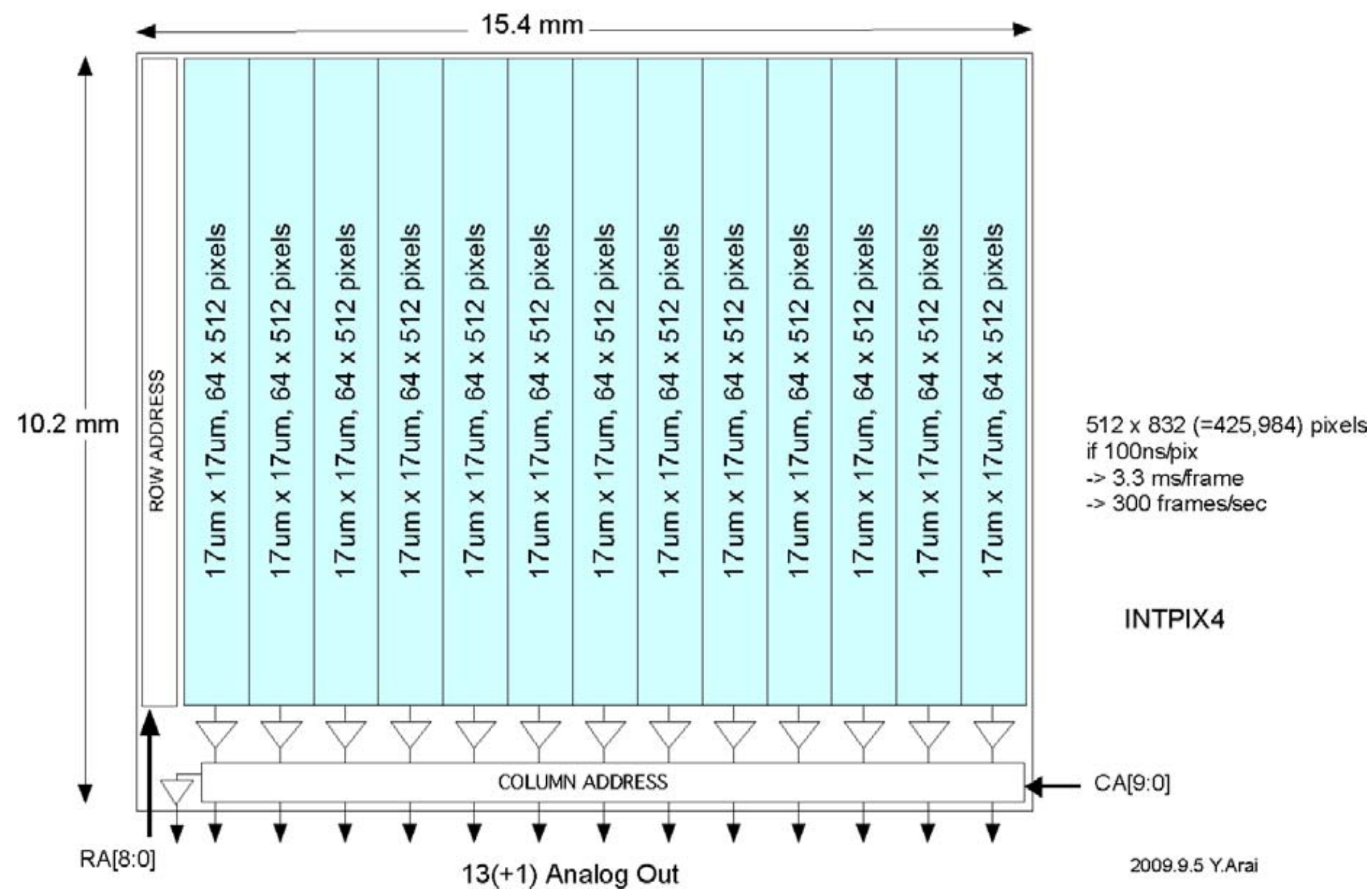


INTPIX4NA

INTPIX4NA is a general-purpose sensor, and it can be used in many applications. Implemented minimum circuit in pixel for analog readout and global shutter imaging. Position resolution is $\sim 1.56 \mu\text{m}$ (120 GeV Proton Beam at FTBF)

Table 1 Main parameters of the INTPIX4 and INTPIX4NA sensors.

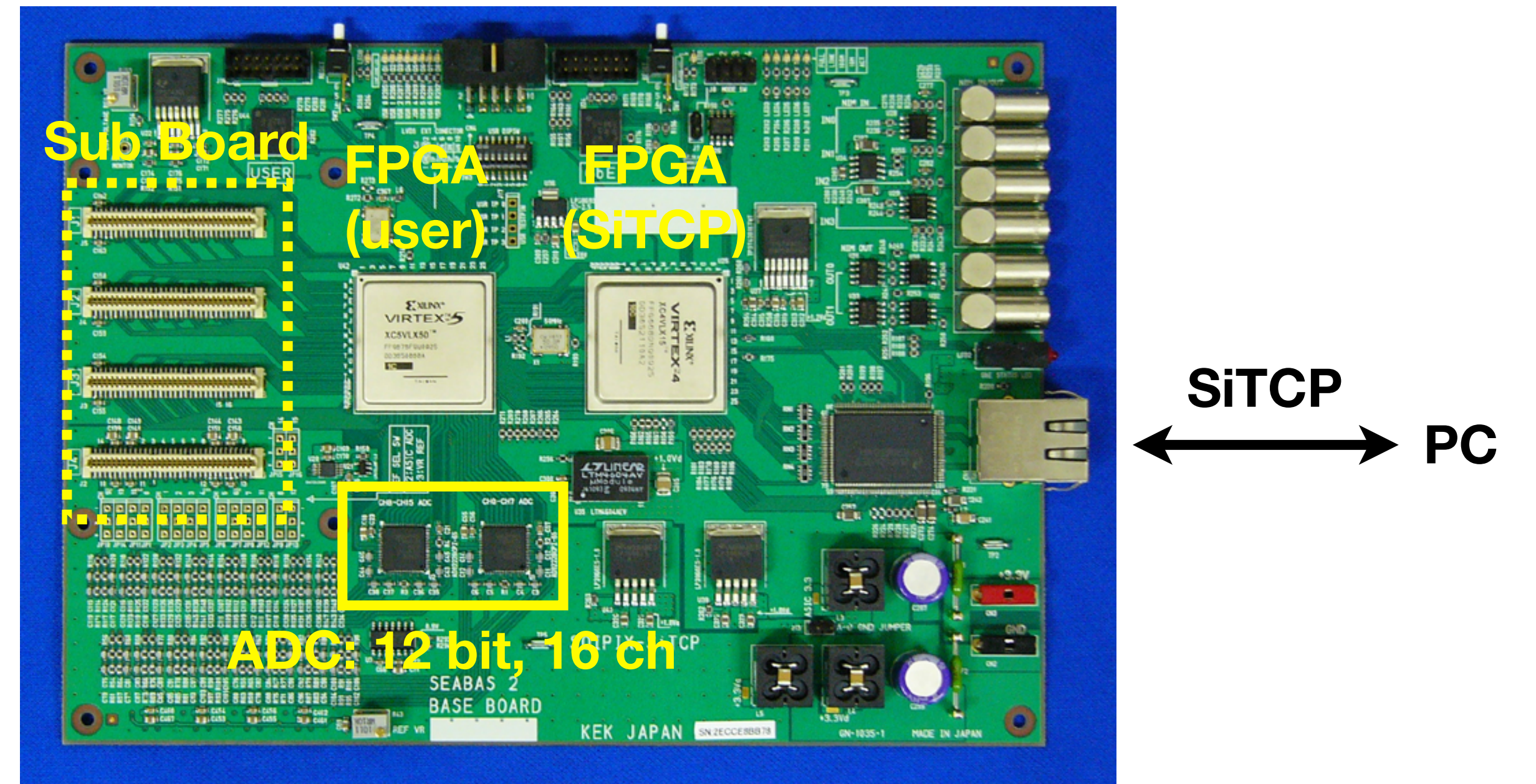
Chip size	$15.4 \times 10.2 \text{ mm}^2$
Active area	$14.1 \times 8.7 \text{ mm}^2$
Pixel size	$17 \times 17 \mu\text{m}^2$
Pixel array	512 (row) \times 832 (column) 13 blocks (64 cols) in parallel readout
Wafer	$\rho \sim 7 \text{ k}\Omega\text{cm}$, 500 μm thick (INTPIX4)
n-type FZ	$\rho \sim 11 \text{ k}\Omega\text{cm}$, 300 μm thick (INTPIX4NA)
modification	Output buffer is enforced for INTPIX4NA



Analog Readout

The Analog signal is read out from all of the pixels, and then digitized by external ADC on the DAQ board.

SEABAS2 FPGA Board



INTPIX4NA

INTPIX4NA is a general purpose sensor, and it can be used in many applications. Implemented minimum circuit in pixel for analog readout and global shutter imaging. Position resolution is $\sim 1.56 \mu\text{m}$ (120 GeV Proton Beam at FTBL)

Expected position resolution by using three upstream sensors for tracking.

Simulated by Geant4

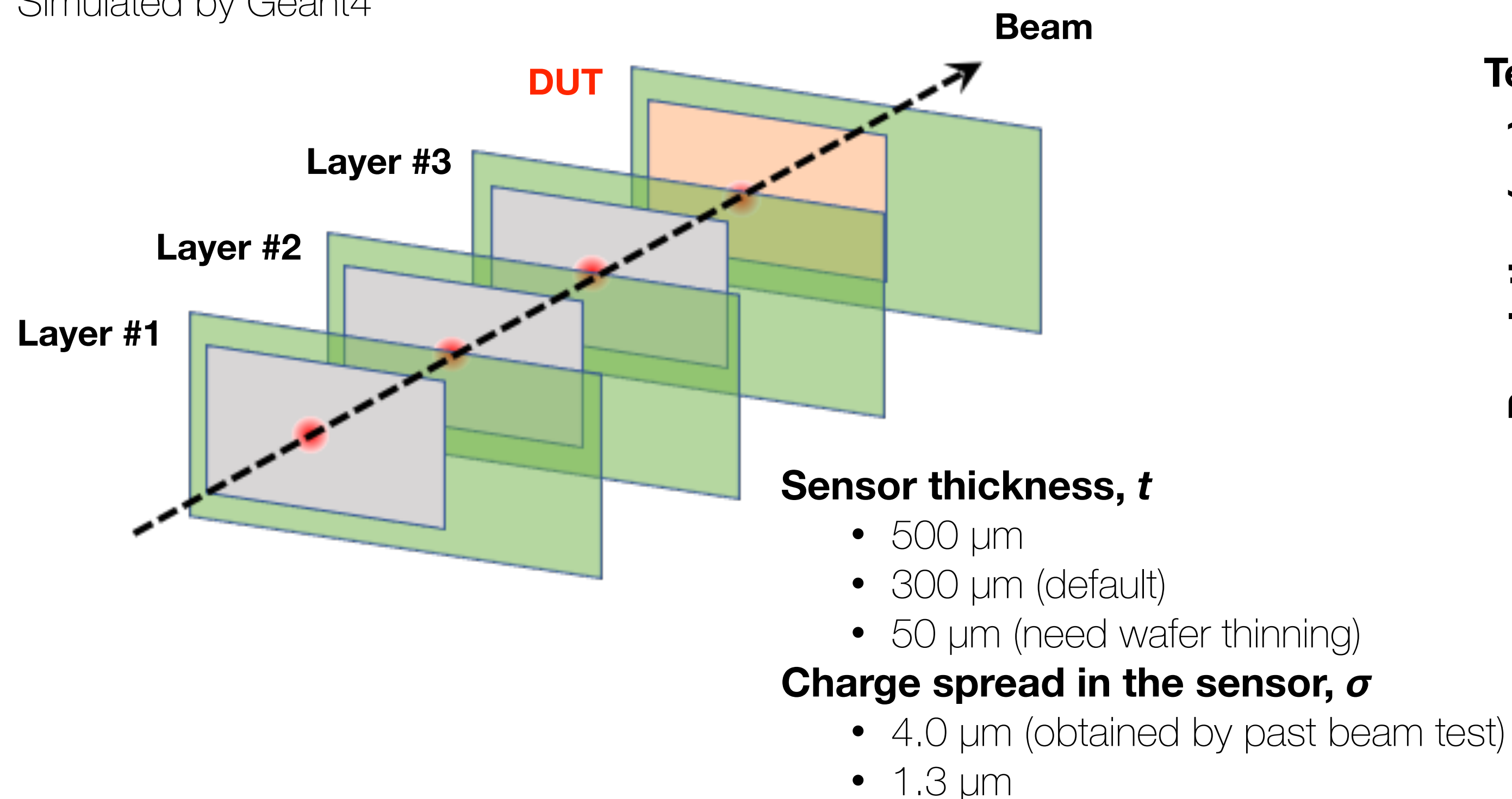
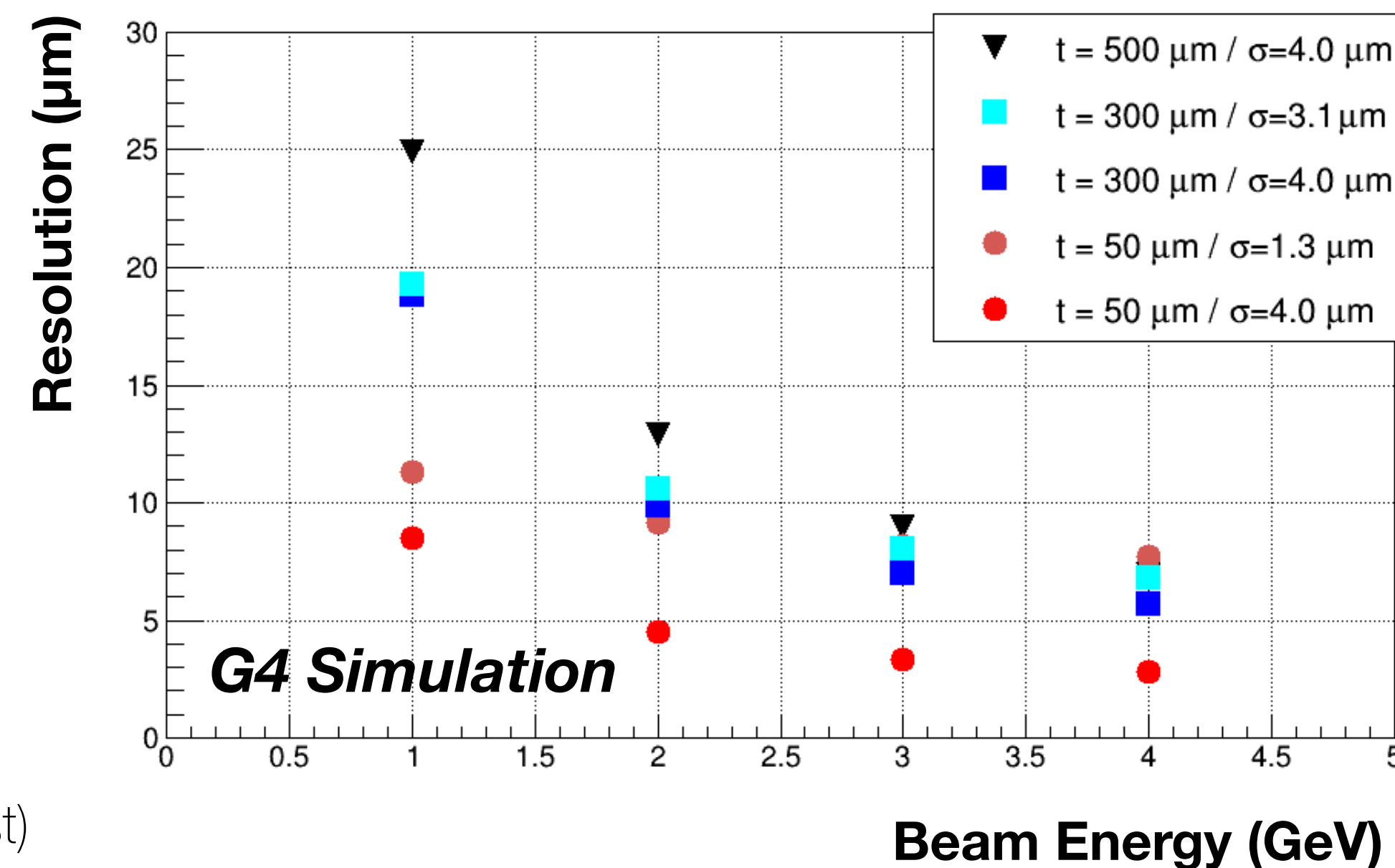


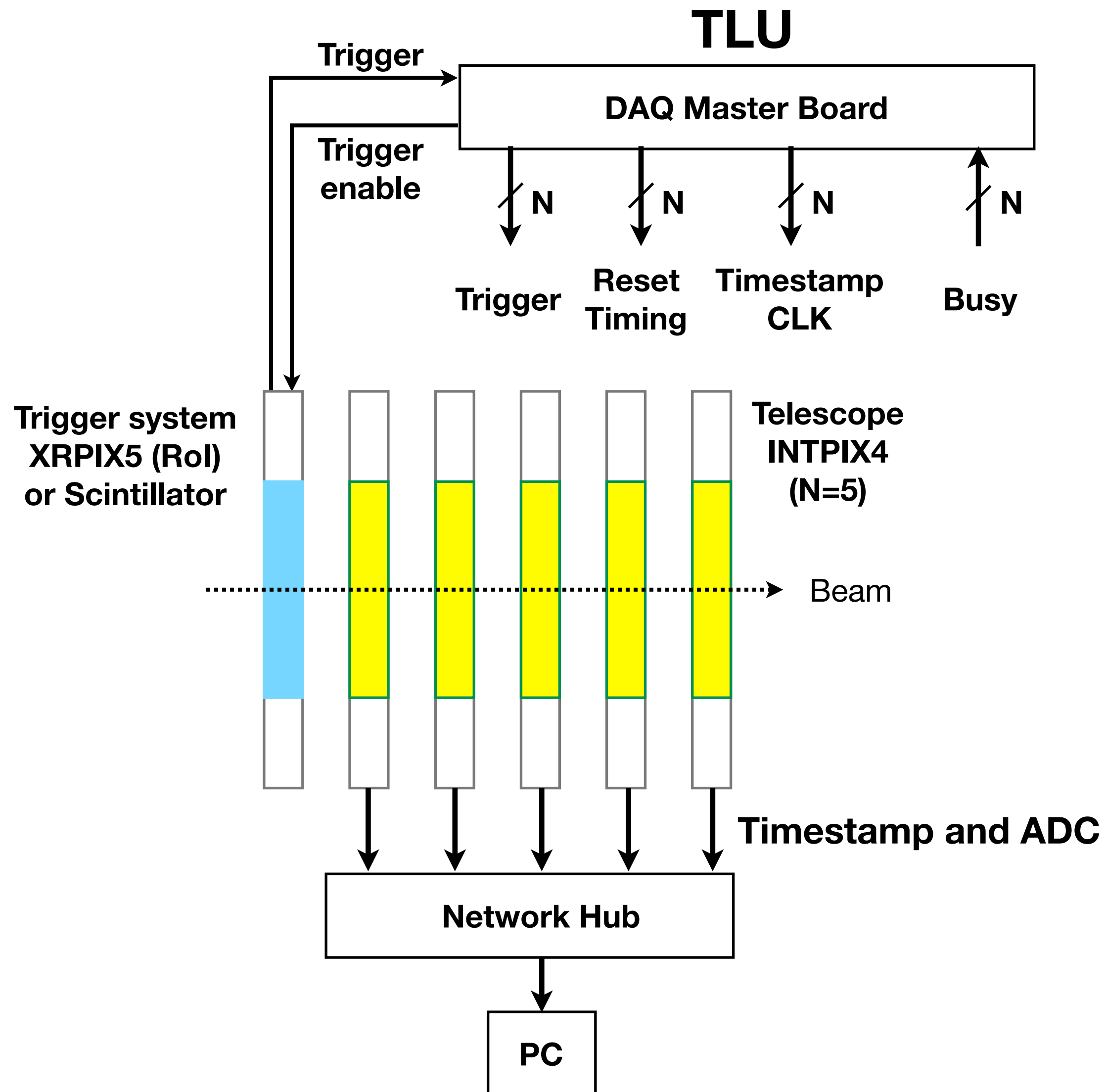
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modification	Output buffer is enforced for INTPIX4NA

Telescope Position Resolution for Electron Beam Energy



SOIPIX Telescope System



Rate

XRPIX5 trigger
rate: > 1 kHz
latency: ~2.5 μ s

Telescope DAQ rate
Full frame readout: ~ 25 Hz
Zero-suppression: ~145 Hz

Breakdown

Time for signal integration
100 μ s

Time for AD conversion
200 ns per pixel

$$200 \text{ ns} \times 518 \text{ row} \times 64 \text{ col} = 6.6 \text{ ms}$$

Time for readout per sensor
Speed: 1Gbps

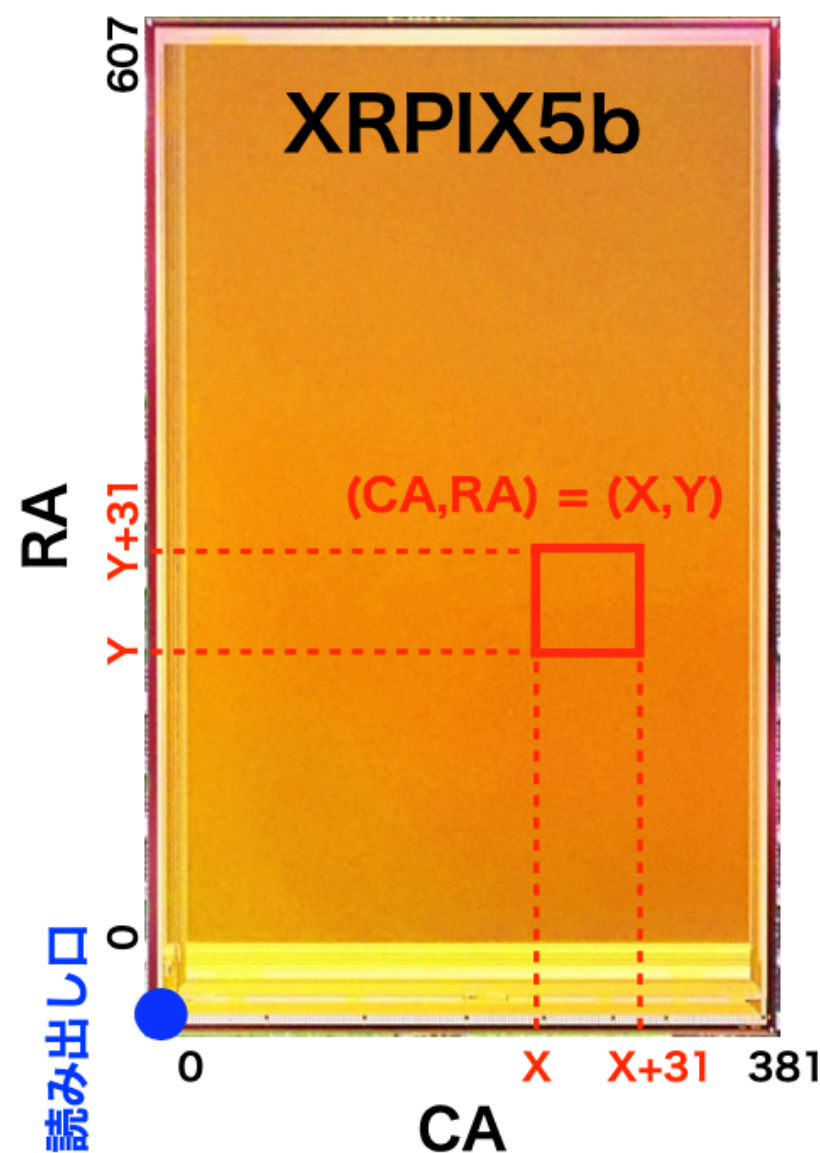
Data size: 16bit/pixel

$$(512 \text{ row} \times 832 \text{ col} \times 16 \text{ bit}) / 10^9 \text{ s} = 6.8 \text{ ms}$$

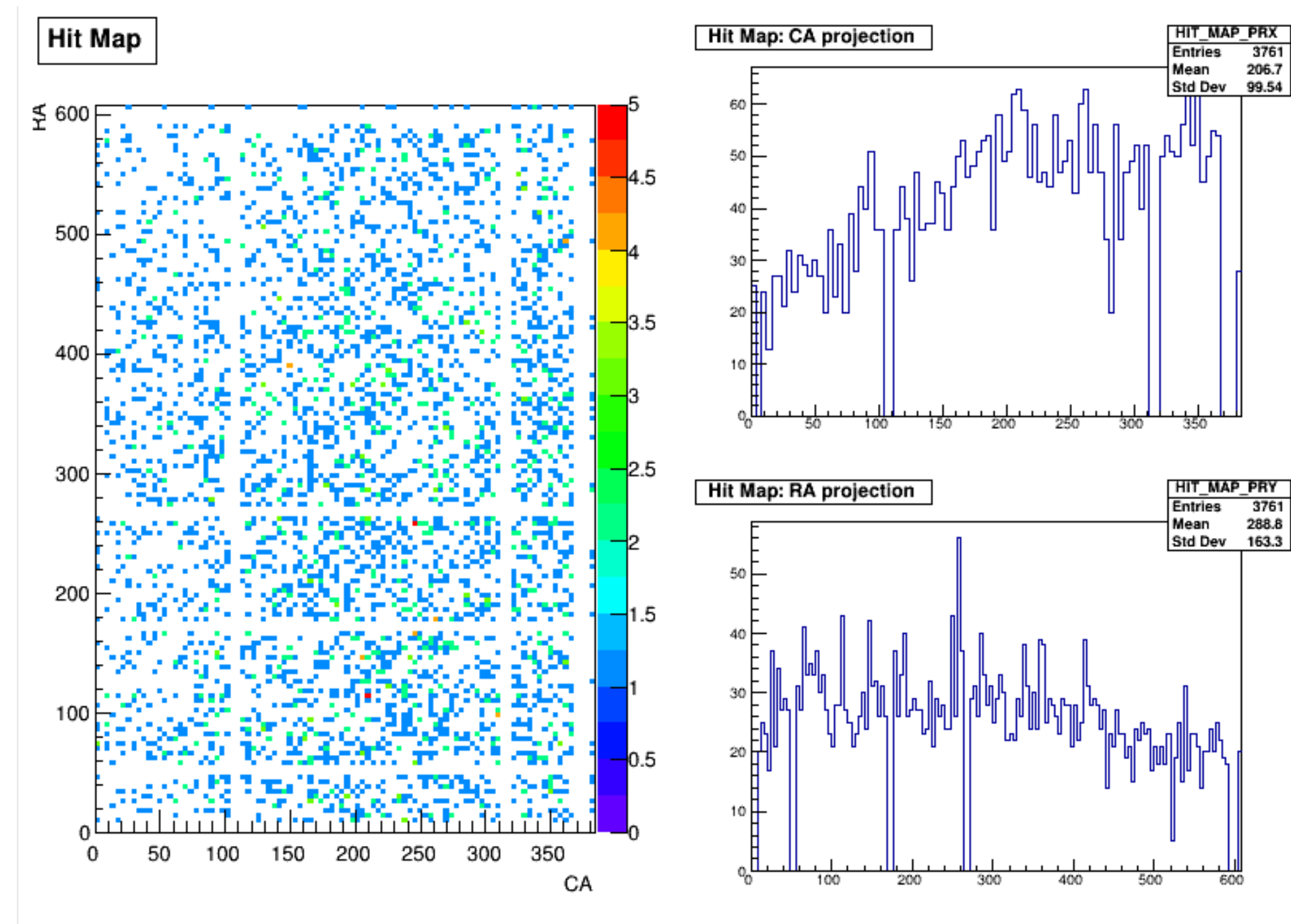
DAQ rate for 5 sensors

$$1 / (6.6 \text{ ms} + 5 \times 6.8 \text{ ms}) = \mathbf{25 \text{ Hz}}$$

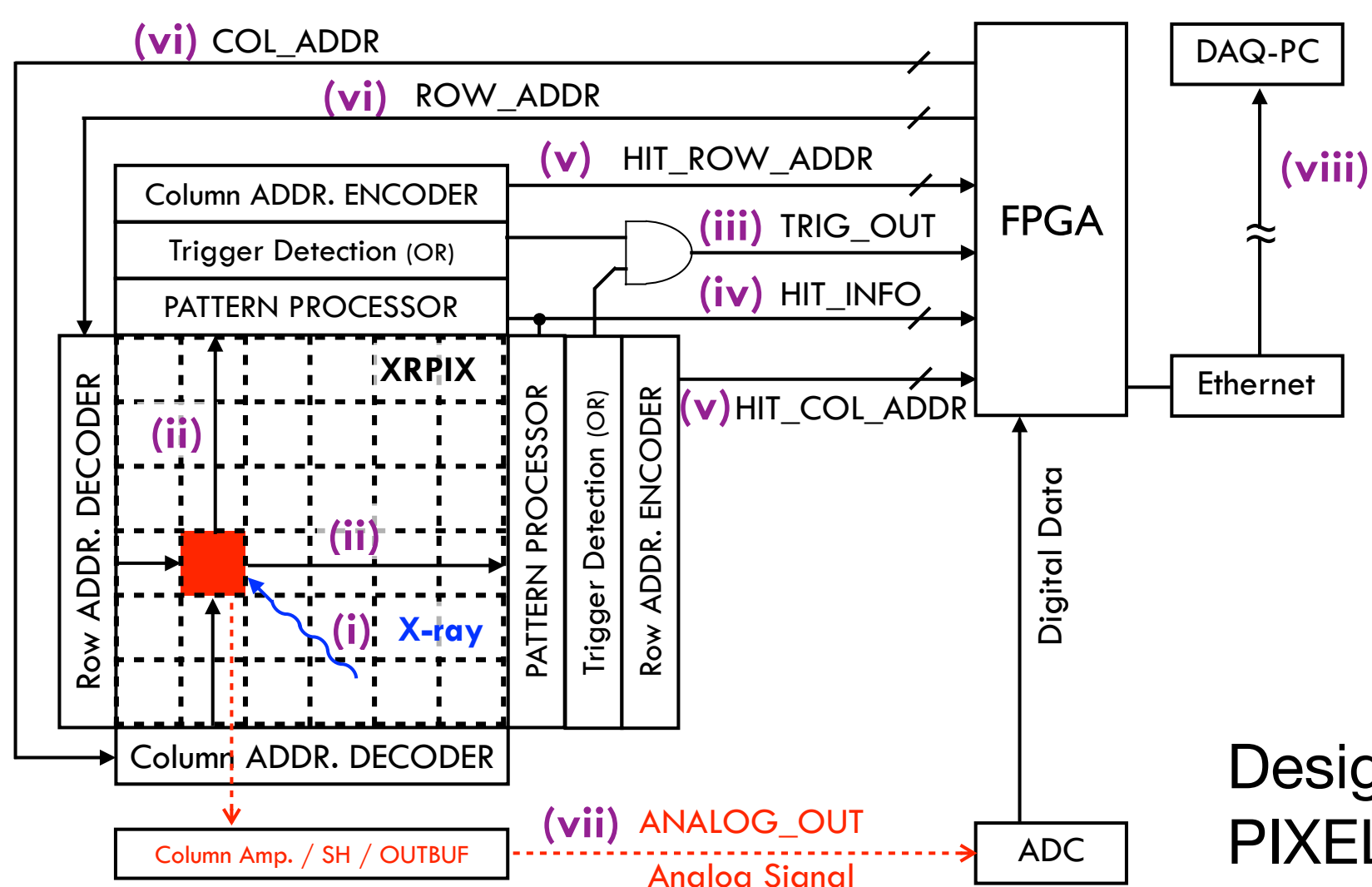
XRPIX5



AR-TB Beam Test in 2022 (3 GeV)



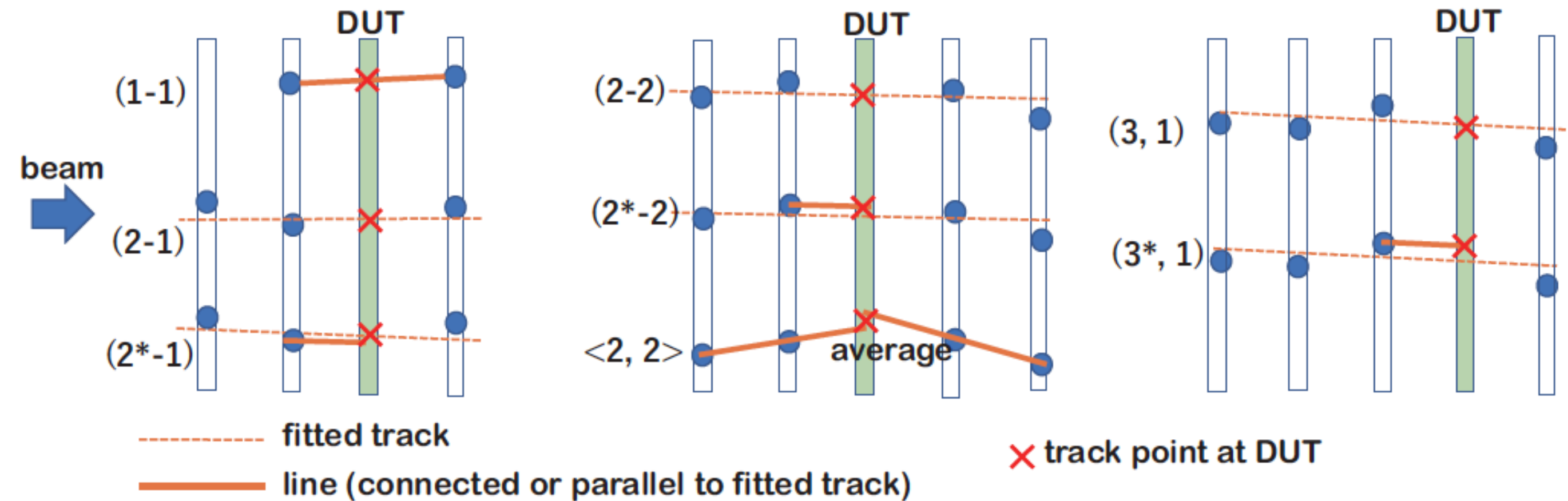
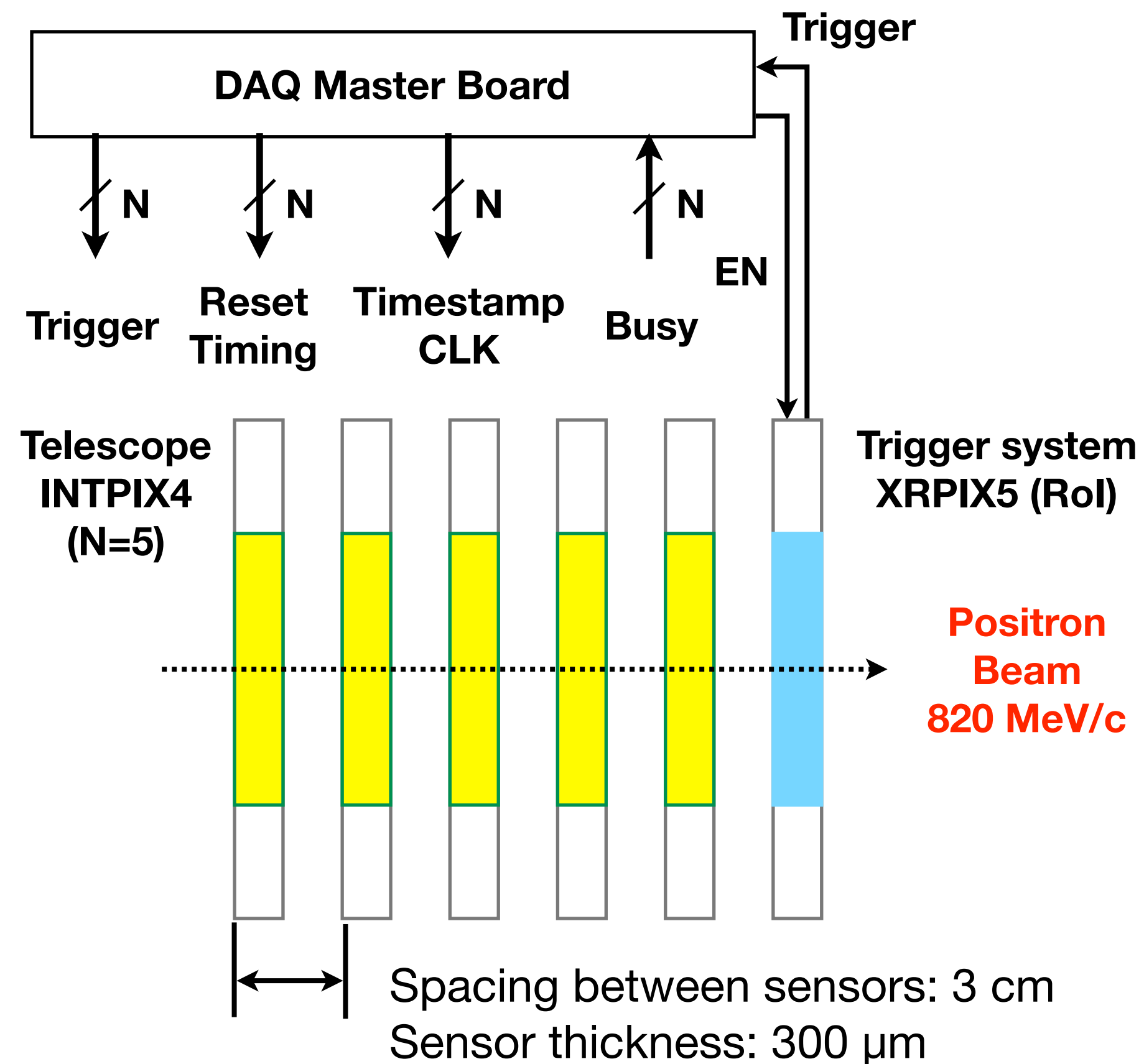
XRPIX series are pixel sensors for X-ray astrophysics. Outputs trigger and hit position address when a hit is detected. Region of Interest function is implemented.



Designed by A. Takeda, Univ. of Miyazaki

PIXEL2022: https://indico.cern.ch/event/829863/contributions/4479488/attachments/2568027/4428082/20221215_PIXEL2022_takeda_v1.pdf

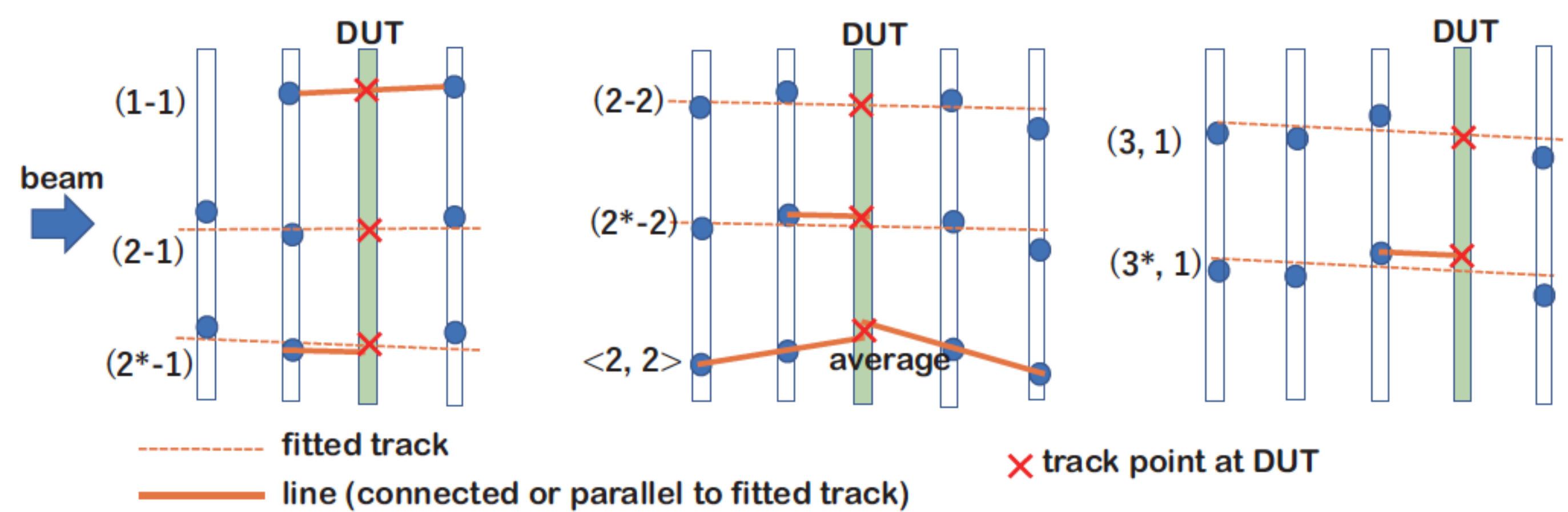
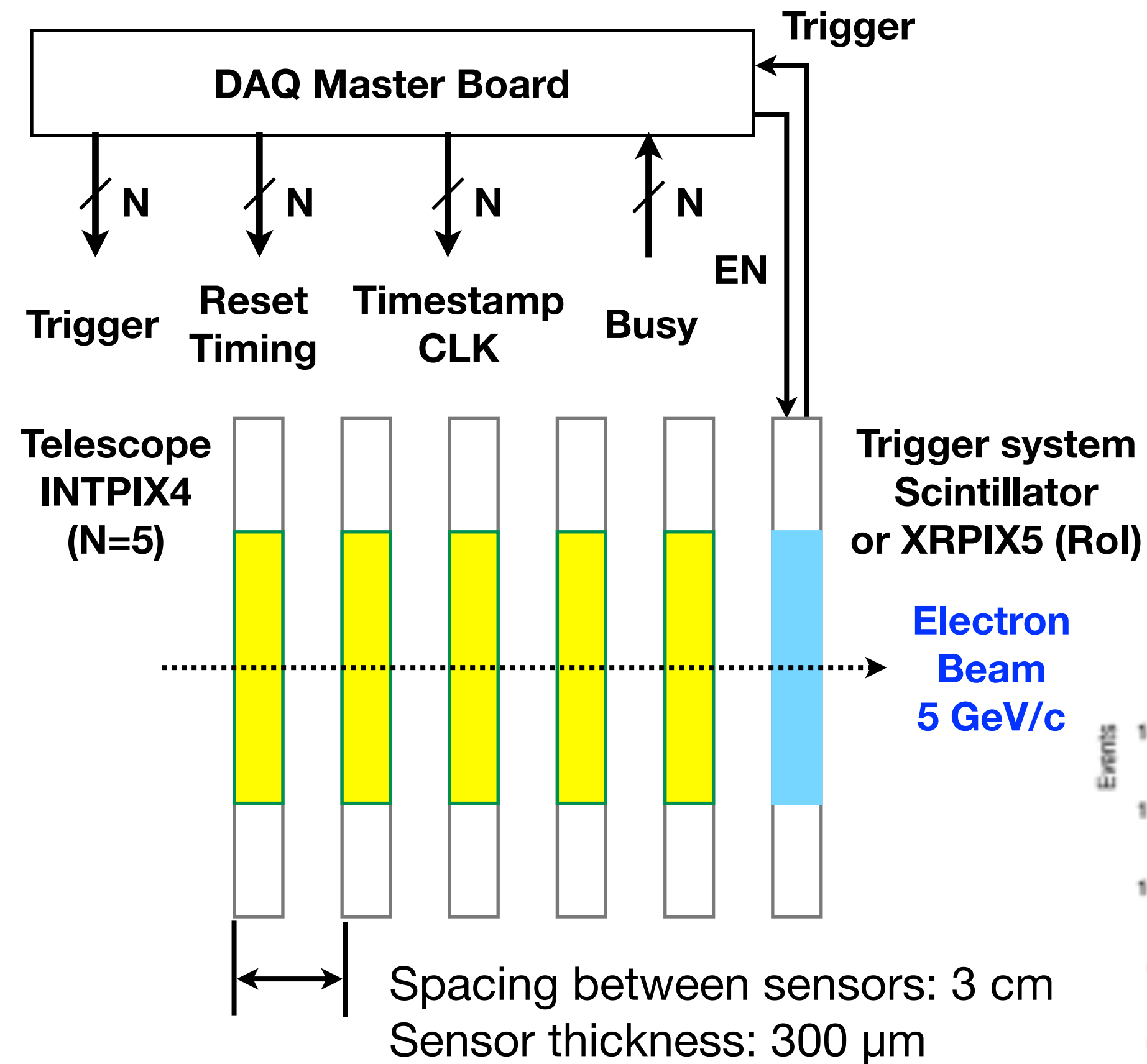
Tracking Study at ELPH in 2021



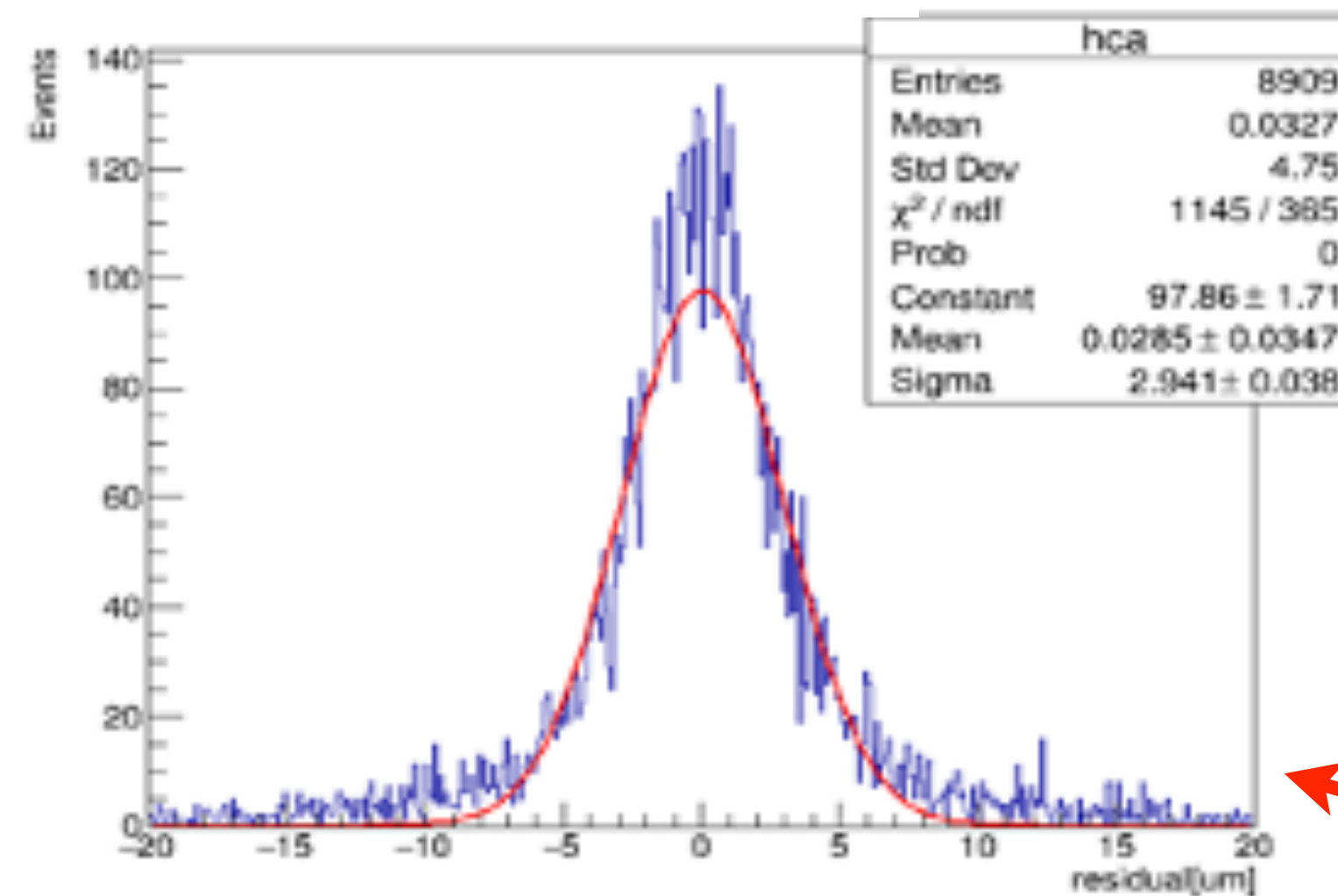
Tracking method	DUT			Average
	L2	L3	L4	
(1-1)	12.06±0.10/11.91±0.10	12.15±0.10/12.24±0.10	12.71±0.12/12.98±0.11	12.34±0.11
(2-1)	-	14.42±0.12/14.54±0.12	14.91±0.13/15.33±0.13	14.80±0.12
(2*-1)	-	11.80±0.10/11.72±0.12	12.23±0.10/12.40±0.10	12.04±0.11
(1-2)	14.32±0.12/14.27±0.17	14.48±0.12/14.48±0.12	-	14.39±0.12
(1-*2)	11.72±0.10/11.63±0.10	12.18±0.10/12.22±0.12	-	11.94±0.11
(2-2)	-	20.28±0.16/20.54±0.17	-	20.31±0.17
(2*-2)	-	14.57±0.12/14.63±0.17	-	14.60±0.15
(3-1)	-	-	16.28±0.14/16.11±0.14	16.20±0.14
(3*-1)	-	-	15.27±0.12/14.27±0.17	14.77±0.15
(1-3)	14.32±0.12/14.27±0.17	-	-	14.30±0.15
(1-*3)	14.87±0.14/15.02±0.12	-	-	14.95±0.13
<2*-1,1-*2>	-	11.10±0.10/10.98±0.09	-	11.04±0.10

- Stack the sensors as close to each other as possible.
- Reconstruct the upstream and downstream tracks of the DUT.
- Extrapolate the track from the hit immediately before the DUT.
- Define the beam position by taking the average of the two tracks.

Beam Test at ARTB in 2022



Residual

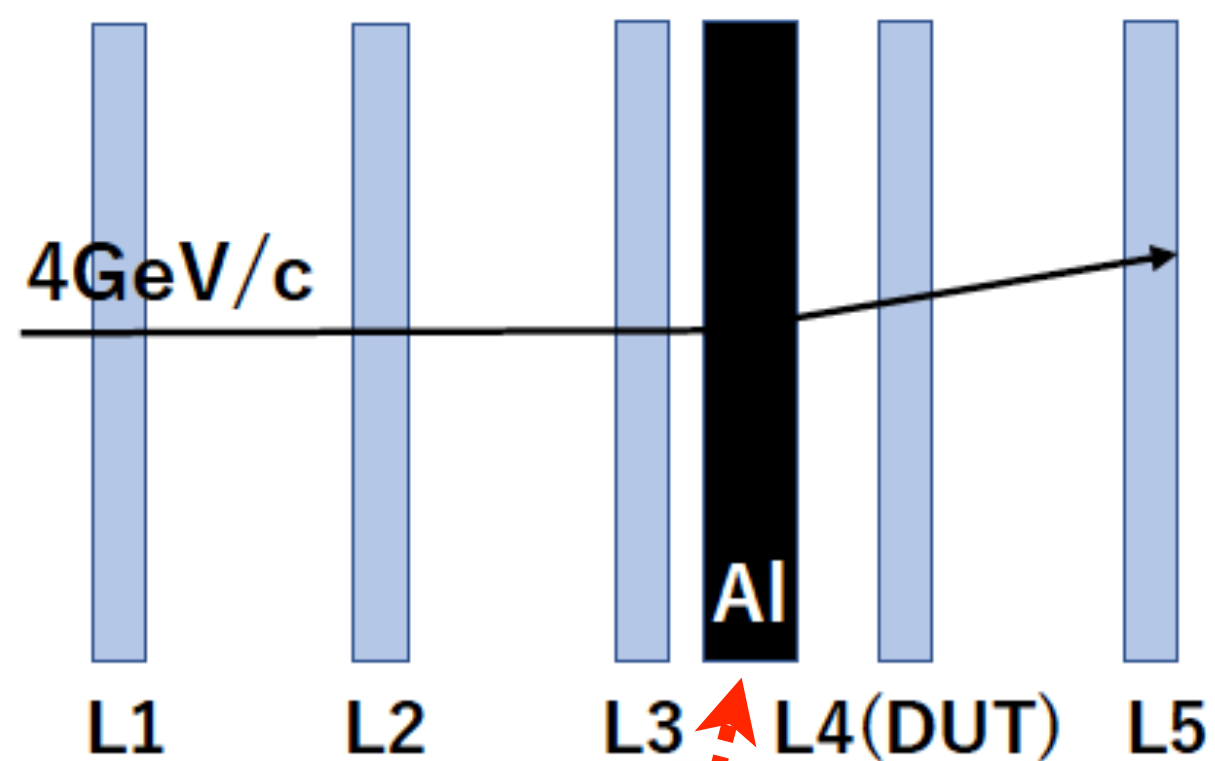


$p = 5 \text{ GeV}/c$

再構成方法	位置分解能[μm]
2*-1	3.34 ± 0.04
2-1	3.73 ± 0.09
3*-1	3.72 ± 0.05
3-1	3.94 ± 0.94
<2-0,0-2>	4.87 ± 0.06
<2*-1,1-*2>	3.02 ± 0.04

Beam Test at ARTB in 2022

Tracking for large amounts of material budget detector.

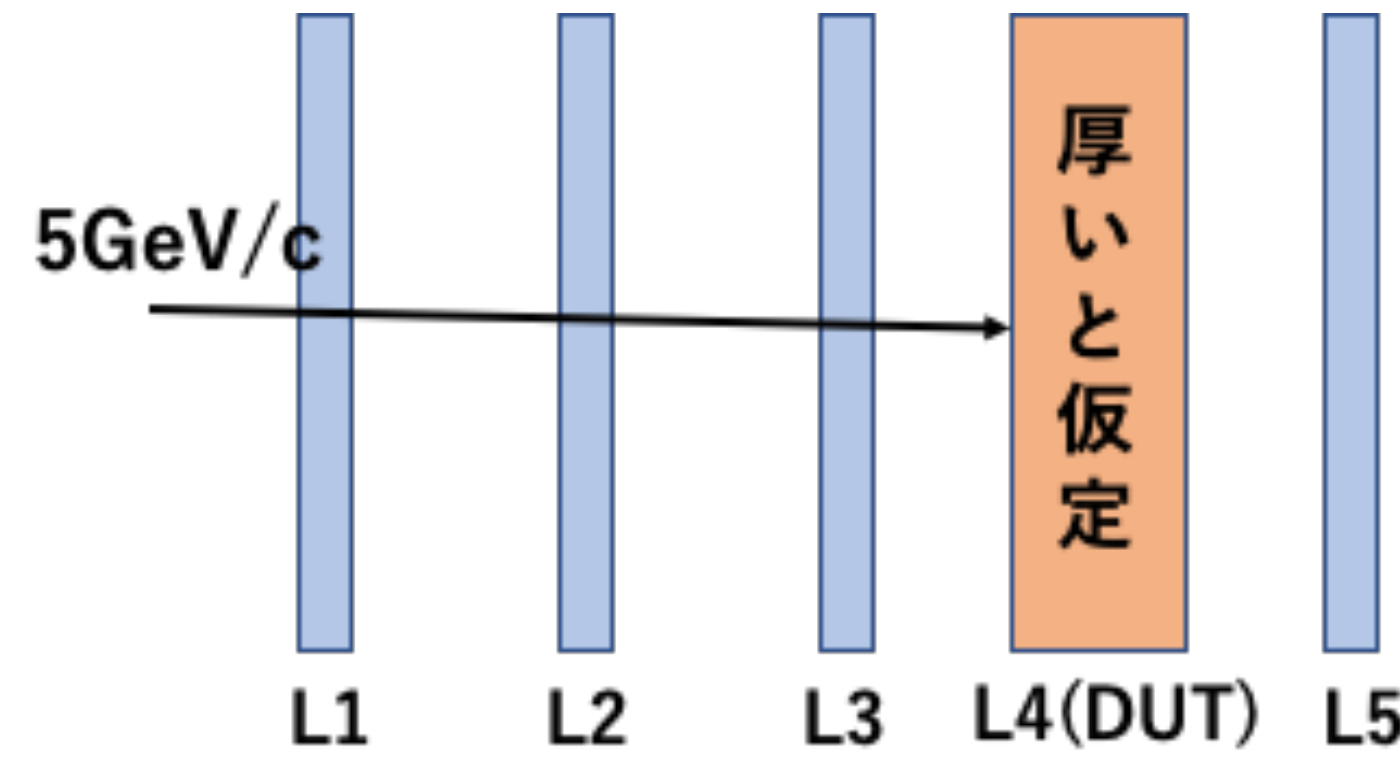


2mm thick Al plate emulates thick DUT.

Residual (μm)

Method	w/o Al (μm)	w/Al (μm)
2*-1	3.80 ± 0.06	4.53 ± 0.07
3*-1	4.44 ± 0.07	4.75 ± 0.08
<2-0,0-2>	5.79 ± 0.10	8.14 ± 0.13
<2*-1,1-*2>	3.41 ± 0.06	3.68 ± 0.06

$p = 4 \text{ GeV}/c$



Assuming DUT is very thick like a calorimeter. L5 can not be used for tracking.

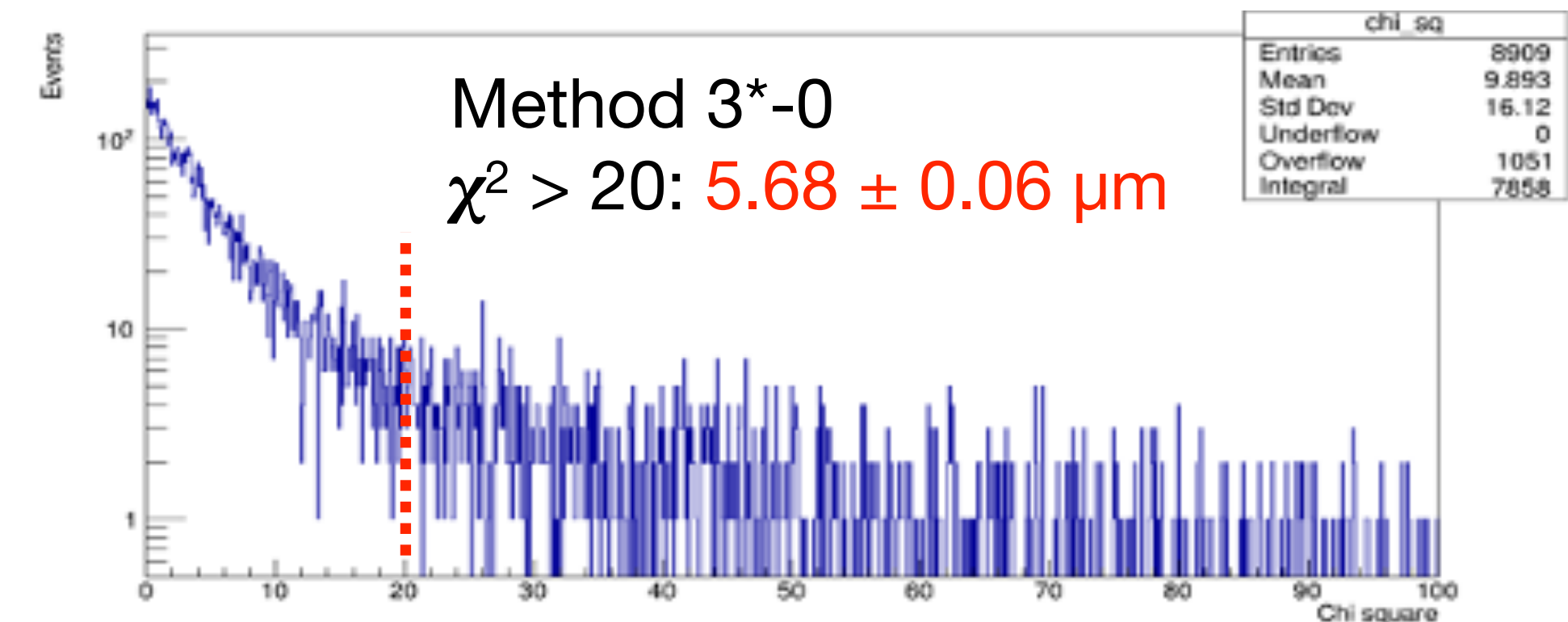
Method	Residual (μm)
2-0	6.01 ± 0.07
3-0	6.98 ± 0.08
3*-0	6.40 ± 0.08
4*-0	7.12 ± 0.08

$p = 5 \text{ GeV}/c$

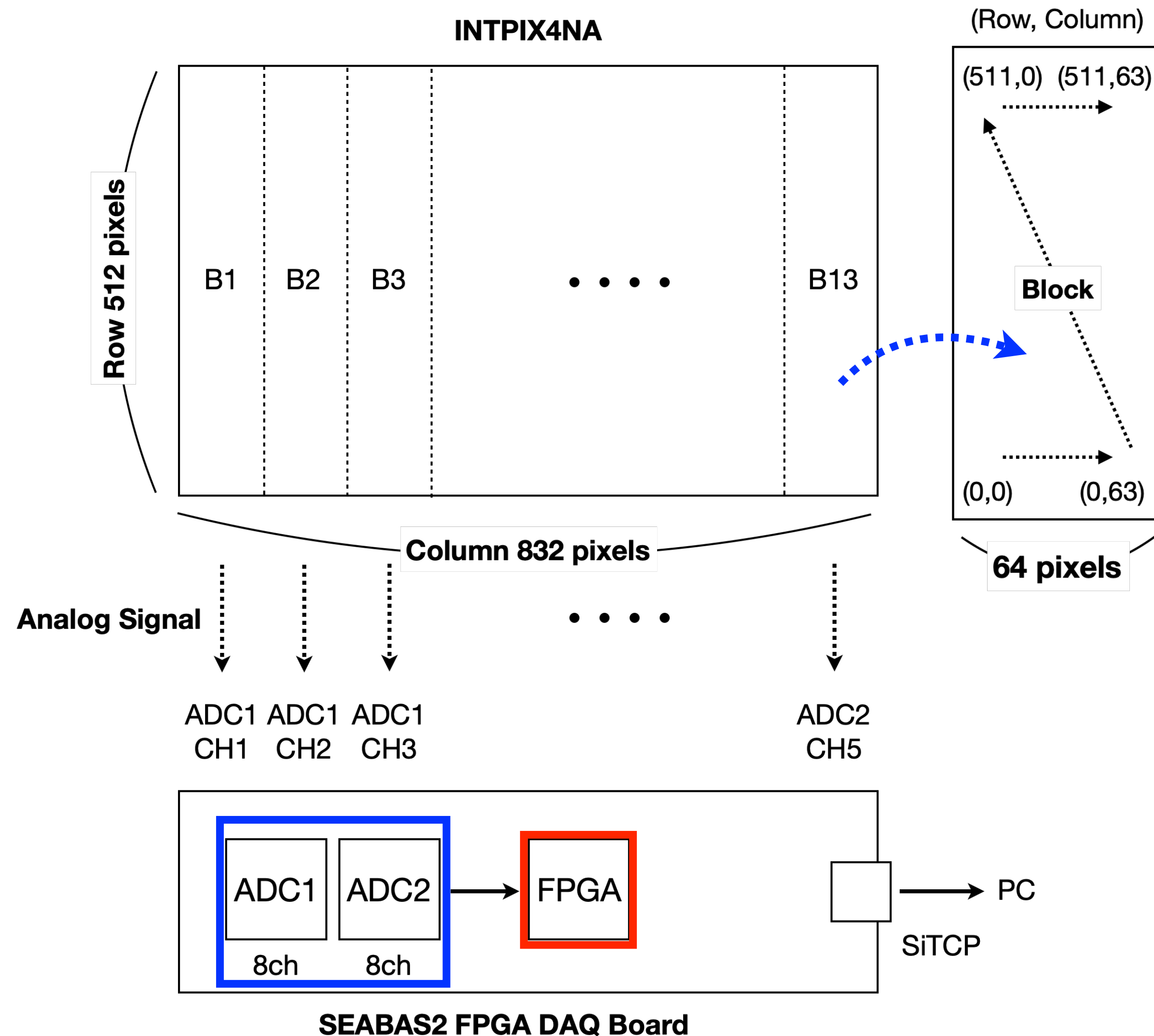
Strasbourg

$$\chi^2 = \sum_{i=L_1}^{L_3} \left\{ \frac{\text{hitpos}_i - \text{recpos}_i}{\sigma_{\text{int}}} \right\}^2$$

$$\sigma_{\text{int}} = 1.5 \mu\text{m}$$



INTPIX4 Sensor, Zero-Suppression Logic

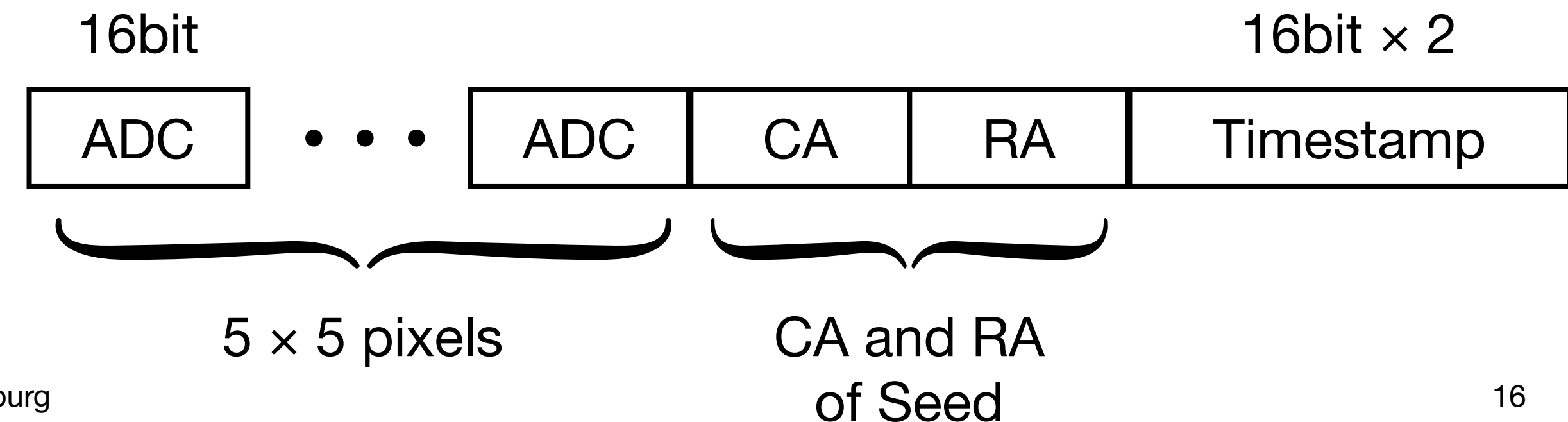


Procedure

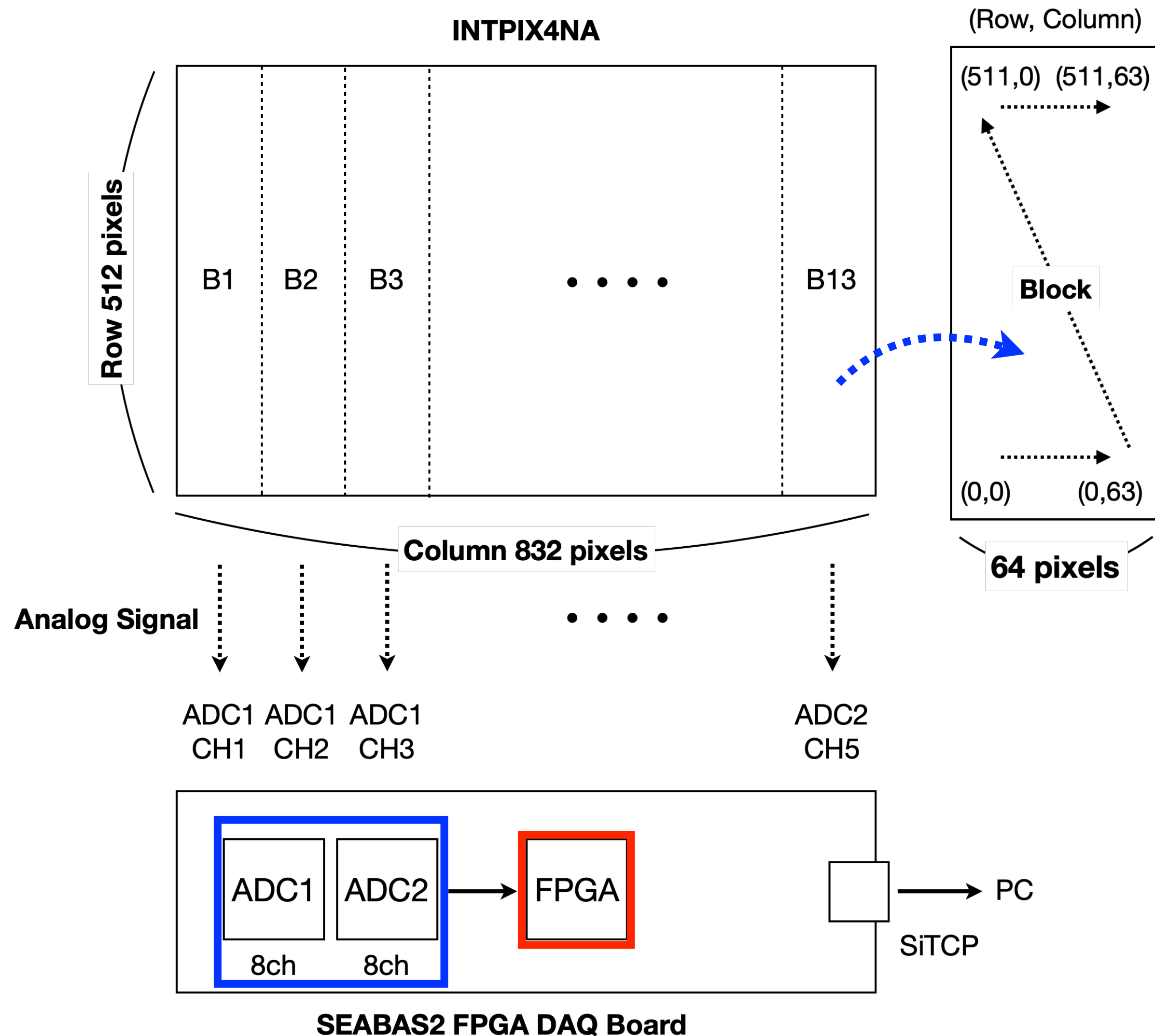
- Column is divided into 13 blocks and 1 block consists of 64 columns.
- Each block is connected to each channel of the on-board ADC.
- The analog signal is read out from all pixels and then digitized by the on-board 12-bit ADC in parallel with 13 blocks.
- Set a threshold for each block to find the cluster seed.
- The ADC counts of the cluster seed and the 5×5 pixels surrounding the seed are read out to the PC.

Data structure

The size of the register for data TX is 16-bit.



INTPIX4 Sensor, Zero-Suppression Logic



Breakdown of DAQ rate

Time for AD conversion

200 ns per pixel

$$200 \text{ ns} \times 518 \text{ row} \times 64 \text{ col} = 6.6 \text{ ms}$$

Time for readout per sensor

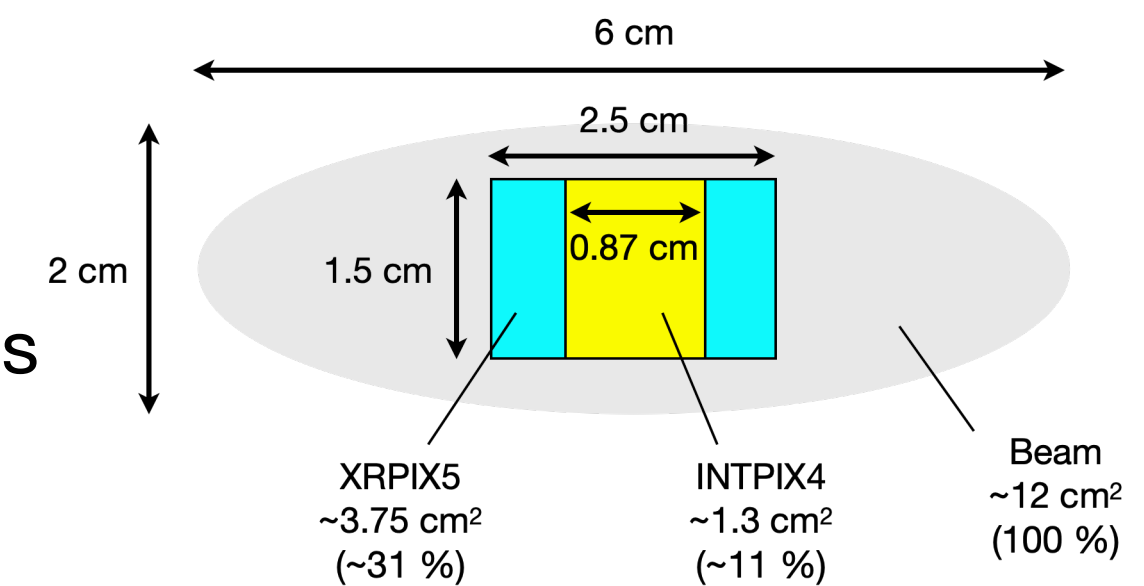
Speed: 1Gbps

Data size: 16bit \times 29

$$(29 \times 16 \text{ bit}) / 10^9 \text{ s} = 0.46 \mu\text{s}$$

DAQ rate for 5 sensors

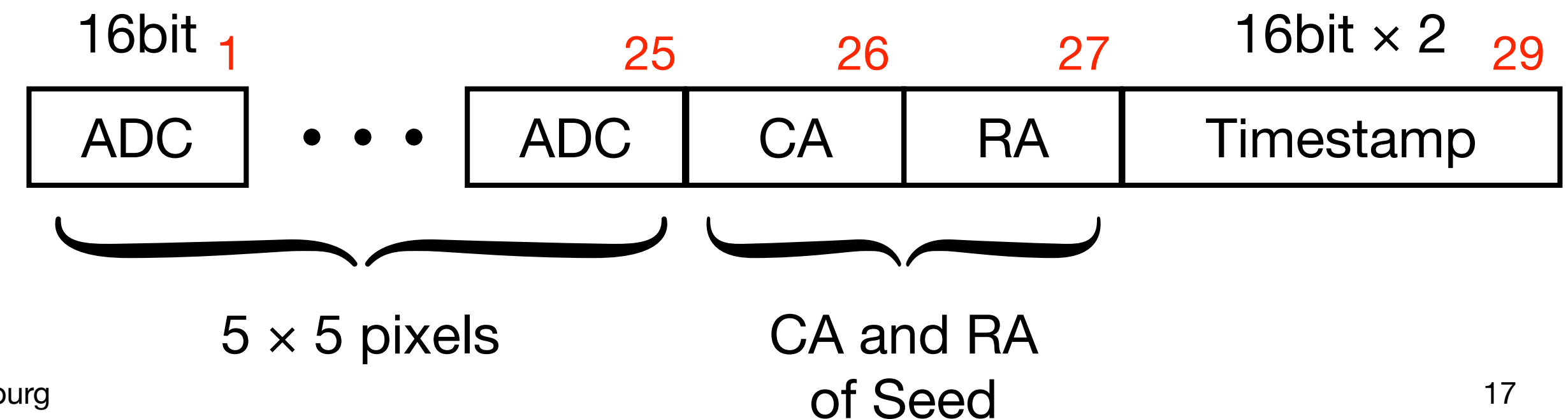
$$1 / (6.6 \text{ ms} + 5 \times 0.46 \mu\text{s}) = \mathbf{150 \text{ Hz}}$$



Assuming a beam rate of **1kHz**, the trigger rate corresponding to the active area of INTPIX4 would be about **100 Hz** (area ratio).

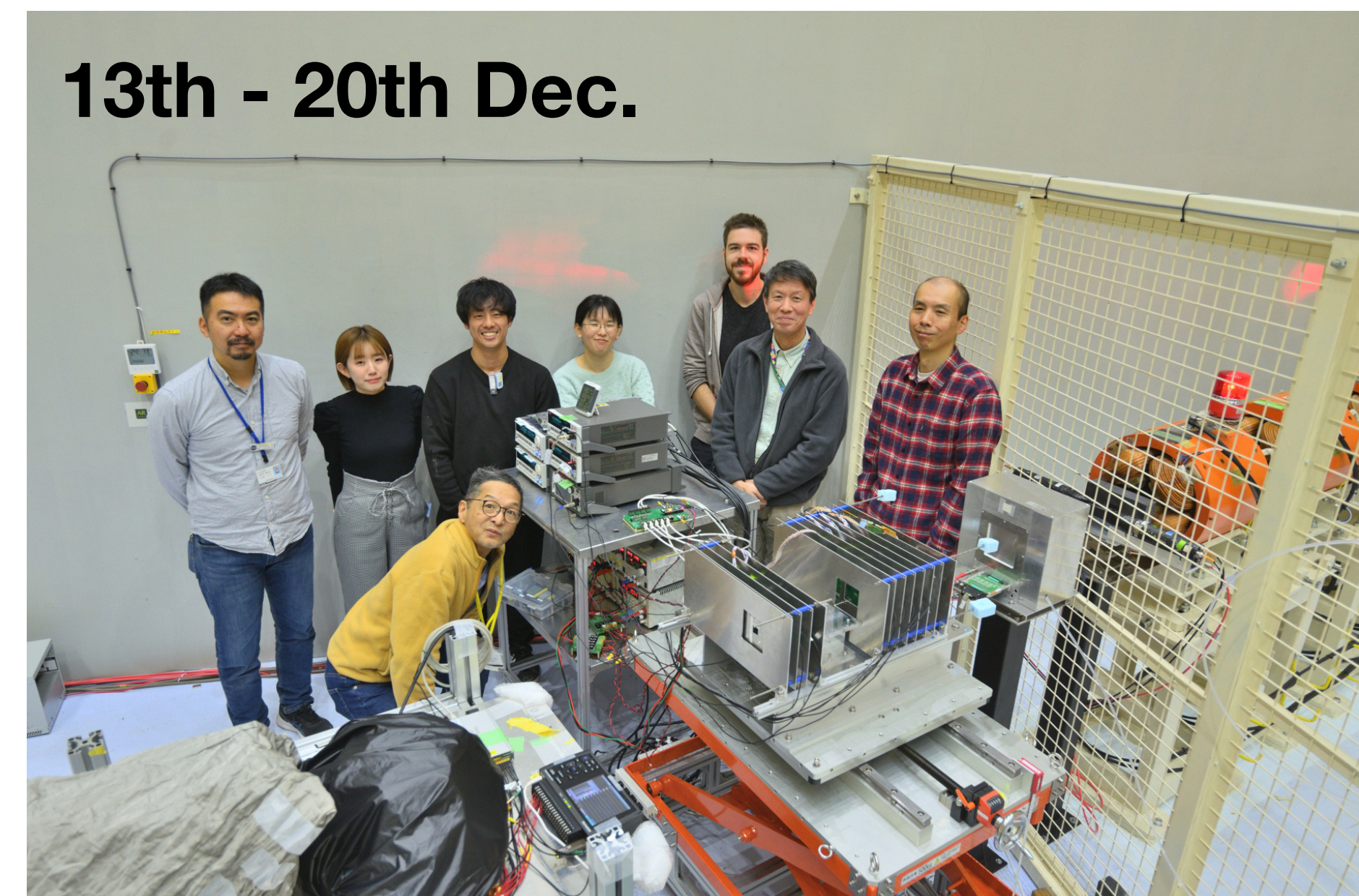
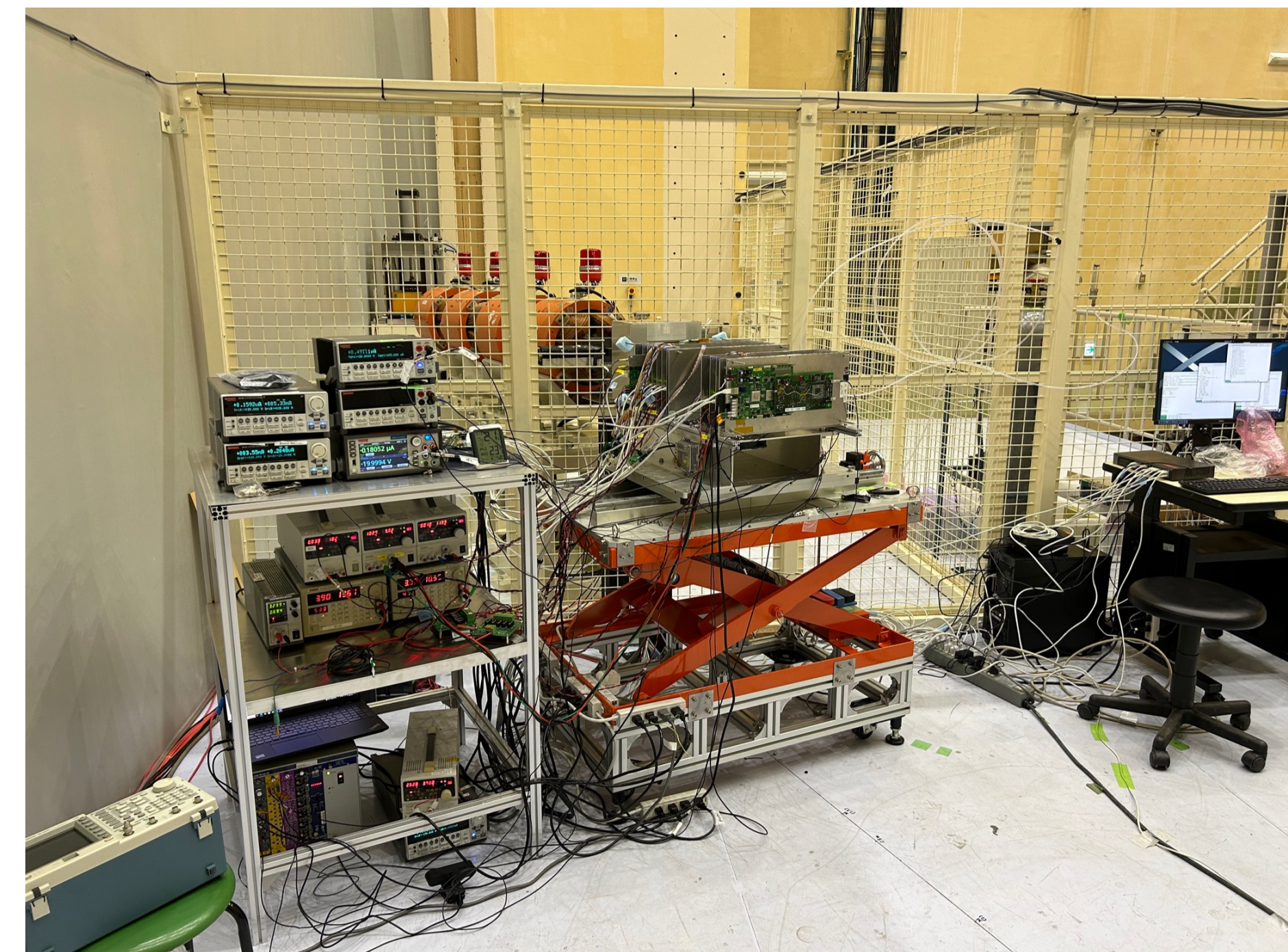
Safety factor 2 \times 100 Hz = 200 Hz ← target value

The size of the register for data TX is 16-bit.

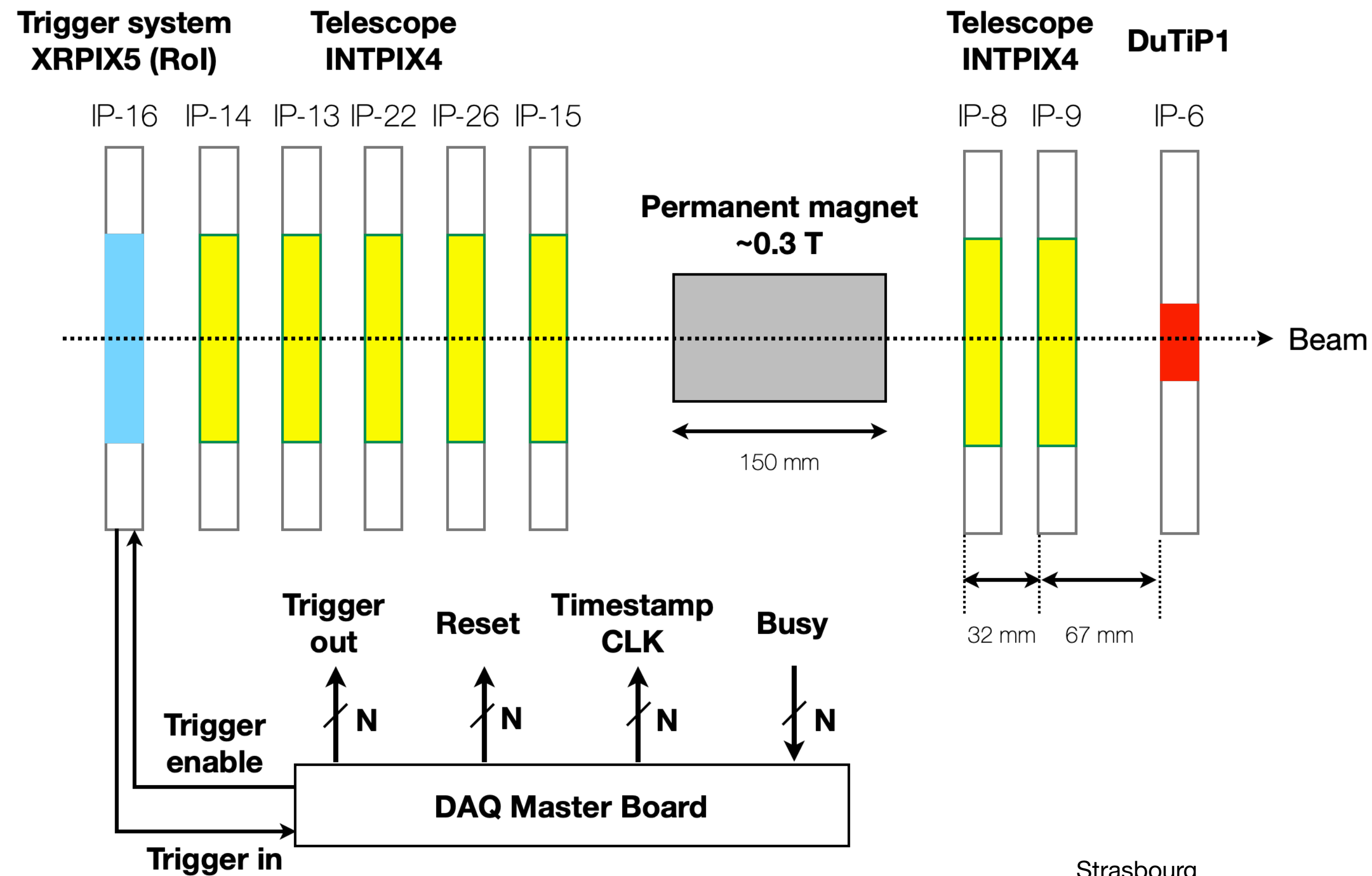


Beam Test at ARTB in 2023

- SOI Telescope system with Zero-Suppression Logic
- DuTiP1 (Ishikawa)
- Micro spectrometer (still work in progress)



13th - 20th Dec.

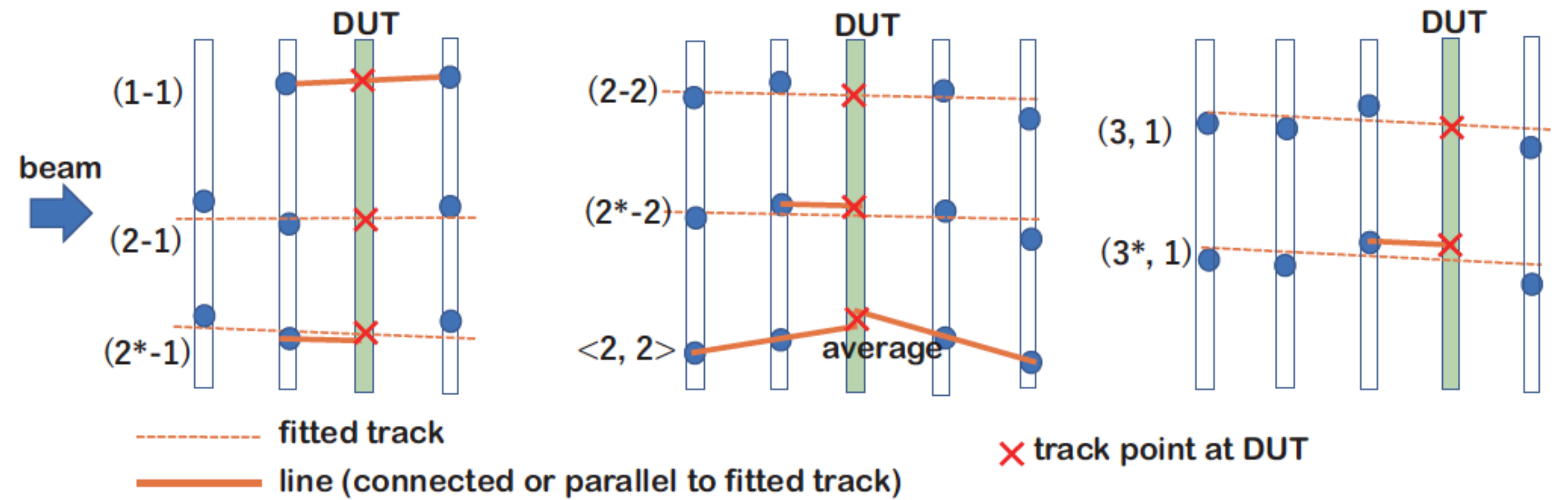
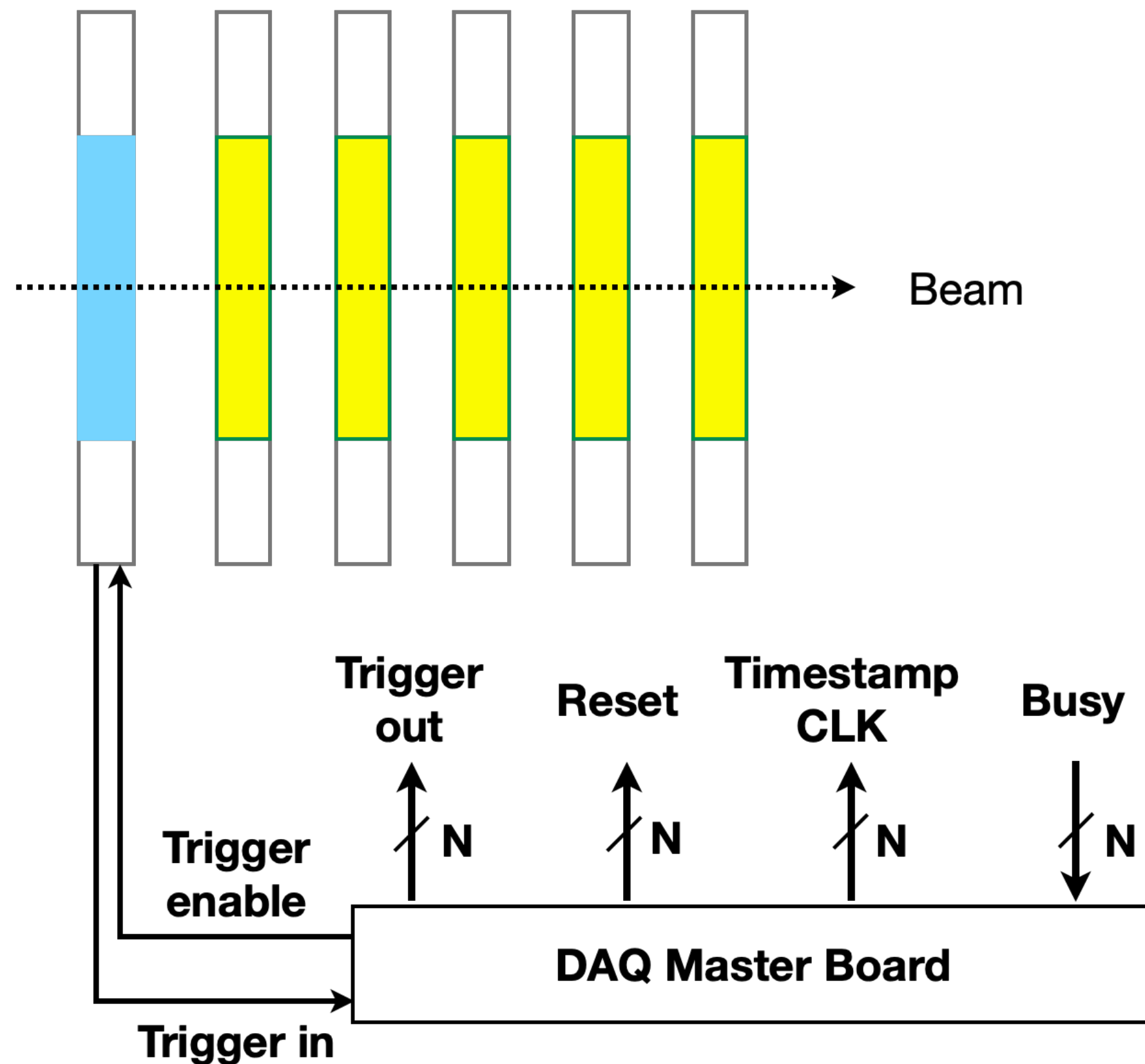


Resolution

Trigger system
XRPIX5 (RoI)

Telescope
INTPIX4

IP-16 IP-14 IP-13 IP-22 IP-26 IP-15



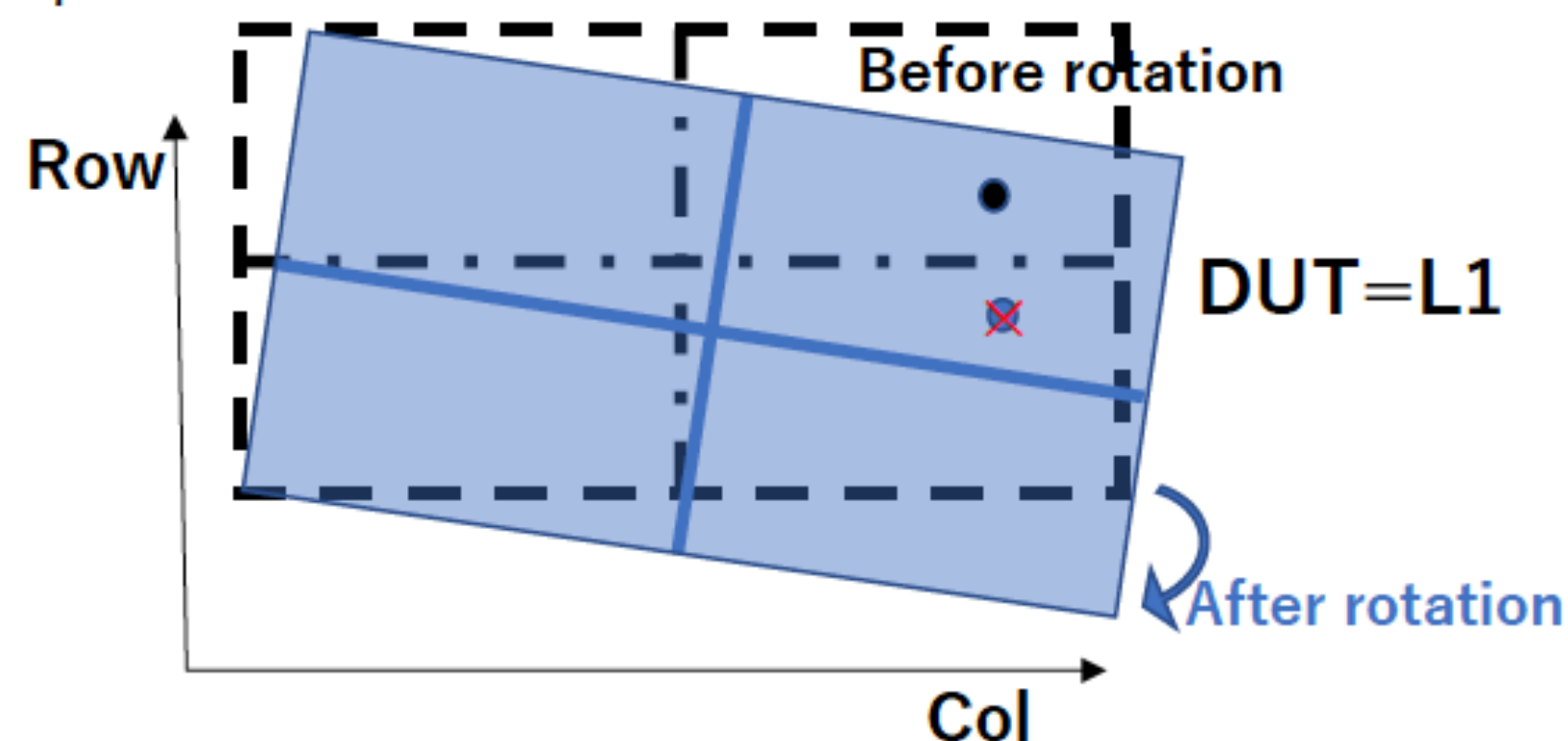
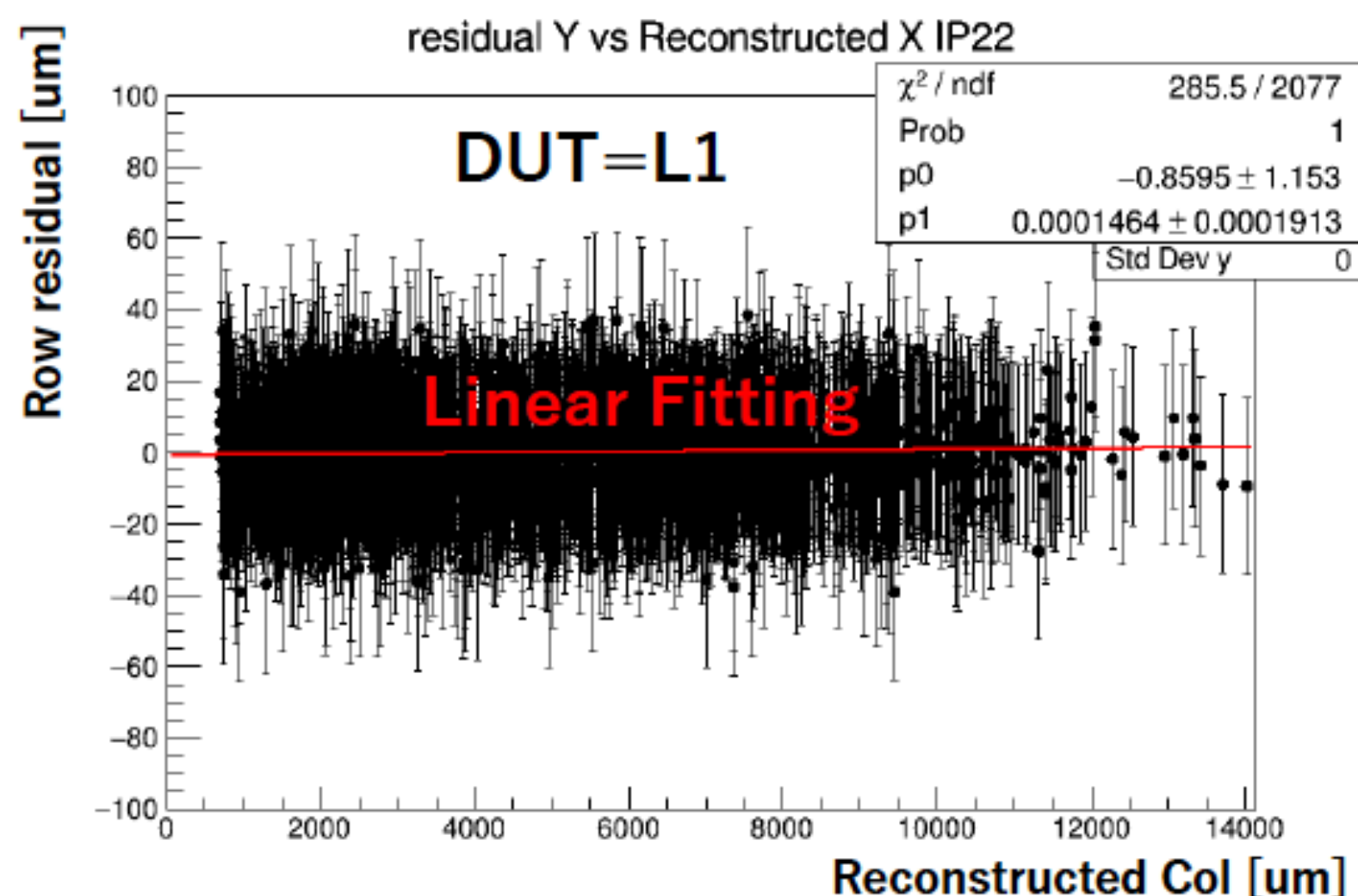
Method	Full Frame (μm)	Zero-Suppression (μm)
1-1(L2)	3.48 ± 0.05	3.78 ± 0.05
2-0(L3)	6.86 ± 0.10	7.36 ± 0.09
3-0(L4)	9.40 ± 0.13	9.24 ± 0.10
2-1(L3)	4.61 ± 0.06	4.94 ± 0.05
3*-0(L4)	8.52 ± 0.12	8.82 ± 0.10
2*-1(L3)	3.58 ± 0.05	4.20 ± 0.05
$\langle 2-0, 0-2 \rangle$ (L3)	6.74 ± 0.09	7.10 ± 0.08
$\langle 2*-1, 1-*2 \rangle$ (L3)	4.11 ± 0.06	4.72 ± 0.06

$p = 5 \text{ GeV}/c$

Backup

5GeV/cビームでのアライメント -回転補正-

- ✓ L3を基準とした回転補正、並進補正によるアライメント
- ✓ 回転補正は下図のような残差分布を基に評価
(並進補正は残差分布の中心値から評価)



- ✓ 完全にアライメントされるとフィットの傾きは0になる
- ✓ アライメントによって生じる最大のずれは1.92um

Col方向の全長 × 傾き

他の層でのアライメントによる最大のずれ

DUT	L1	L2	L4	L5
Track	0-2	1-1	1-1	2-0
X	2.08um	1.63um	0.49um	1.01um
Y	1.92um	0.28um	0.50um	1.60um

- ✓ ずれは位置分解能より小さく (特に低運動量1,2GeV/c)
アライメントが内挿とのずれの原因とは考えにくい
→ビーム運動量にある程度の不確かさがある可能性

再構成方法と (4GeV/cに対する) 位置分解能 16/9

Method \ DUT	L1	L2	L3	L4	L5
1-1	-	3.59 ± 0.06	3.57 ± 0.06	3.65 ± 0.06	-
2-0	-	-	6.78 ± 0.11	6.67 ± 0.11	6.84 ± 0.11
3-0	-	-	-	7.94 ± 0.14	8.12 ± 0.13
3*-0	-	-	-	7.36 ± 0.12	7.29 ± 0.11
4*-0	-	-	-	-	8.41 ± 0.14
2*-1	-	-	3.79 ± 0.06	3.81 ± 0.06	-
1-2*	-	3.78 ± 0.06	3.77 ± 0.06	-	-
3*-1	-	-	-	4.44 ± 0.07	-
1-3*	-	4.46 ± 0.07	-	-	-
<2-2>	-	-	5.79 ± 0.10	-	-
<2-1,1-2>	-	-	3.41 ± 0.06	-	-

- 同じ再構成方式では、DUTに依らず同じ位置分解能を示す
 - 820MeV/cではやはり下流センサーは散乱の影響を受けた
- ELPH同様*付きの方法が優位

位置分解能[um]

4600トラック (Run 2 回分のデータ)

5GeV/cアライメントアパメタ使用

*付き:直前センサーからの内挿による評価

<>:得られる2点の再構成位置の平均で評価

再構成方法と (5GeV/cに対する) 位置分解能 17/9

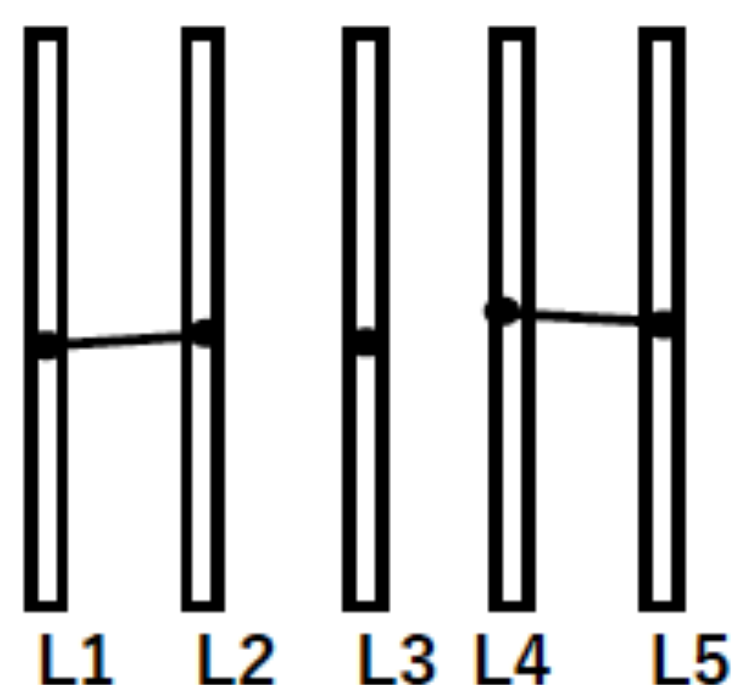
Method \ DUT	L1	L2	L3	L4	L5
1-1	-	3.18 ± 0.04	3.15 ± 0.04	3.02 ± 0.04	-
2-0	-	-	6.09 ± 0.07	6.08 ± 0.07	5.87 ± 0.07
3-0	-	-	-	6.89 ± 0.08	7.07 ± 0.08
3*-0	-	-	-	6.34 ± 0.08	6.45 ± 0.08
4*-0	-	-	-	-	7.12 ± 0.08
2*-1	-	-	3.43 ± 0.04	3.24 ± 0.04	-
1-*2	-	3.38 ± 0.04	3.17 ± 0.04	-	-
3*-1	-	-	-	3.72 ± 0.05	-
1-*3	-	3.89 ± 0.05	-	-	-
<2-0,0-2>	-	-	4.87 ± 0.06	-	-
<2*-1,1-*2>	-	-	3.02 ± 0.04	-	-

- 同じ再構成方式では、DUTに依らず同じ位置分解能を示す
 - 820MeV/cではやはり下流センサーは散乱の影響を受けた
- ELPH同様*付きの方法が優位
- バックアップに残差分布掲載してあります。

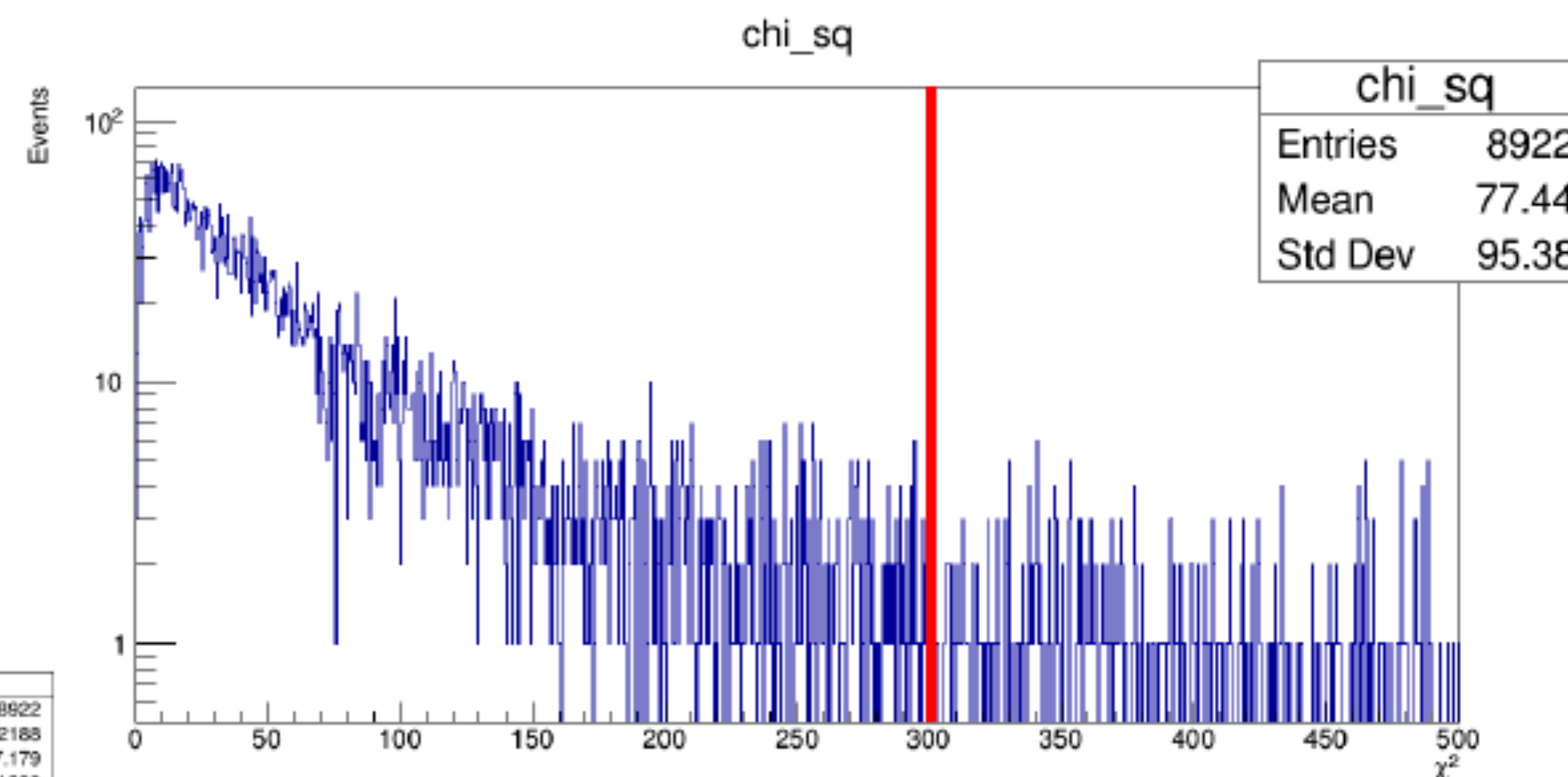
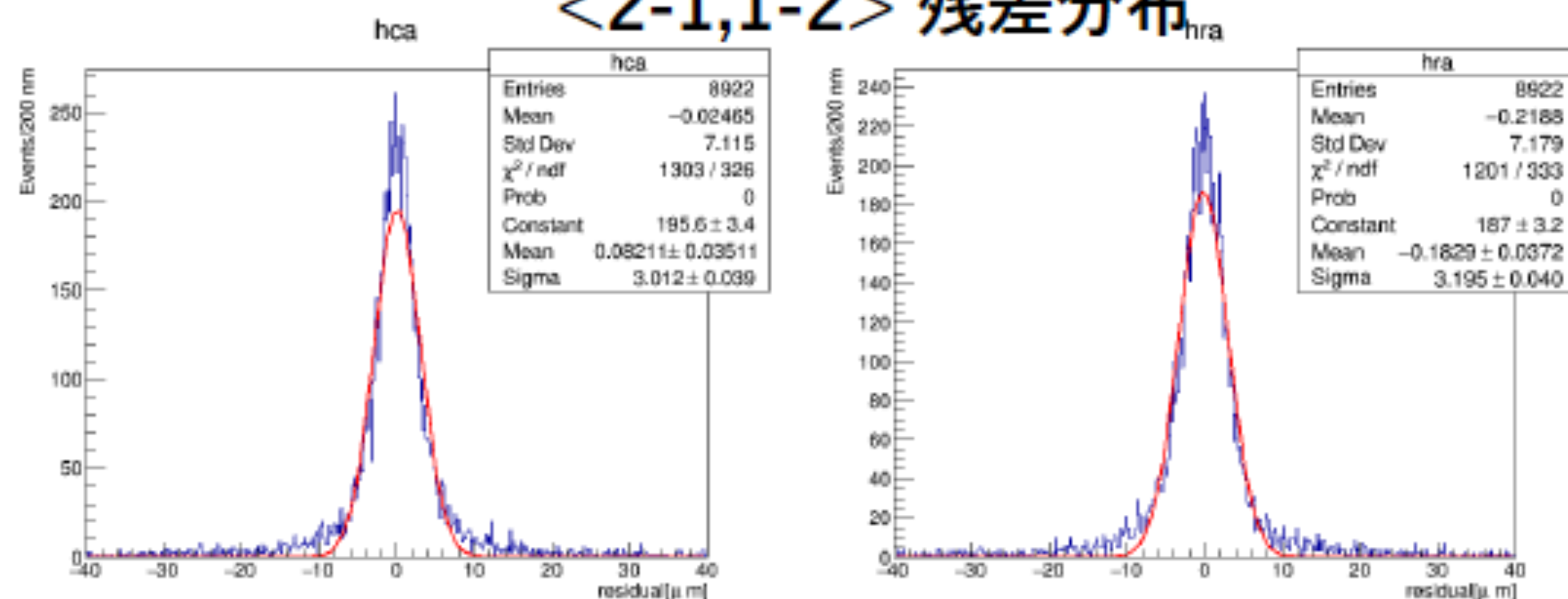
位置分解能[um]
 8909トラック (Run3回分のデータ)
 5GeV/cアライメントパラメタ使用
 *付き:直前センサーからの内挿による評価
 <>:得られる2点の再構成位置の平均で評価

ヒット検出効率

- トラッキングベースで評価
 - 分母D : L1, L2, L4, L5 にクラスタがあるフレーム数 ($\chi^2 < 300$)
 - 分子N : 全Layerにクラスタがあり, 残差が $\pm 3\sigma$ (σ by $\langle 2-1, 1-2 \rangle$) のフレーム数



$\langle 2-1, 1-2 \rangle$ 残差分布

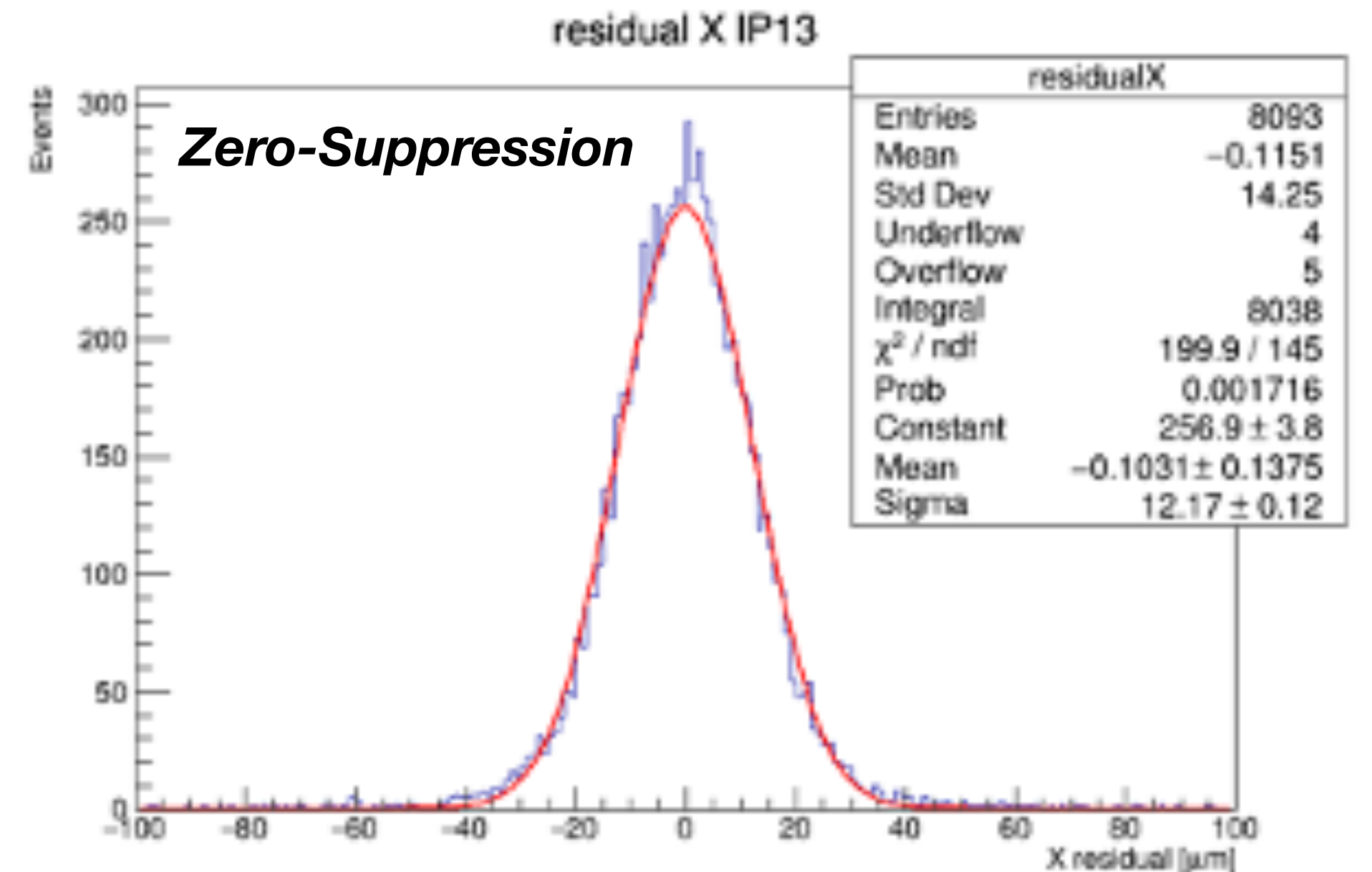
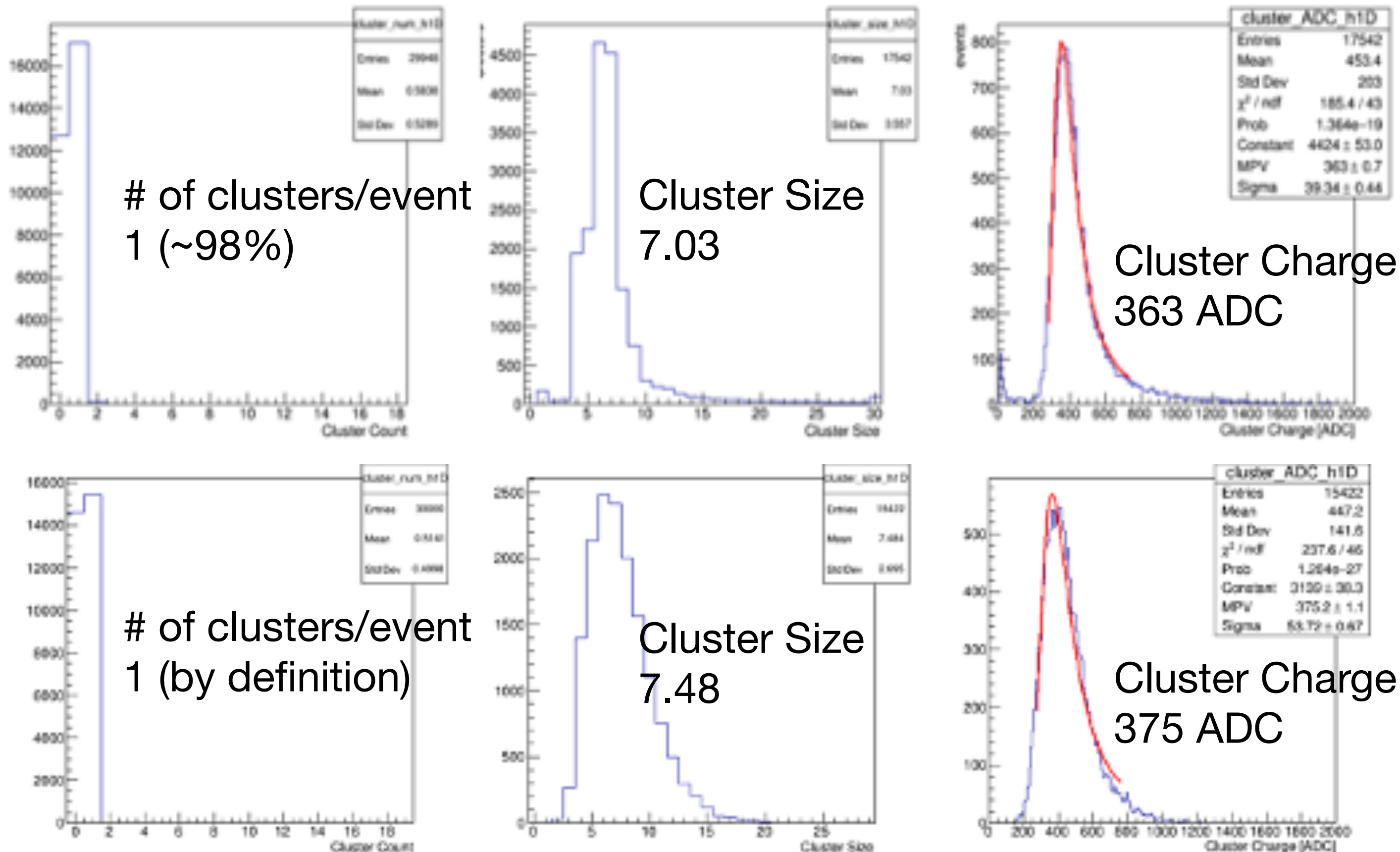


	Run7	Run8	Run11
D	1754	1835	1717
N	1632	1712	1595
$\eta (=N/D)$	0.93	0.93	0.93

Emulation of Zero-Suppression Logic

Data: Full frame readout. Pedestal is evaluated by the on beam full frame readout data.
 Emulation: Set threshold for each block. Seed is the first pixel which exceeds the threshold.

$p = 820 \text{ MeV}/c$ at ELPH



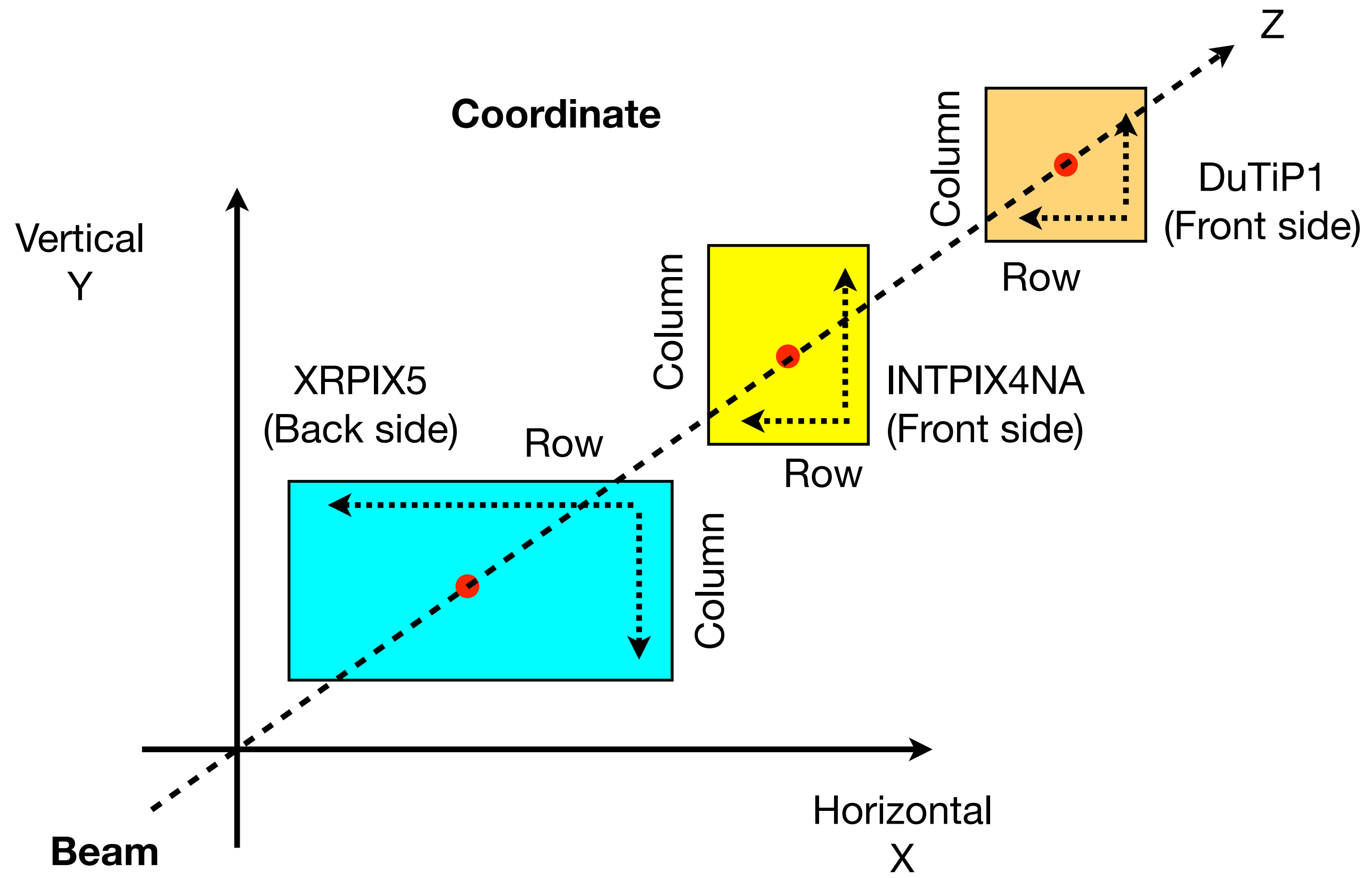
Residual

Full frame readout: $\sigma = 11.10 \pm 0.10 \mu\text{m}$
 Zero-Suppression: $\sigma = 12.17 \pm 0.12 \mu\text{m}$

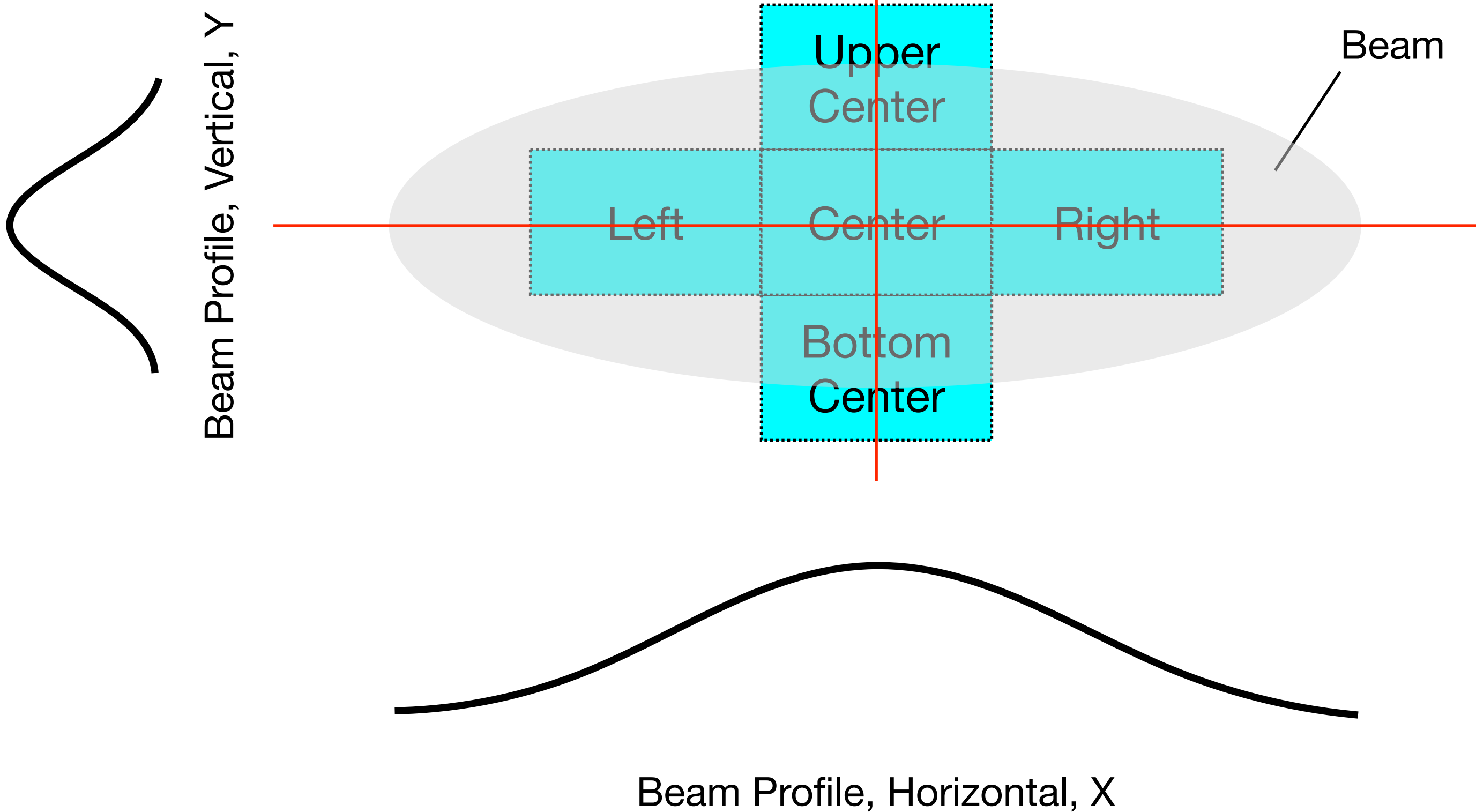
Emulation of Zero-Suppression Logic

```
Block Threshold (60 sigma) Set Now ...  
[Threshold0] 60*1.7739 = 1096.69  
[Threshold1] 60*1.78184 = 1087.8  
[Threshold2] 60*1.76579 = 1094.13  
[Threshold3] 60*1.81057 = 1084.11  
[Threshold4] 60*1.75291 = 1074.86  
[Threshold5] 60*1.73815 = 1070.18  
[Threshold6] 60*1.76574 = 1039.14  
[Threshold7] 60*1.7417 = 1056.66  
[Threshold8] 60*1.71296 = 1067.11  
[Threshold9] 60*1.68594 = 1082.52  
[Threshold10] 60*1.72112 = 1075.68  
[Threshold11] 60*1.66207 = 1097.8  
[Threshold12] 60*1.65497 = 1090.82
```

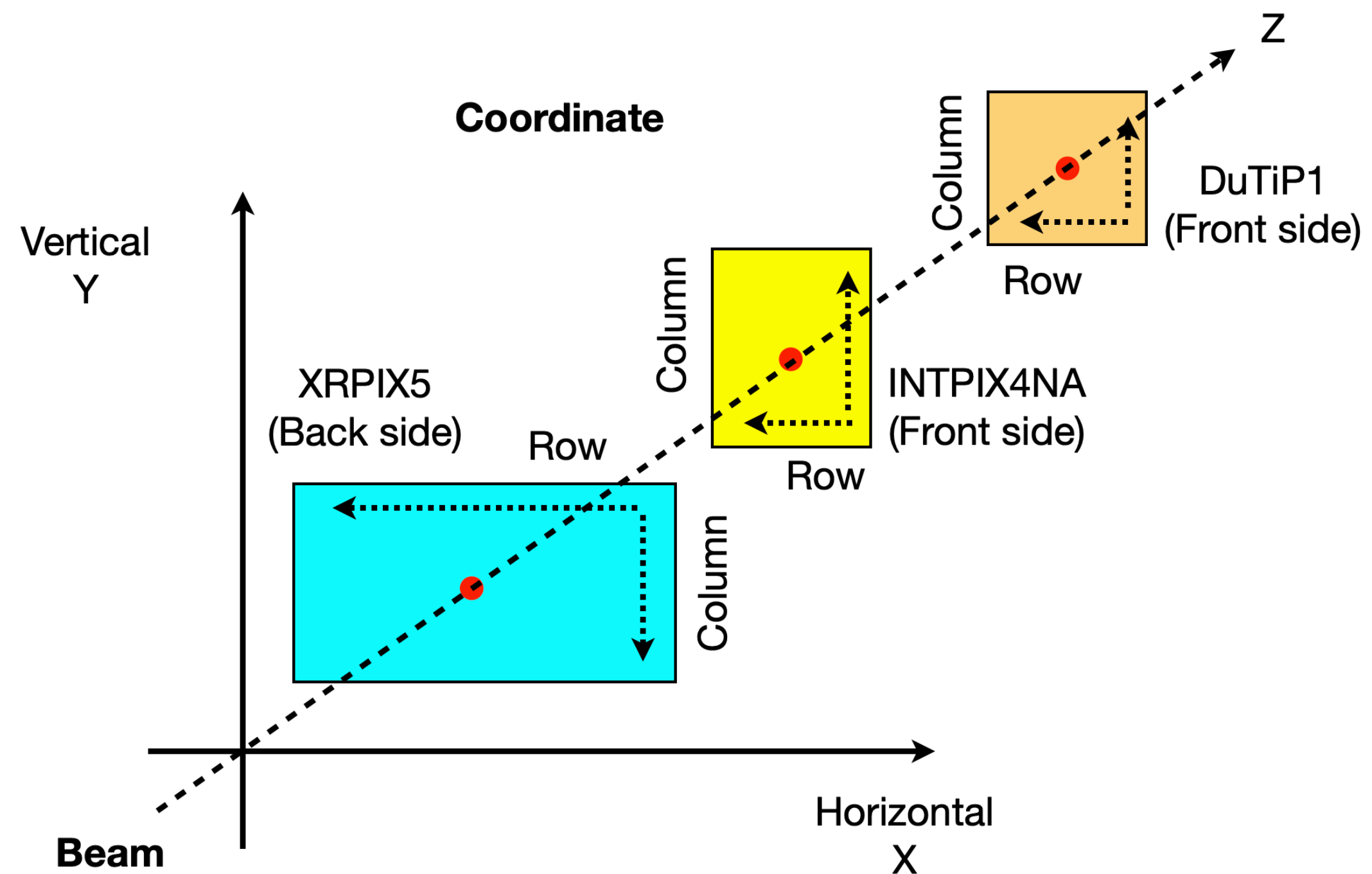
Setup at AR-TB in 2023



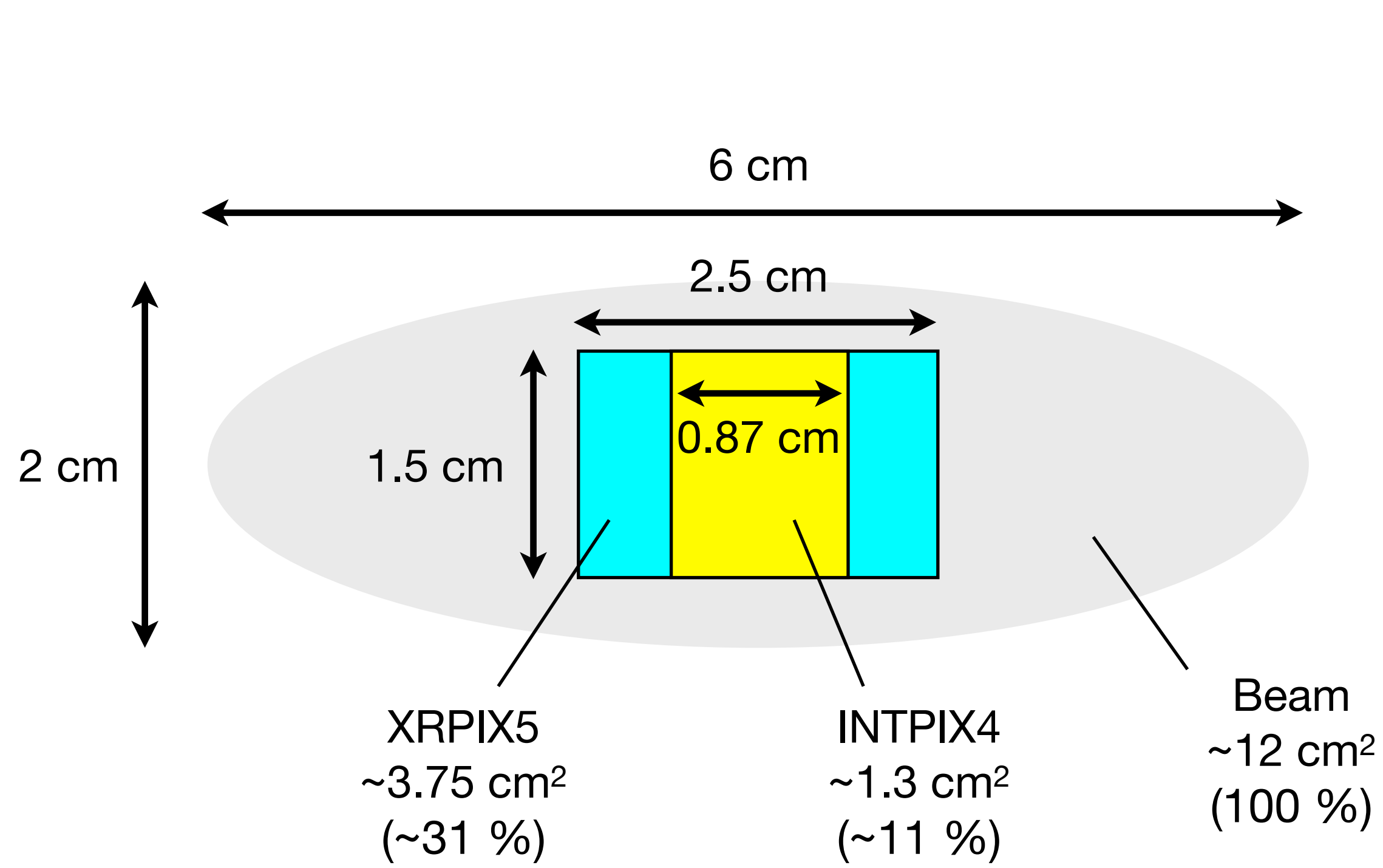
Beam Profile



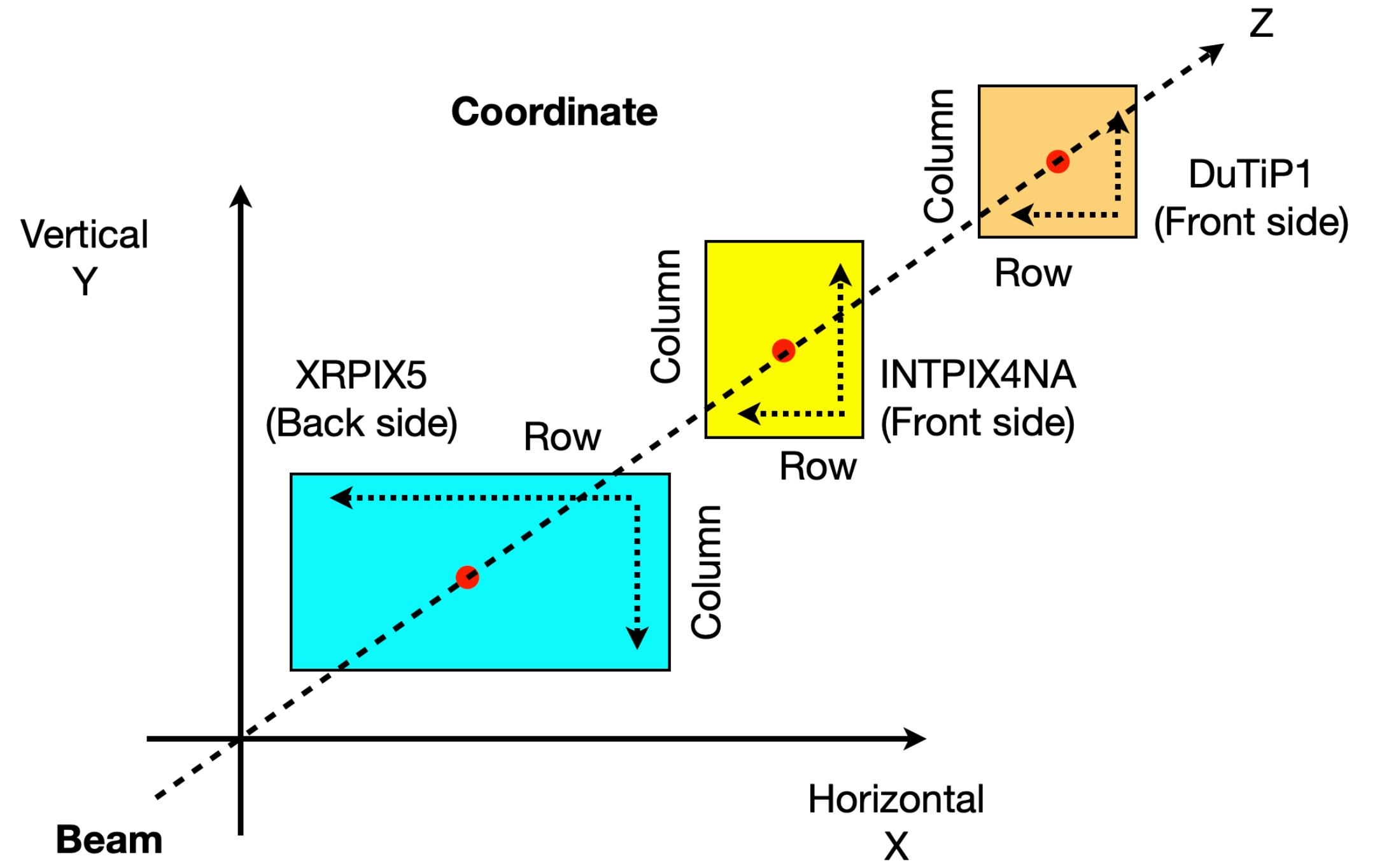
Coordinate



Beam Profile



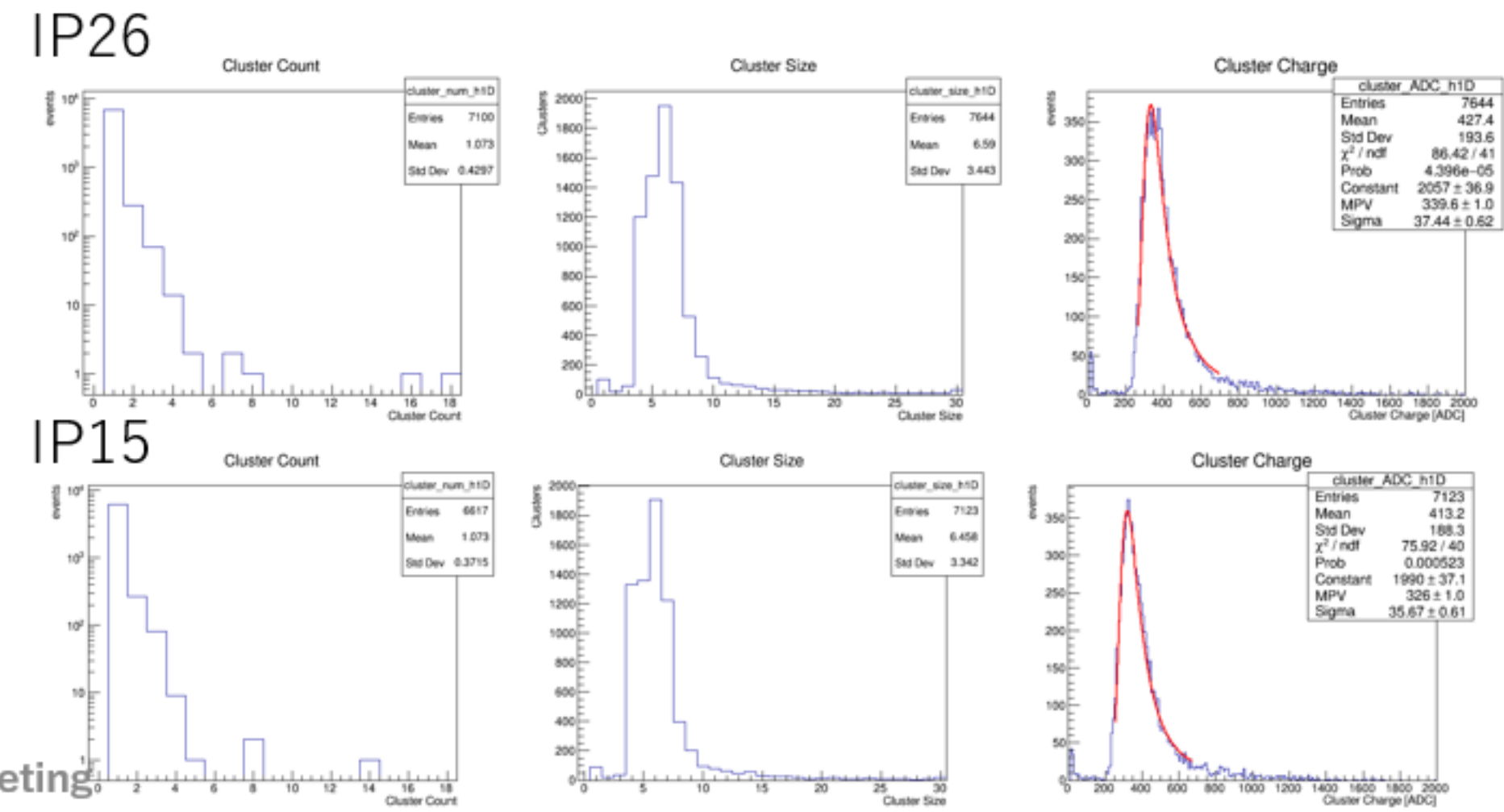
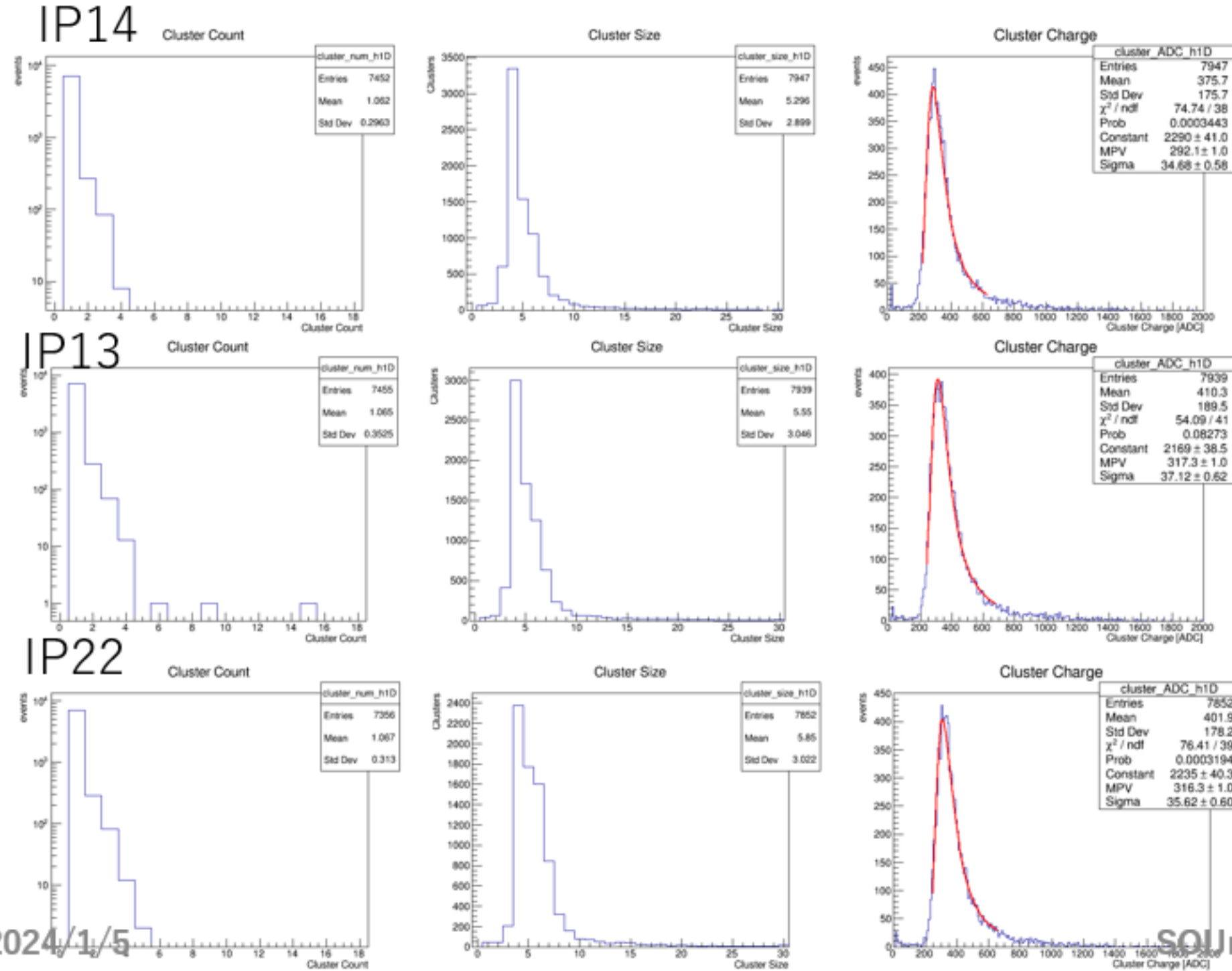
Coordinate



Full Frame ペDESTアル+クラスタリング

特に去年と変わったところはない…
(むしろ, 全層ゲインを調整したため, ばらつきが少ない)

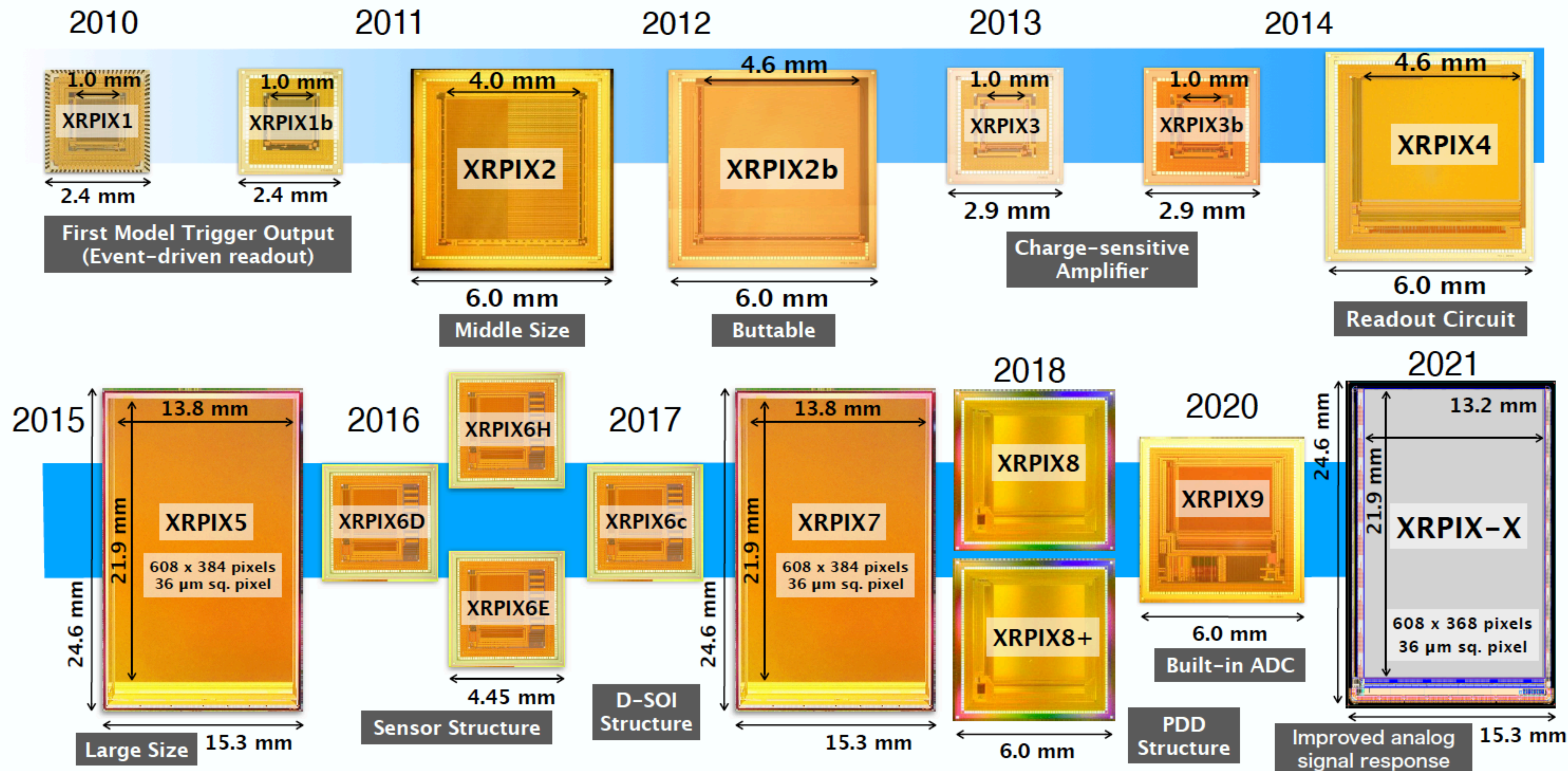
	S [ADC]	N [ADC]	SN
IP14	292.1 ± 1.0	2.06	141.8
IP13	317.3 ± 1.0	2.27	139.8
IP22	316.3 ± 1.0	2.02	156.6
IP26	339.6 ± 1.0	1.81	187.6
IP15	326.0 ± 1.0	1.78	183.1



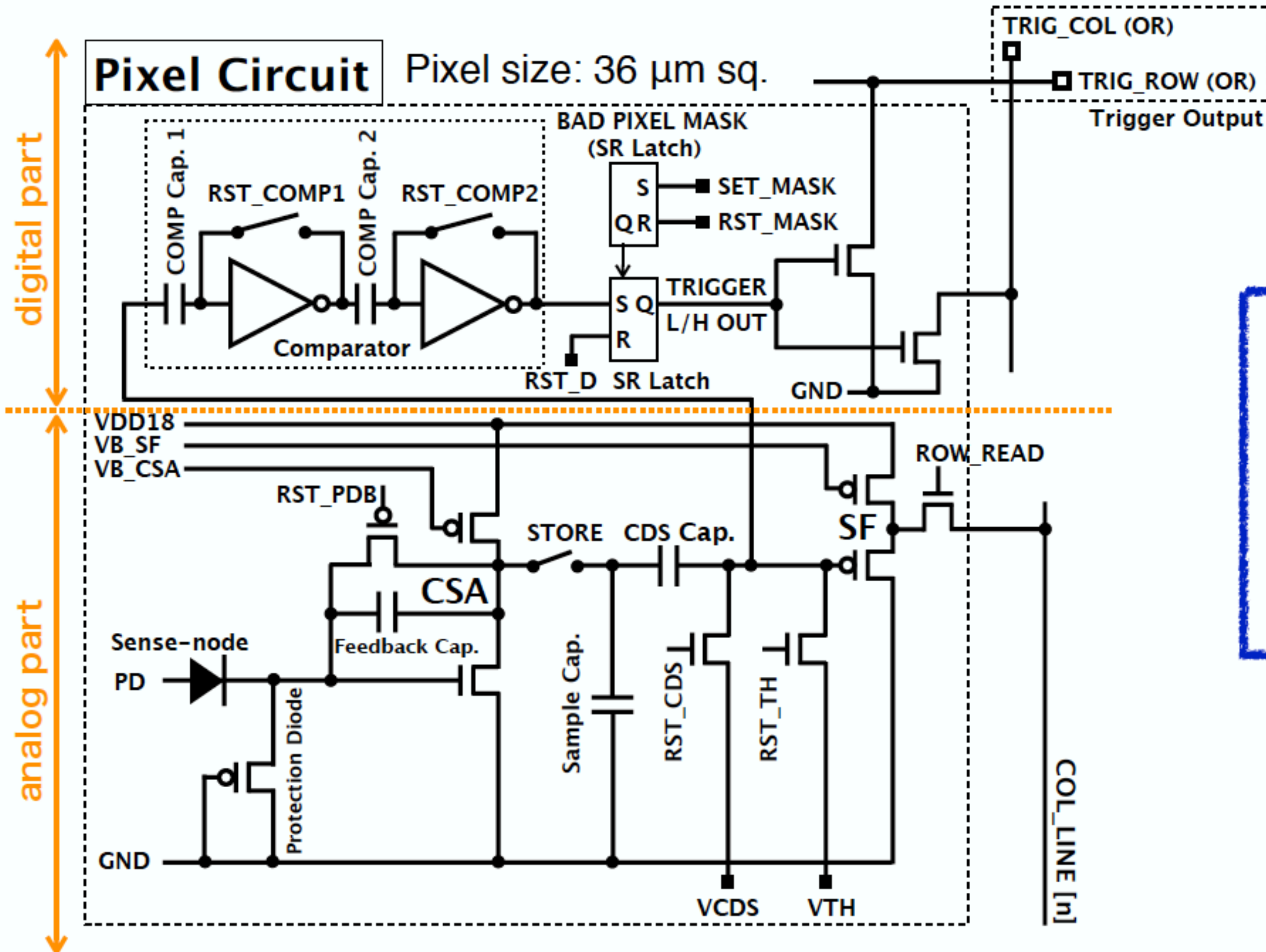
2024/1/5

SQLmeeting

History of XRPIX Series



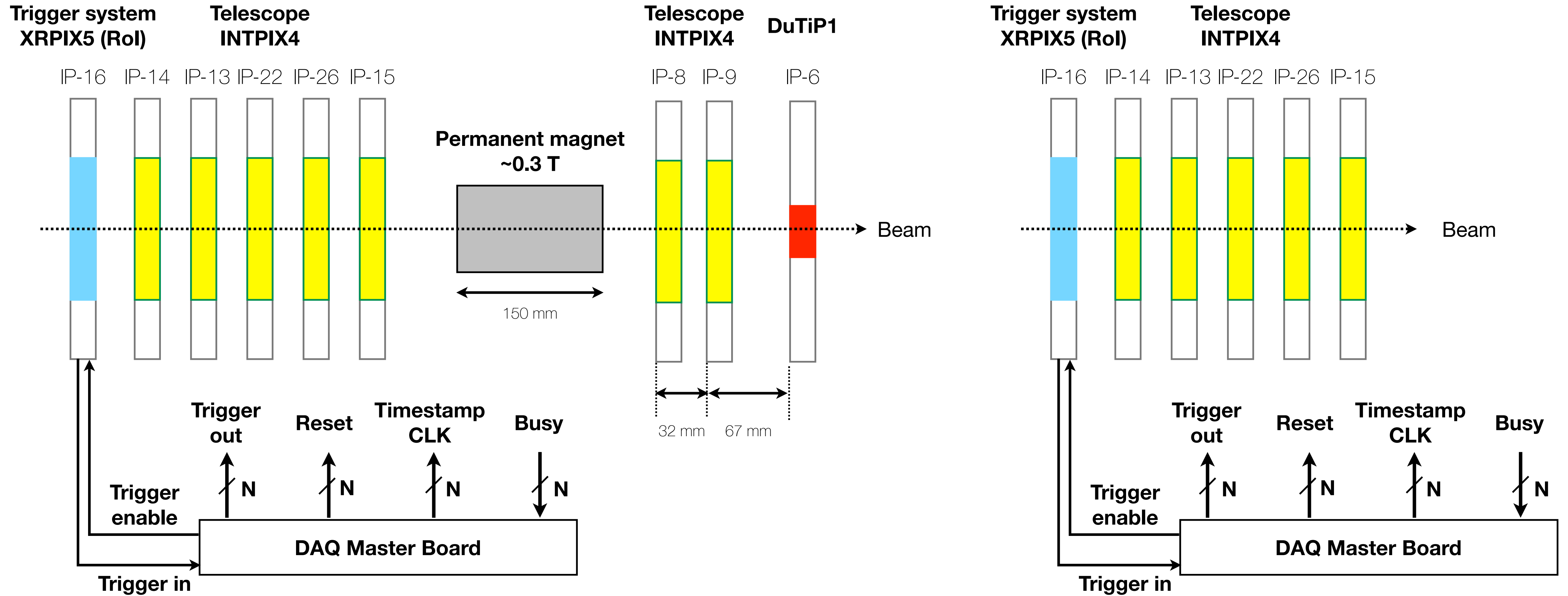
Pixel Circuit



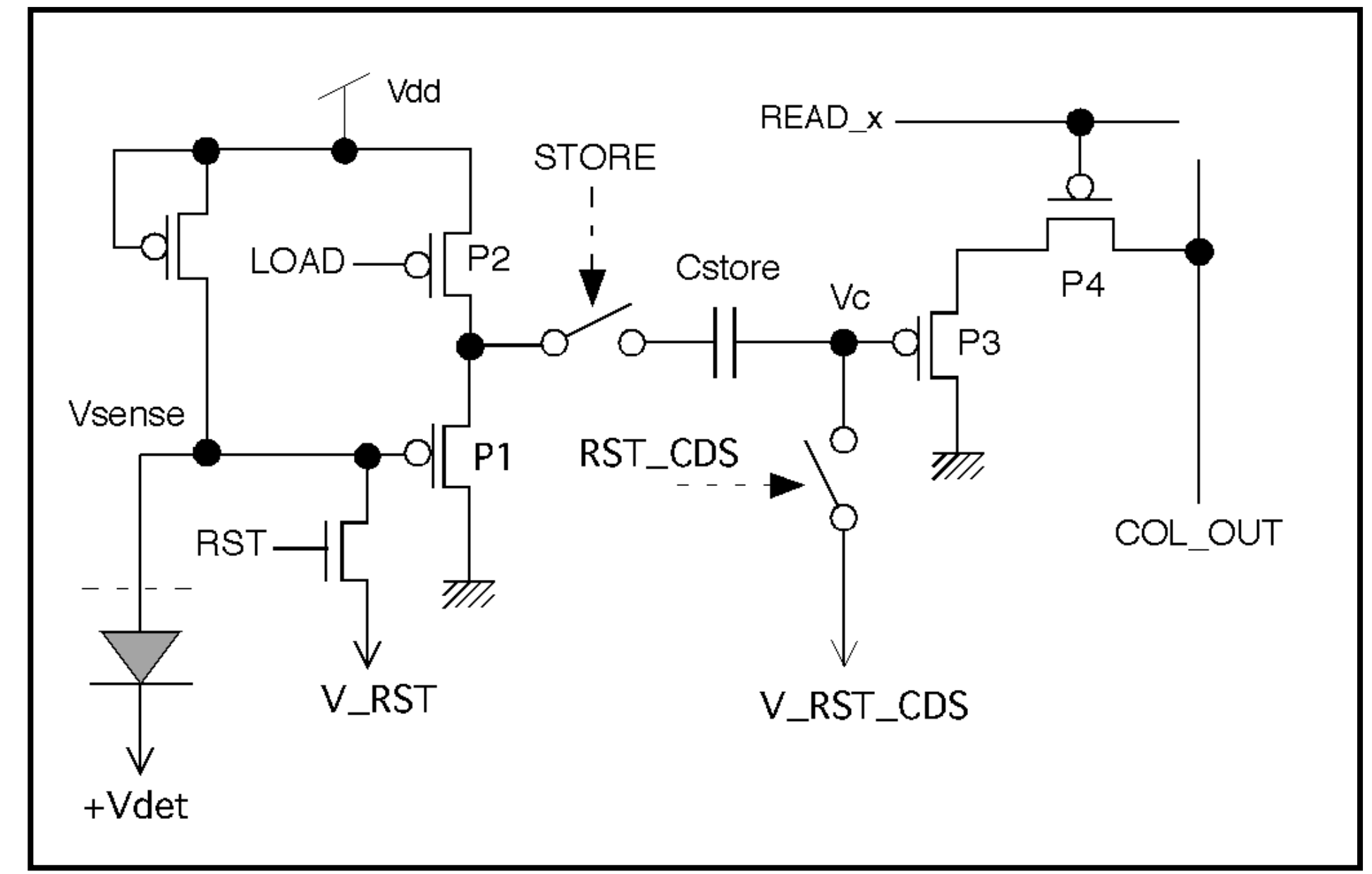
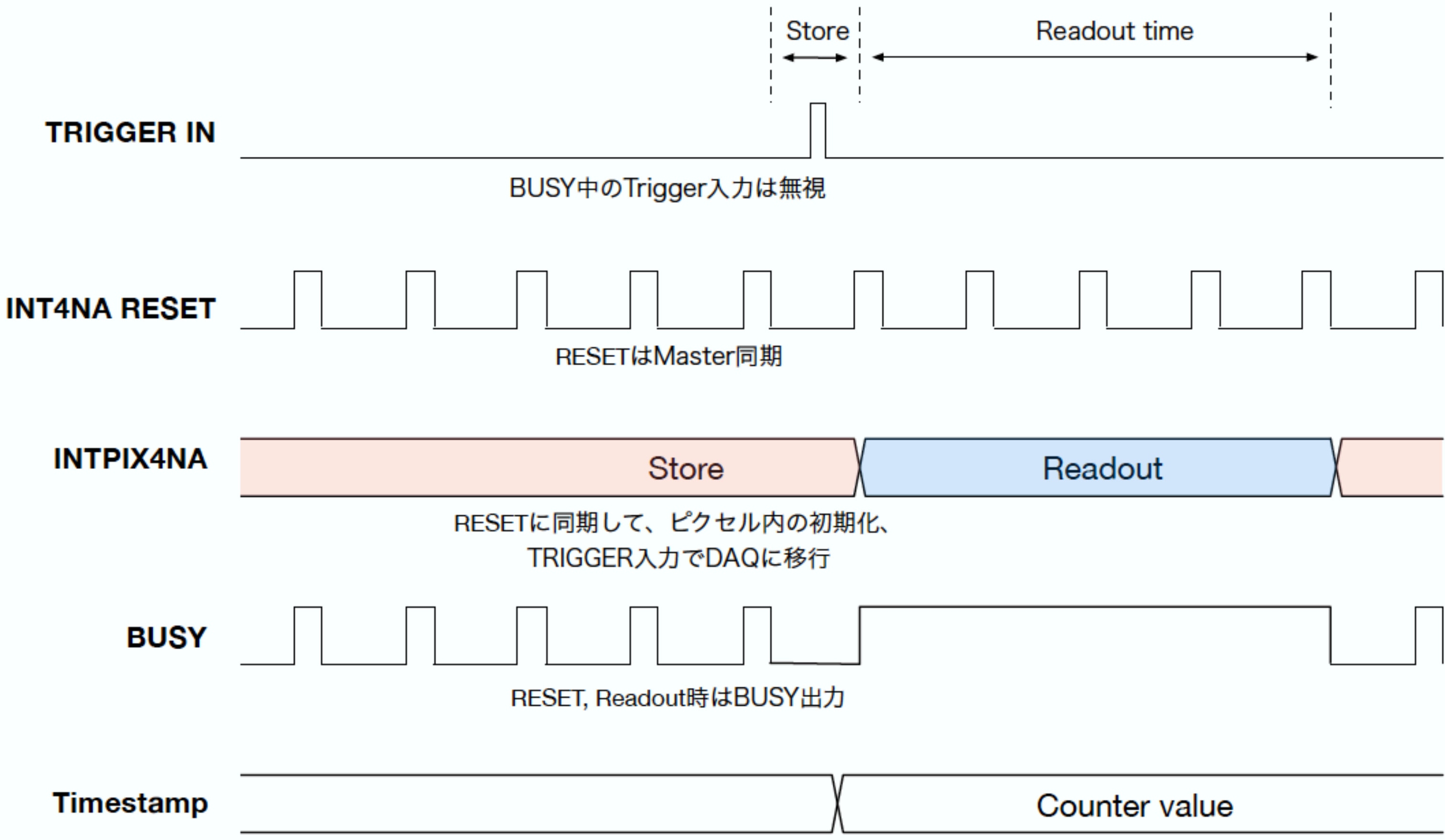
Pixel Circuit consists of ...

- Charge-sensitive amplifier (CSA)
- Correlated Double Sampling
- Inverter-chopper type comparator
- SR Latch for bad pixel mask

Setup at AR-TB in 2023



INTPIX4NA Time Chart and Pixel Circuit



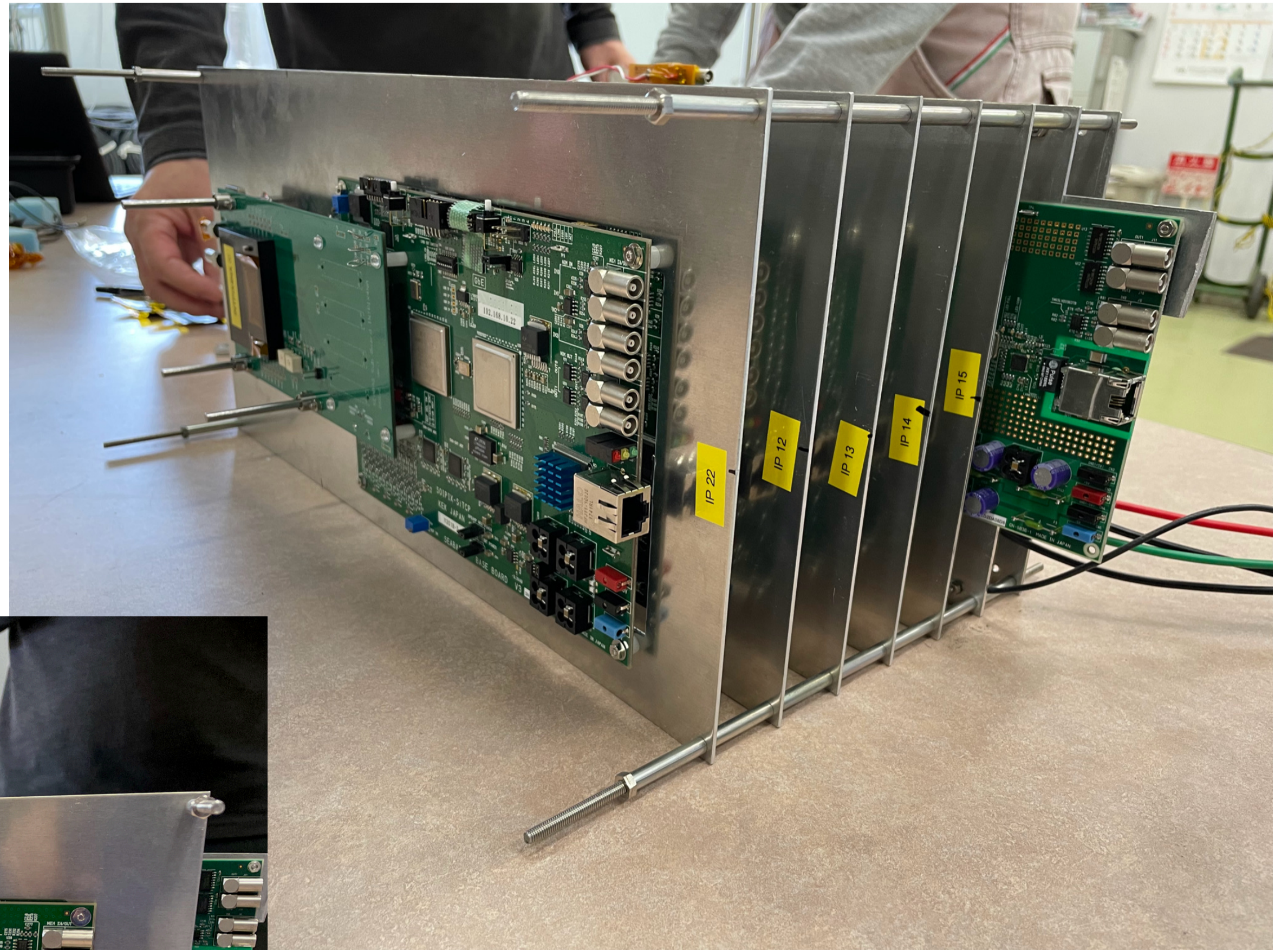
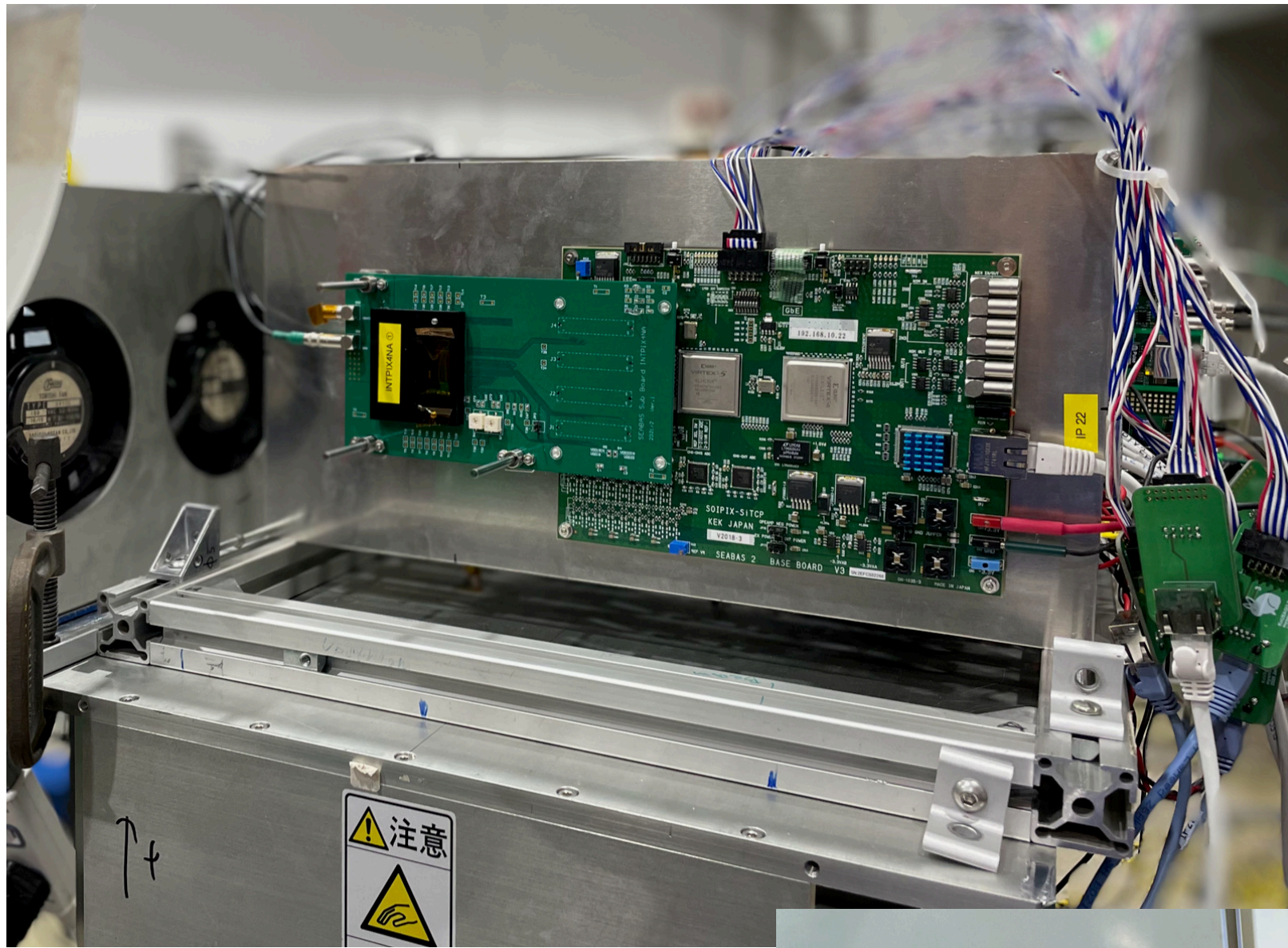
Run 74, $p = 4\text{GeV}/c$

INTPIX4NA Integration Time: 100 μs

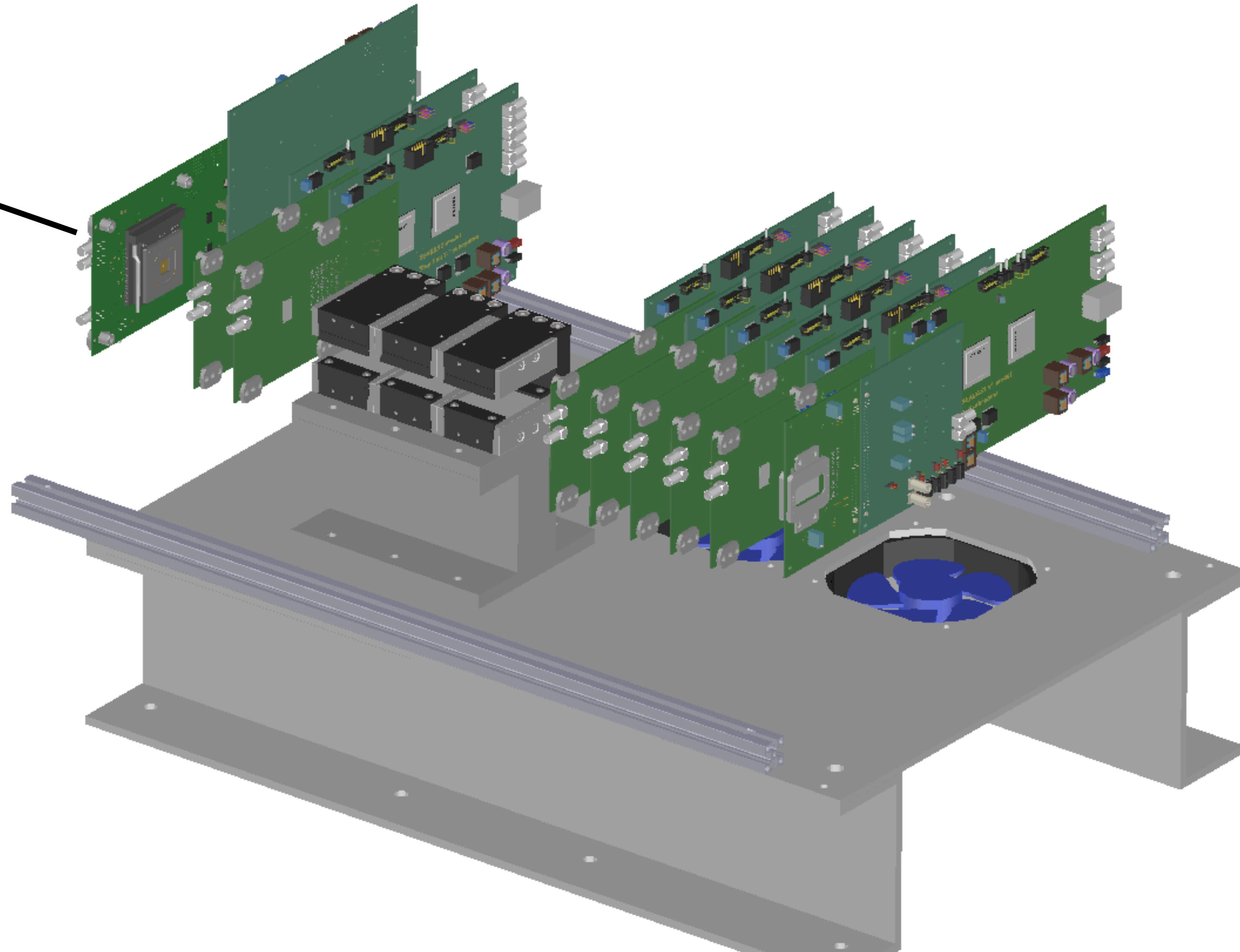
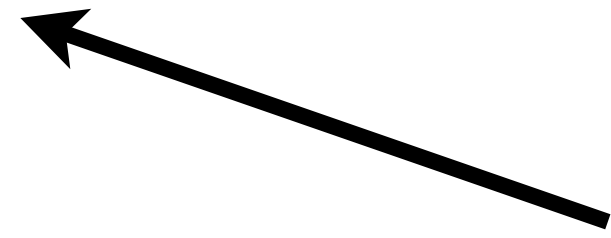
V_RST and V_RST_CDS Width: 150 and 160 ns

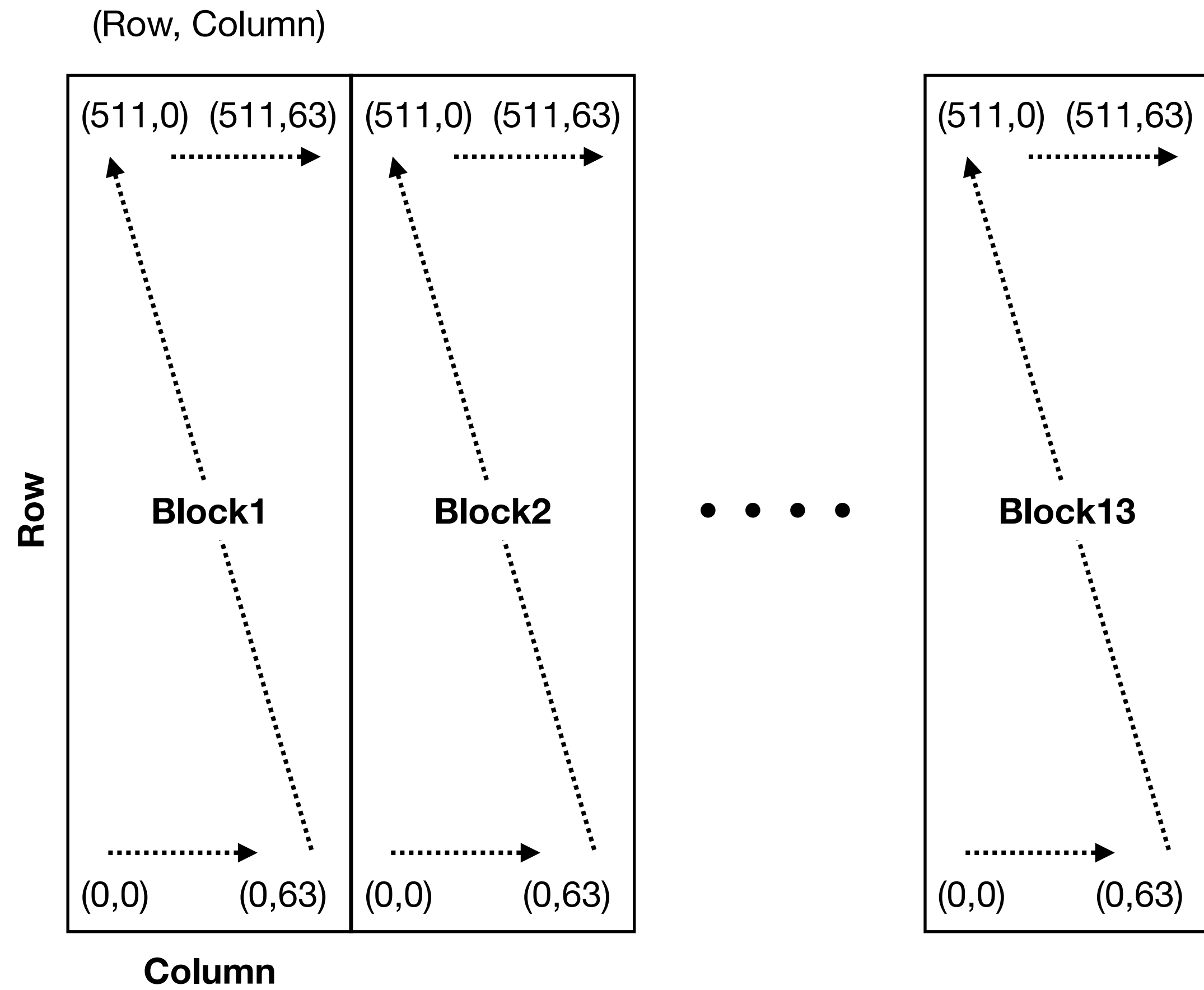
V_RST and V_RST_CDS Period: corresponds to Integration Time

XRPIX5 Trigger Latency: $\sim 2.2 \mu\text{s}$



Beam





Order of Readout

Block** (Row, Column)

Block1 (0, 0)

⋮

Block1 (0, 63)

Block1 (1, 0)

⋮

Block1 (1, 63)

⋮

Block1 (511, 0)

Block1 (511, 63)

Block2 (0, 0)

Data Structure (RAW)



Data in ROOT file

Decode



event_tag

ADC[832*512]

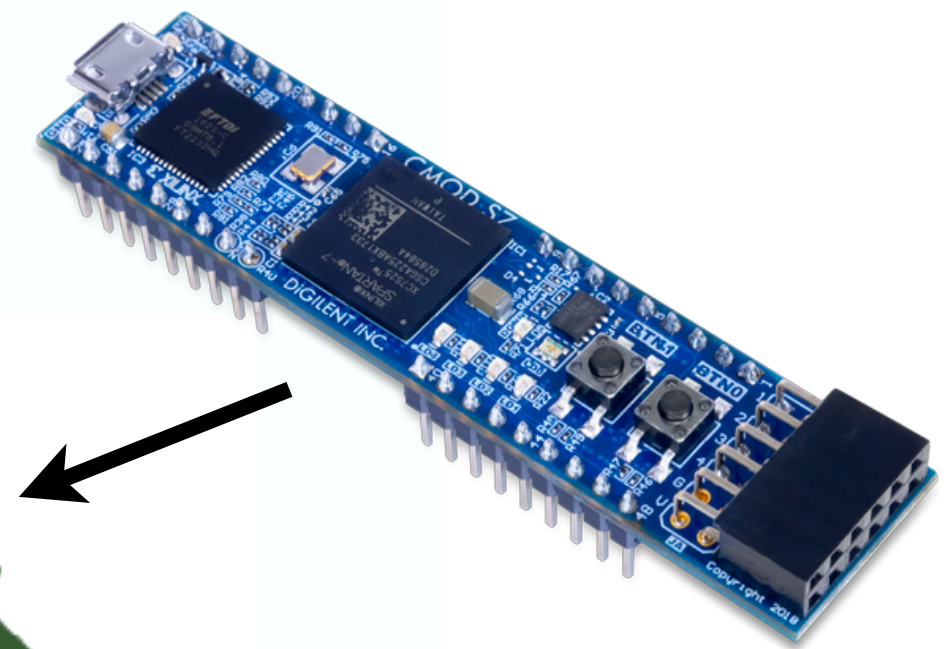
TS: Timestamp, 32-bit, 1kHz Clock
There are no header and footer.

DAQ Master

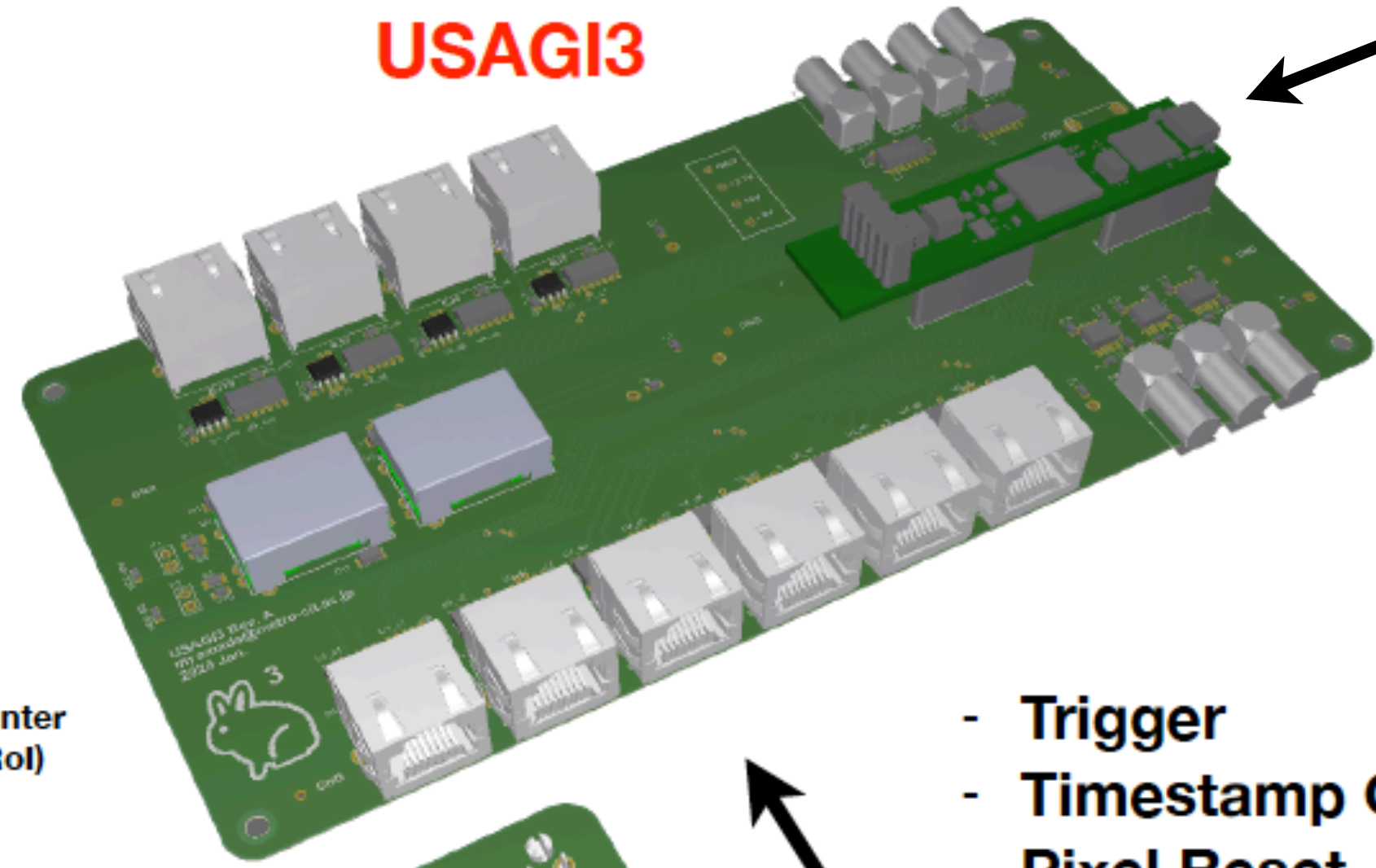
- FPGA Module: SYNC_MASTER for USAGI3
- I/O Board for Slaves: USAGI3

USAGI3 も問題なく動きました。

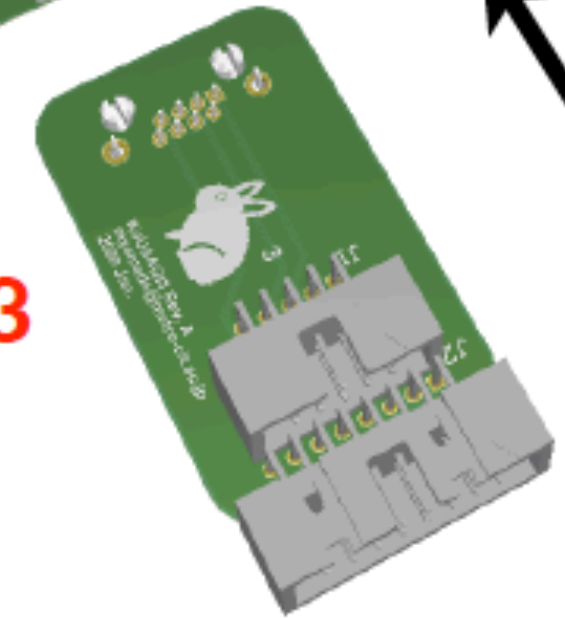
2020 年の FTBF で動かなかったのは
やはり静電気による IC の破損だったか？



Digilent Cmod S7
FPGA: Spartan 7

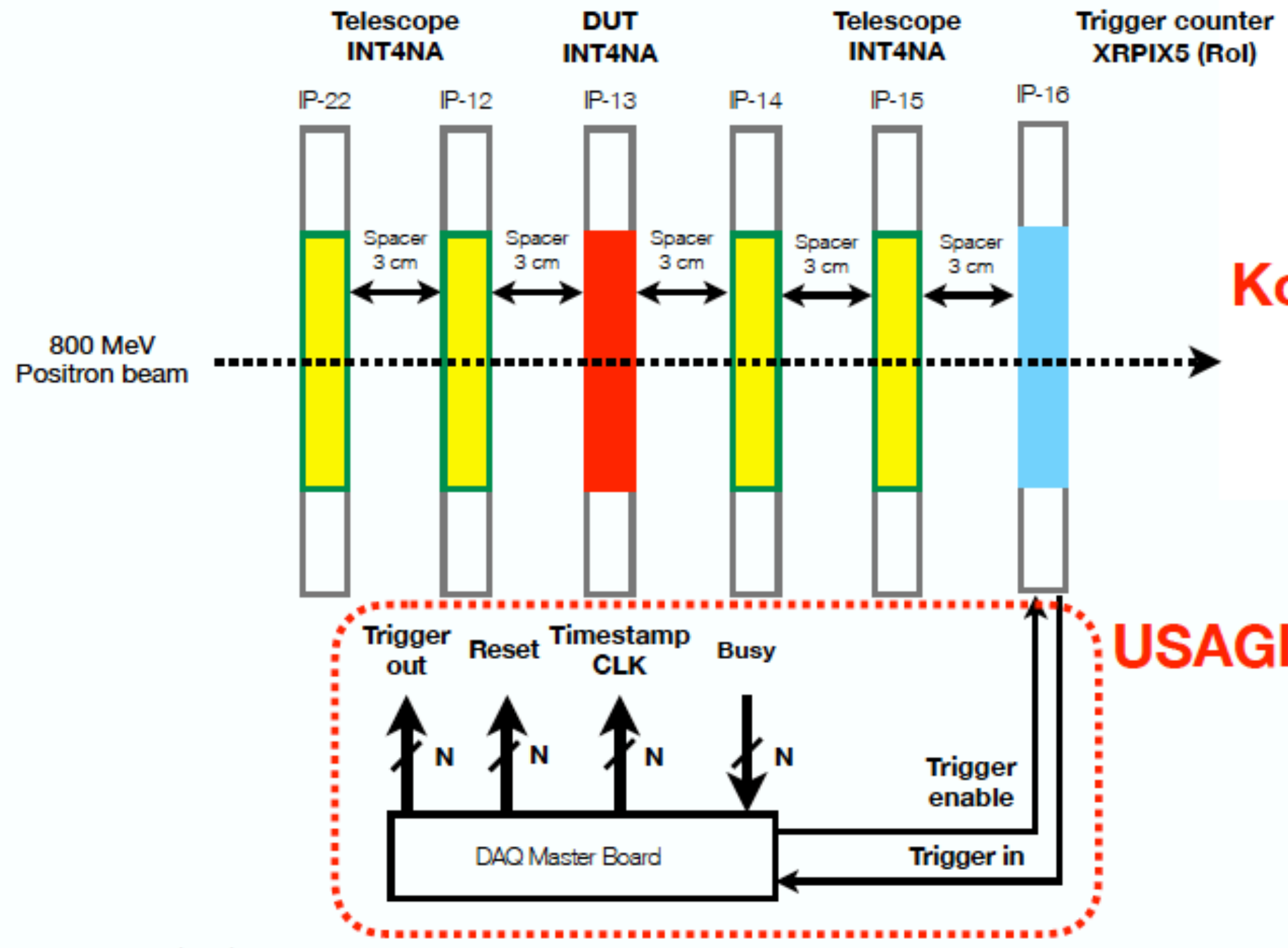


USAGI3

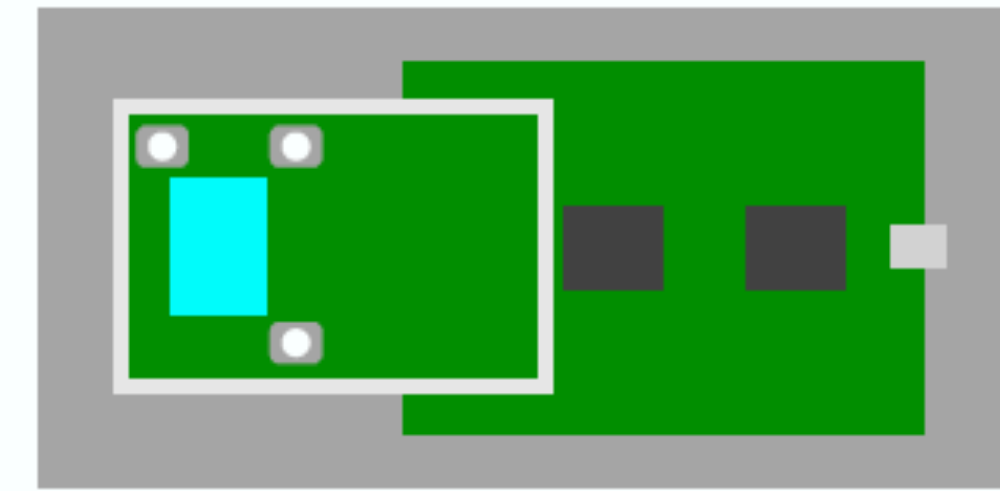


KoUSAGI3

- Trigger
- Timestamp Clock
- Pixel Reset
- Busy

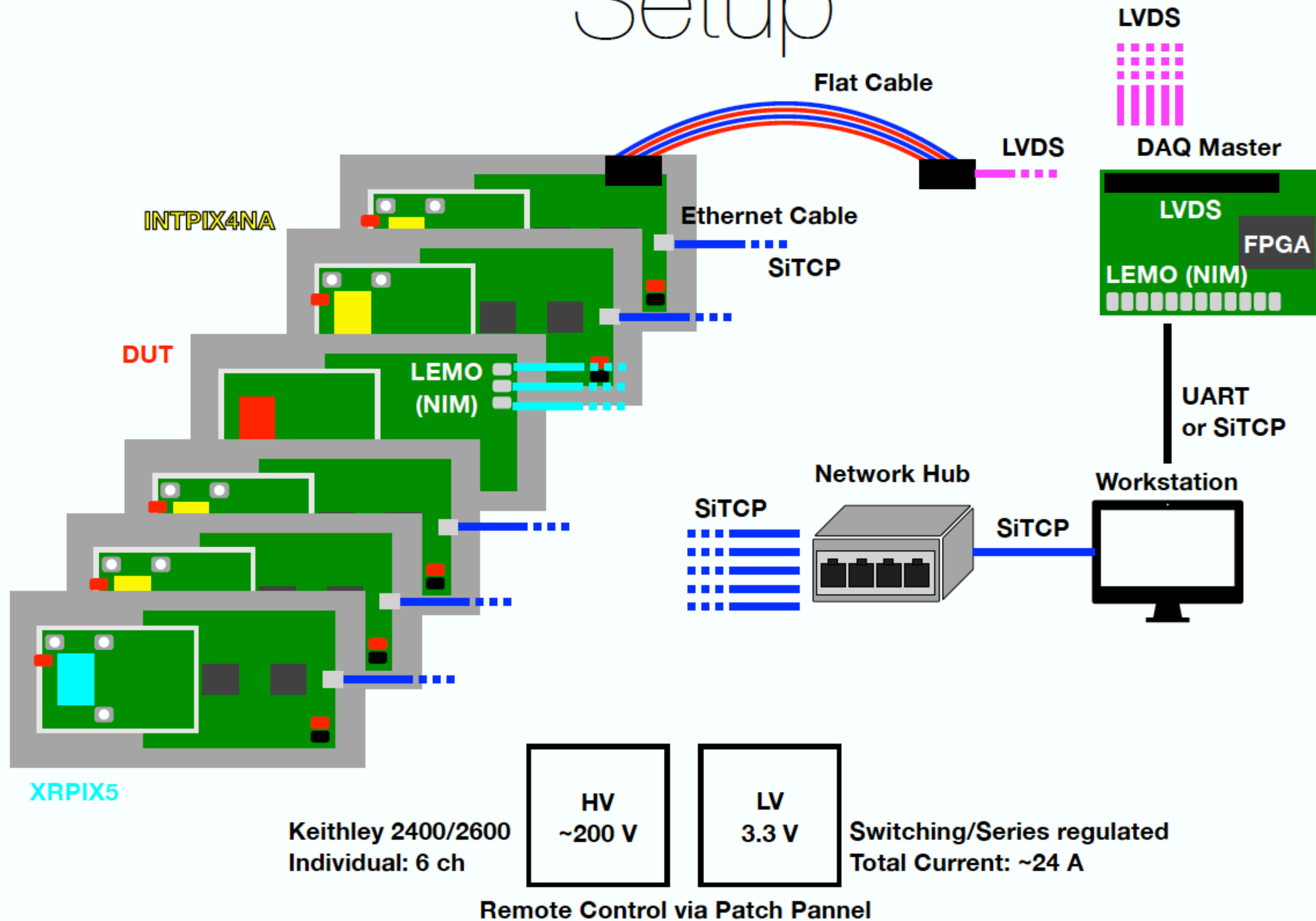


USAGI3

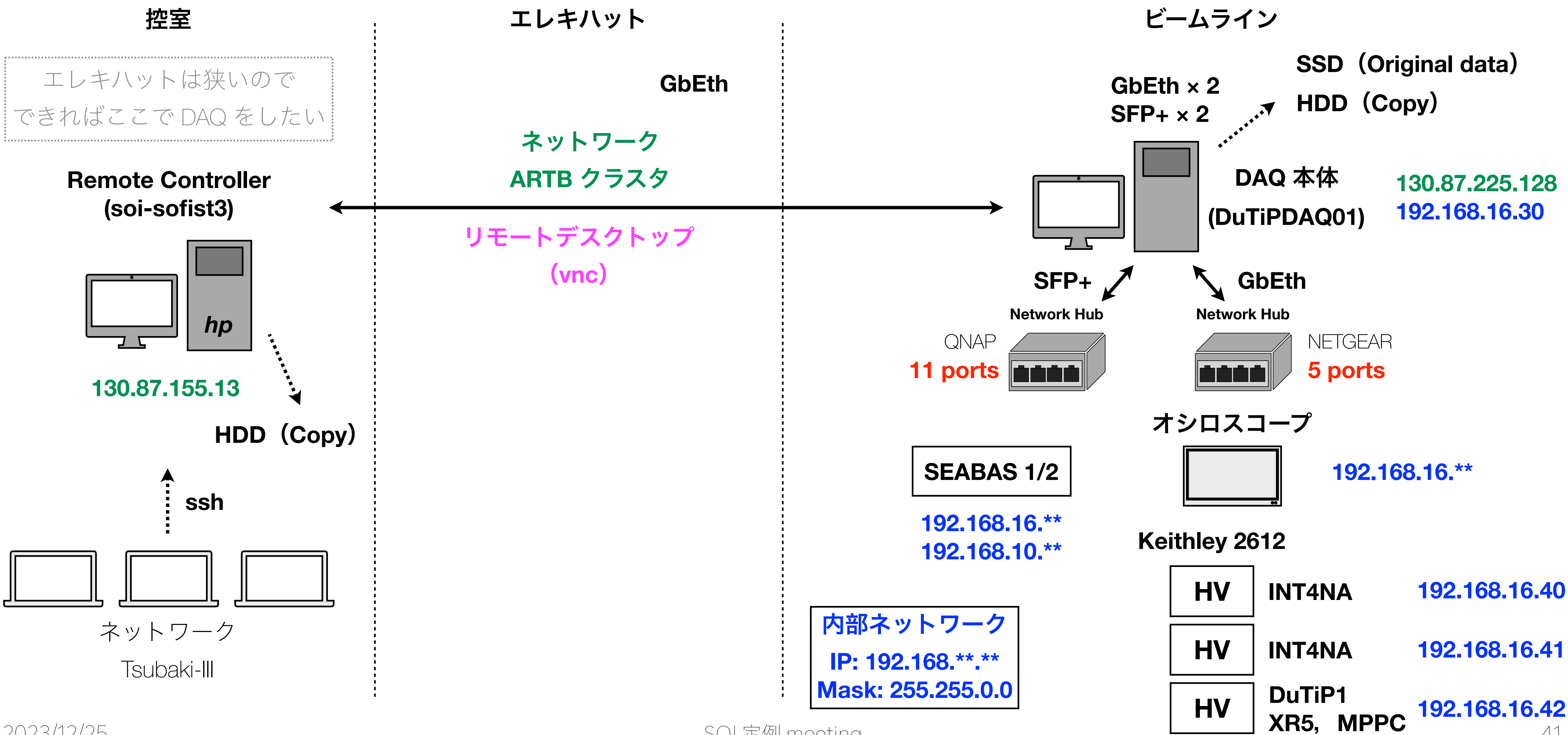


SEABAS2

Setup

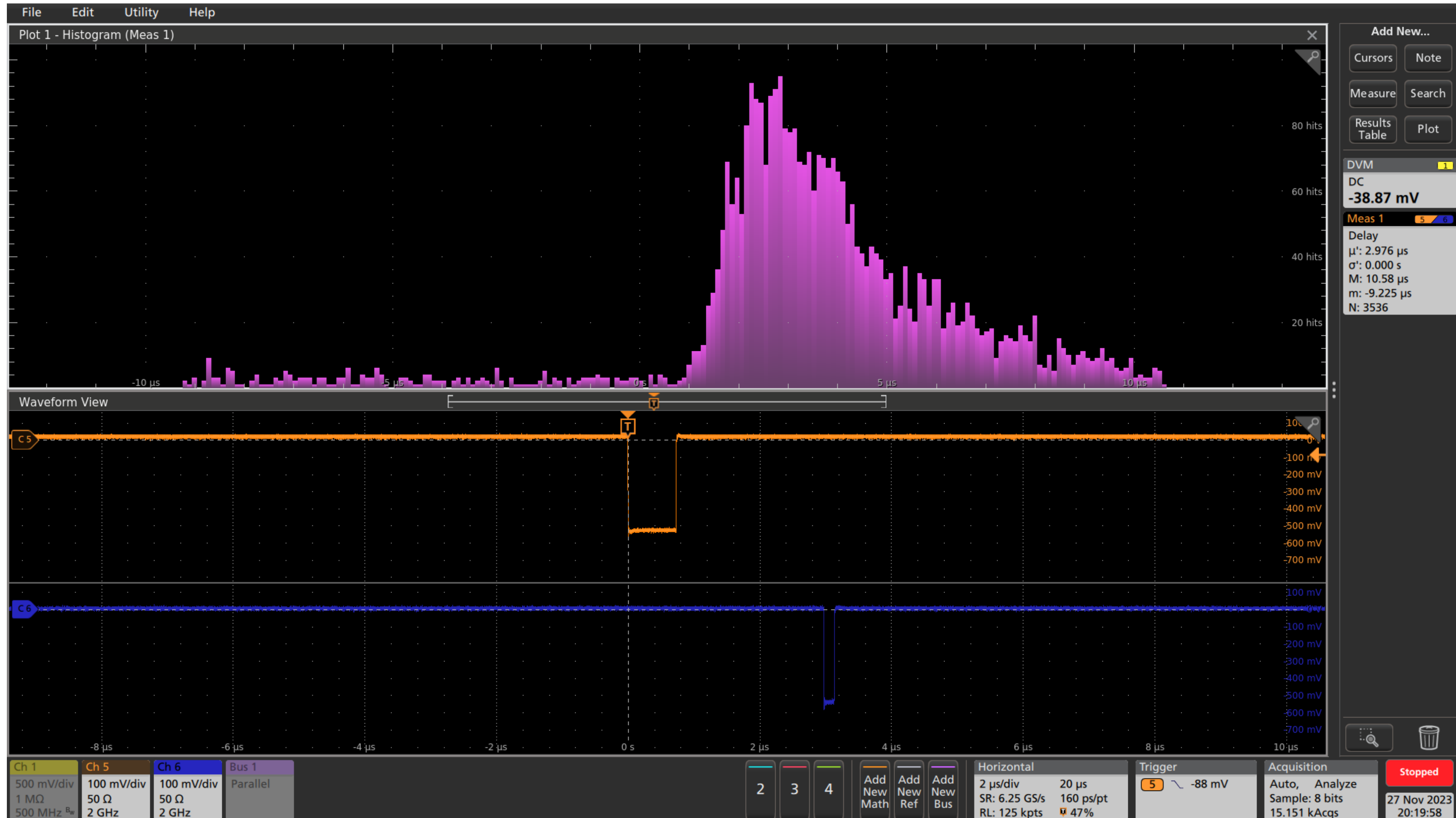


Network



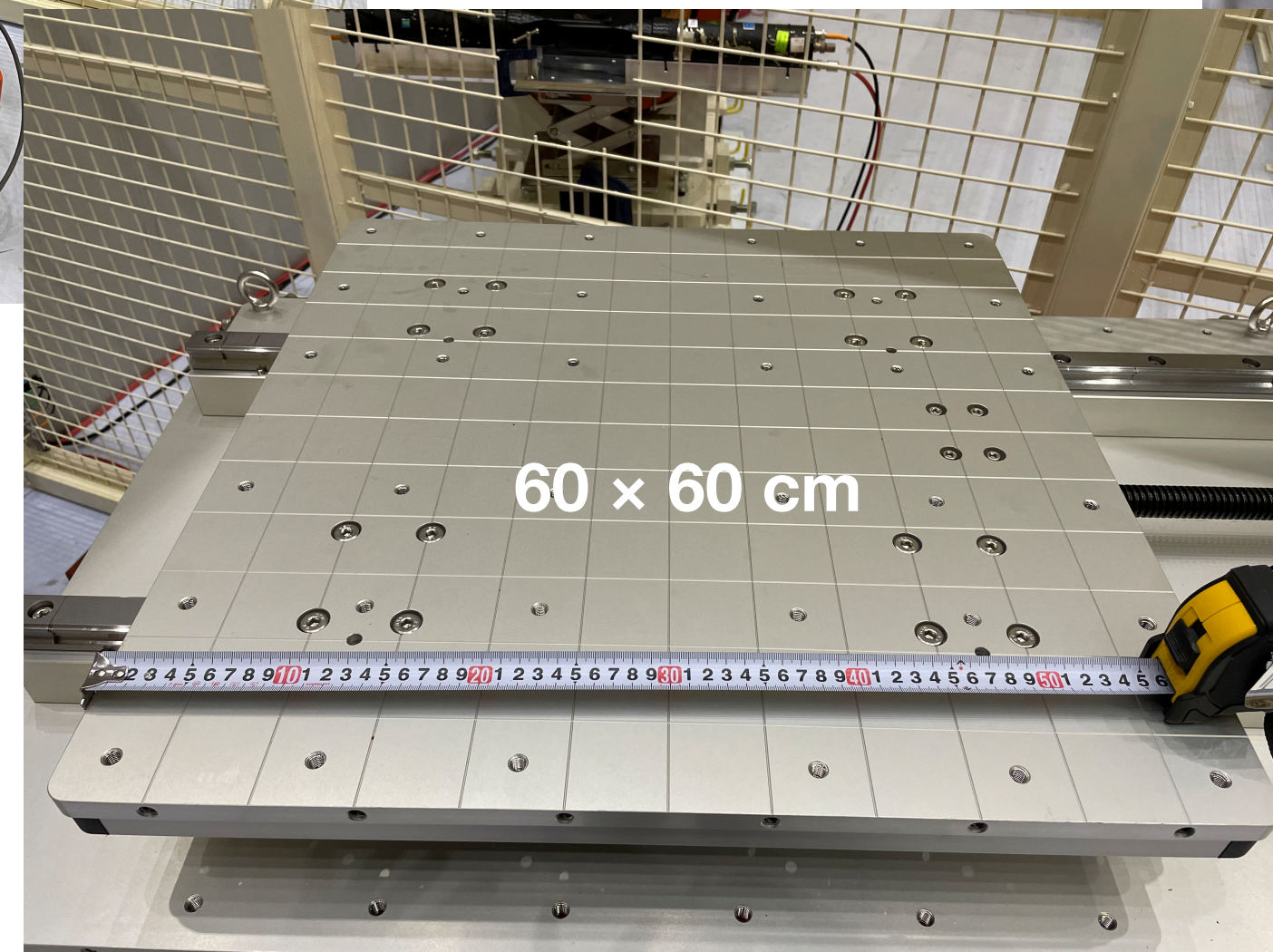
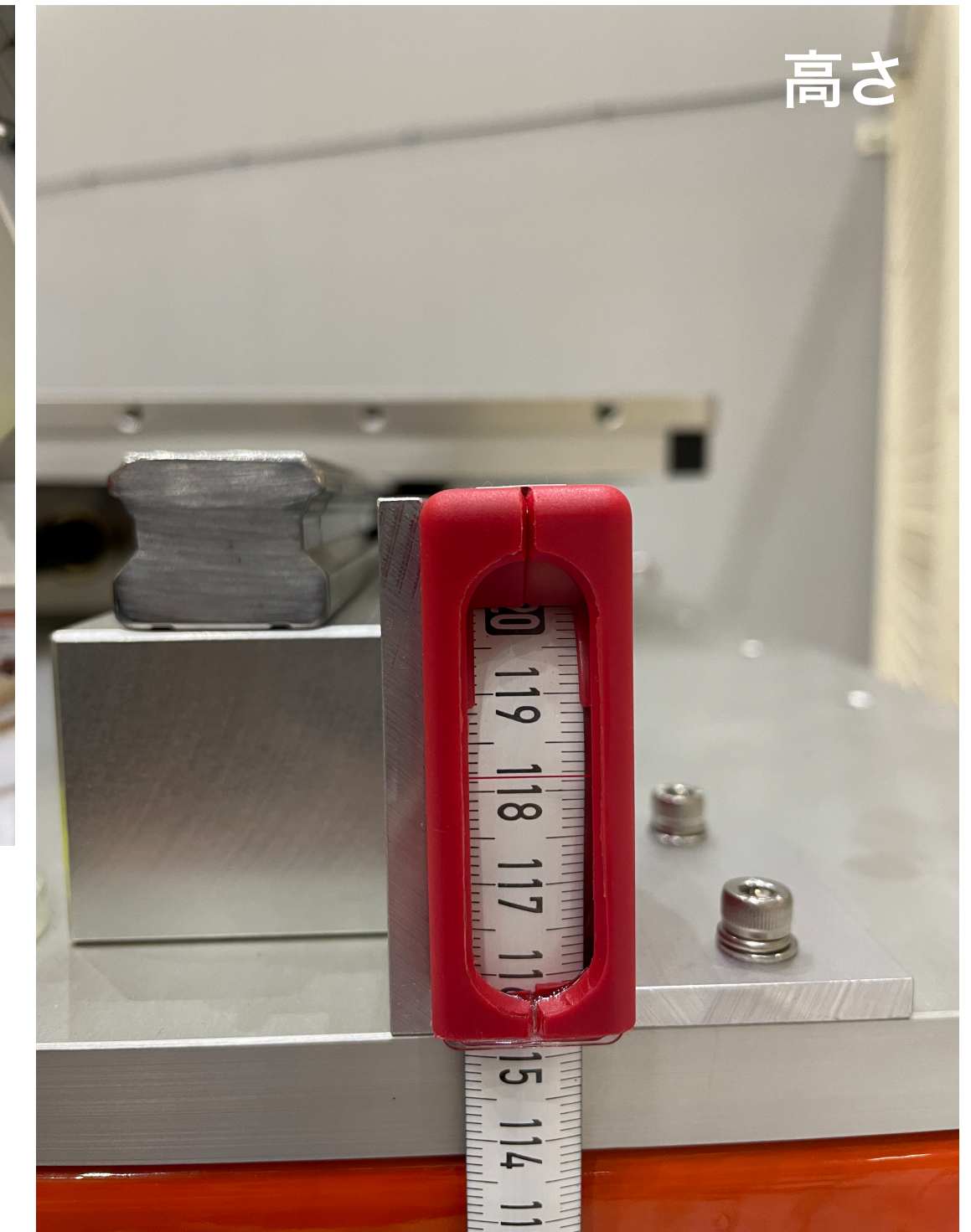
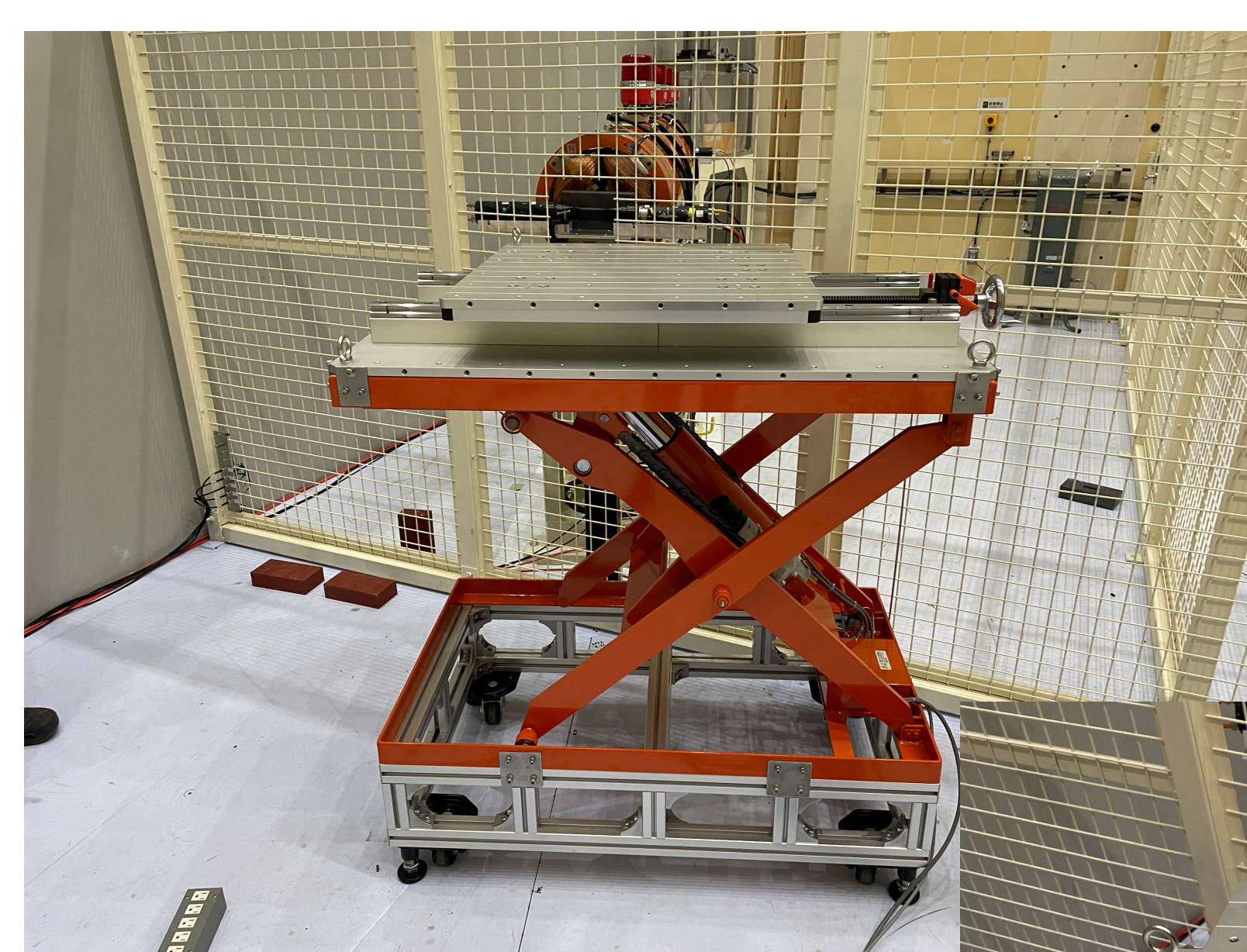
Trigger Latency

XRPIX5 Trigger latency via USAGI3



メカ

ビームライン設置の半電動ステージ。ステージの大きさは 60 × 60 cm で 10 cm ごとに固定用のネジ穴がある。垂直方向が電動の足踏みペダル式。メジャーの最小目盛 1 mm を目視で確認。水平方向は手動。ハンドルを回し、メーターで 0.1 mm 単位で確認可能。



Collaboration Members



IN2P3/IPHC, France

Jerome Baudot

Mathieu Goffe

Yitong Liu

Ziad El Bitar

Christian Finck



TMCIT, Japan

Miho Yamada

IPNS/KEK

Akimasa Ishikawa

Tristan Fillinger

Toru Tsuboyama

Takehiko Takayanagi

Univ. Tsukuba

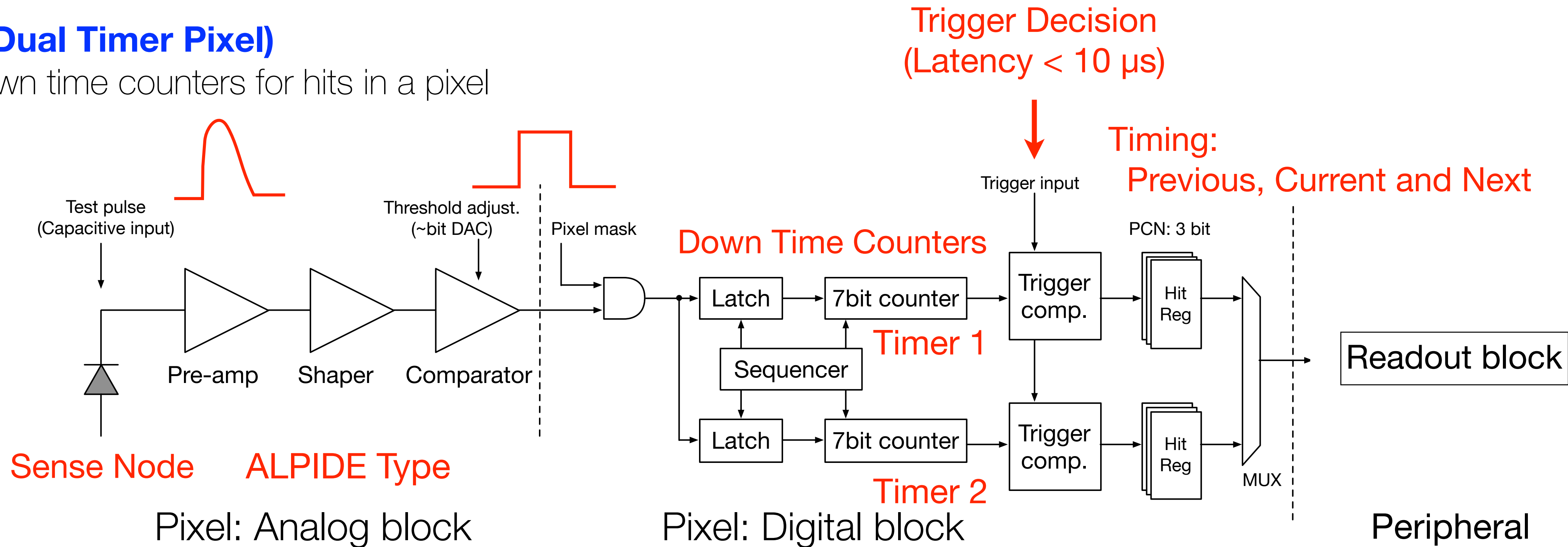
Takumi Omori

Previous Project: D_RD_16, PIs: M. Winter and Y. Arai

DuTiP, SOI Pixel Sensor

DuTiP (Dual Timer Pixel)

Two down time counters for hits in a pixel



Analog block: Usual configuration for the binary detector

Hit memory: Timing of Previous, Current and Next collision

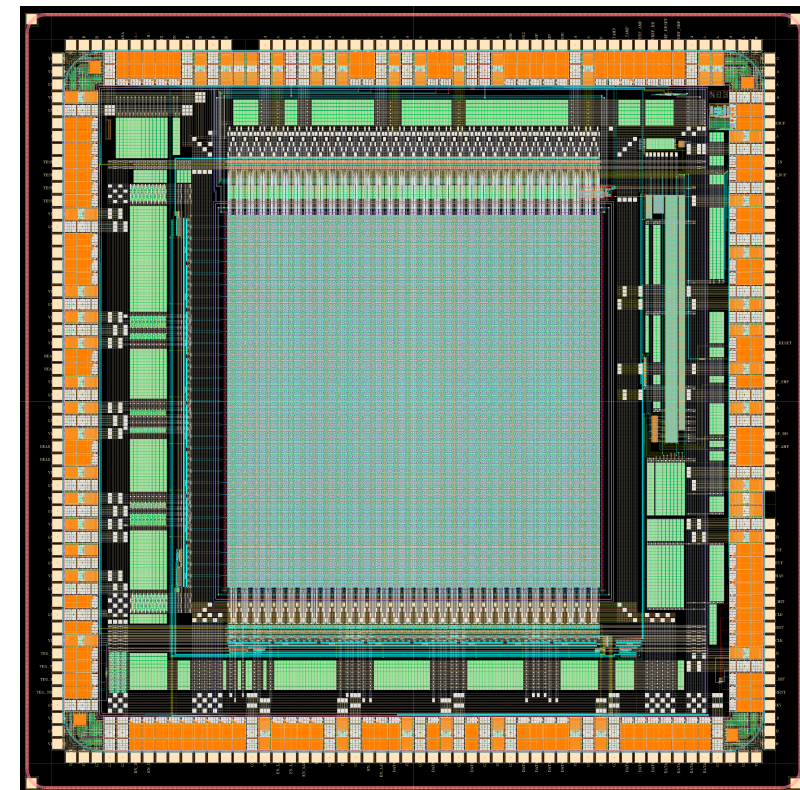
Signal: Coincided with event trigger ← Down time counter corresponds to trigger latency

Background: Random, out of time window ← Suppressed by coincidence

Multiple hits in trigger latency: Multiple timer and memory are controlled by Sequencer

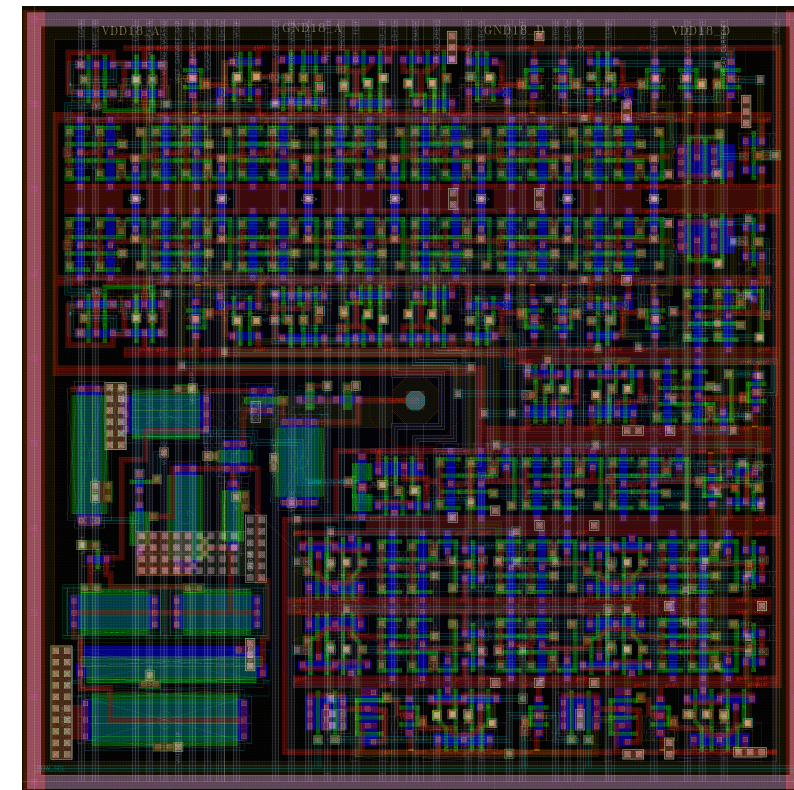
DuTiP 1 - 3

DuTiP1 (2020—)



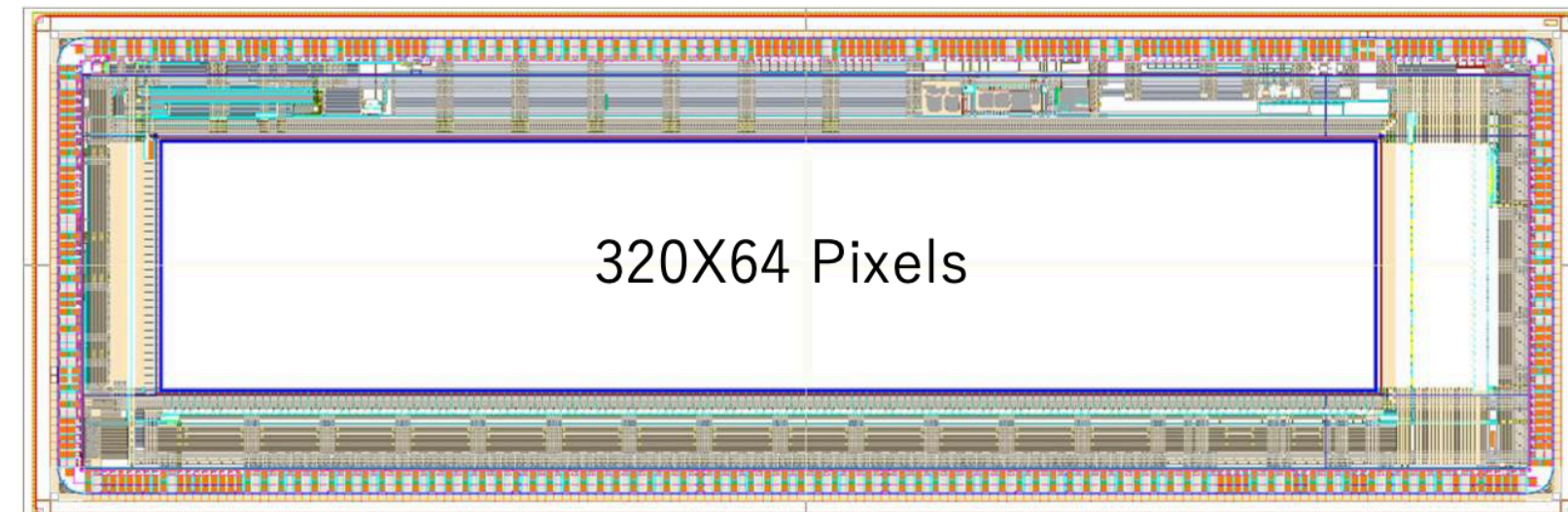
6 × 6 mm²

DuTiP1 Pixel



45 × 45 μm²

DuTiP2 (2021—)



18.4 × 6 mm²

DuTiP3 (2023—)

Pixel

- Pre. amplifier (ALPIDE type)
- Shaper
- Comparator
- Dual down time counters (7 bit)
- Timing memory (Previous/Current)

Readout

- Row address (5 bit)
- Column address (5 bit)
- 2 bit hit (Previous/Current)
- CMOS in/out

⁹⁰Sr β-ray test: Obtained hit signal

Design

- Dec. 2021 submitted → deliver in Spring 2022
- Pixel design is almost completed by DuTiP1
- Row 320 pixels (Full size for Belle II) for design of large-area sensor
- FIFO, LVDS in/out, DAC

Design

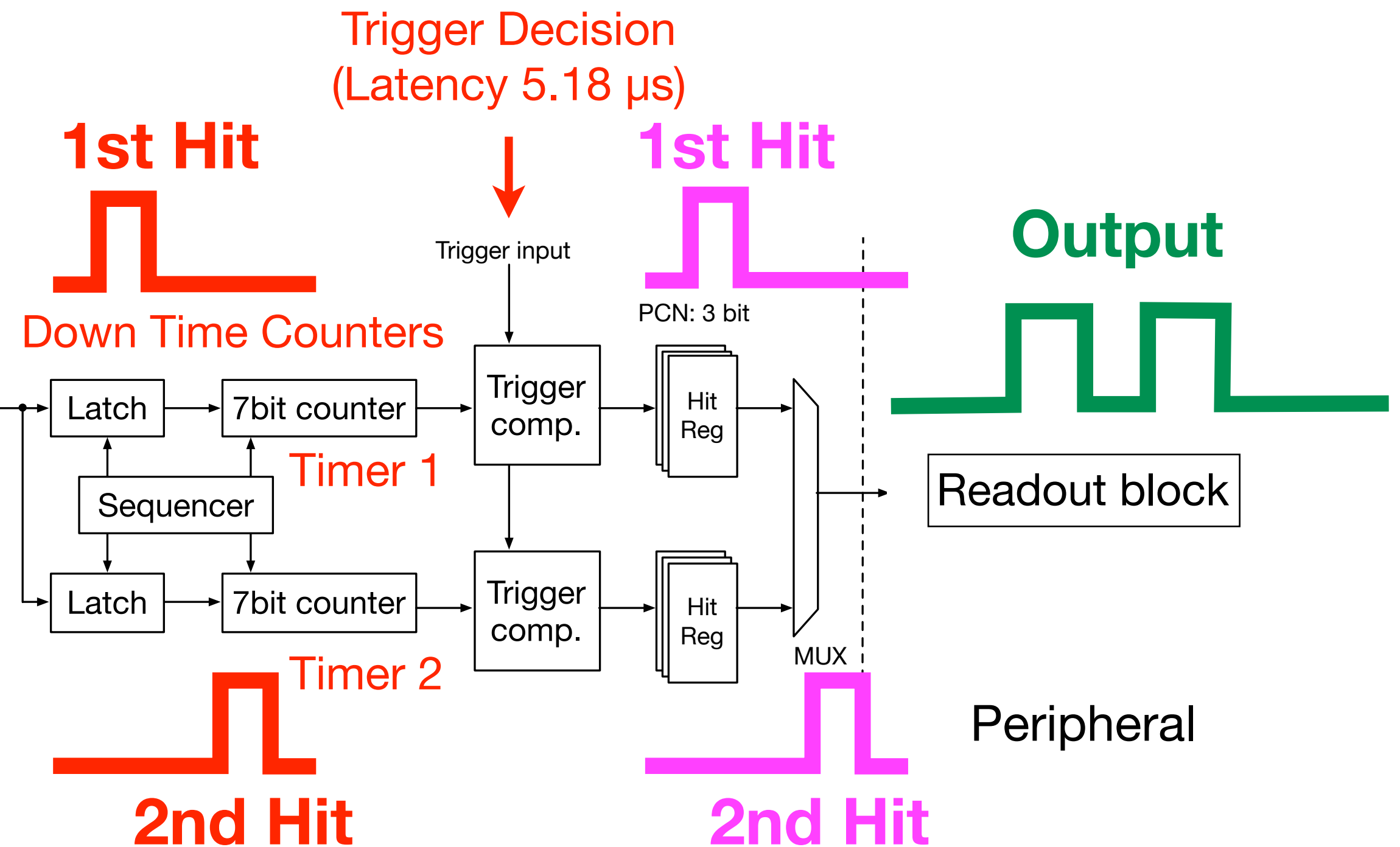
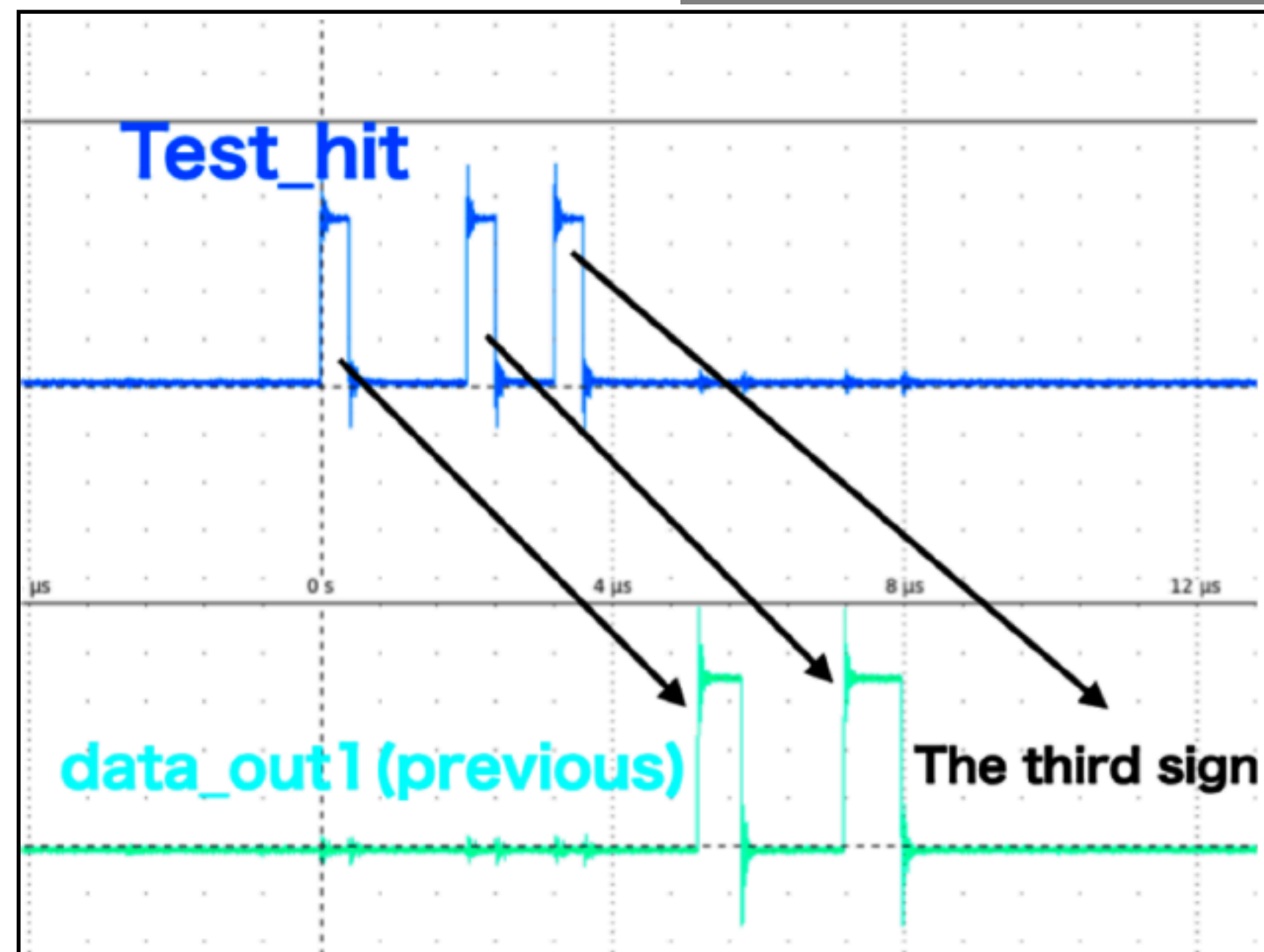
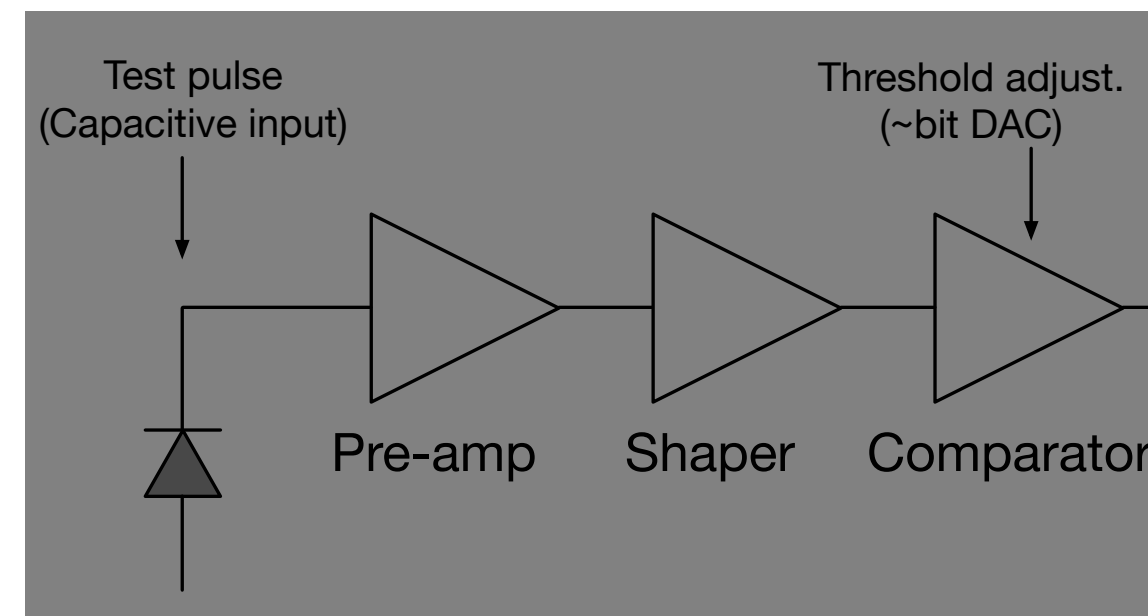
- June 2023 submitted

DuTiP, SOI Pixel Sensor

Confirmation of the Double-Timer Function

Double-pulse wave was input to simulate the hit in a pixel.

Test Pulse



Test Result

- The dual counter operation was confirmed.
- Two pulses were separated by the sequencer.
- The third hit was properly ignored by the sequencer and did not appear in the output.

Position Resolution

Estimation of tracking precision in GeV range

Data

ELPH: 200, 300, 500 and 822 MeV/c, Positron Beam
 Fermilab: 120 GeV, Proton Beam

G4 Simulation

200 MeV/c - 5 GeV/c, Electron Beam

Tracking method: ②

Improvement with thinner sensors

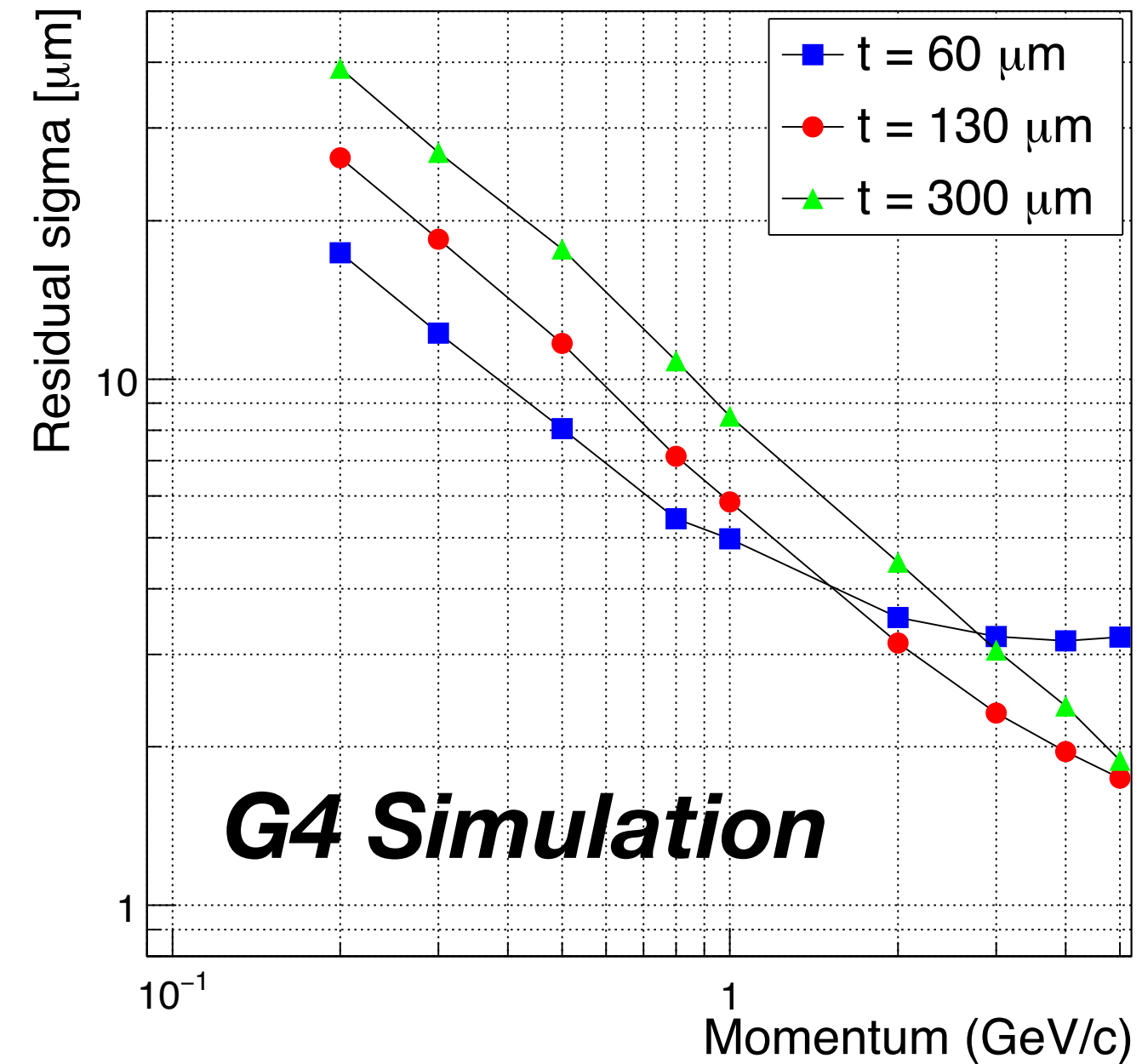
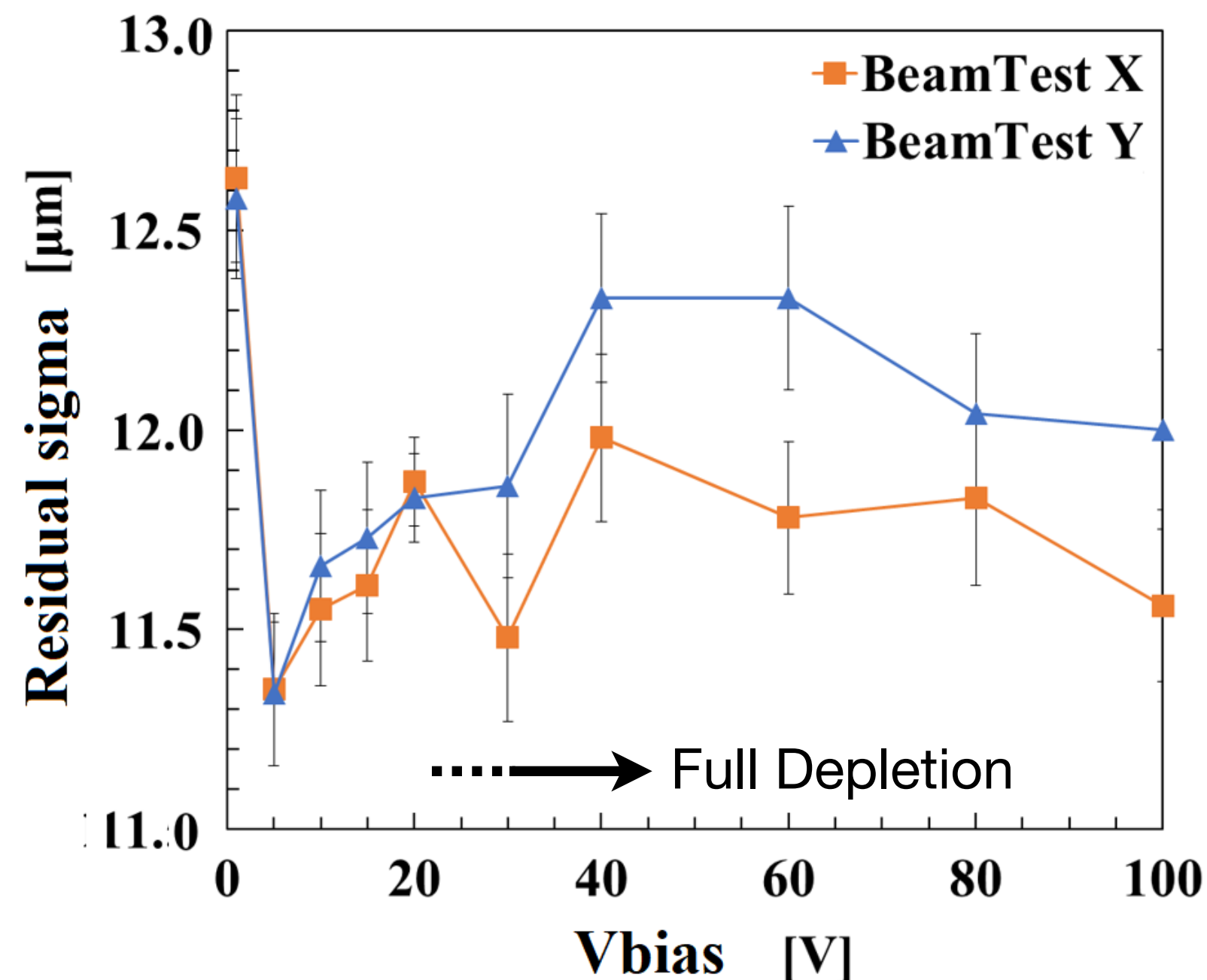
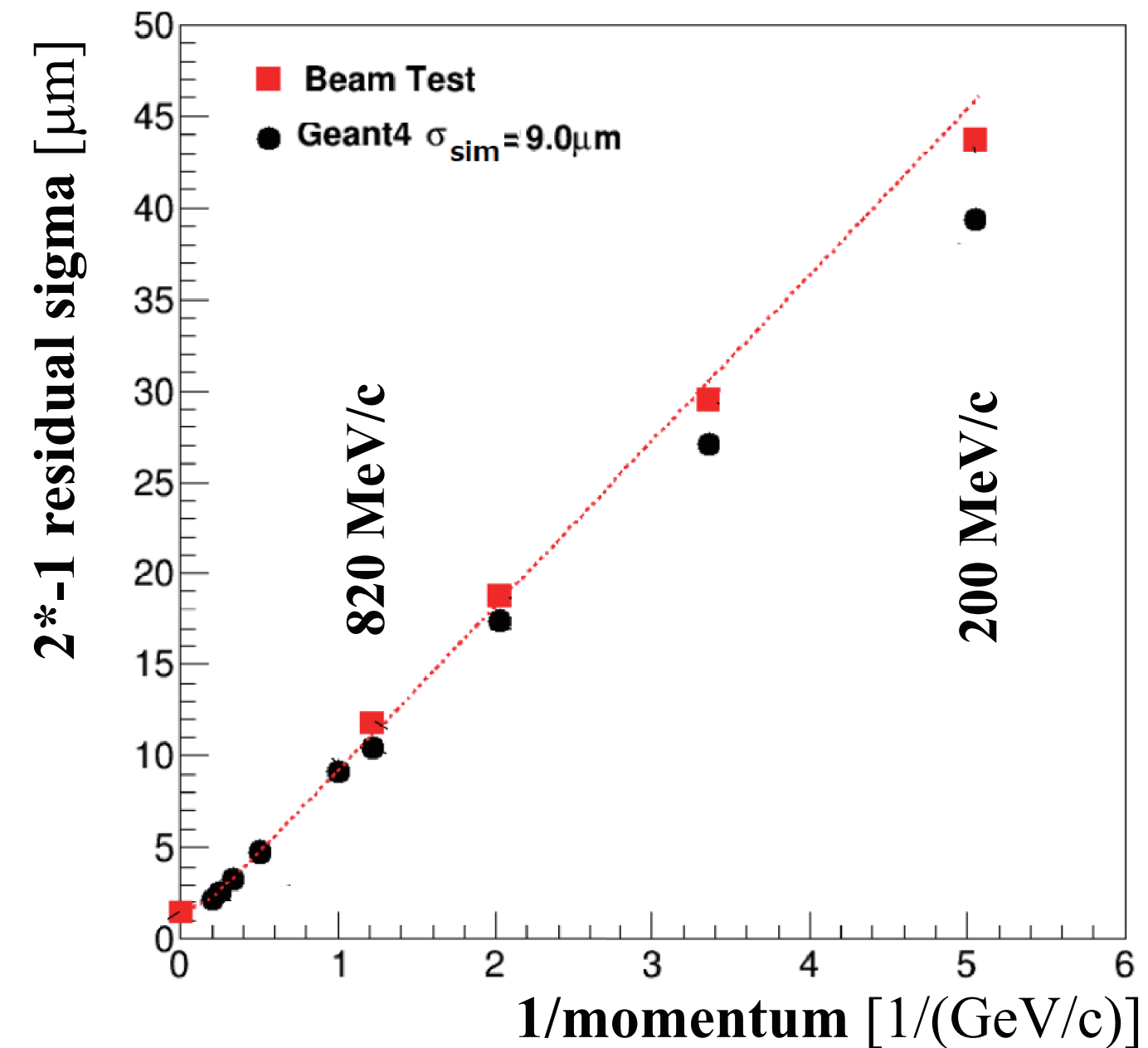
Tracking performance improvement at low-energy electrons.

Sensor thickness for G4 simulation

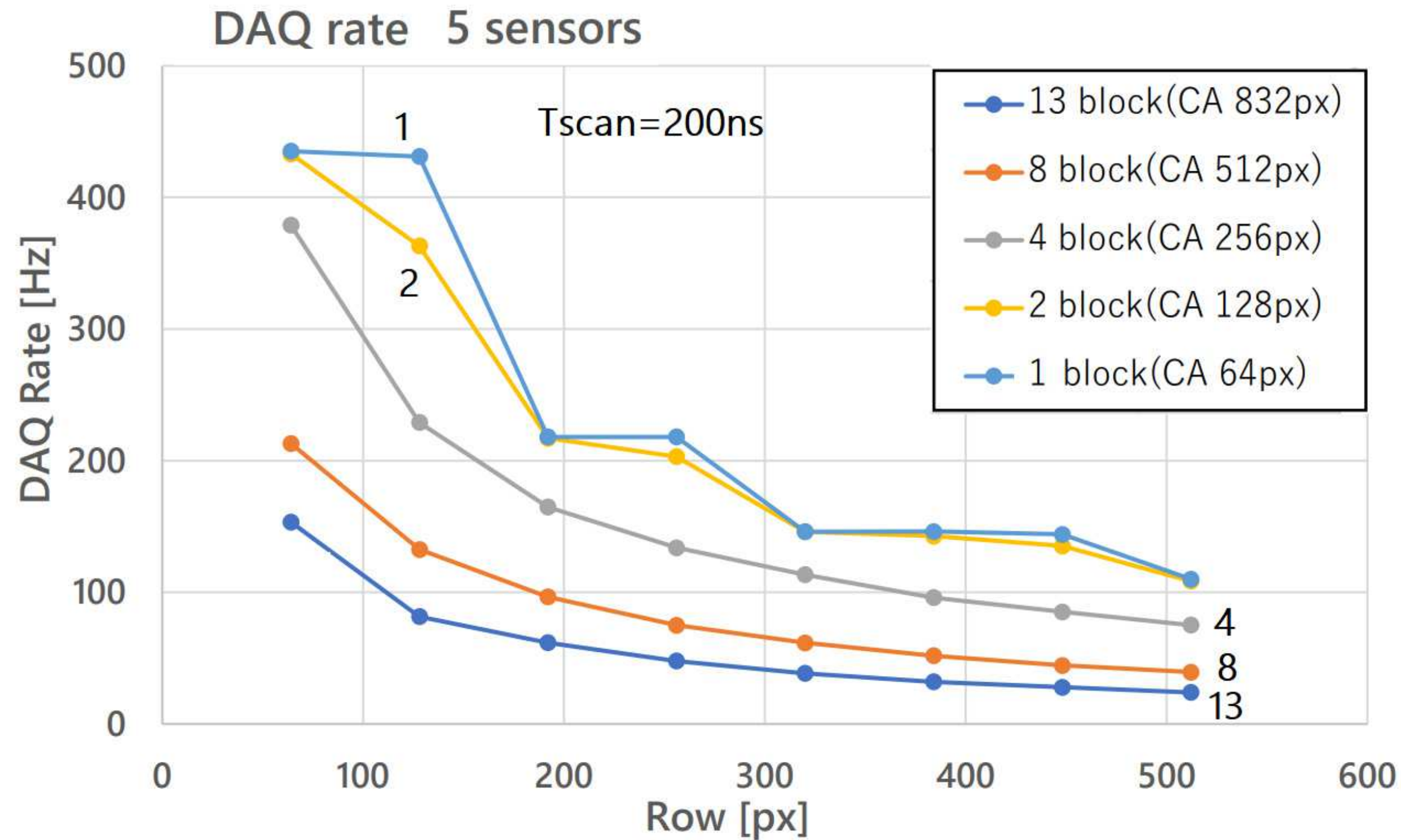
300 μm : σ is better than 10 μm at 1 GeV/c
 ~2 μm at 5 GeV/c

130 μm : the best performance

60 μm : not improve due to low S/N



DAQ Rate



Breakdown

- Row address scan time (200 ns/1 row)
- Analog to digital convert time (external ADC)
- **Data transmission to PC**

Number of cluster per event is ~1.

→ Necessary pixels are maximum 5×5 pixels for each event.

Zero-suppression logic based on FPGA

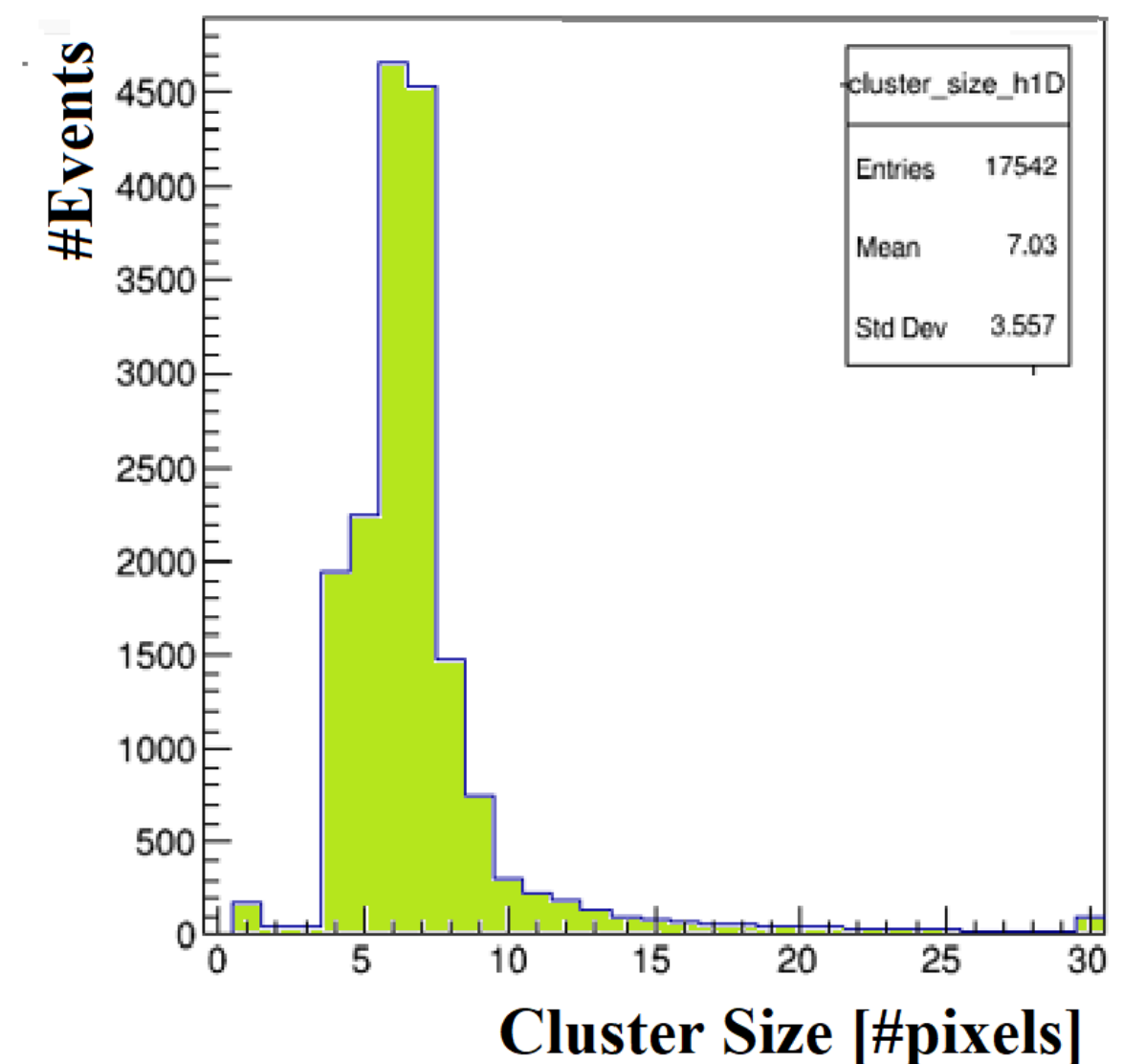
After AD conversion, pixels are selected by threshold on FPGA.

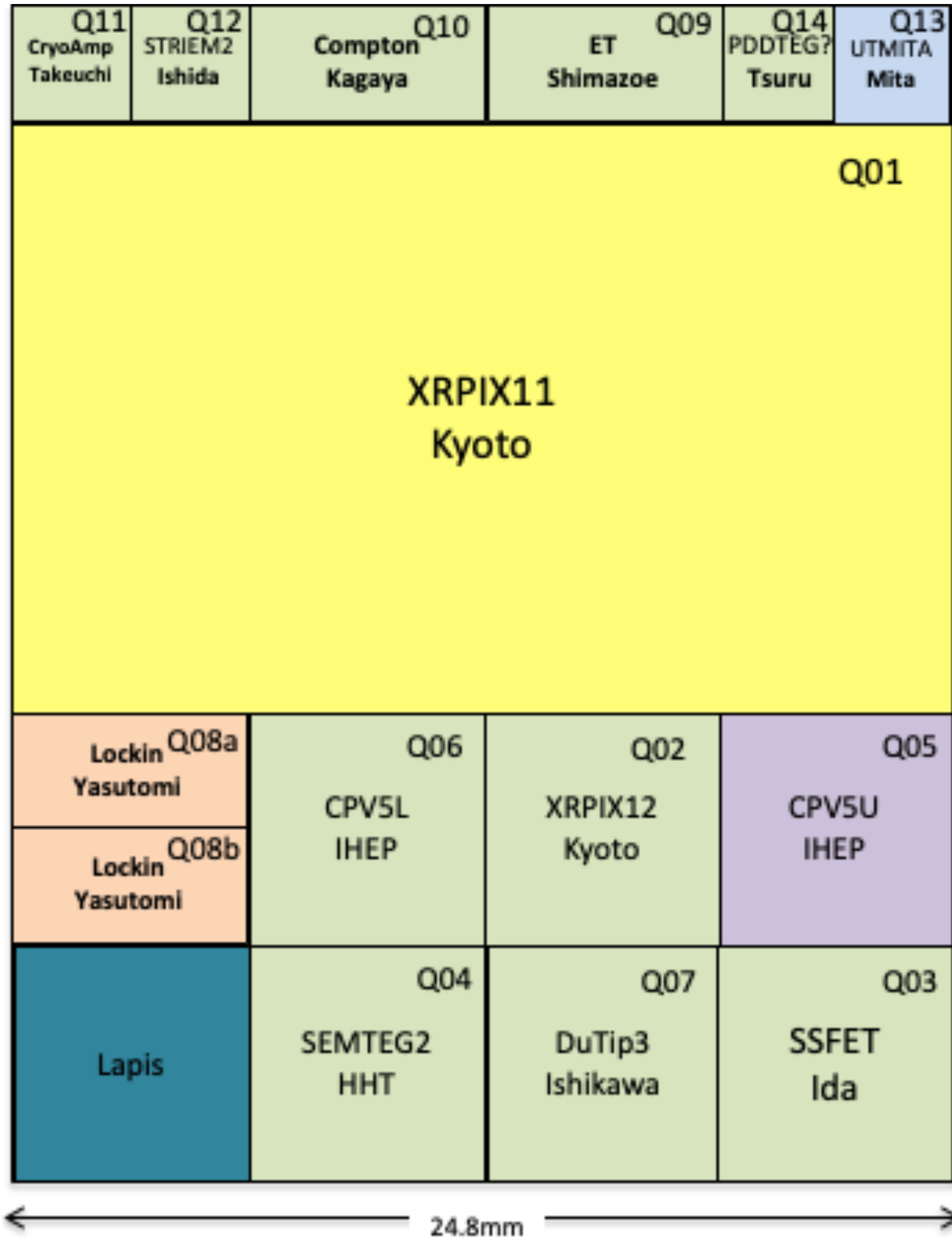
Threshold is evaluated by pedestal data (all the pixels).

(Maximum value of pedestal) is set as threshold.

Pixel which has maximum ADC value is identified as center of cluster.

Surrounding 5×5 pixels ADC, CA and RA are send to PC.





Reticle size: 31.0 mm × 24.8 mm