# C4Pi Telescopes DAQ
# Migration to TLU + EUDAQ framework

- 1 – C4Pi Telescope DAQ (now)
- 2 – EUDAQ & TLU ➔ T.JACQUES slides
- 3 – Integration of C4Pi Telescope DAQ in EUDET – TLU framework
- 4 - TLU goal and functionalities
- 5 - TLU versions
- 6 - Conclusion

# 1 – C4Pi Telescopes DAQ architecture 1/2

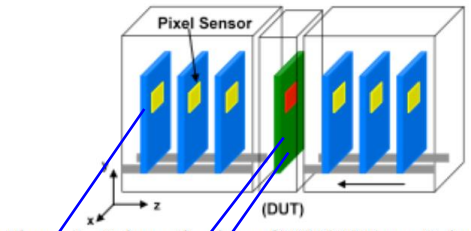
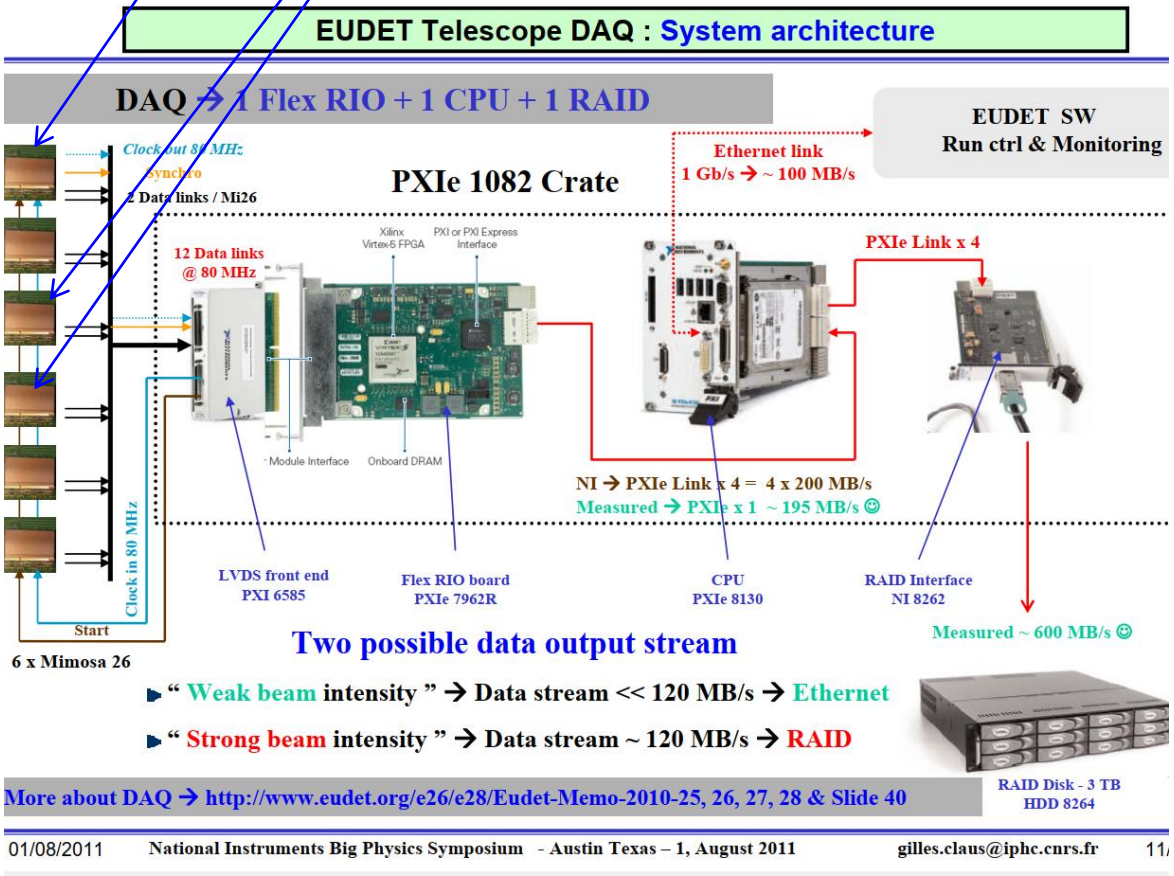



Figure 1 : Schematic view of EUDET Beam Telescope




**Most cases → Reference planes = same CPS as DUT**

- Mimosa 26, 28, Mimosis 1,2

- Simplifies Ref / DUT synchronization
- No need of TLU
- Allows to have same DAQ for Ref & DUT
- Allows for high events rate
- National Instrument COST HW used
  - Flex RIO FPGA board
  - Digital front end NI6585 (300 Mb/s) – NI6587 (1 Gb/s)

**Some case → Reference planes <> CPS DUT**

- DUT Mimosa 32 (Analogue) + Ref Mi26

- Two NI DAQ
  - Ref = Flex RIO + digital FE (NI6585)
  - DUT = Flex RIO + analogue FE (NI)
- Home made TLU on a FPGA board

# DAQ Systems based on NI COTS for pixels sensors characterization in beam test

**CNRS** Centre National de la Recherche Scientifique ( France ) ~ 25 000 People
**IN2P3** Institut National de Physique Nucléaire et de Physique des Particules ~ 2 500 People
**IPHC** Institut Pluridisciplinaire Hubert Curien ( France – Strasbourg ) ~ 400 People

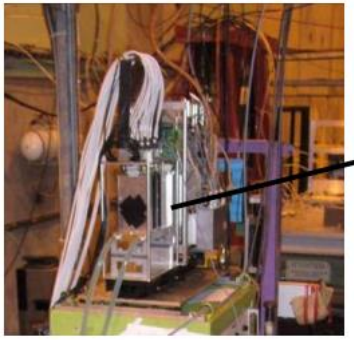
## From the idea …

Pixels sensor – Mimosa 26
~ 2 cm² - 600 K Pixels

Module PXI 6585
32 I/O LVDS

Flex RIO Board
PXIe 7962R

## to the implementation …



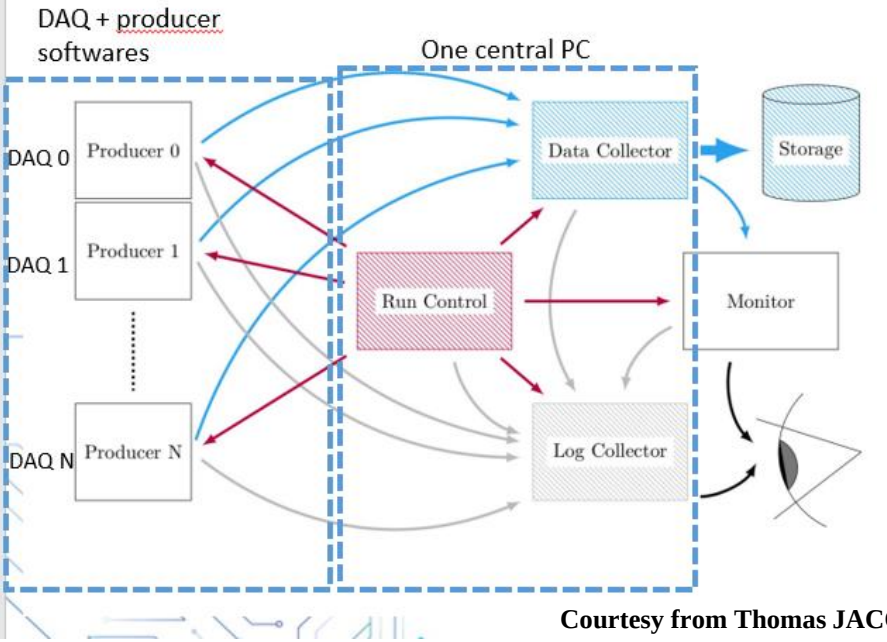
Beam Telescope @ CERN
6 Sensors Mimosa 26
8680 pictures/s → 120 MB/s

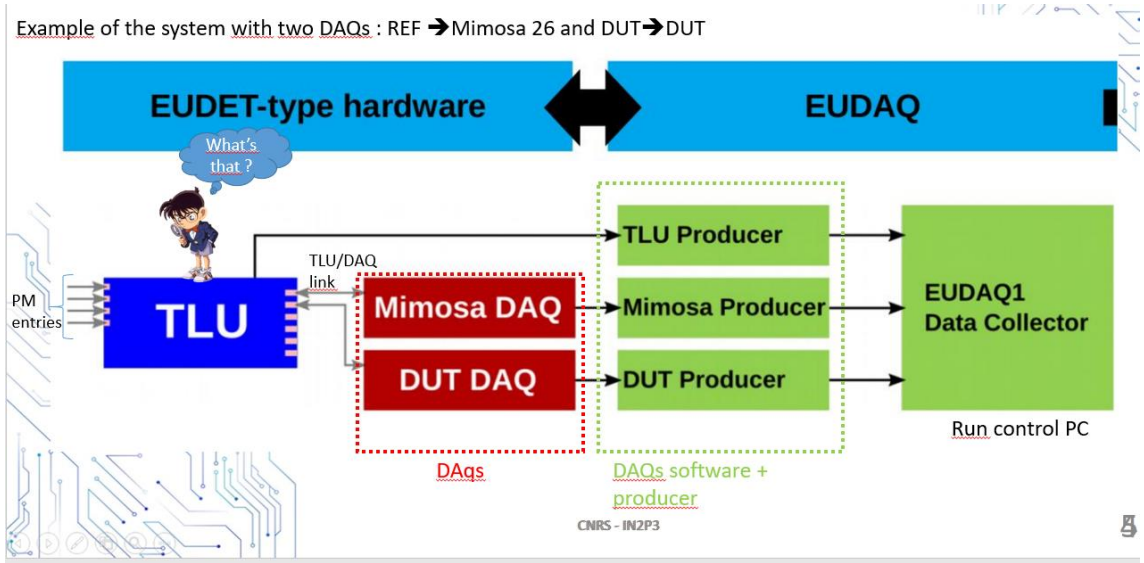
*DAQ : Flex RIO - PXIe*

**PICSEL group - ASICs Test & Characterization team**
http://www.iphc.cnrs.fr/-PICSEL-.html - Gilles CLAUS – gilles.claus@iphc.cnrs.fr

# What is EUDAQ ?

Software part




**Courtesy from Thomas JACQUES BUT GEII**

➔ **More info on T.JACQUES's slides**

# 3 – Integration of C4Pi Telescope DAQ in EUDET – TLU framework

- **The goals**
  - **Allow to integrate our CPS as DUT in a Telescope using the EUDAQ & TLU framework**
  - **Provide a DAQ for our telescopes (Mimosis 1,2 …) using and supporting EUDAQ & TLU framework**

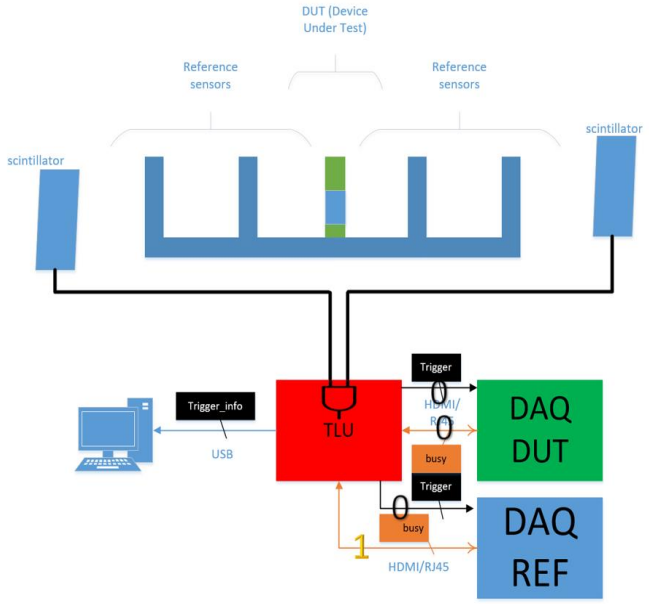
- **Project steps / milestones**
  - Learn how to use EUDET TLU and EUDAQ
    - Test TLU to learn how it works (max trigger rate still to be tested)
    - Emulating two DAQ (by two SW on a raspberry PI) controlled by TLU
    - Integrating the two DAQ emulator in EUDAQ SW framework
  - Decision to produce AIDA – TLU ?
    - No more EUDET (?) or AIDA-TLU available
    - Study started : we get the design, components ordered, optional obsolete component / cancelled, ➔ decide to launch PCB prod)
  - Integrating one of our BT DAQ (Mimosa 26 or Mimosis 1,2) in TLU  EUDAQ environment

There is a strong contribution from our apprentice BUT student  (T.JACQUES) to this project, green items have been mainly handled by him.

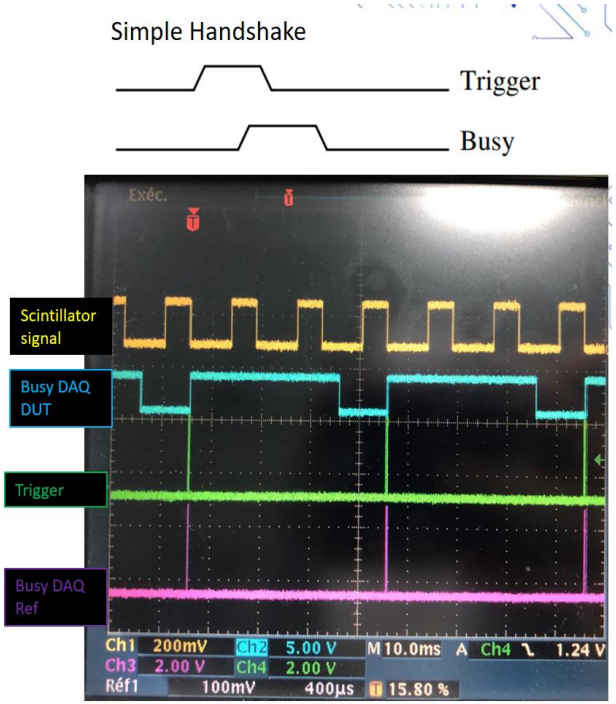
➔ **Next part on T.JACQUES's slides**

# 4 – TLU goal and functionalities

**EUDET TLU = V0.2C**




**Courtesy from T.JACQUES BUT GEII**




CNRS - IN2P3

8

### 5.2 Simple Handshake

1. TLU receives trigger from beam scintillators
2. TLU asserts TRIGGER
3. On receipt of TRIGGER going high, the detector asserts BUSY
4. On receipt of BUSY from DUT, the TLU de-asserts TRIGGER
5. On receipt of TRIGGER going low and the detector being ready to take more data, the DUT de-asserts BUSY
6. System is ready for triggers again. (state of Trigger-Clock is irrelevant in this mode)

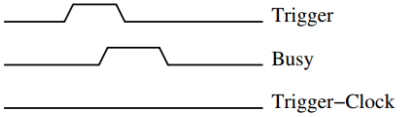
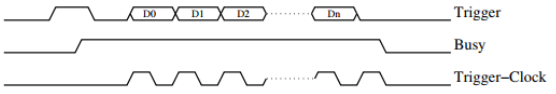



Figure 5: Timing of signals in "Simple Handshake"

### 5.1 Trigger Data Handshake

1. TLU receives trigger from beam scintillators
2. TLU asserts TRIGGER
3. On receipt of TRIGGER going high, the detector asserts BUSY
4. On receipt of BUSY going high, TLU de-asserts TRIGGER and switches the TRIGGER line to the output of a shift register holding the trigger number/data.
5. The DUT clocks data out of the shift register by toggling TRIGGER_CLOCK. Data changes on the rising edge of TRIGGER_CLOCK[3]. The least significant bit of the trigger data is shifted out first. Only the bottom 15-bits of the 32-bit trigger counter are clocked out. If more than 15 clock pulses are issued on the TRIGGER_CLOCK line the TRIGGER output is set to zero. The DUT should issue 16 clock pulses which will clock out the bottom 15-bits of the trigger number and return the TRIGGER line to logical low. This will avoid glitches on the TRIGGER line when the DUT returns the BUSY line to logical low.
6. After clocking out the trigger number (and the detector being ready to take more data, the DUT de-asserts BUSY)
7. System is ready for triggers again.




**TLU EUDET Memo 2009-4 courtesy from D.Cussans Bristol Univ**

**EUDET TLU = V0.2C**

### 5.3 No-Handshake

In this mode the TLU issues a fixed-length pulse on the trigger line (default pulse width is two cycles of the internal clock).

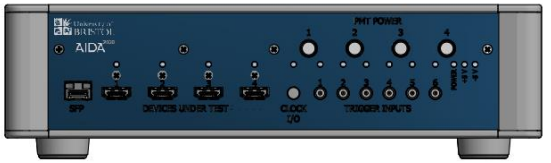
# 5 – TLU versions 1/3

## EUDET TLU - V0,2C

- Configured & read / PC via USB
- Up to 4 triggers inputs (analogue PM signal in or NIM + comparator, configurable trigger logic AND, OR, etc)
- Up to 6 DAQ controlled by TLU (RJ45 connectors)
- Operating modes
  - Simple handshake
  - Trigger data handshake (Trigger no read 15 bits by DUT at up to 10 MHz ⇔ 1,5 us )
  - No_handshake (TLU distributes triggers to DUT without handshaking / DUT)
- Triggers time stamping (64 bits up 3,125 ns resolution), read via USB

**EUDET TLU = V0.2C**

**AIDA TLU (table top or 19 ” rack)**





## AIDA TLU – V1E-F = AIDA 2020 TLU

- Configured & read / PC via Ethernet
- Up to 6 triggers inputs (same as EUDET version, but threshold conf by DACs)
- Trigger rate 1 MHz (peak 20 MHz)
- Up to 4 DAQ controlled by TLU (HDMI connectors)
- Operating modes
  - Simple handshake = EUDET mode
  - Trigger data handshake = EUDET mode + trigger no readout
  - AIDA mode = simpler mode than “EUDET simple handshake” ➔ Faster
  - AIDA mode + trigger no readout

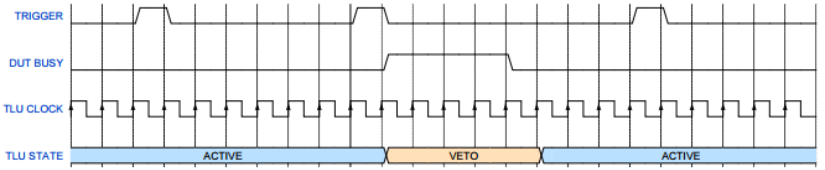



**Figure 6**. AIDA handshake mode. No data is exchanged between DUT and TLU; upon the reception of a trigger, the unit is ready to issue new triggers after 1 clock cycle unless a device asserts its busy line.

- Others functionalities not listed here ( each PM input time stamping, shutter signal, etc … )

**Remark : I am not a TLU expert, just playing with for few days**
**➔ Reference = David Cussans & al (TLU designer) Univ Bristol**

# 5 – TLU versions 2/3

Courtesy from T.JACQUES BUT GEII

- **AIDA Innova TLU**
  - Under development
    - https://indico.cern.ch/event/1191719/contributions/5358750/attachments/2635339/4559047/cussans_wp3_AIDAINNOVA_Annual_Apr23.pdf
  - Main improvement = Picosecond timing
  - Compatible with AIDA 2020 TLU

AIDA innova

Advancement and Innovation for Detectors at Accelerators

Task 3.3:
Sub-ns timing capabilities
for EUDET-style telescopes:

A Trigger Logic Unit (TLU)
for AIDA-Innova
With Picosecond Timing Support

David Cussans

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

AIDA innova

Task 3.3 Goals

- From AIDAinnova grant agreement, part A:
  - "To provide a O (100) ps timing for particle hits, a dedicated timing layer as well as a trigger logic unit (TLU) with picosecond-timing support need to be developed, integrated and installed at both CERN and DESY. The precision timing layer will be provided by a TimePix4 plane, which will be fully integrated into the telescope hardware and the EUDAQ2 framework. We foresee having such planes available at all beam lines. To provide an ultimate timing resolution of 30 ps, an LGAD plane based on current developments for the HL-LHC will be included in the EUDET-style pixel telescopes. In order to benefit from this exquisite timing, the TLU needs to provide a stable clock with a 10 ps or better stable edge, which will be part of the AIDA TLU upgrade."
- Fast timing detector WP: NWO-I/Nikhef, UNIVBRIS, CSIC-IFCA, DESY,UCL, USC

25 April 2023

Nikhef University of BRISTOL UCL CSIC Consejo Superior de Investigaciones Científicas IFCA Instituto de Física de Cantabria USC Universidade de Santiago de Compostela DESY.

AIDA Innova – TLU : courtesy from D.Cussans Bristol Univ

# 5 – TLU versions 3/3

**Courtesy from T.JACQUES BUT GEII**

- **AIDA Innova TLU**
  - Under development
    - https://indico.cern.ch/event/1191719/contributions/5358750/attachments/2635339/4559047/cussans_wp3_AIDAINNOVA_Annual_Apr23.pdf

## Picosecond TLU

AIDA-2020 TLU connected to beam telescope

- Timing specification:
  - Clock jitter < 10ps RMS
  - Timing-stamping of input signals O(10ps) RMS
    - c.f. O(1ns) for AIDA-2020 TLU
- Backwards compatible with AIDA-2020 TLU
  - Same signals on DUT connections
    - trigger/busy/DUT-clk in EUDET-mode
    - Global-clk, trigger, busy, shutter, T0 in AIDA-mode
  - Small change to data format – timestamp will need more bits

## Picosecond TLU - I/O

- Trigger inputs
  - Probably 8
    - (c.f. 6 for AIDA-2020 TLU)
  - One or more threshold discriminator per channel with ADC for time-walk correction
    - (c.f. threshold discriminator only in AIDA-2020 TLU)
  - TDC with O(10ps) bins
    - Looking at using PicoTDC (3ps bins)
  - Aim to contribute less to timing uncertainly than detector.
- Device Under Test (DUT) connectors
  - Compatible signal definitions as AIDA-2020 (also LVDS)
  - Move to “Display Port” from HDMI - mechanically more robust. Five good quality pairs (c.f. 4)
    - Passive adaptor to existing HDMI connector.
    - Opinions?

**AIDA Innova – TLU : courtesy from D.Cussans Bristol Univ**

# 6 – Conclusion

- **Project to migrate our BT Daq to EUDAQ started in fall 2023**
- **Mainly handled by me and our BUT apprentice student (50 % od his time at lab)**
- **First of all ➔ Evaluation of AIDA TLU reproduction … done … cost ~ 3 weeks**
  - **Design is available on GIT but the current version can't be modified**
  - **A component (IC flip-flop) is obsolete but is not mandatory (fast SFT Eth)**
  - **Components have been ordered**
  - **We can decide to launch PCB prod**

- **Now ➔ Since mid-December**
  - Learn how to use EUDET TLU and EUDAQ
    - Test TLU to learn how it works (max trigger rate still to be tested) ➔ Done
    - Emulating two DAQ (by two SW on a raspberry PI) controlled by TLU ➔ Done
    - Integrating the two DAQ emulator in EUDAQ SW framework ➔ For spring 2024
  - Decision to produce AIDA – TLU ? If we produce it ➔ For summer 2024
  - Integrating one of our BT DAQ (Mimosa 26 or Mimosis 1,2) in TLU EUDAQ environment ➔ For end of 2024