New Comet :
Demonstrator of a scalable triggerless data acquisition system

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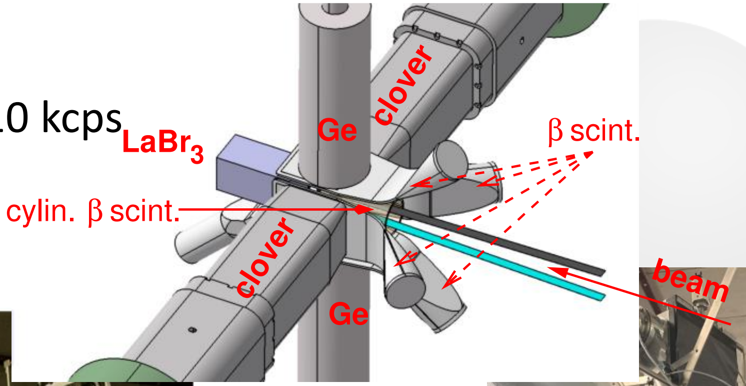
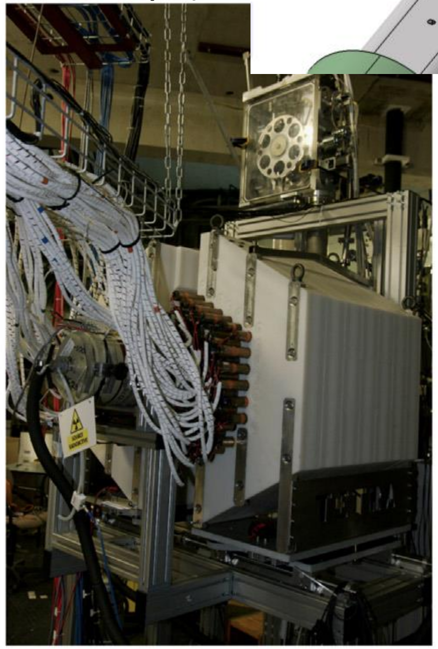
Outline

- The New COMET board
- A versatile, scalable signal acquisition
- Wide-range, high-accuracy clock synchronization
- Acquisition of Germanium signals
- Conclusions

Context

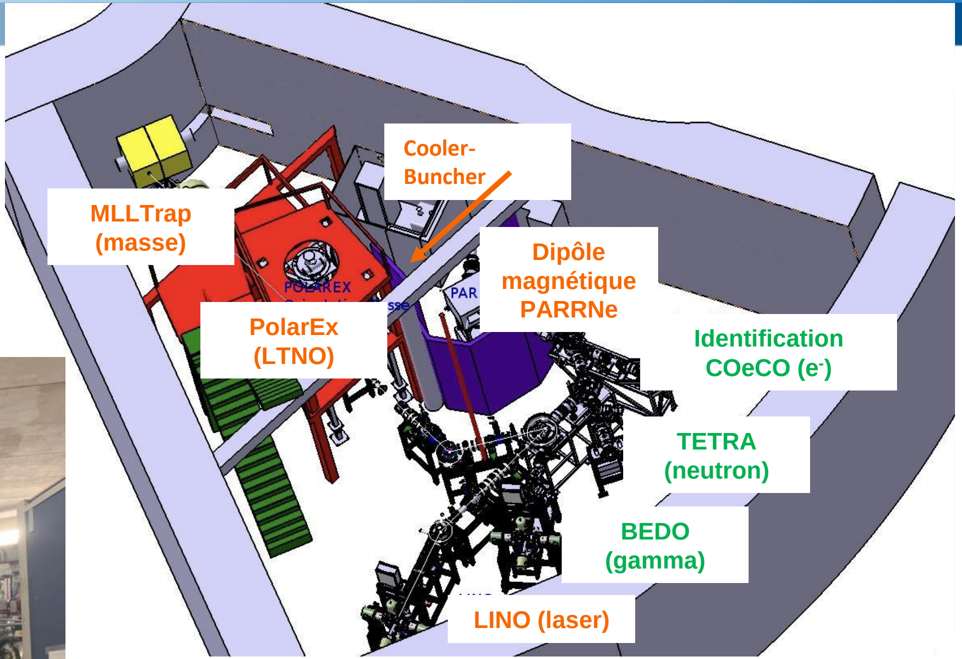
BEDO
4-16 HPGe channels, 10 kcps
4 AC shield
1 $LaBr_3$, 50 kcps
5 PMT (50-100 kcps)





TETRA
1 HPGe channel, 10 kcps
1 PMT (50 kpcs)
1 TTL + 1NIM signal, 1 kcps

COeCO
4 HPGe channels, 10 kcps
1 SiLi, 10 kcps
1 PMT, 50 kcps

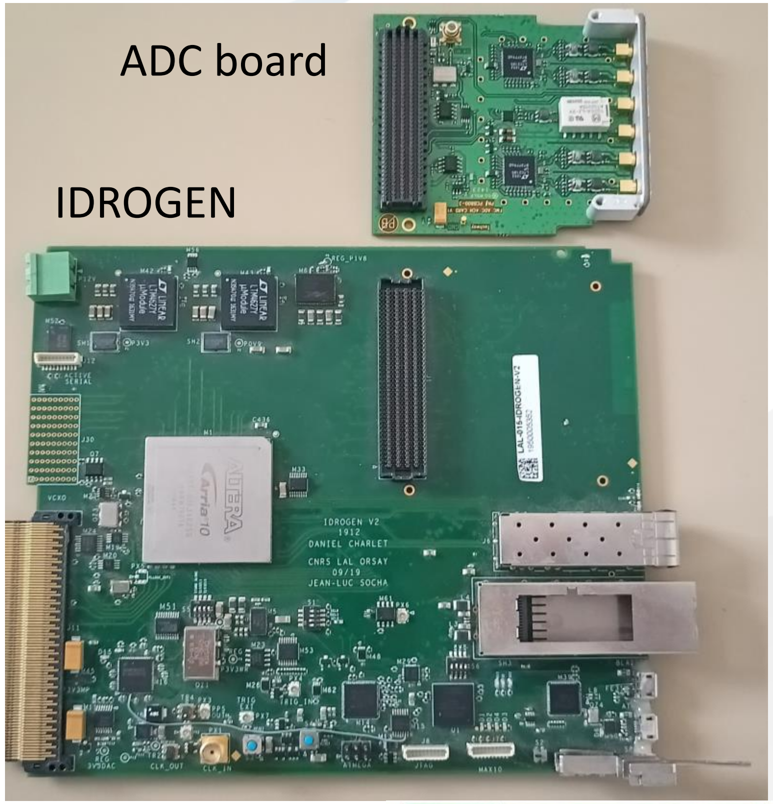


- Versatile configuration
- Different detectors
- Triggerless
- Analysis on the whole detectors

COMET vs New Comet: stakes

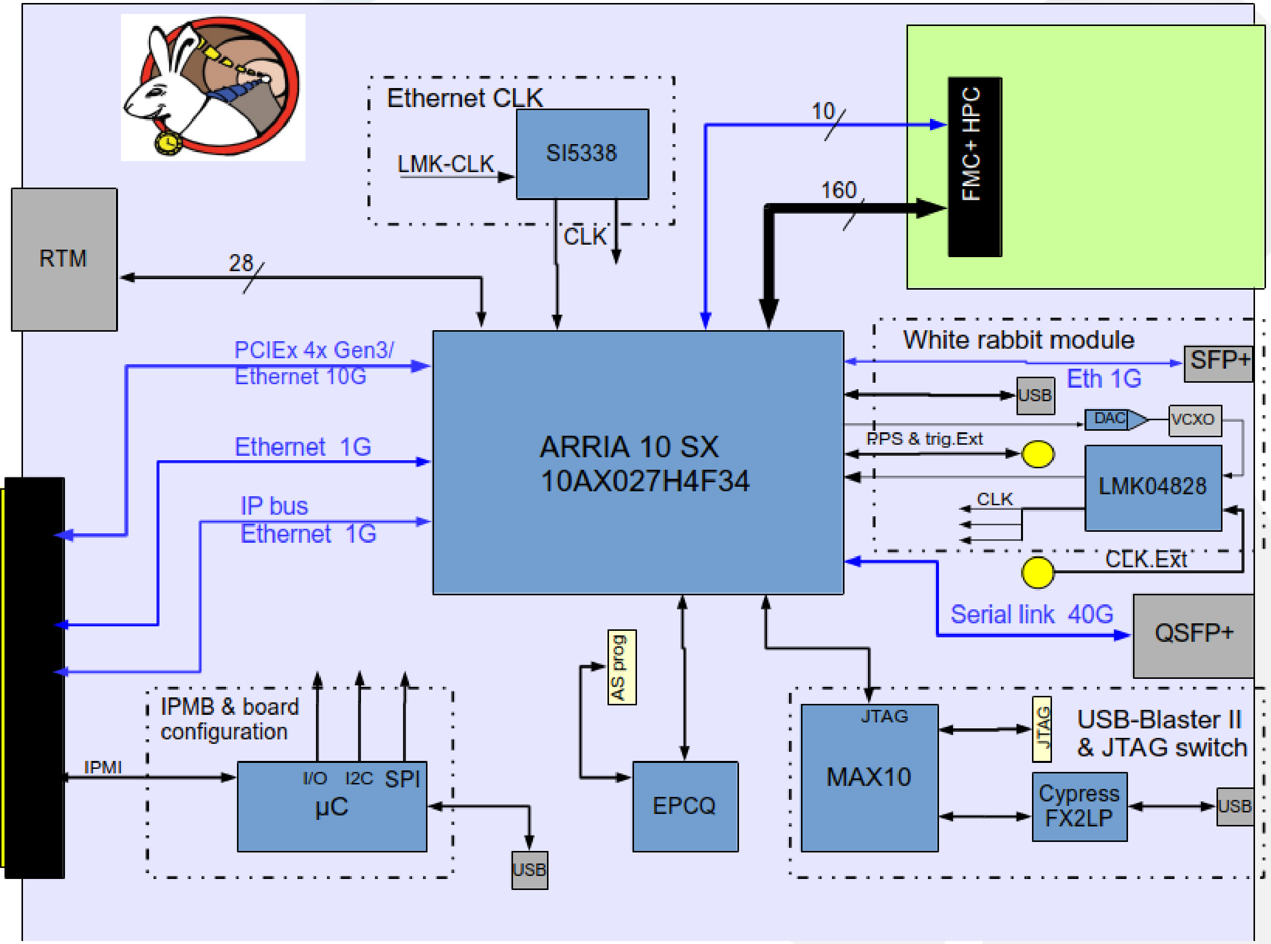
	COMET	New COMET – expected (see appendix)
Technology	E: Wilkinson ADC t: counter	E, t: digitizer + digital signal processing
HPGe charge measurement	50-µs preamp + 6-µs shaper	Direct preamp. digitization (50-µs const)
Input range (keV)	10 – 15e3	10 – 15e3
Effective number of bits	15 (1 LSB = 460 eV)	15
Differential Non Linearity	< 2e-3	< 1e-4 (FADC = 0.6 LSB/16 bits + preamp + digital processing)
Time stamping	49 bits, 400-ps time bin after analog filter + discriminator	64 bits, FADC time bin (4 or 8 ns) + calculated offset (error < 300 ps FWHM)
Dead time for E conversion	10 µs	≈ 2 µs (detector dependent)
Max. rate per channel (kcps)	10	10-20 (detector dependent + data flux)
Pile-up disentanglement	Depending on the analog processing	Digital processing
Number of channels (max.)	30	Limited by the data flux
Geometric span (m)	5	> 1000
Scripting	C visu	Python, C++ (via DCOD)

IDROGEN, the core board of New COMET



- High performance data acquisition system:
  - PCI express > 30Gbs, Ethernet > 20Gb
- Time tagging with picosecond-range White Rabbit
  - Accuracy < 20ps RMS
  - Jitter < 1ps RMS
- FMC+ carrier board for additional functions
- Crate (µTCA) or stand alone use
- Design & development done by IJCLab
  - CERN schematic improved
  - Components upgrade : PLL, VCXO, FPGA
  - PCB design compliant with EMC rules
- Collaboration
  - Firmware development done by Nançay Observatory and IJCLab
  - Clock expertise and qualification by SYRTE (Observatoire de Paris)

IDROGEN technical details



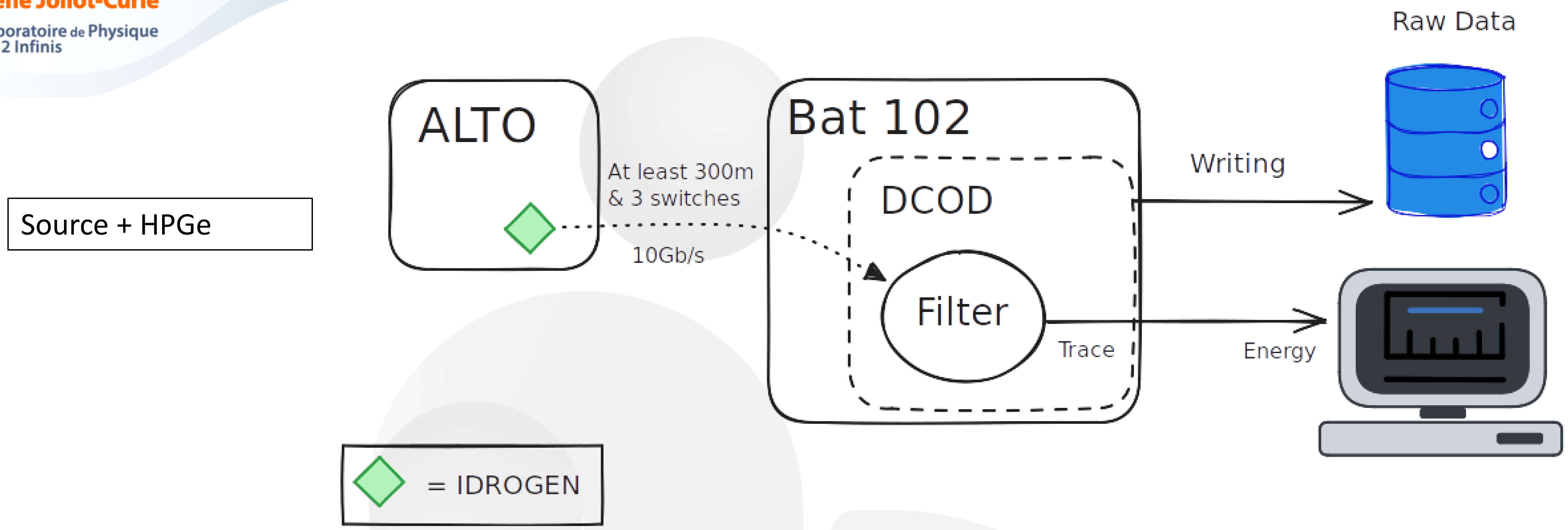
- TCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC+ slot)
- 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant
- Configurable output clock
- Front panel connectivity :
- WR SFP+
- QSFP+ 40G, USB
- Backplane connectivity :
- 1Gbe Ipbus, PCI 4x Gen3
- IPMB, CLK & trigger lane
- RTM connector : J30

New Comet: front-end

- Tested digitizers (FMC boards)
  - ADC 125 MSPS, 15 bits (LTC 2185)
  - ADC 250 MSPS, 16 bits (TI ADS42JB69, ENOB = 11.8 bits, DNL = 0.6 LSB)
- Firmware development + test in two months FTE
  - Trigger
  - Sliding window for data transfer

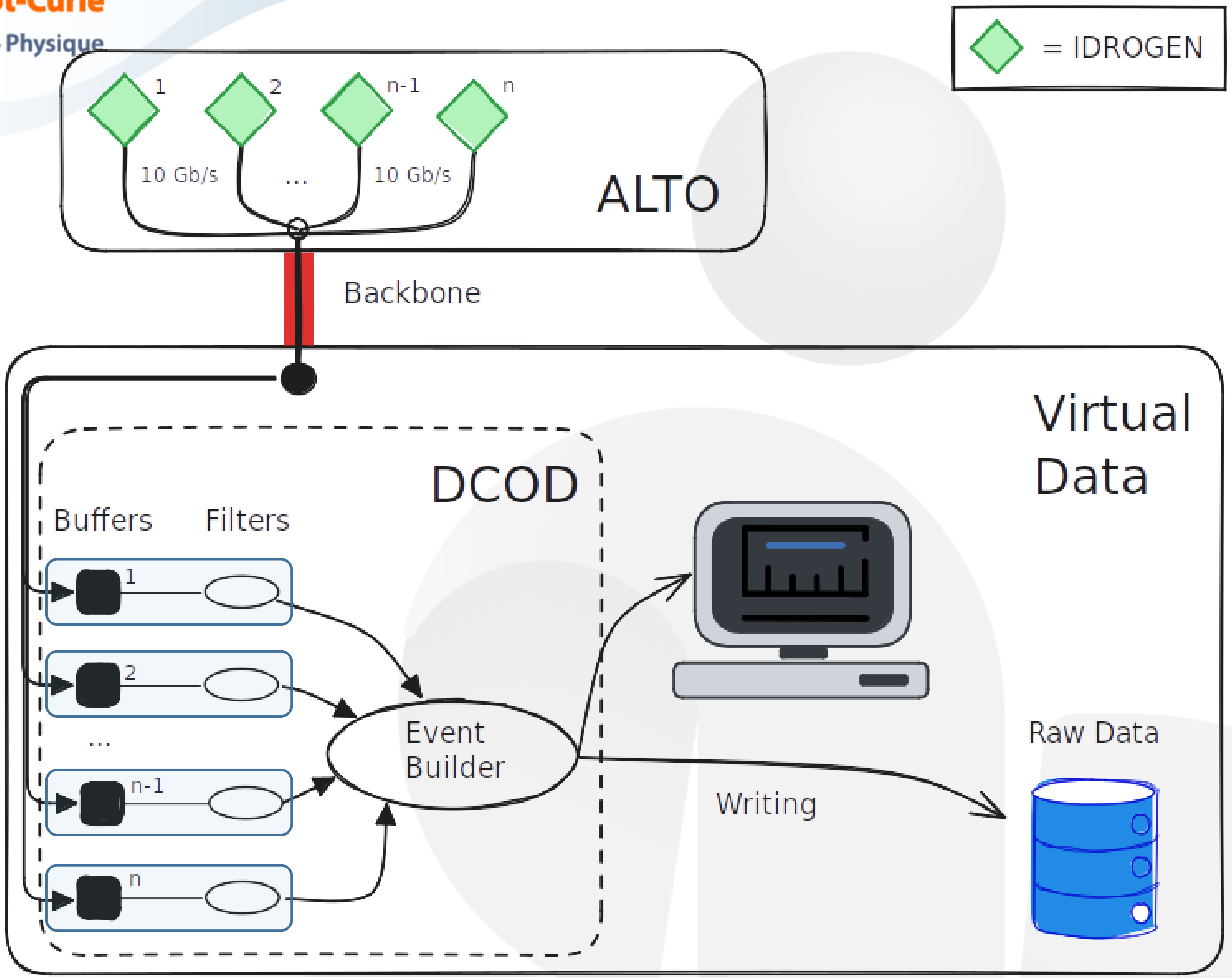
A versatile, scalable data acquisition

What we tested



- 1 channel
- Event rate: 5 kcps (typical rate for BEDO/COeCO = 2 kcps)
- 0 dead time at 125 MSPS (continuous mode, limited by the disk) 2 Gbit/s
- Recorded also by windows (50, 100 µs)

Data acquisition architecture



Remote acquisition servers

Non dependent on the experiment

Split acquisition as "micro-service"
flexibility, expendability

Containerization

Micro service

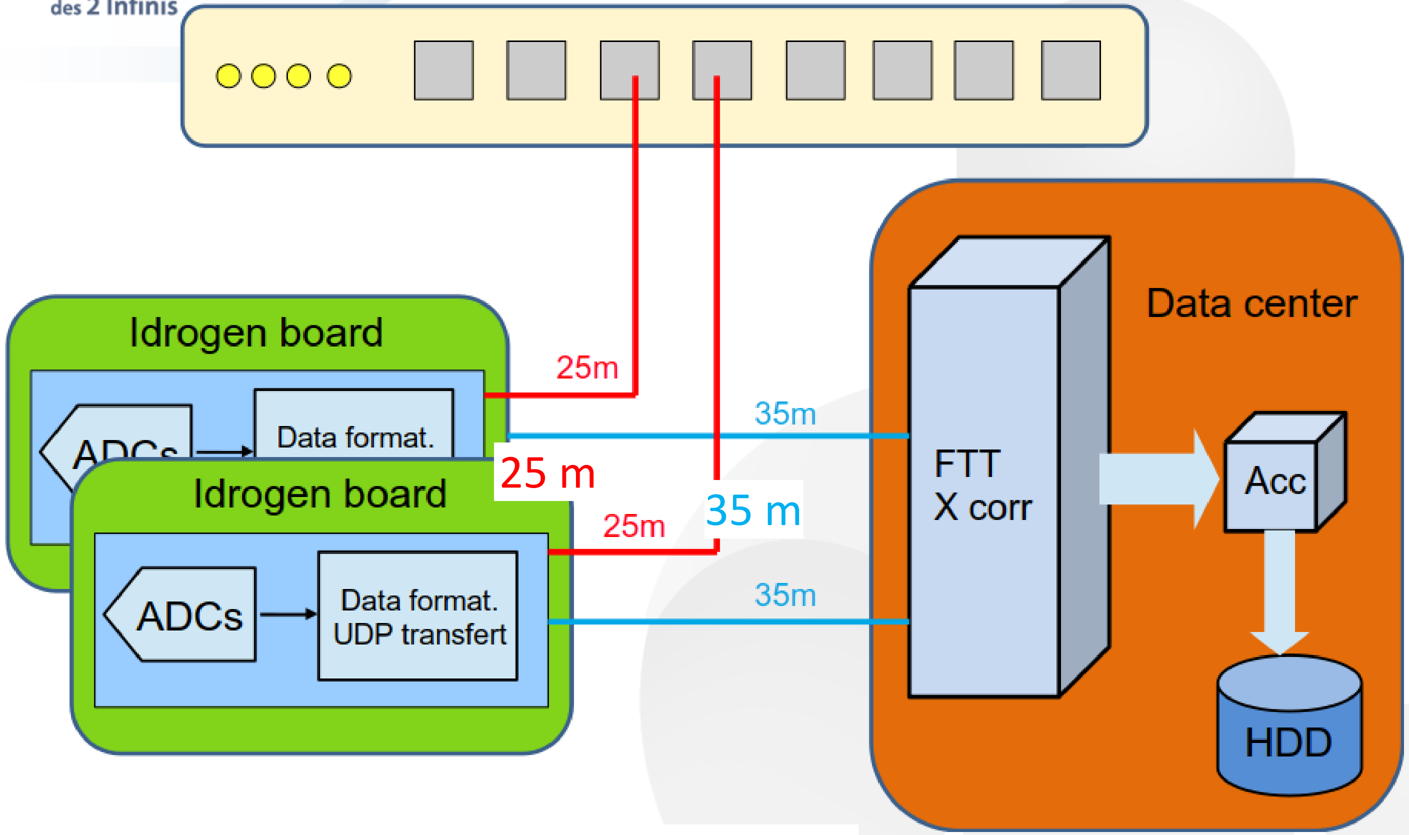
Each buffer + filter in a dedicated container

Synchronization with White Rabbit

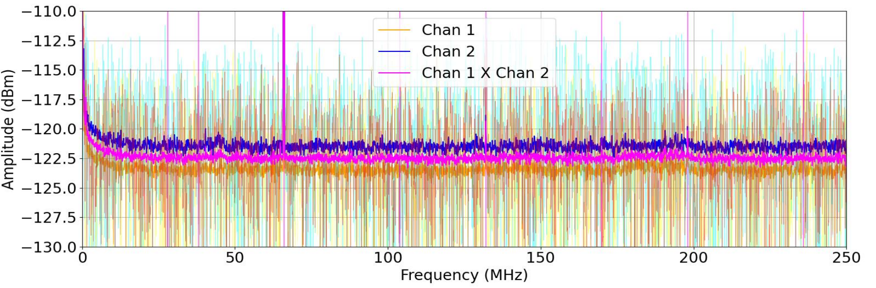
Clock stability in time and space

- The IDROGEN board embeds an **enhanced White Rabbit protocol:**
  - **< 1 ps RMS jitter**
  - **< 5 ps RMS board-to-board accuracy** (standard version: a few ns)
- Greater signal digitization accuracy
- Time stamping accuracy on a large distance (above 1 km)

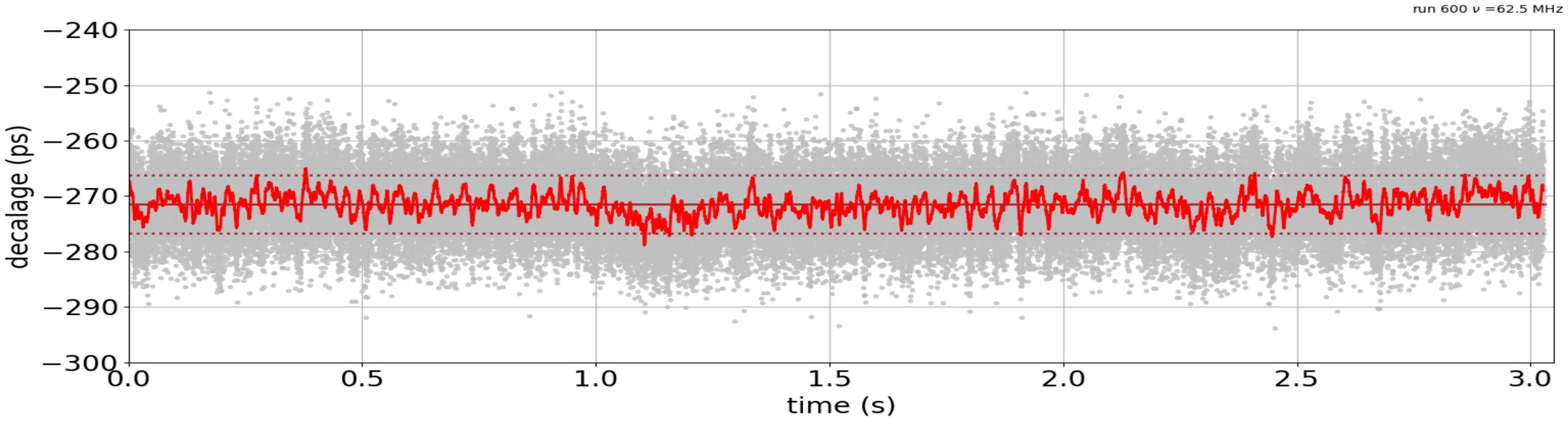
White Rabbit validated with PAON-4

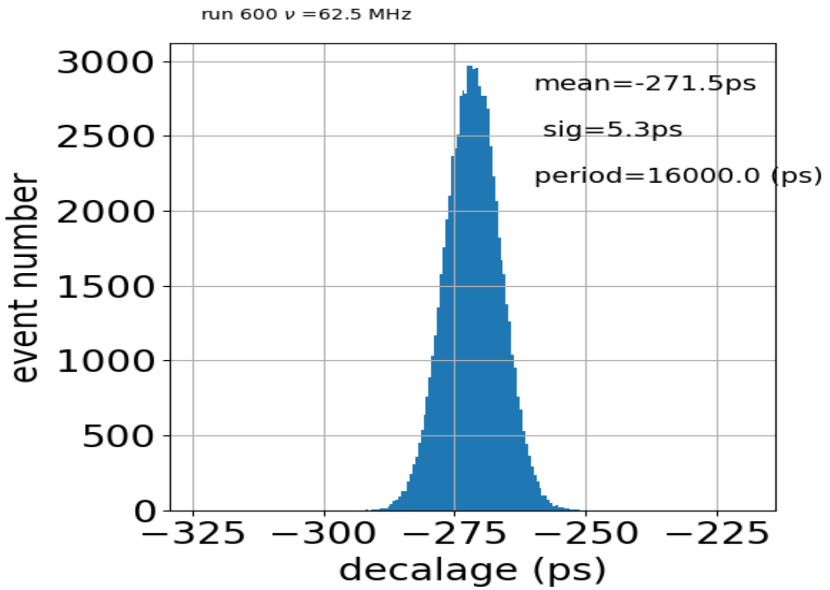


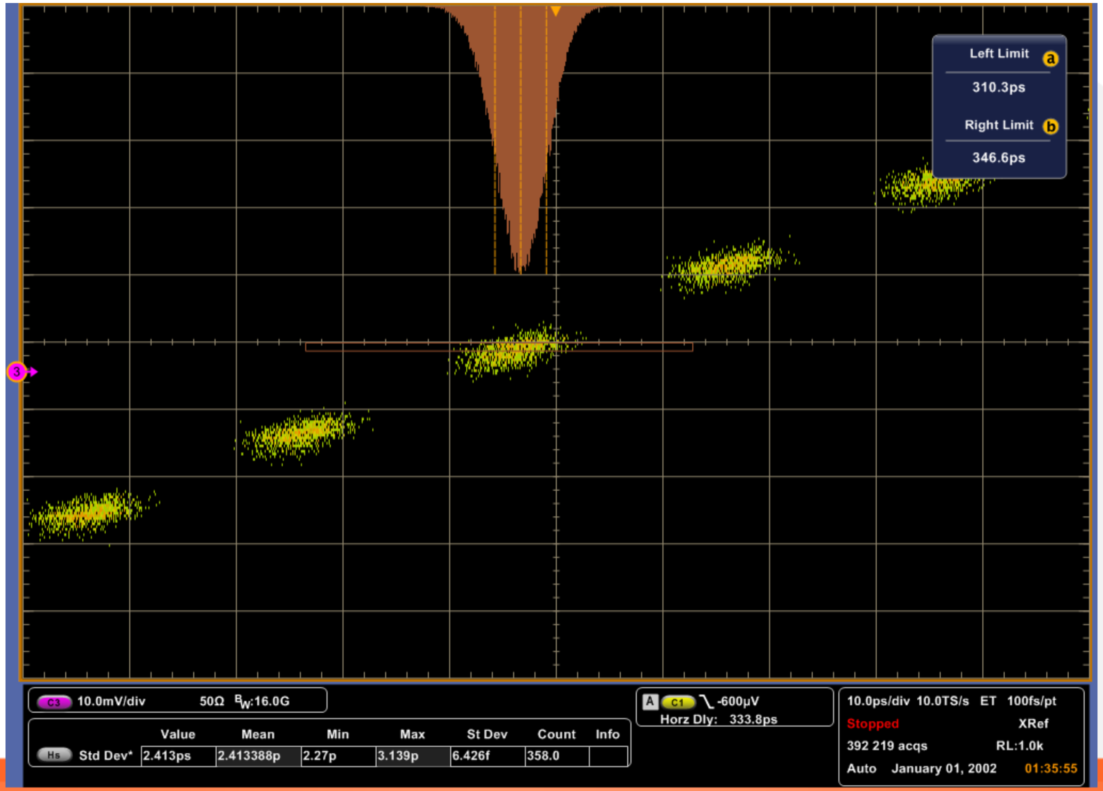
- Radioastronomy project
- 2 IDROGEN boards synchronized by WR
- Digitization: FMC board with 500 MSPS AD9680 ADC
- Test setup
  - Data fiber length 35m
  - WR fibers length 25 m
  - FFT 16K point
  - Cross correlation
  - Analog signal 63MHz split on 2 boards
  - 1Ghz generated clock on 2 boards

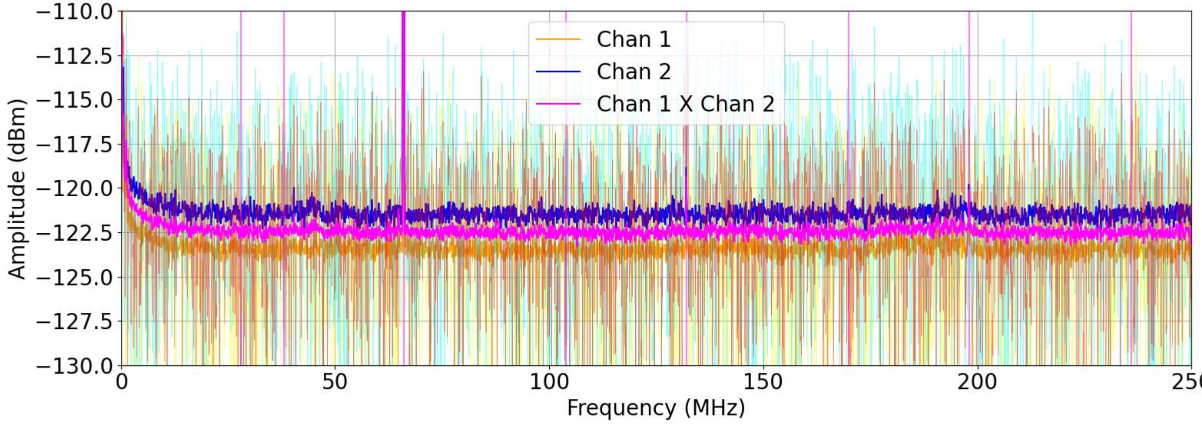


Time shift between boards < 5 ps RMS







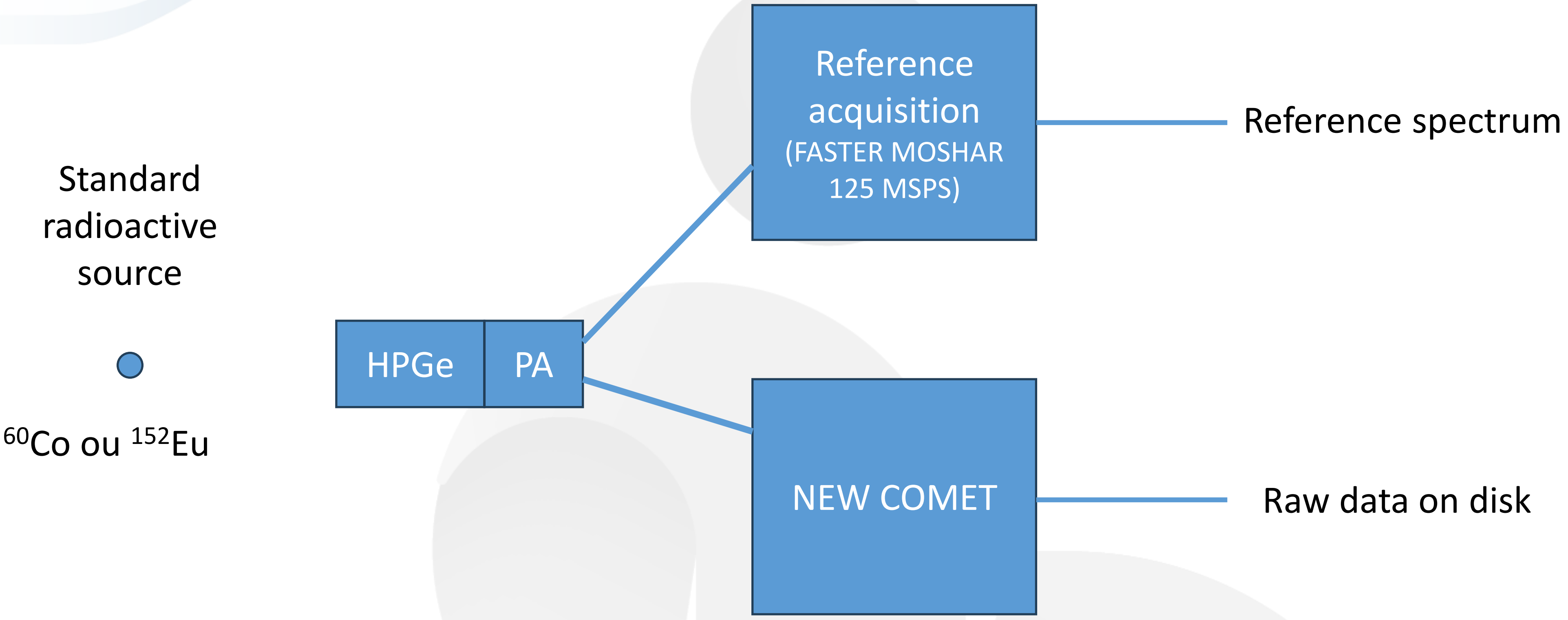


Test setup 2

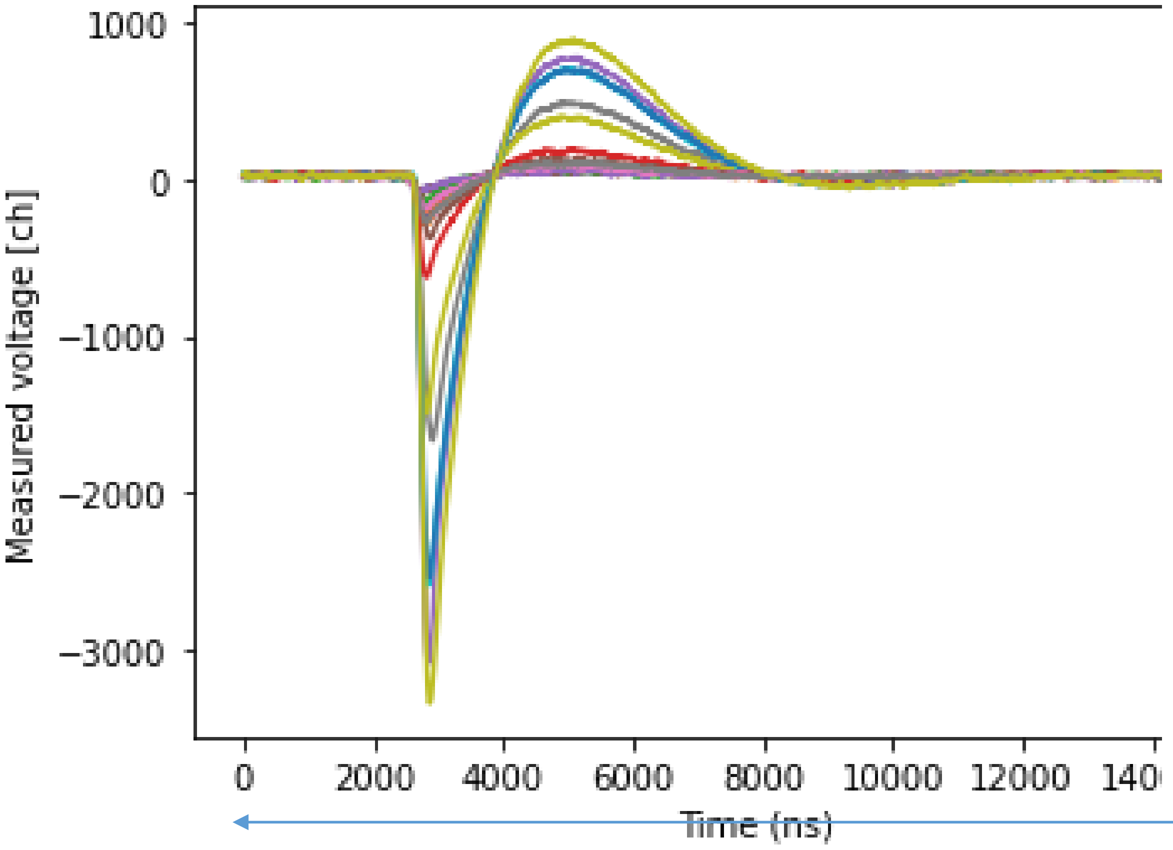
Test setup 3

Acquisition of Ge signals

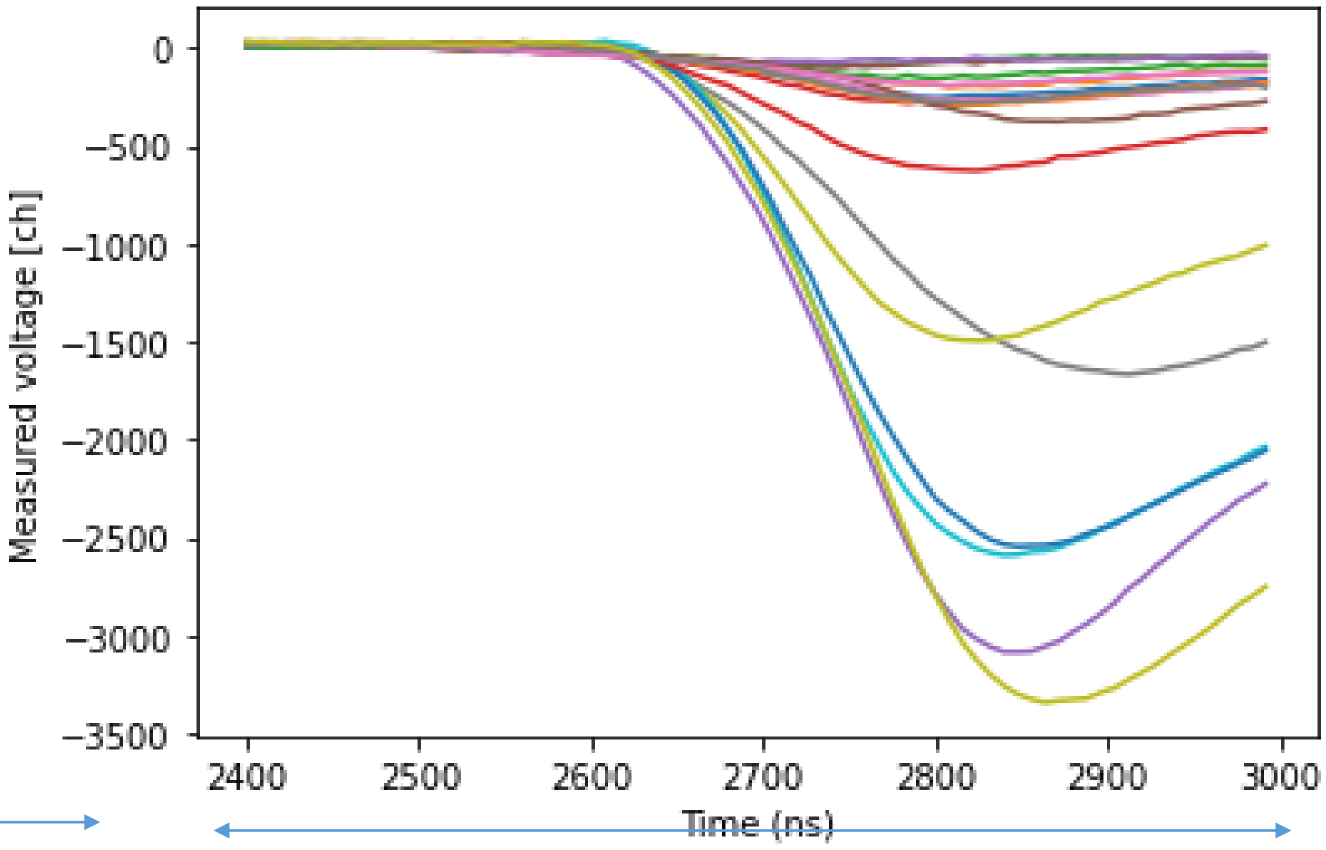
Validation at ALTO



HPGe signals digitization



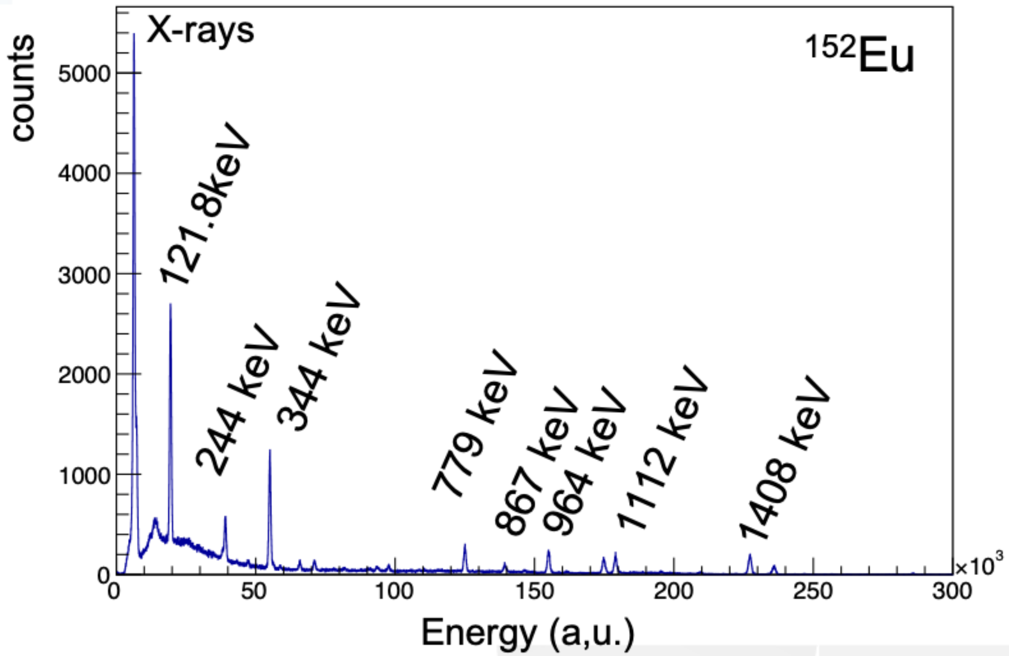
16 µs

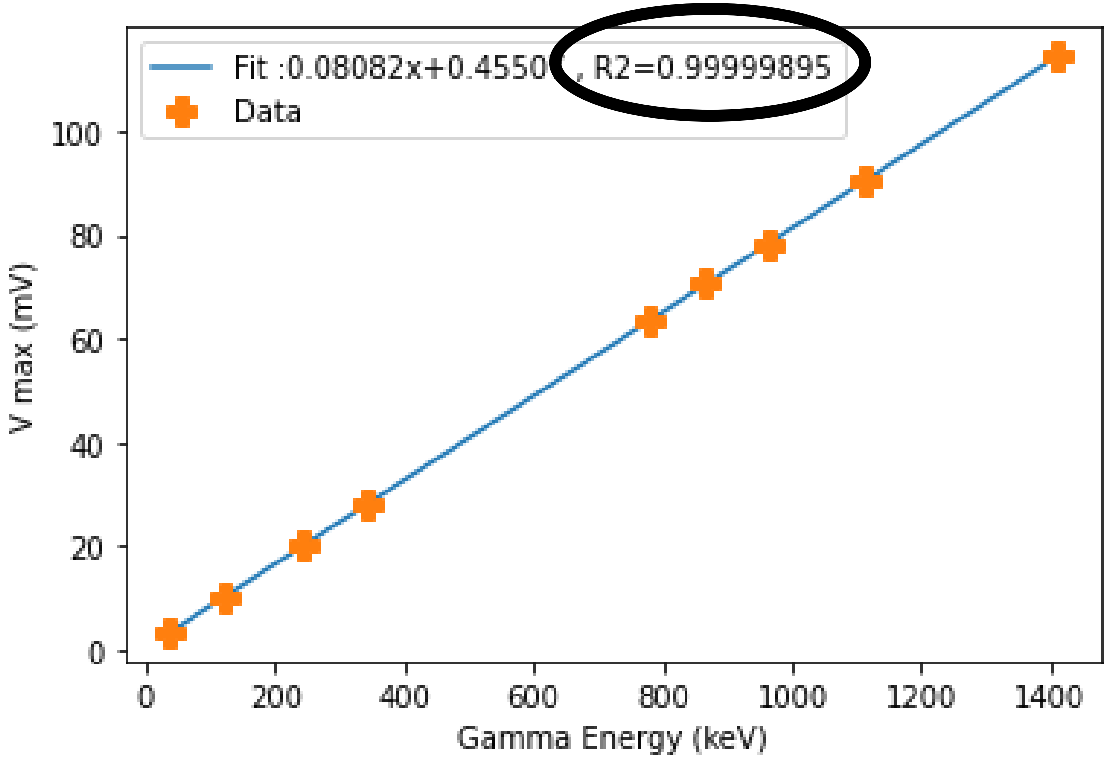


3 µs

Differenciation due to the board input filter

Linearity





Resolution around 6‰ <- not sufficient
(Reference spectrum : ~2.5‰)

- Validated also with a pulser

100 keV ~ 8 mV as maximum amplitude

Expected energy resolution

- Safer solution for energy: 125 MSPS if higher effective number of bits

- Theoretical possibility to gain above 2-3 effective bits with digital signal processing

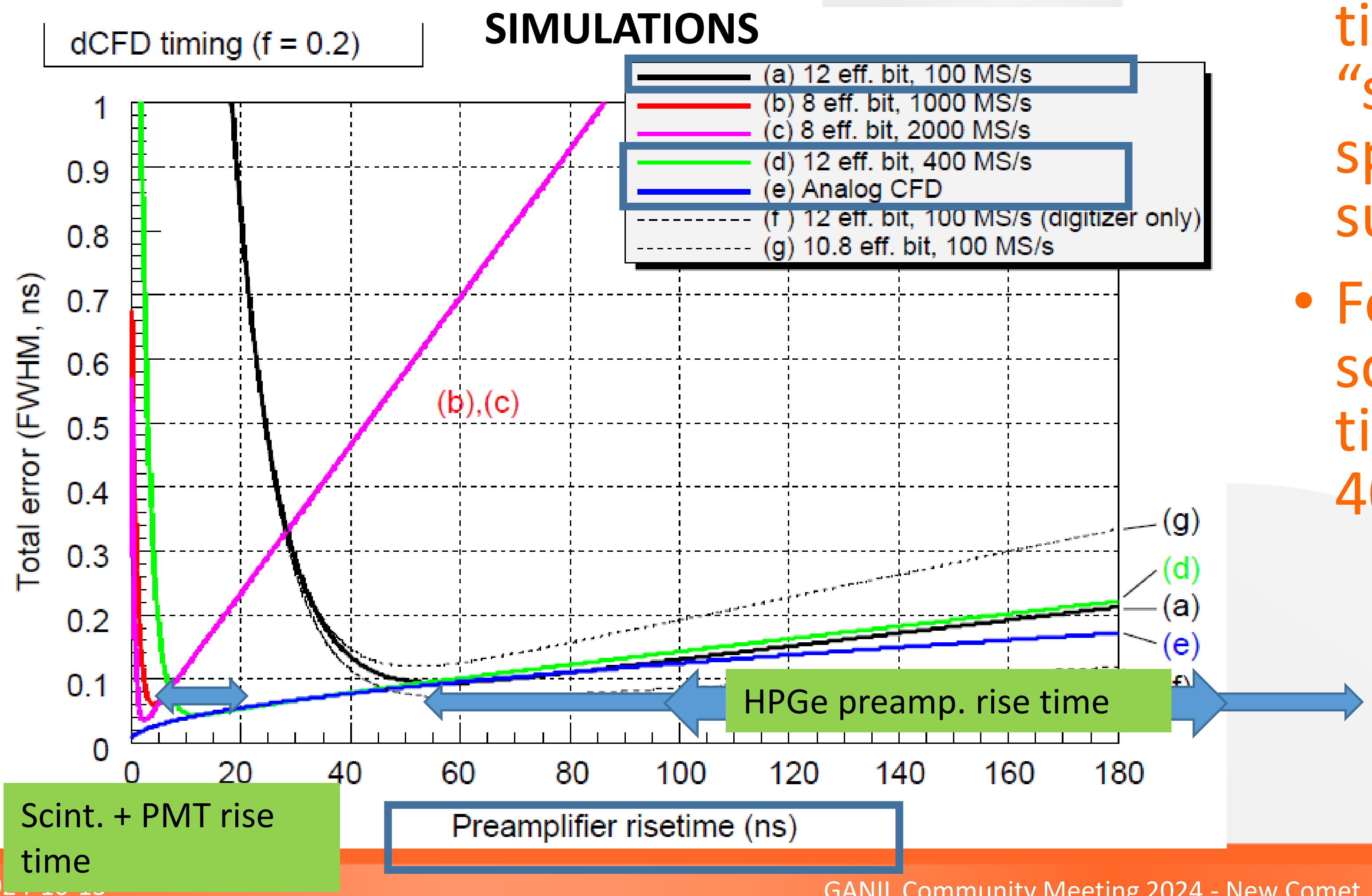
L. Bardelli et al., ***Digital-sampling systems*** *in high-resolution and* ***wide dynamic-range*** *energy measurements:* ***Comparison with peak sensing ADCs***, NIMA 2006

- Limitation due to the input filter and its high low-pass cutoff frequency

L. Bardelli et al., ***Digital-sampling systems*** *in high-resolution and* ***wide dynamic-range*** *energy measurements:* ***Finite time window, baseline effects, and experimental tests***, NIMA 2006

Expected time resolution for HPGe and scintillators

L. Bardelli et al., *Time measurements by means of digital sampling techniques: a study case of* ***100-ps FWHM time resolution with a 100-MSPS 12-bit digitizer***, NIMA 2004



- No major impact on HPGe timing (dominated by the “slow” preamp rise time, charge spread and range): 125 MSPS is sufficient
- For timing measurements with scintillators: add a 50-ns rise time preamp / move to 300 or 400-MSPS, 12-bit ENOB ADC

Conclusion

- Data acquisition as a microservice (containerization)
- Data online and offline processing on distant virtual machines
- Data storage separated from the signal acquisition site
- Signal acquisition of HPGe signals with a board assembled in two months – working on the processing to reach the 2.5 keV at 1 MeV
- Installation for data taking with COeCO at ALTO in 2025