future ASICs for calorimetry at OMEGA

Ch. de LA TAILLE FCC-France Strasbourg 2023

Organization for Micro-Electronics desiGn and Applications

Trends for calorimeter readout

- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction

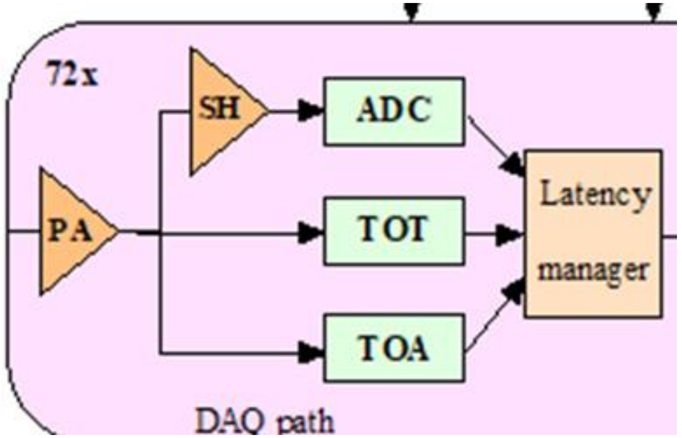
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction

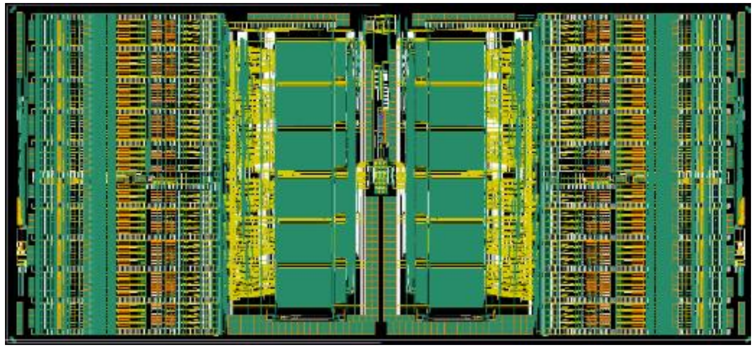
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Embedded ASICs

- Pioneered with CALICE R&D (SKIROC, SPIROC..)

- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)





- Difficulties
  - Analog/digital couplings

Example : HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

Control

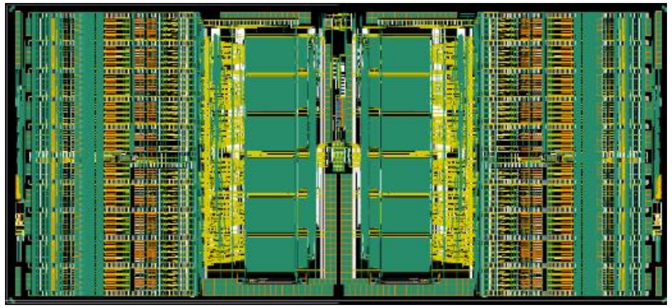
- Fast commands

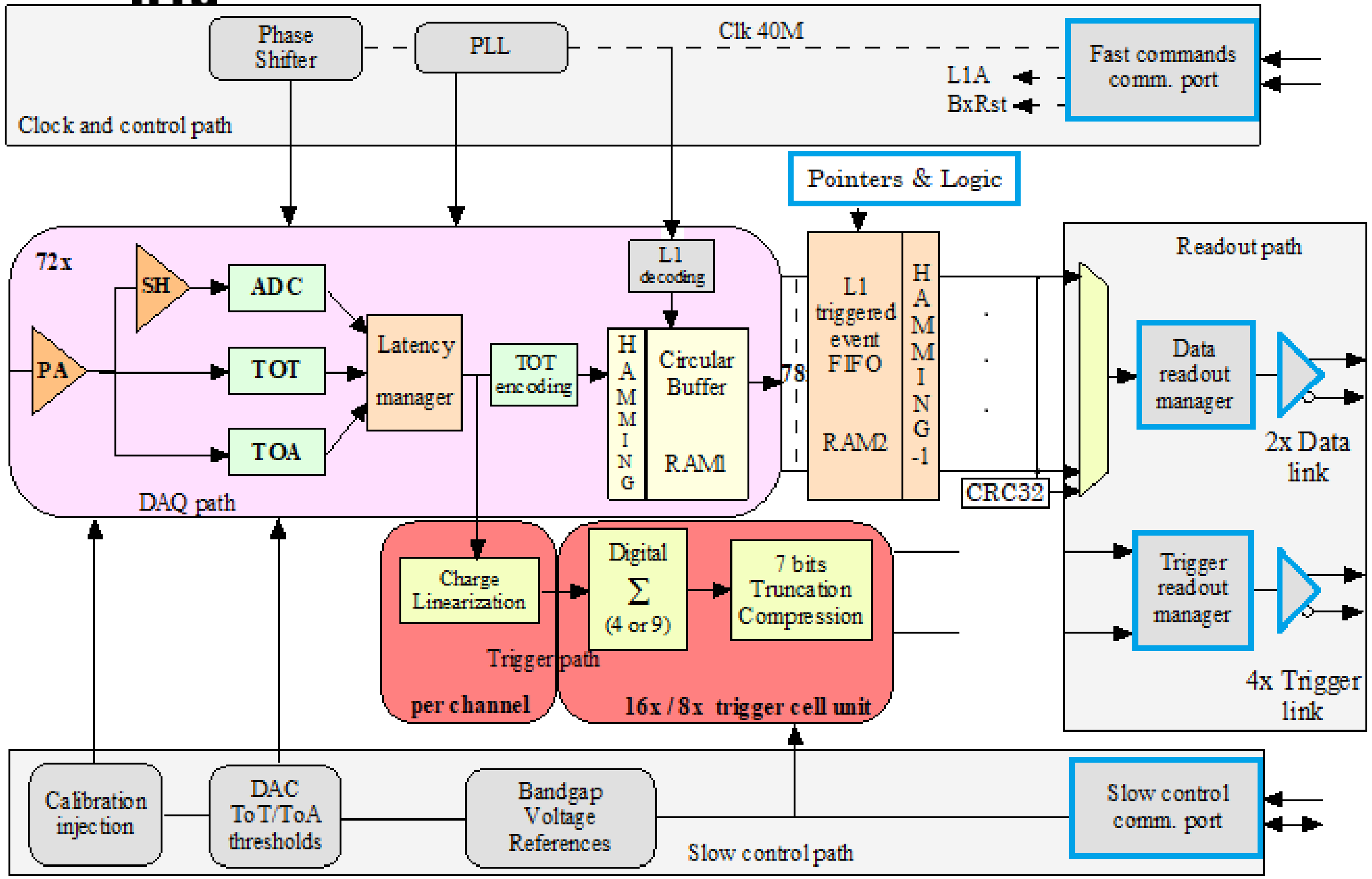
$Q_{MIP}/Cd \sim 3$ fC/30 pF = 100 µV

- I2C protocol for slow control

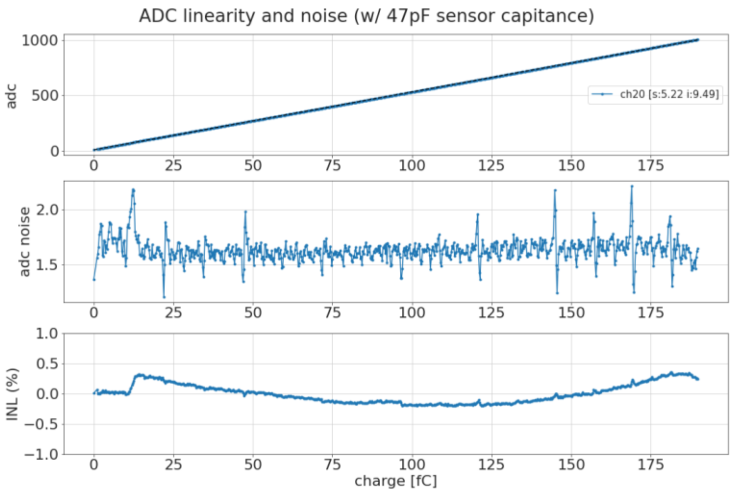
Ancillary blocks

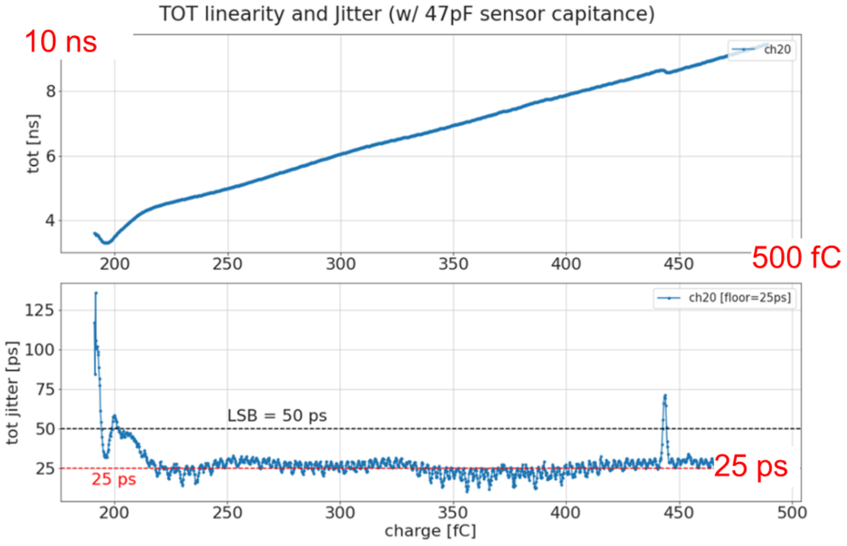
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

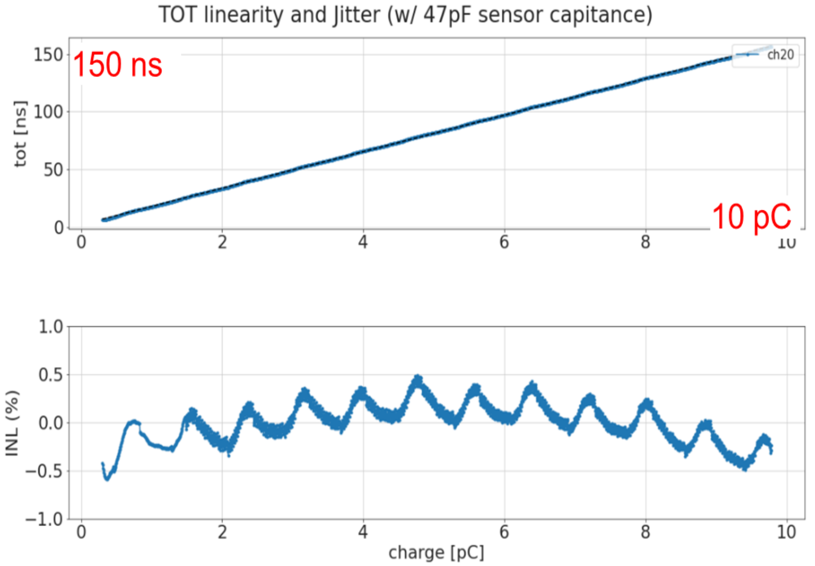


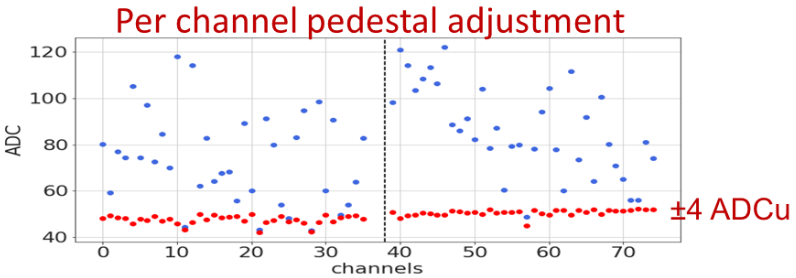


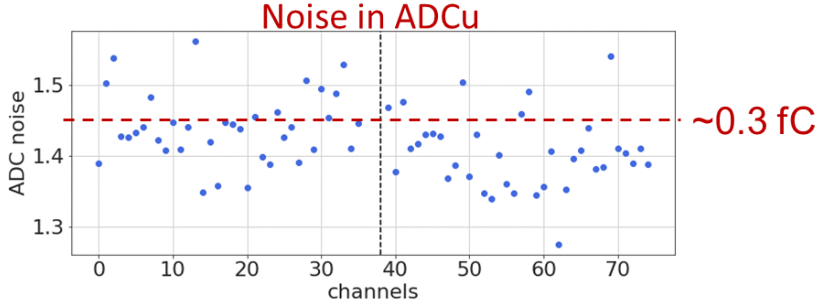
Performance

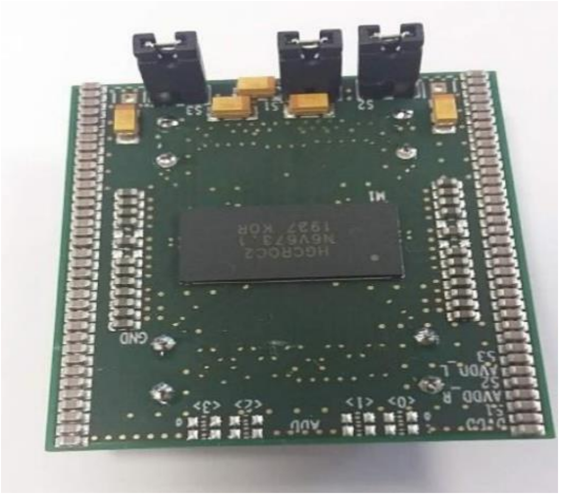


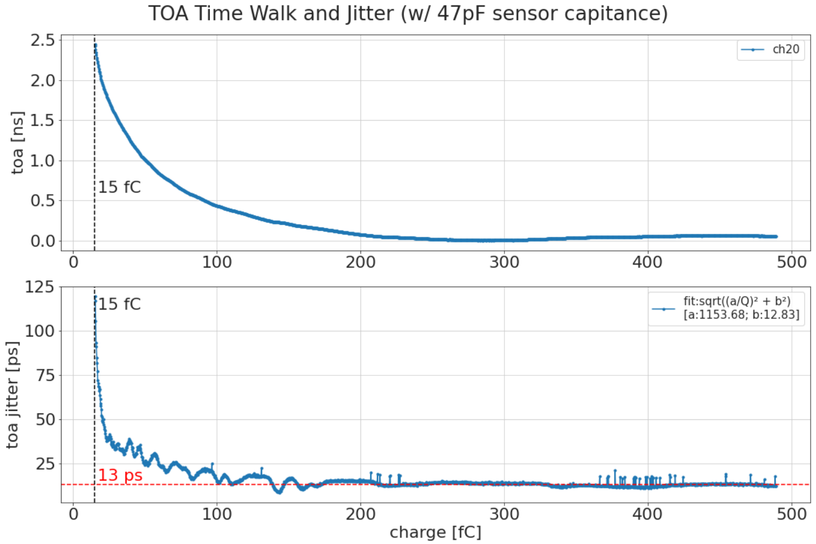






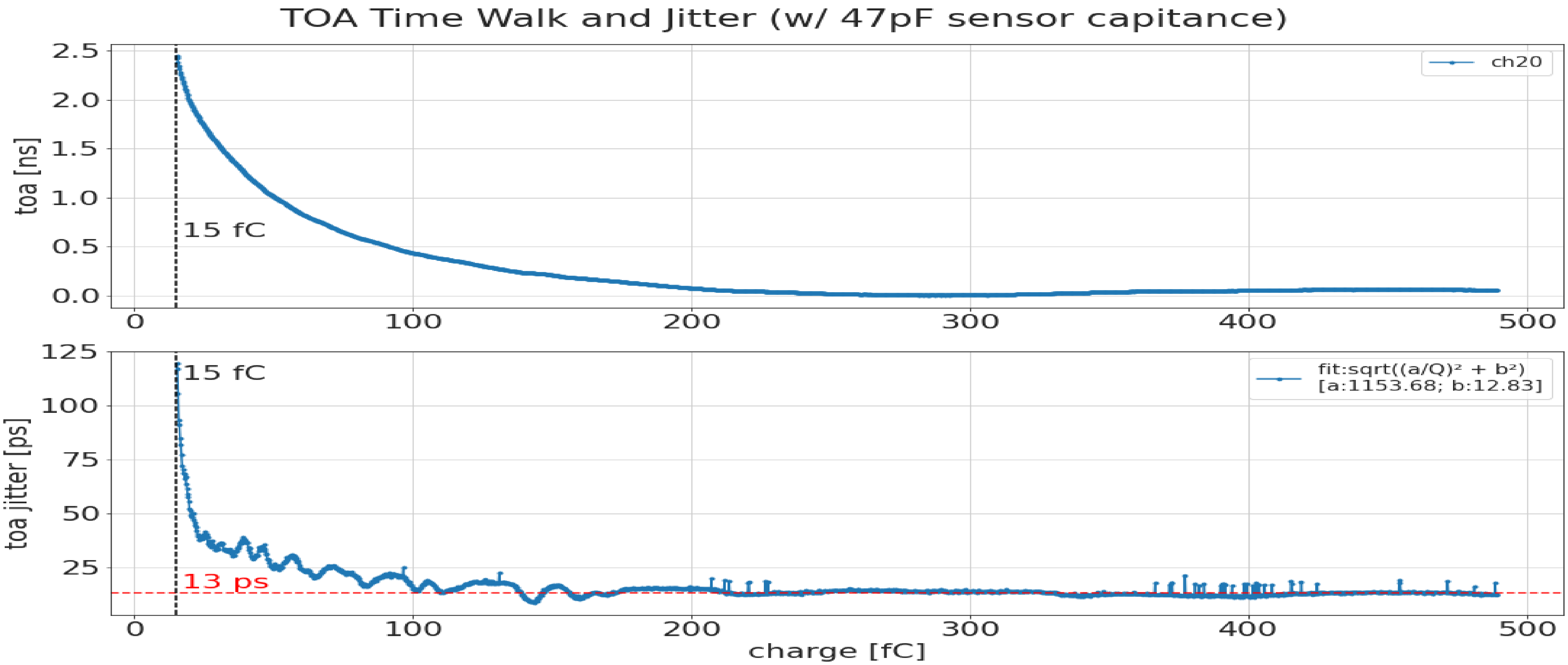






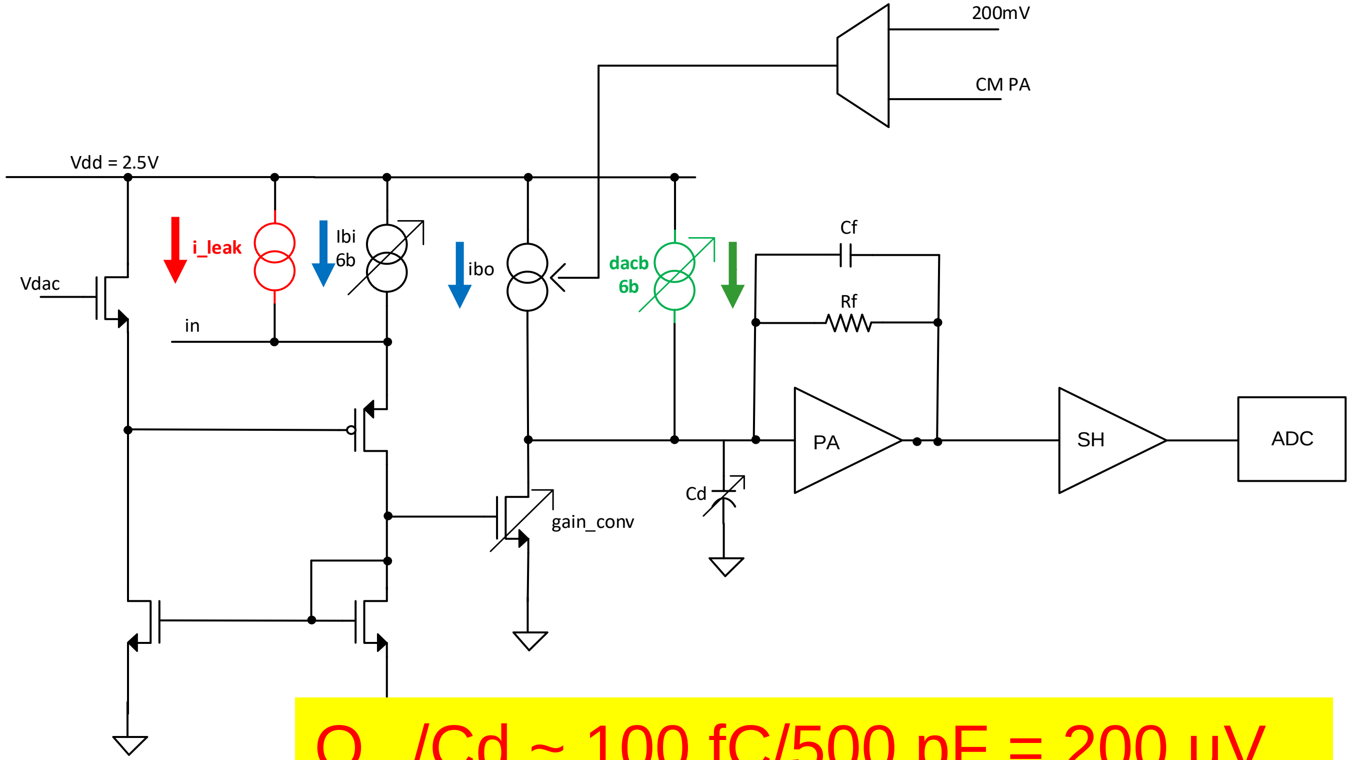
Zoom on timing

- ~2.5 ns time walk, 13 ps jitter for Q>100fC at Cd = 47 pF
- Fits also well MCPs for PID @EIC (HRPPD)

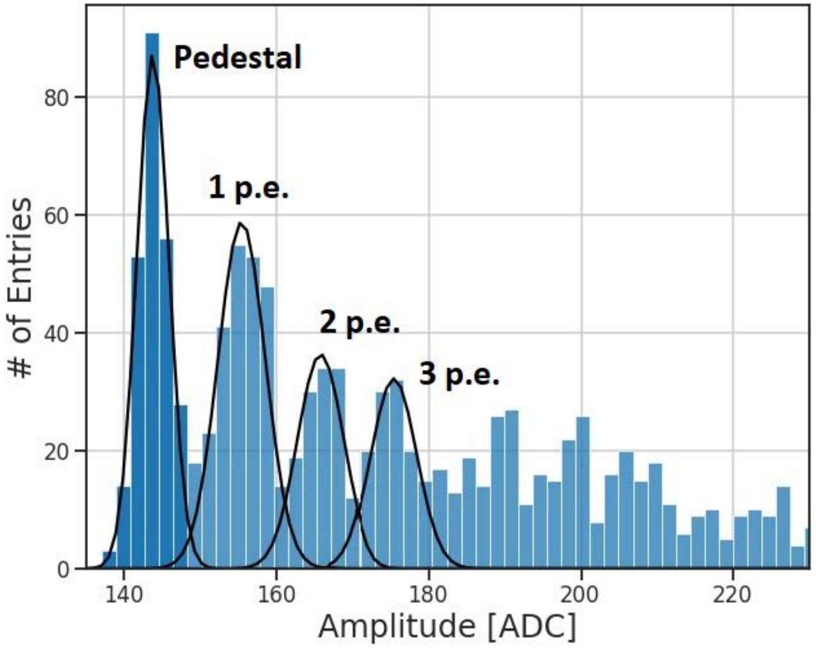


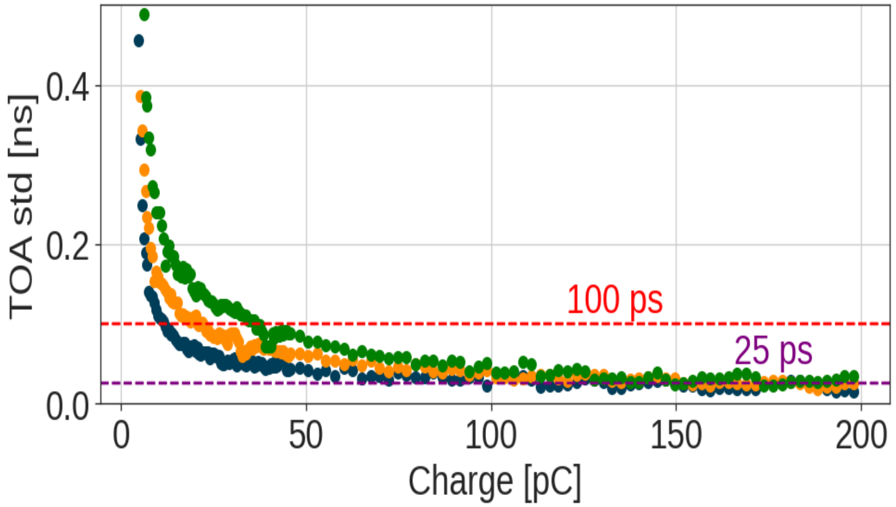
H2GCROC: SiPM version current conveyor

- **Current conveyor (Heidelberg design) to adapt to Si version**
- **Dynamic range : 50 fC – 300 pC**
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**
- **Measurements in backup slides**



$Q_{pe}/Cd \sim 100\ fC/500\ pF = 200\ \mu V$

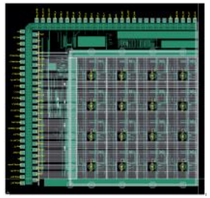


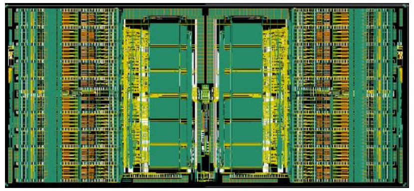


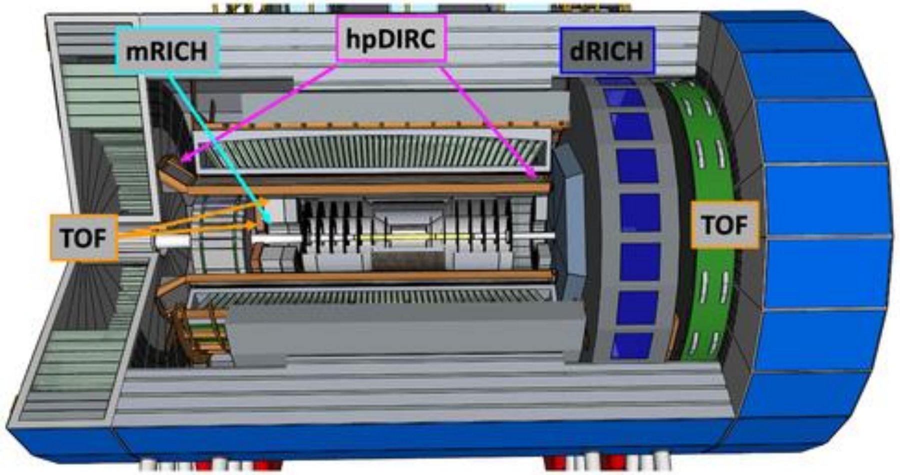
Chips for EIC : electron-ion collider at BNL

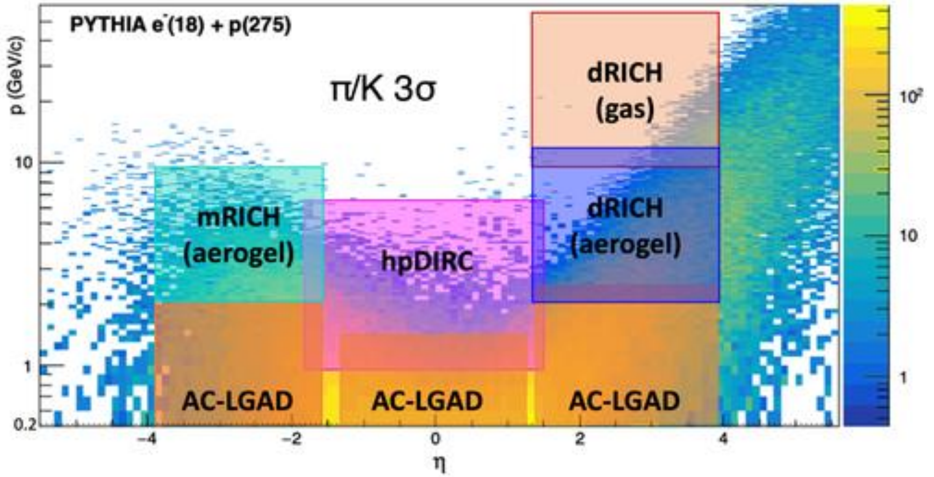
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - H(2)GCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA

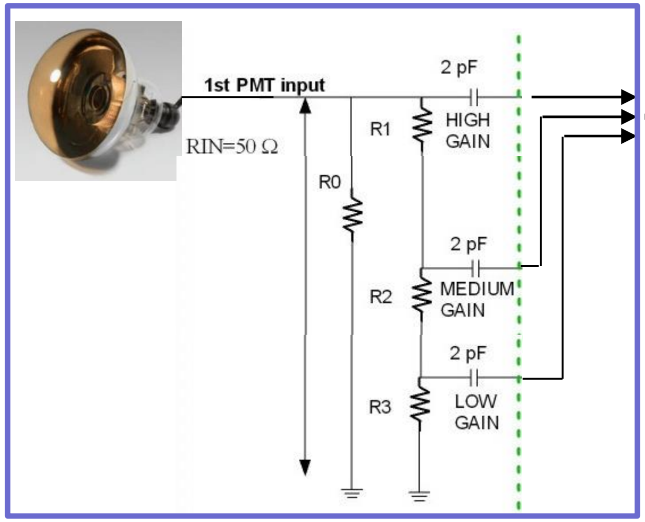


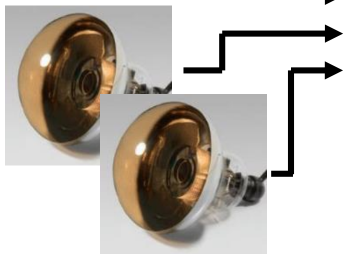


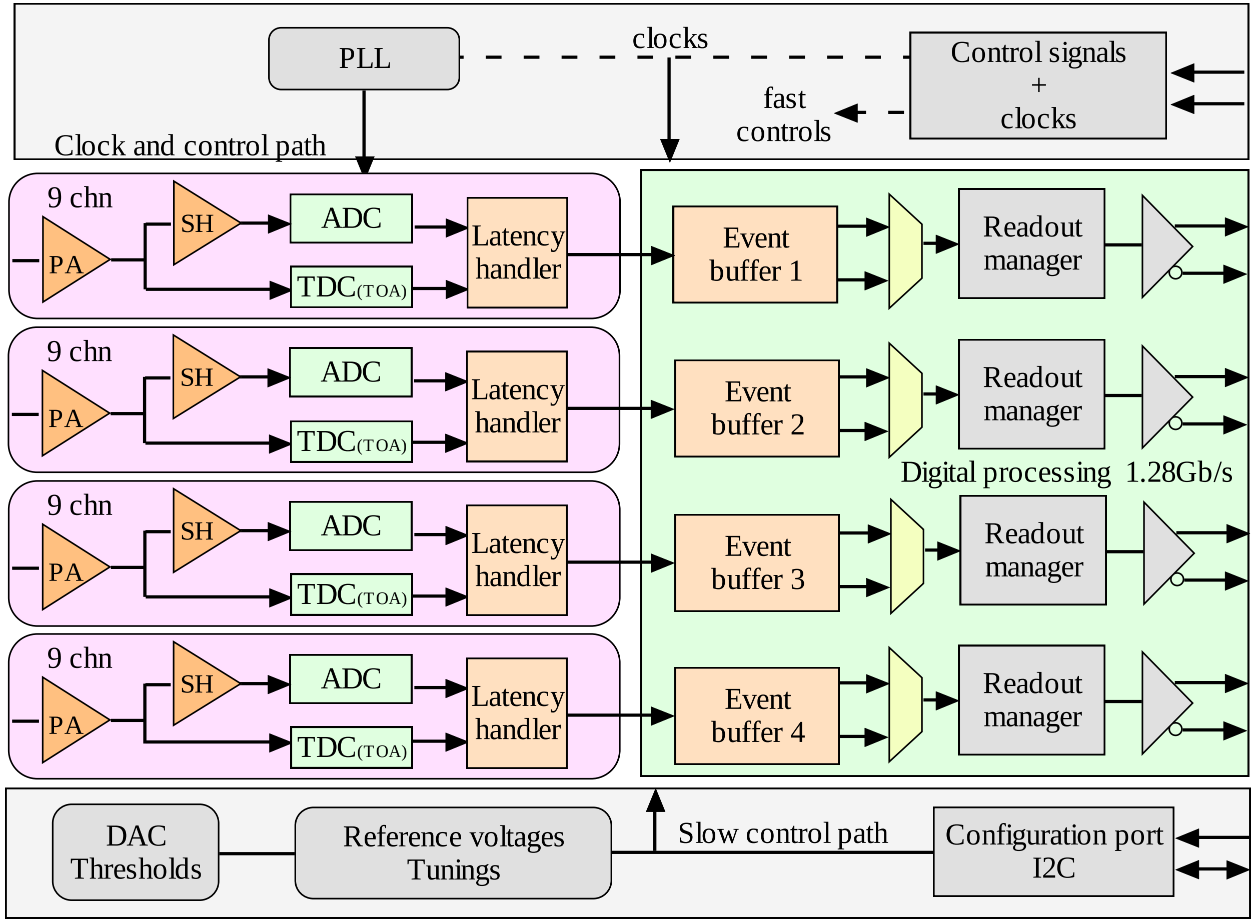




- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain

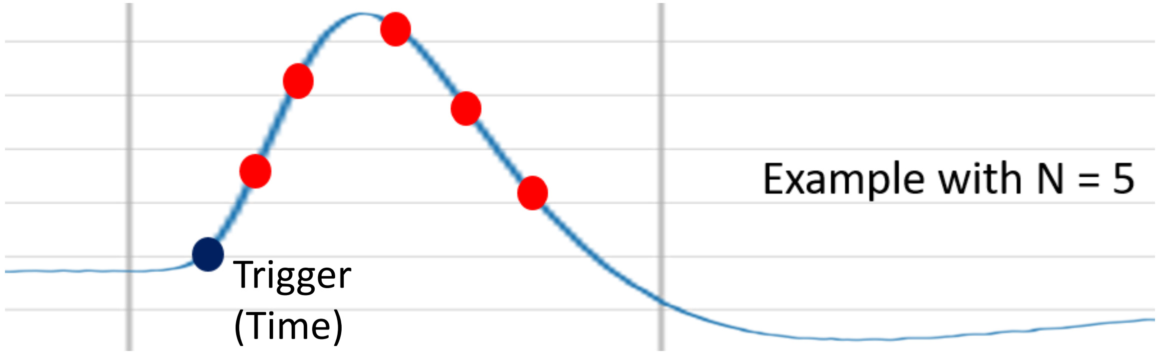




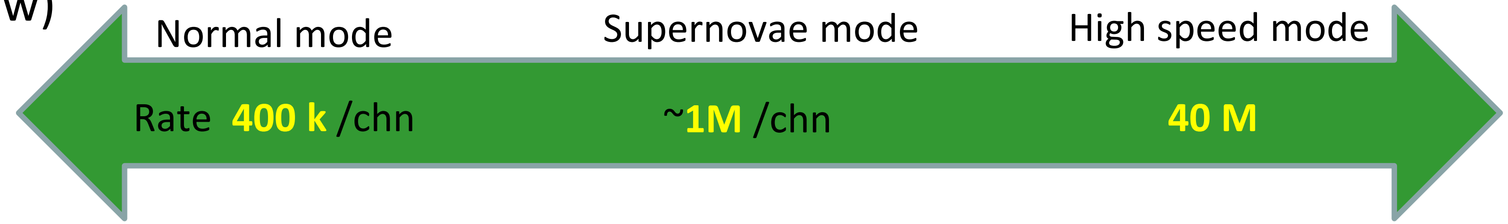


- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA
    - 5% resources of a modern XILINX FPGA



- When using 3 gains / PMT (high, medium, low)
  - Hit rate capability up to 400 kHz / PMT
  - Increased up to 1 MHz by focusing on high gain
    - Dynamic selectable by the user
  - Average values only limited by readout speed



- Measurements in backup slides

HKROC can accept consecutive events (separated by ~30 ns)

Internal HKROC memory writing is without dead time

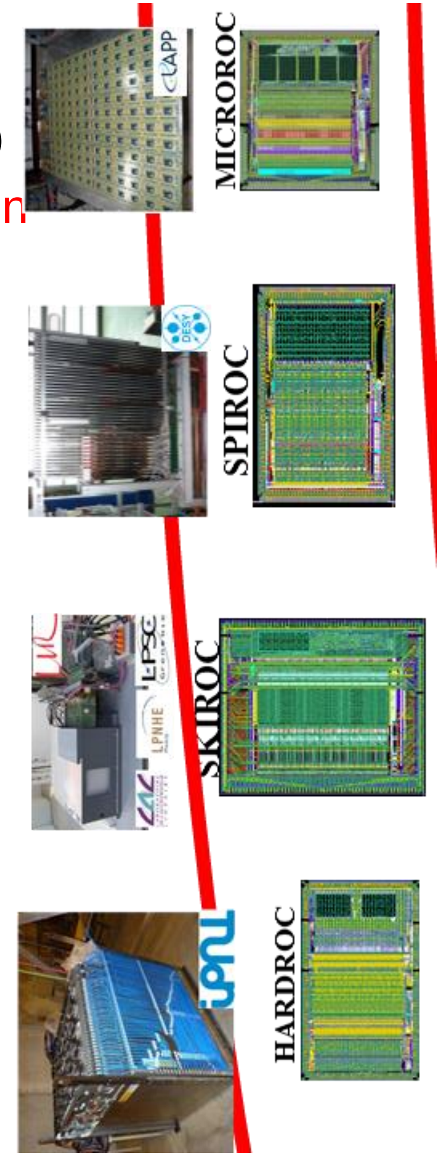
Readout speed is only limited by serial link bandwidth (average values above)

DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL



CALOROC1 (2024)

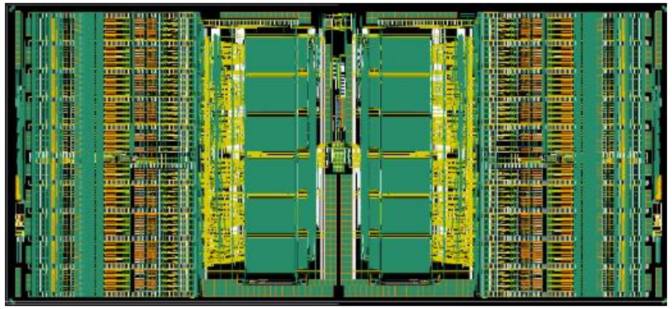
- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

- Channel number tbd : 32 (HKROC) or 64 (HGCROC)

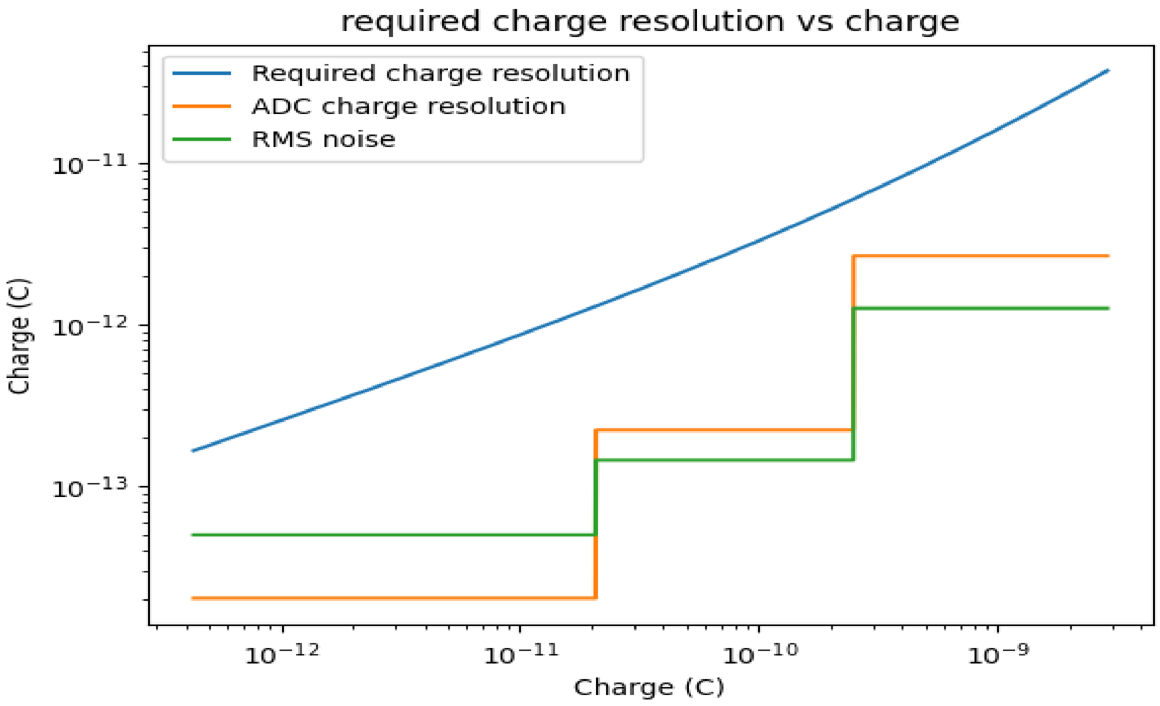
- Could fit FCC SiPM calorimeters
- A Si version would fit FCC Si calorimeter

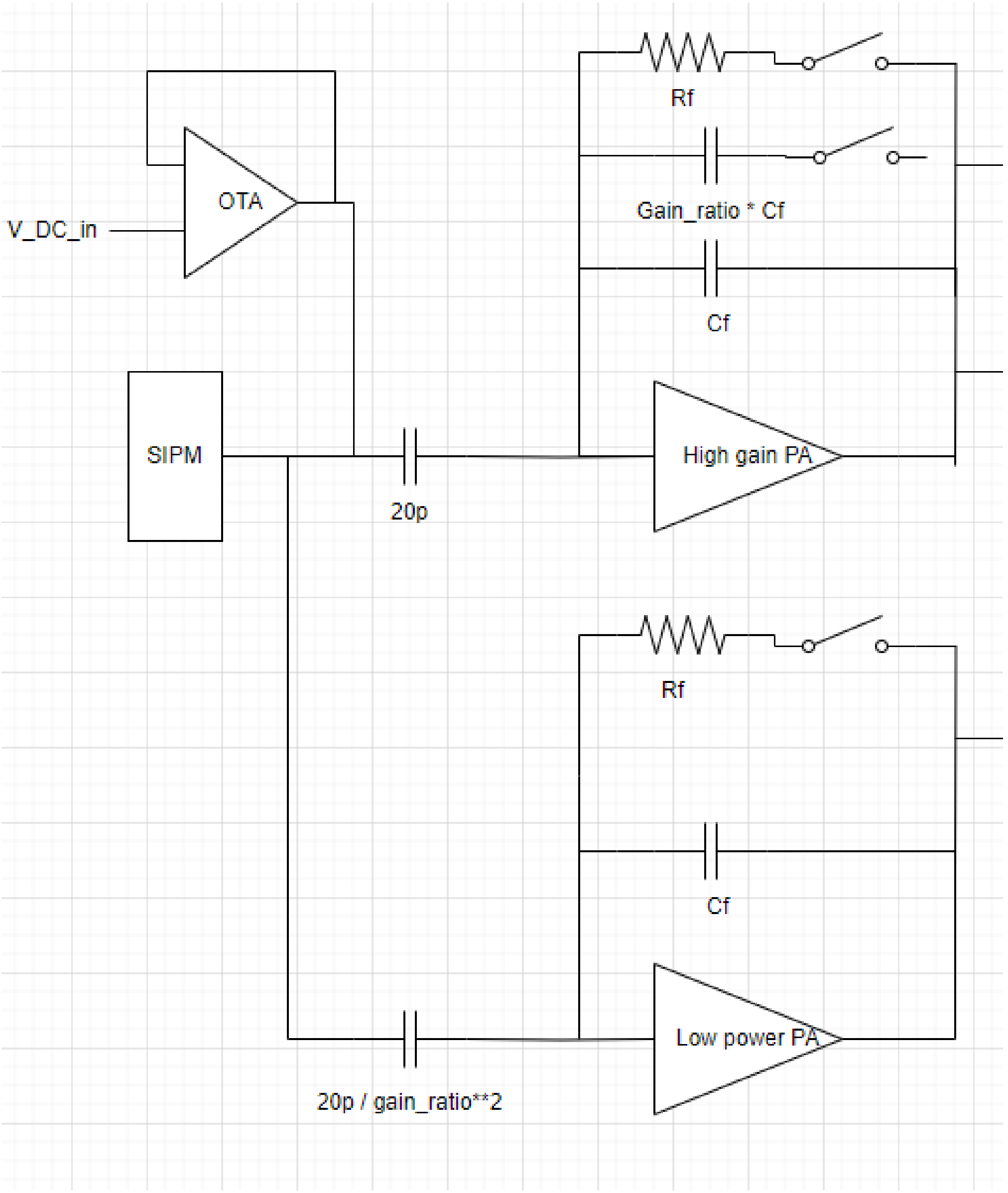
HKROC



CALOROC1A (also 2024)

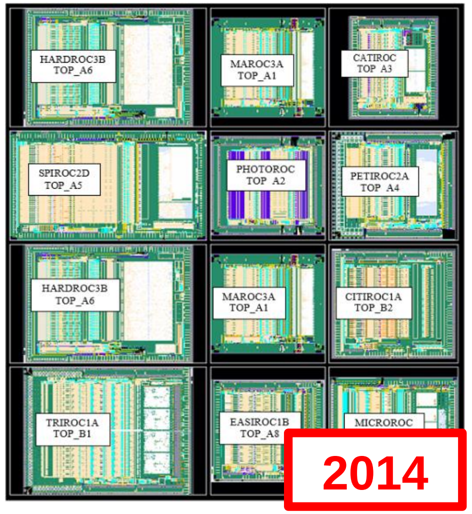
- Variant with new analog part
- Dynamic gain switching
- Study of current conveyor and voltage amplifiers « à la spiroc »
- Study low power ADCs (clock gating)
- Will fit (most) FCC needs

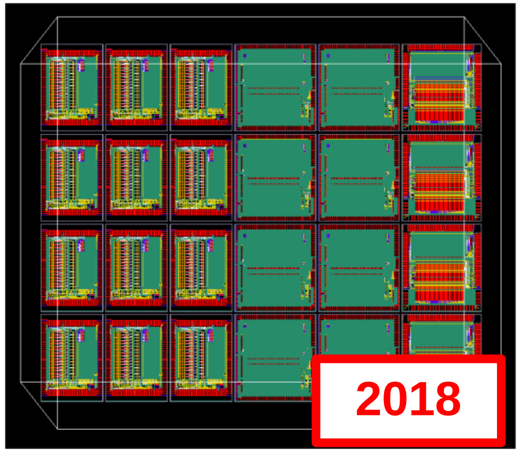


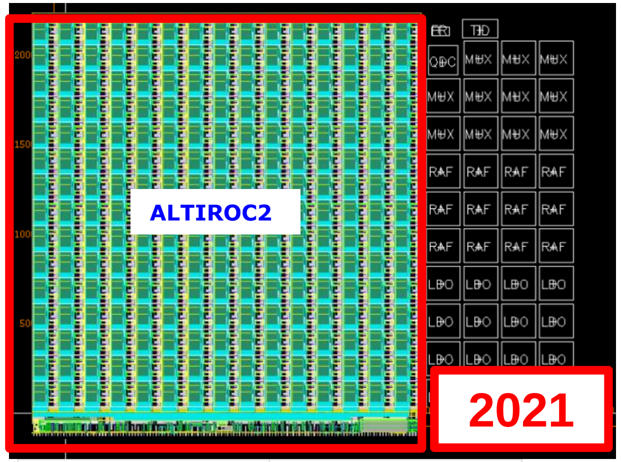


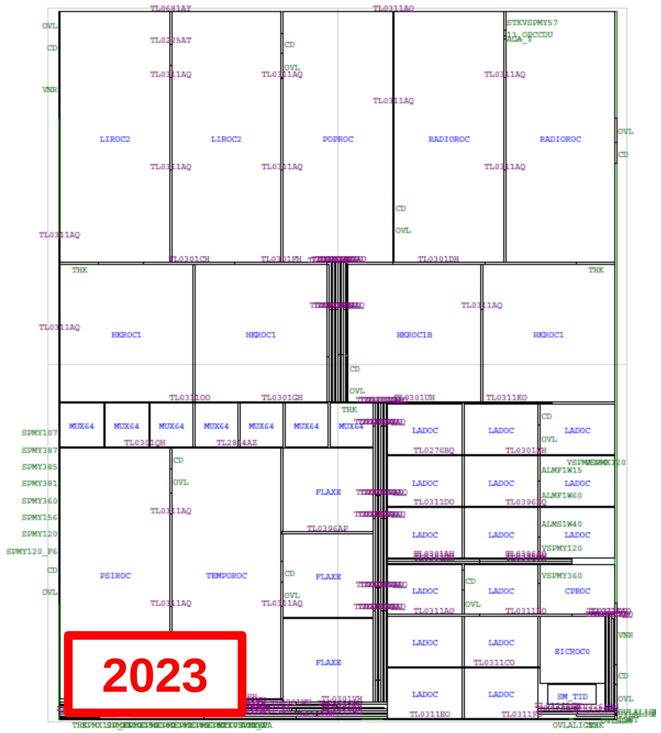
OMEGA Engineering runs

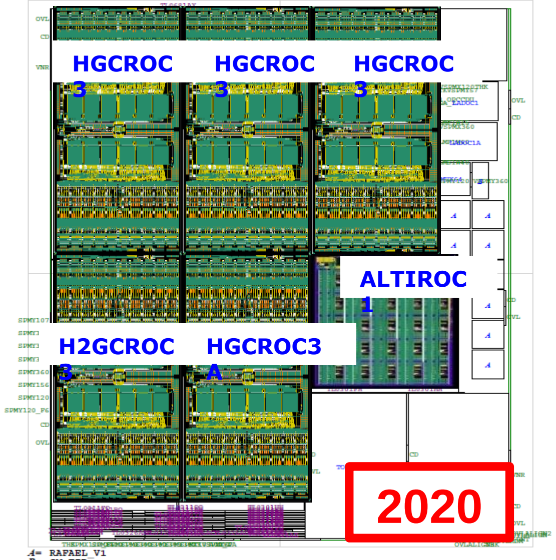
- 8 engineering runs in 9 years !
  - AMS SiGe 0,35um 2014, 2016, 2018
  - TSMc 130nm : 2019, 2020, 2021, 2x2023
  - Cost : 200-300 k€, shared between projects

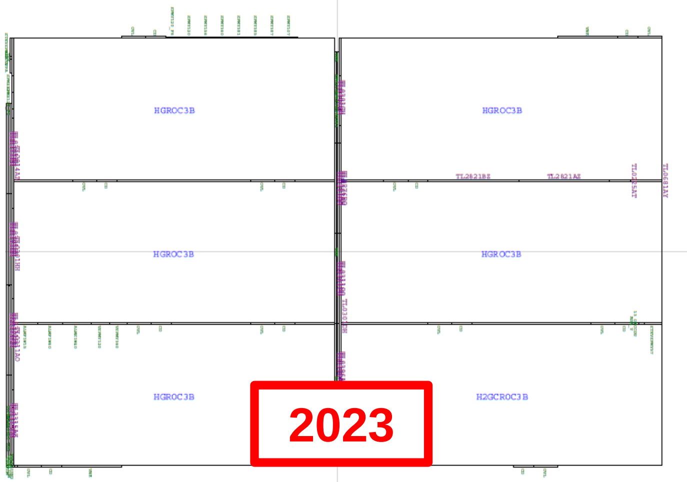






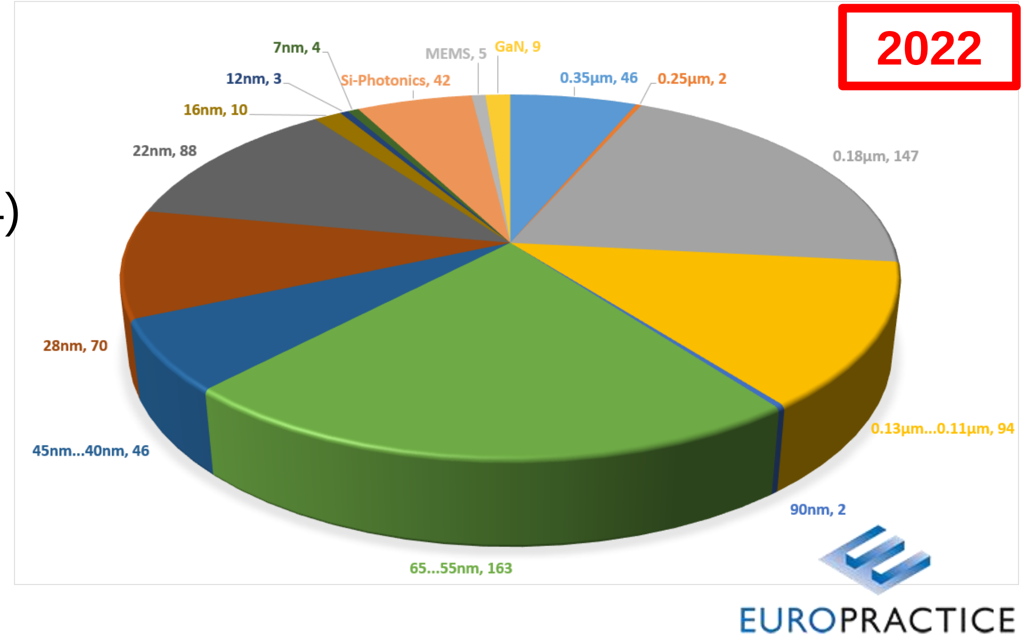


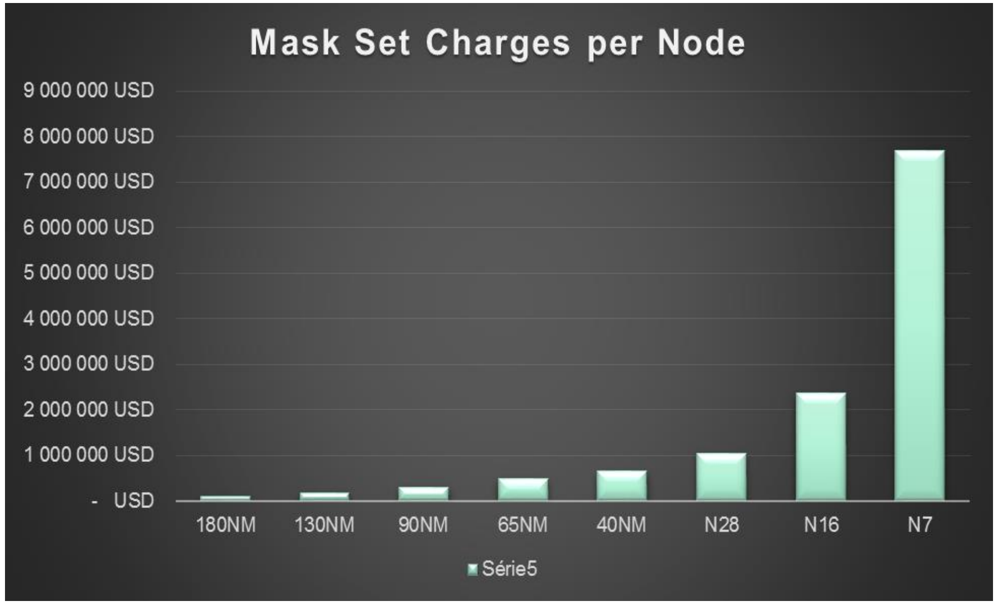




Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?
- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run



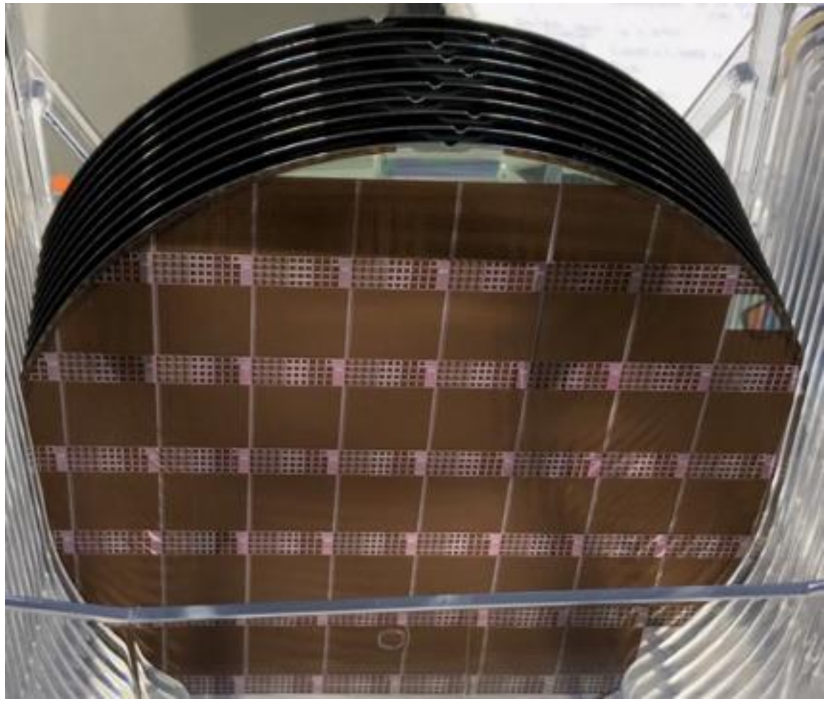


conclusion

- Importance of joint optimization detector/readout electronics

- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)

- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O



- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing : CALOROC1 and 1A
  - Mid 2024
  - Further R&D needed to bring power down to ~1 mW/ch (Lar)

- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

backup

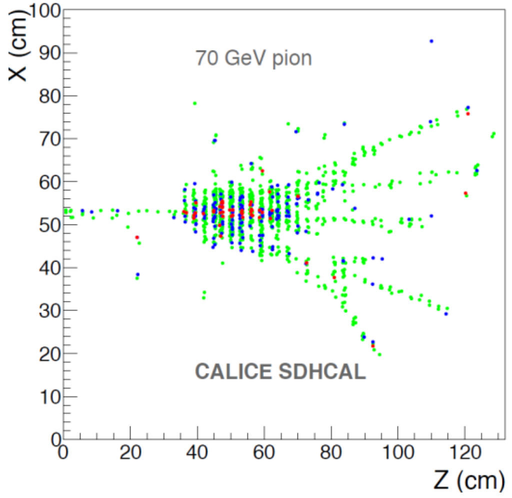
DRD6 (calorimetry) readout schemes

Omega

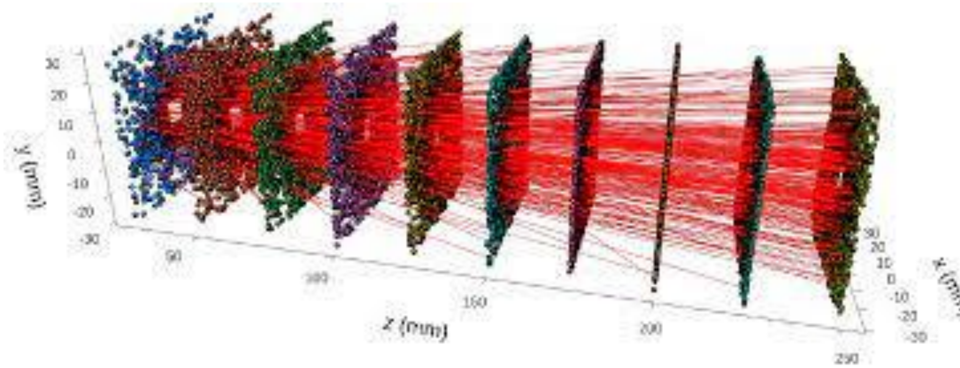
Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added



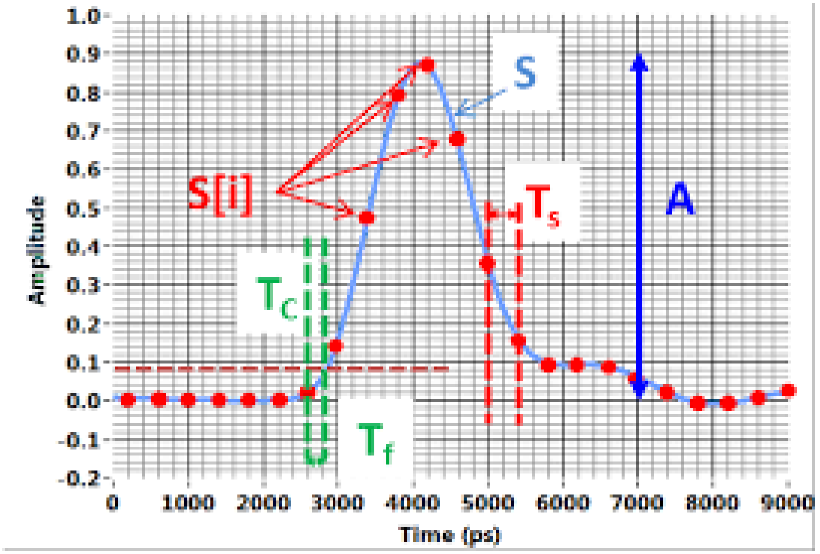
- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

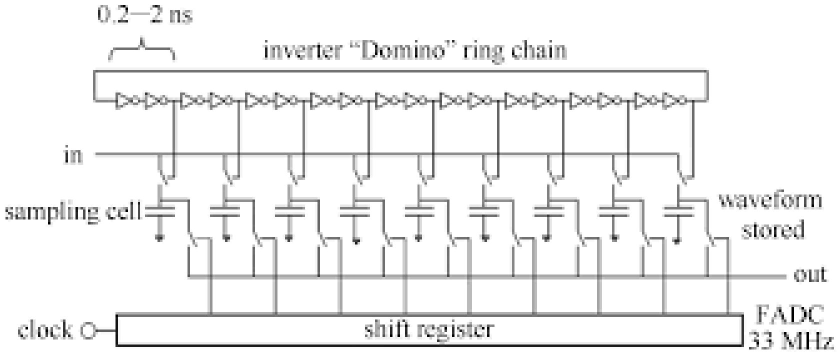


Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SAMPIC…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade





HKROC0 specifications

Min requirements	
Discriminator **threshold**	**1/6 p.e.** (**0.33 pC**)
Charge linearity	1% for 1 p.e. to **1250 p.e.** (**2 pC to 2500 pC**)
Charge resolution	**0.1 p.e. for < 10 p.e.** (**0.2 pC** for Q< 20 pC) **Better than 1% for >10 p.e.** (1% for 20 pc)
Maximum **hit rate**	**1 MHz/ch** **For close Supernova**
Timing resolution	**300 ps for 1 p.e.**(2 pc) **200 ps for > 6 p.e.** (12 pC)

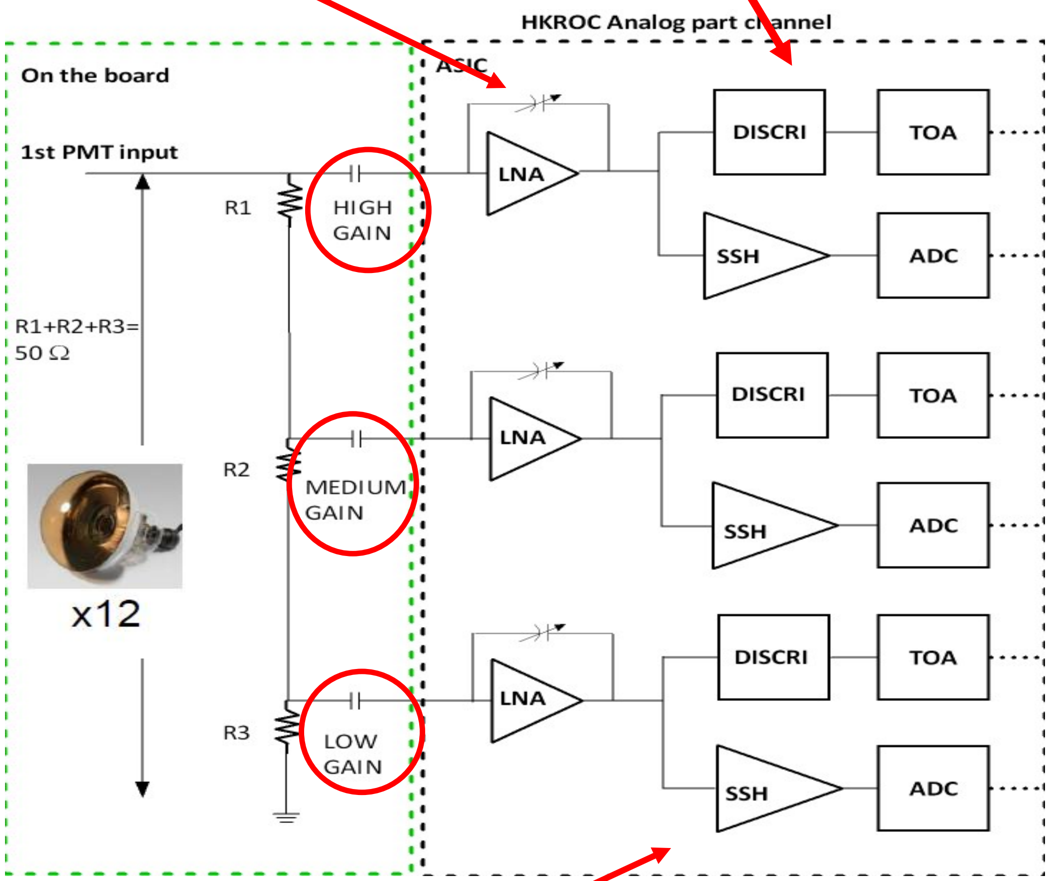
To extend the charge dynamic range:

1 PMT channel connected

to **3 HKROC channels**

Low Noise PA
With variable gain

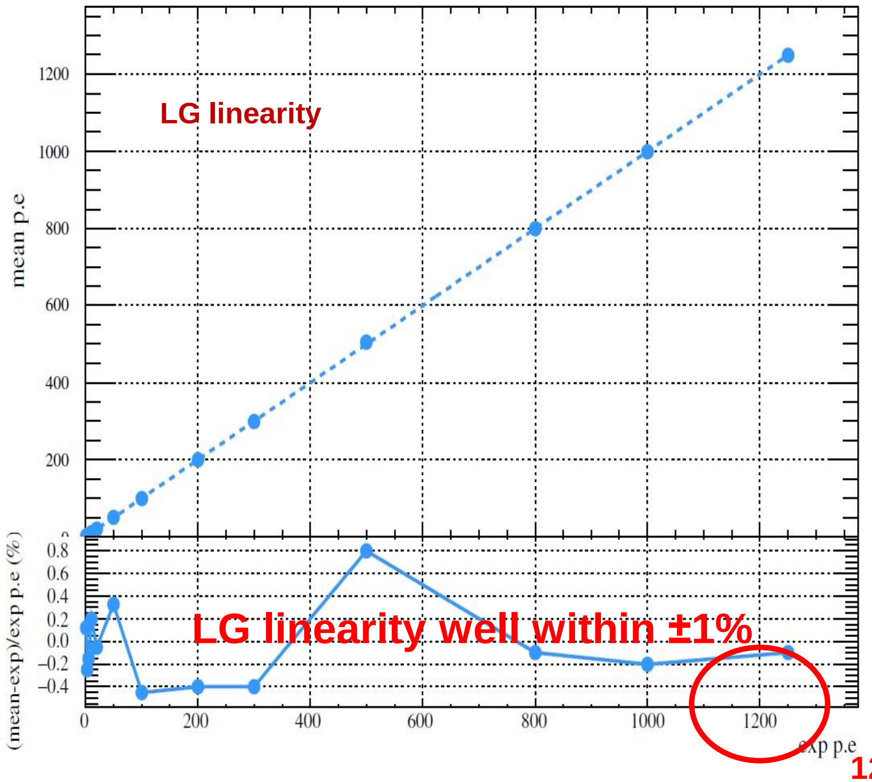
Trigger and Time path
10-bits TDC

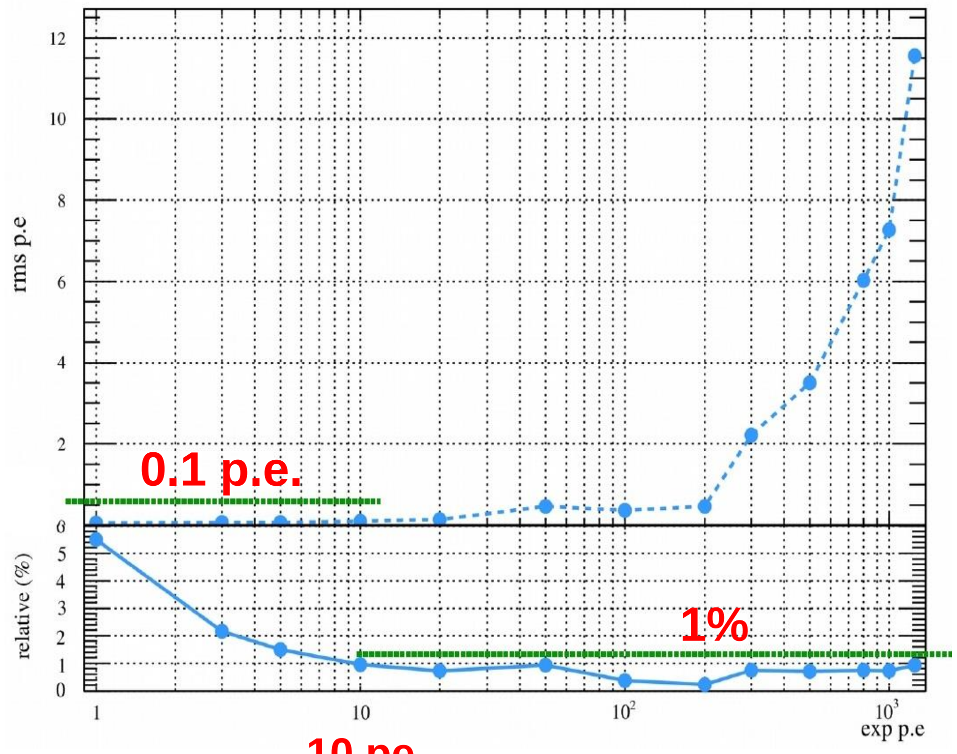


Charge path
Slow shaper with variable shaping time and gain
SAR 10-bits ADC

HKROC0 Charge measurements

The **whole** acquisition **chain** is tested:
The signal is **amplified**, **auto-triggered** and **converted** by the internal **ADC**.





HG, MG and LG tested!!

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

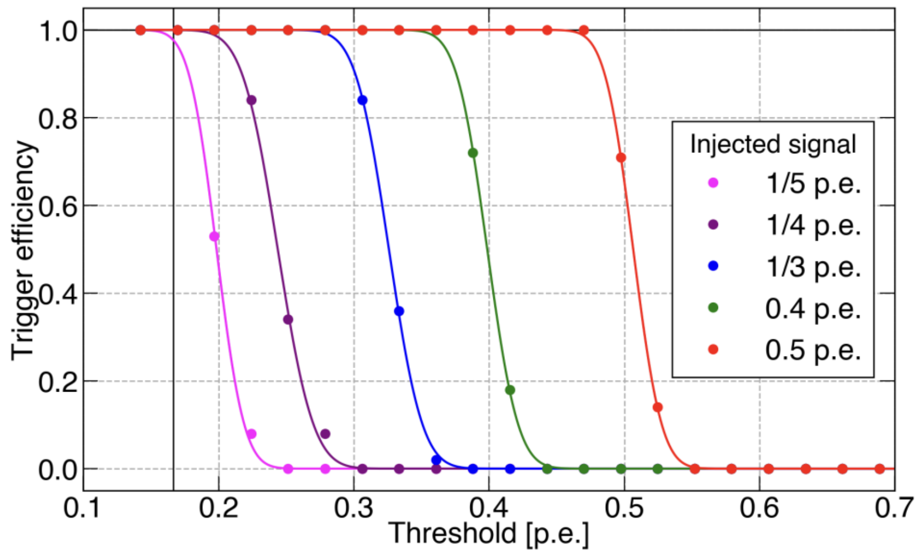
Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

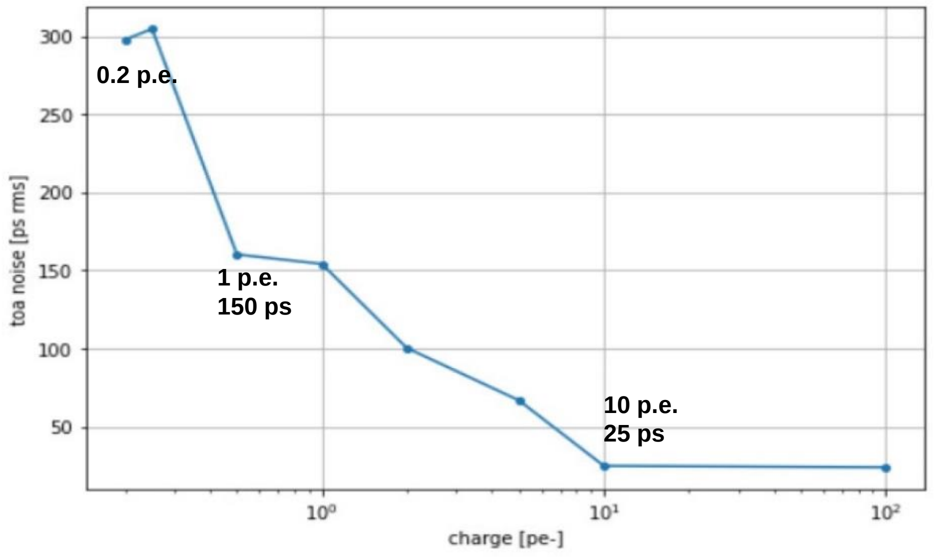
HKROC0 Trigger measurements

The HyperK specifications require the trigger **threshold** to be set at **1/6 p.e (330 fC)**



- **Hit efficiency : 90 % for 1/5 p.e events (400fC)**

  ~100 % if ≥ 1/4 p.e
- Extracted **threshold** value corresponding at **1/6 p.e**
- **Very low noise** : < 1 Hz **(0 noise hit in 10s @ 1/6 of p.e.)**



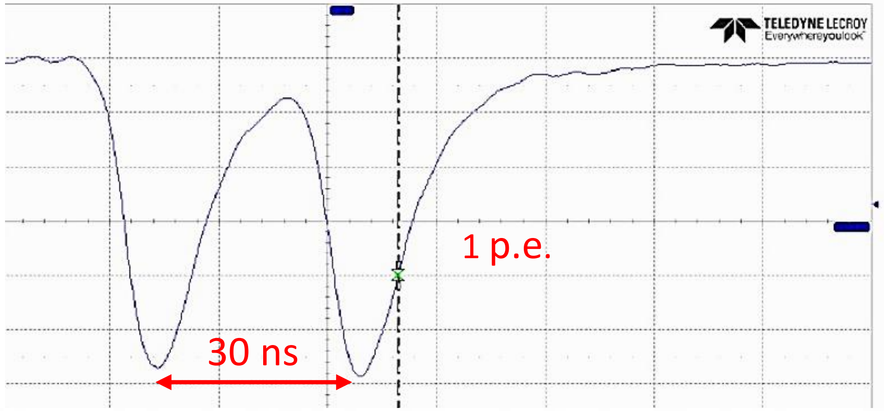
TDC characterization with **1/6 p.e. threshold**

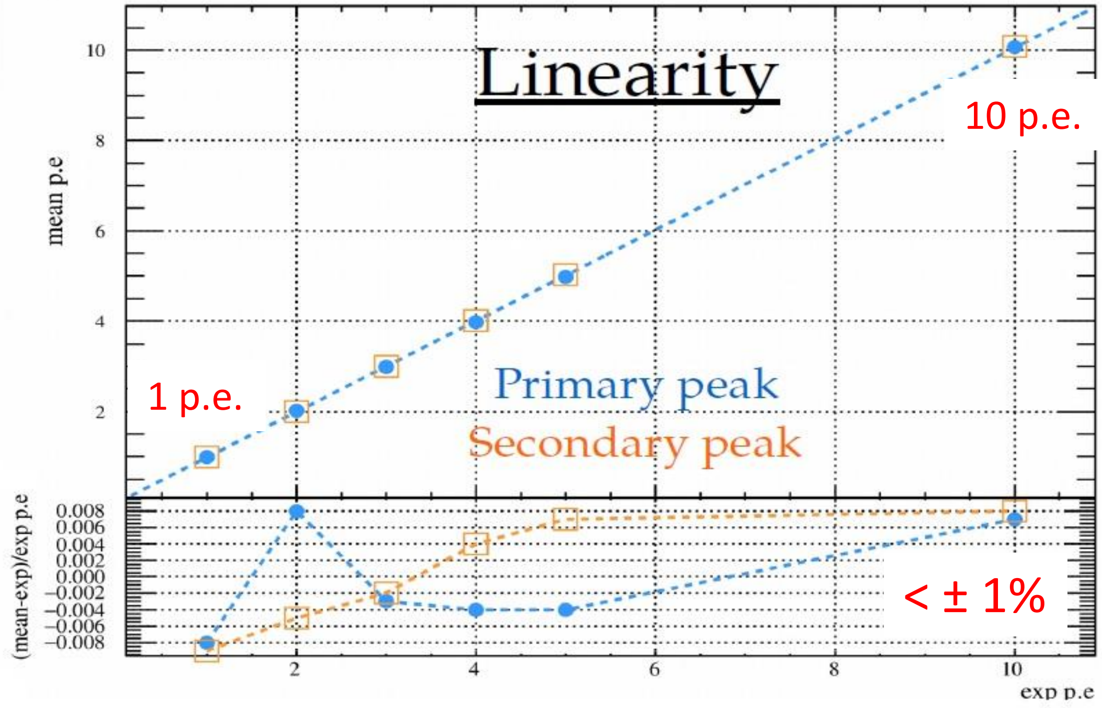
TDC resolution :

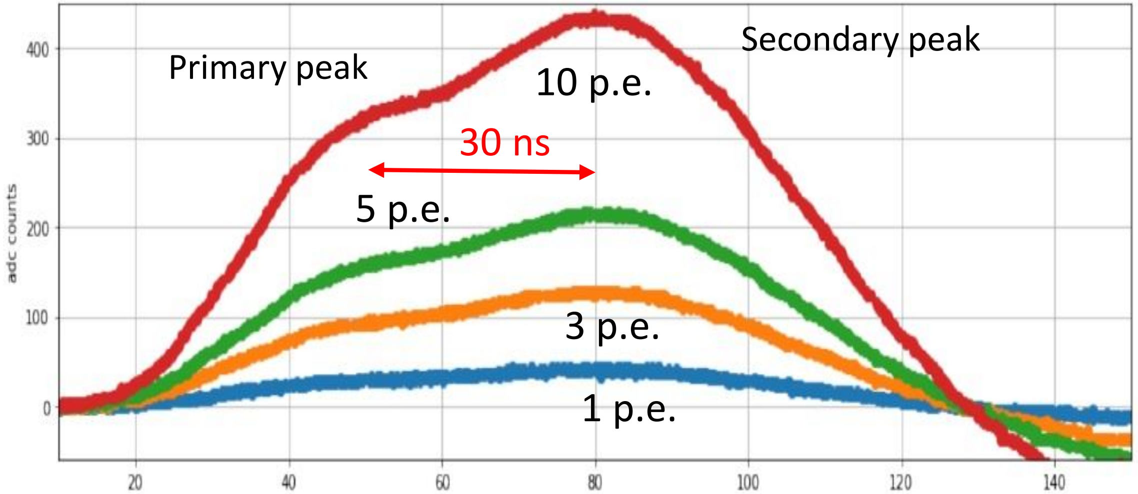
150 ps rms @ 1 p.e [300 ps required]

≤ 25 ps rms @ 10 p.e [200 ps required]

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)







Internal signal after slow shaping

Charge reconstruction algorithm of the two peaks

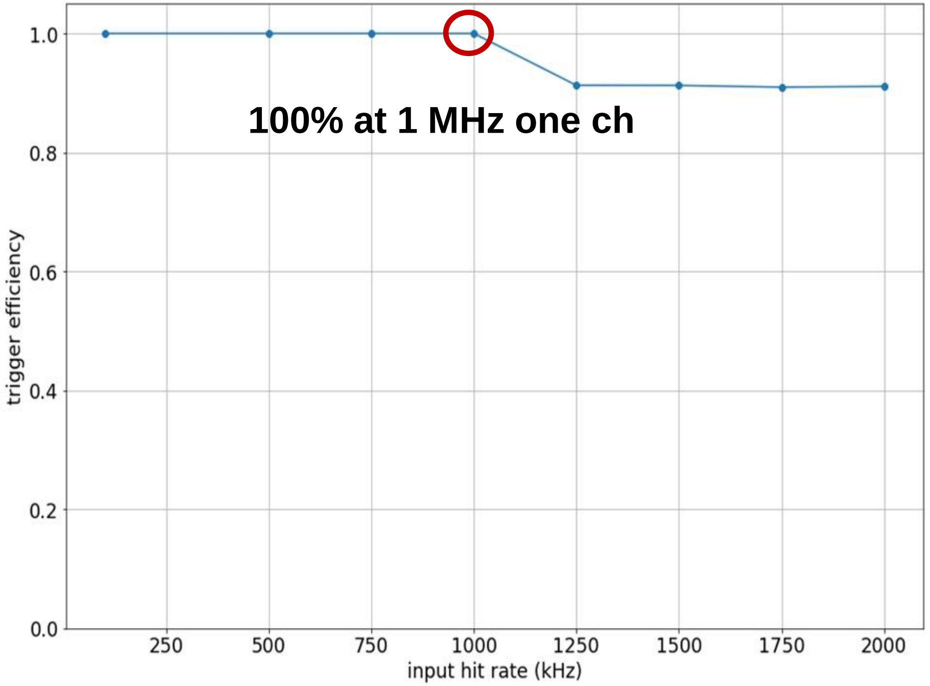
Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

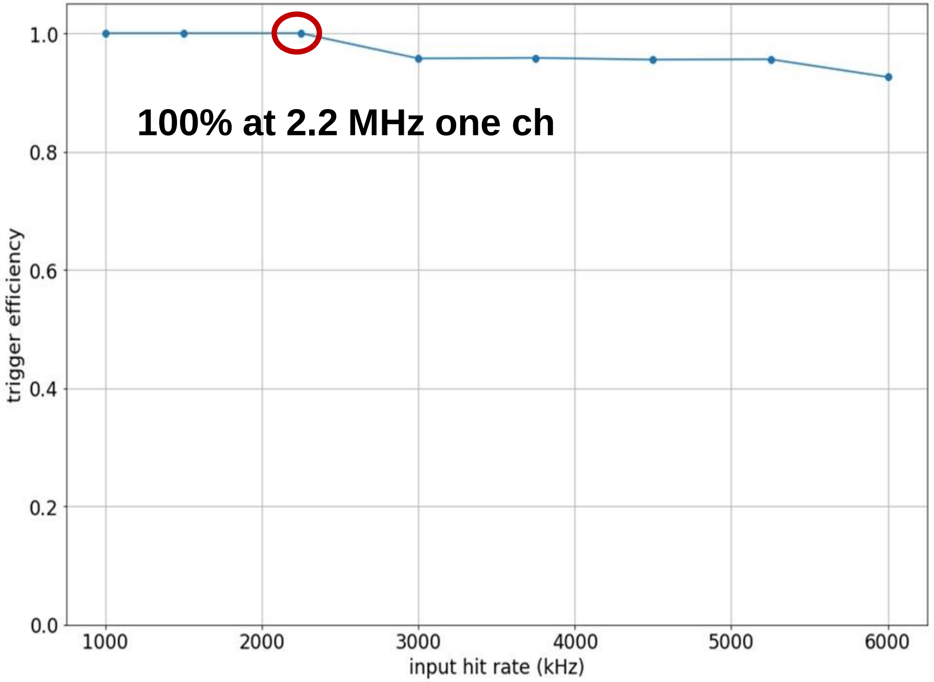
HKROC Trigger rate measurements

FAST hit rate (~ 1MHz) required for close Supernova signals (~ 1 p.e.)

Normal mode:



Super Nova mode



1 PMT channel →

3 HKROC channels tested in Normal Mode:

100% Trigger efficiency up to **415 kHz 3 chs**

1 PMT channel →

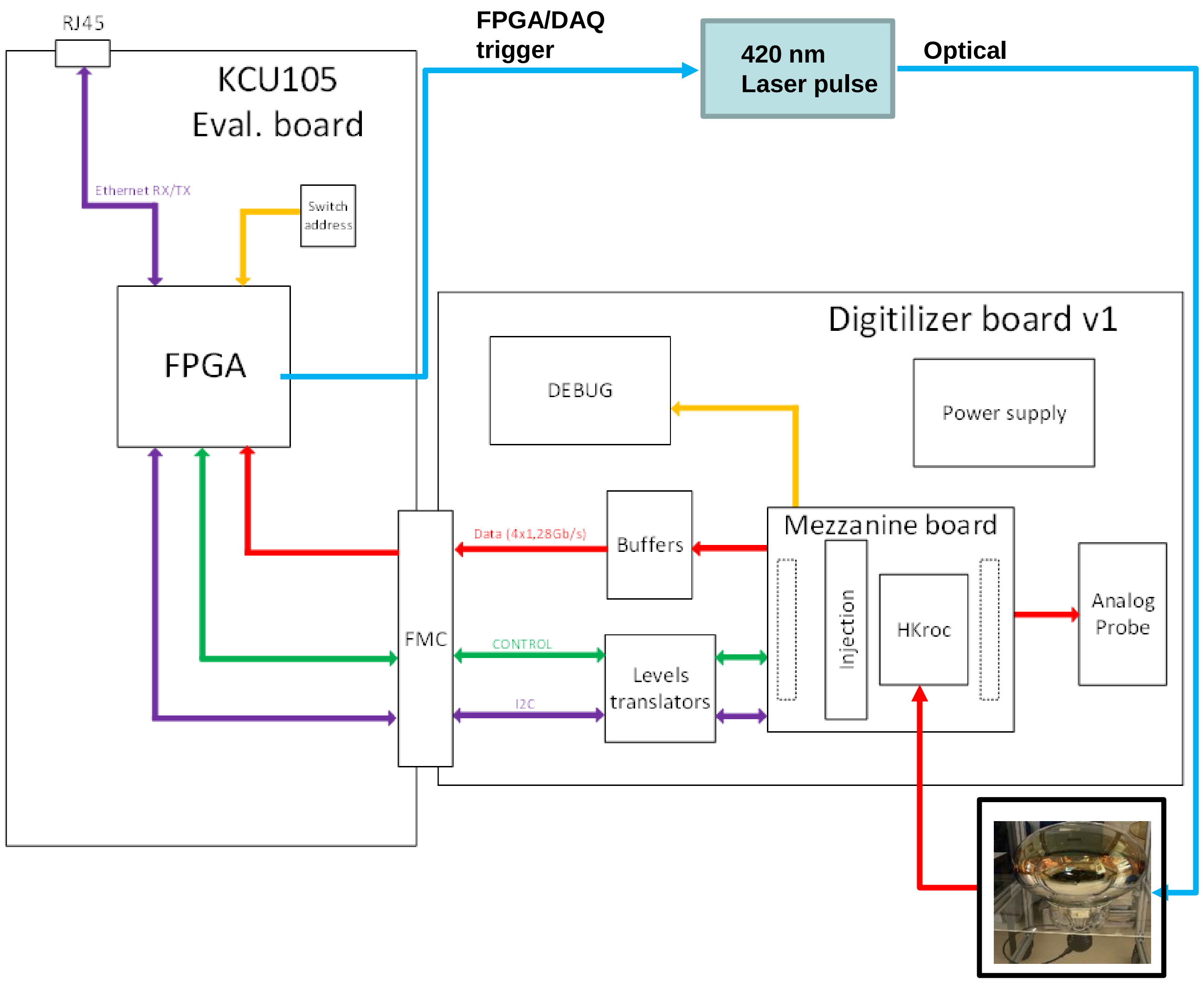
3 HKROC channels tested in SuperNova Mode:

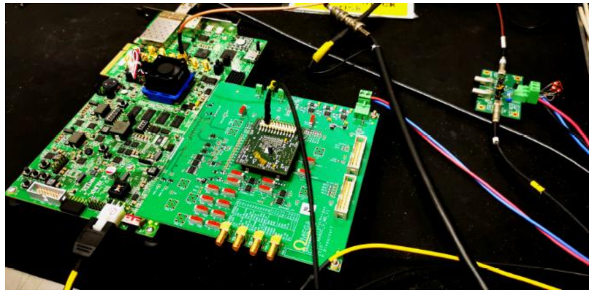
100% Trigger efficiency up to **950 kHz 3 chs**

The HKROC saturation naturally appears when the chip internal memory is full. The chip has one independent memory for each read-out link at 1.28 Gb/s, which gather 3 PMTs.

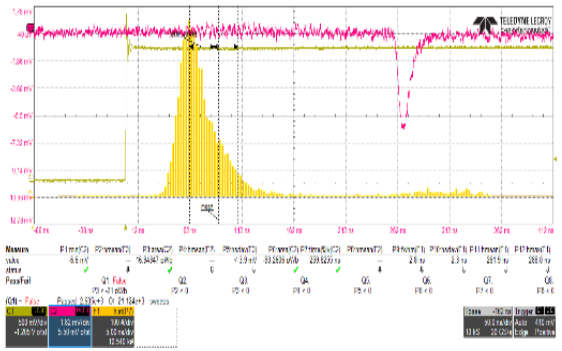
PMT testbench

Connected Hamamatsu R12680 PMT to HKROC illuminated by a PILAS 402 nm laser diode





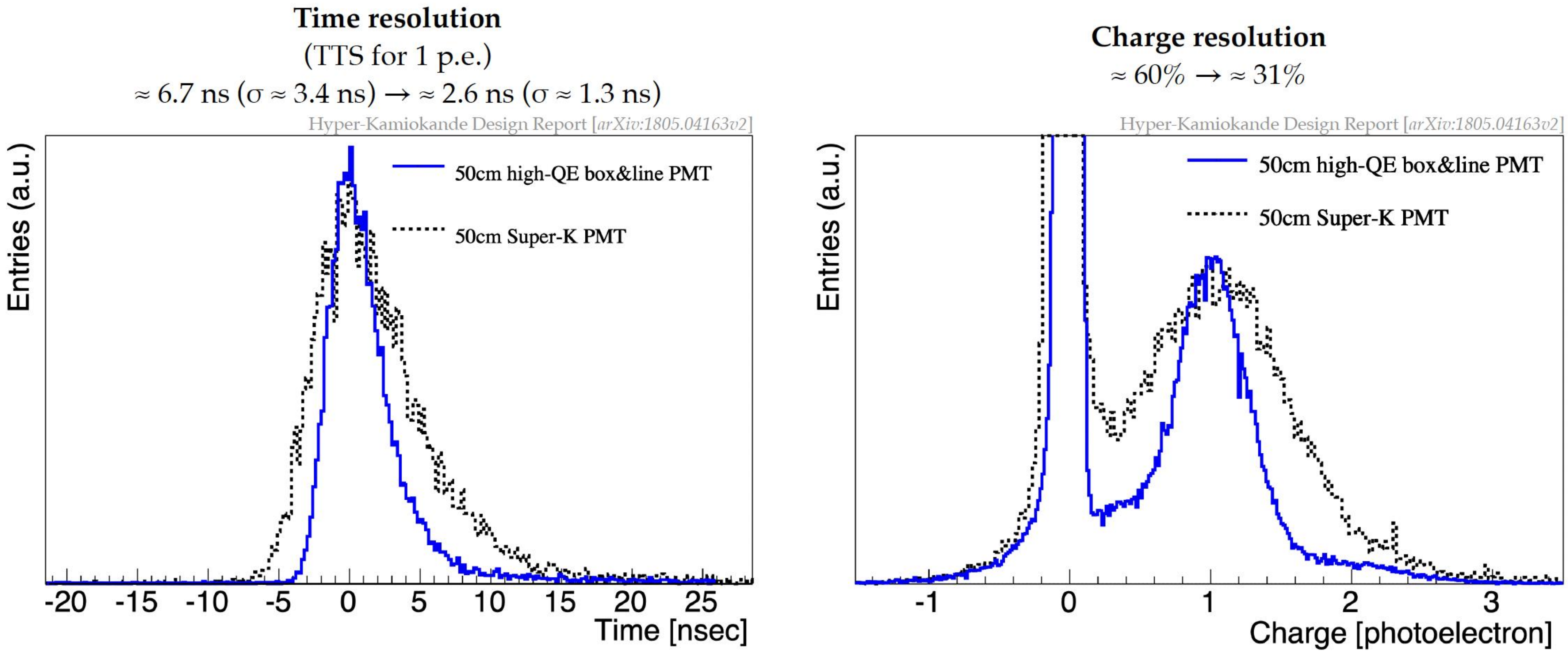
- PMT HV set to have the 1 p.e peak amplitude at -6 mV
- Charge calibrated
- TTS : FWHM= 2.8 ns, σ= 1.2 ns



PMT measurements

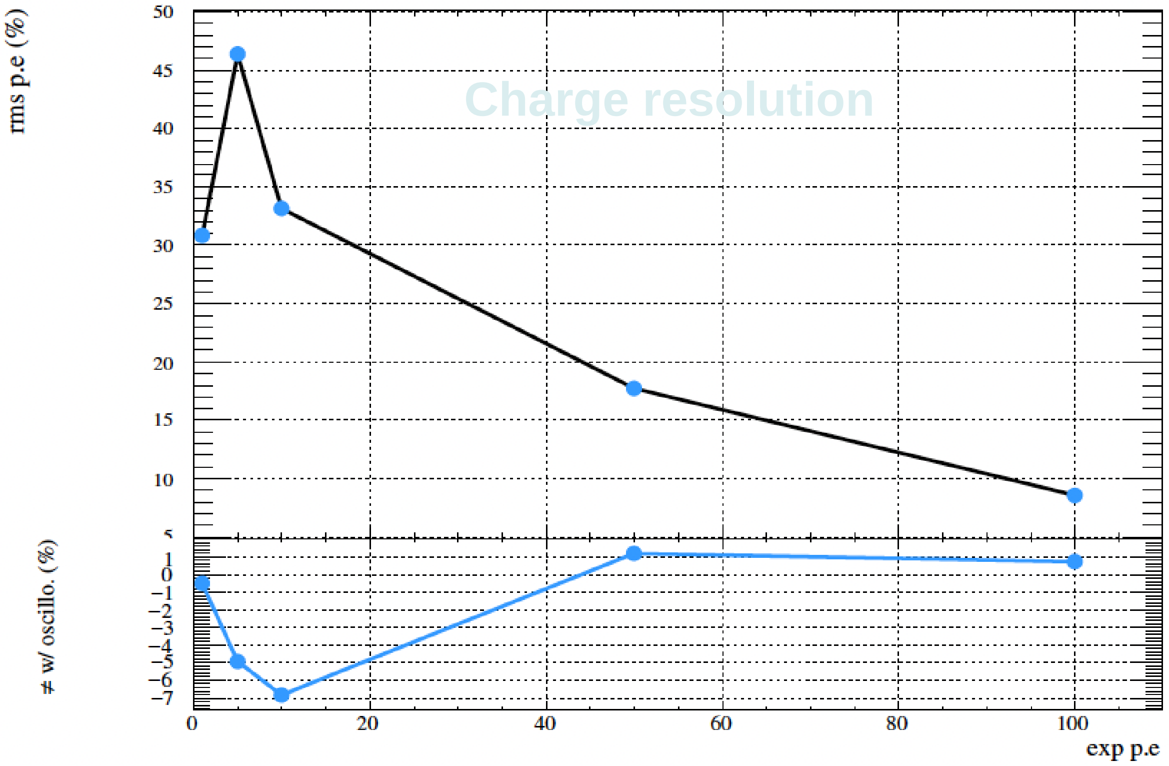
Trigger time distribution for events having charge ≤ 1.5 p.e : FWHM of **2.6 ns**

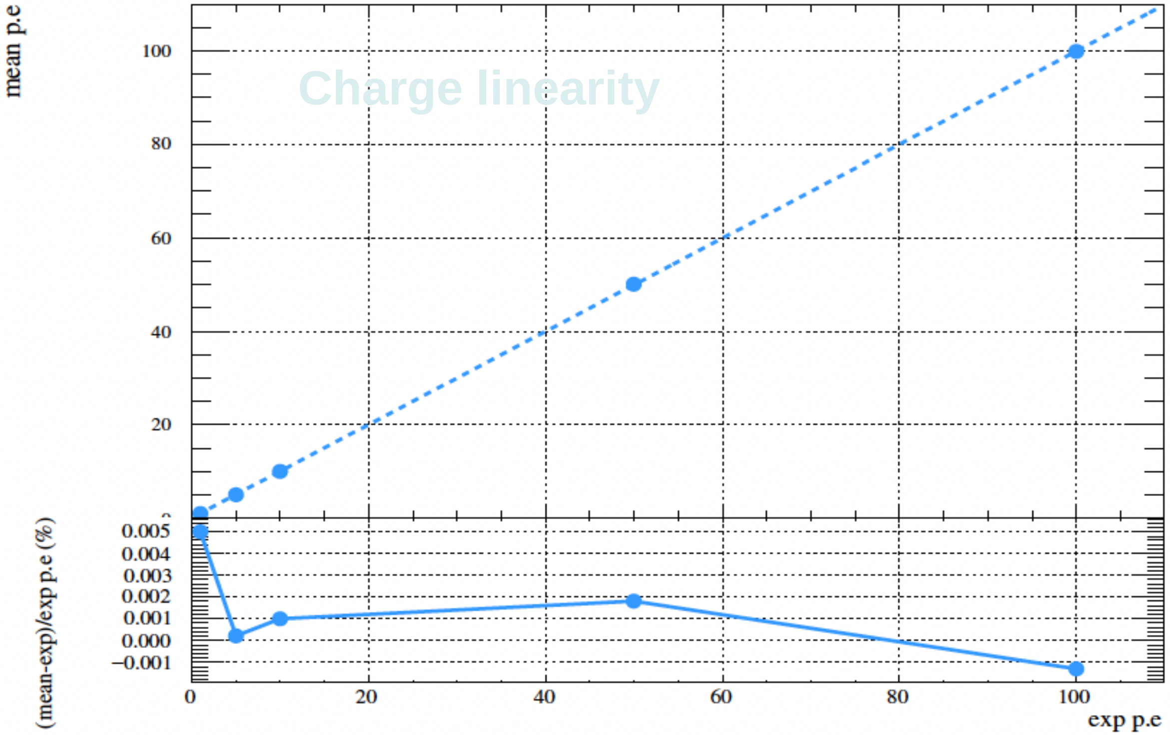
- **Excellent agreement with the 2.8 ns found for the PMT only**
- Digitizer does not degrade the PMT time resolution !



PMT measurements

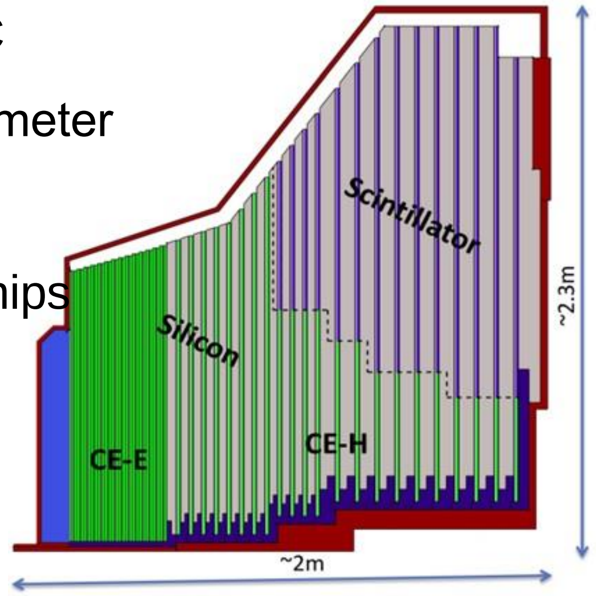
- Charge linearity and resolution
  - Similar with PMT as with pulse generator



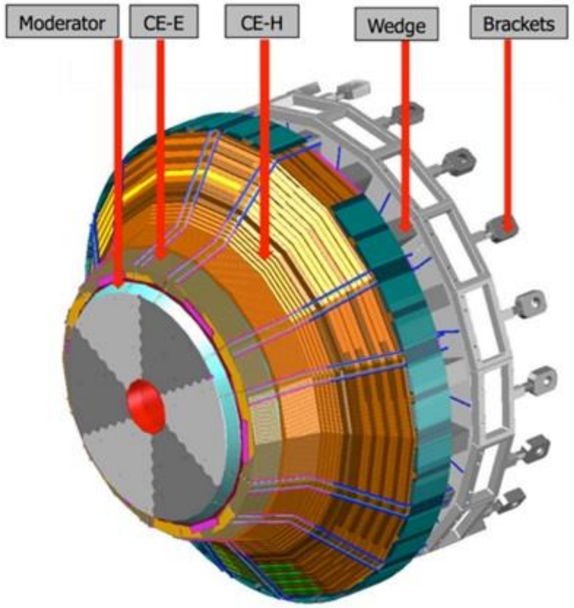


CMS High Granularity Calorimeter (HGCAL)

- **Upgrade of CMS at HL-LHC**
  - New “5D” imaging calorimeter
  - Si and SiPM sensors
  - HGCROC/H2GCROC chips



[5]



	CE-E Silicon	CE-H Silicon	CE-H Scintillator	Total
HGCROC	60 324	31 596	8 496	100 416
Motherboards	5 004	2 556	384	7 944
Bidirectional data/control links	5 004	2 556	384	7 944
Trigger links	4 020	2 556	768	7 344

Requirement: Use very similar FE electronics for the readout of both detectors

- Si (~ 4 fC / MIP)
- SiPM-on-tile (~ 1.7 pC / MIP) [2]

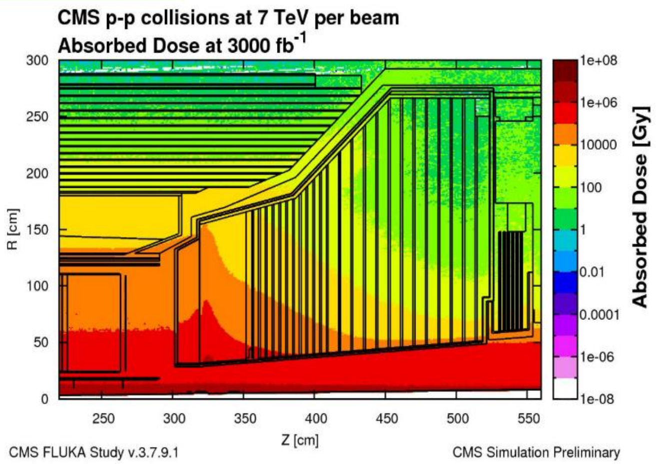
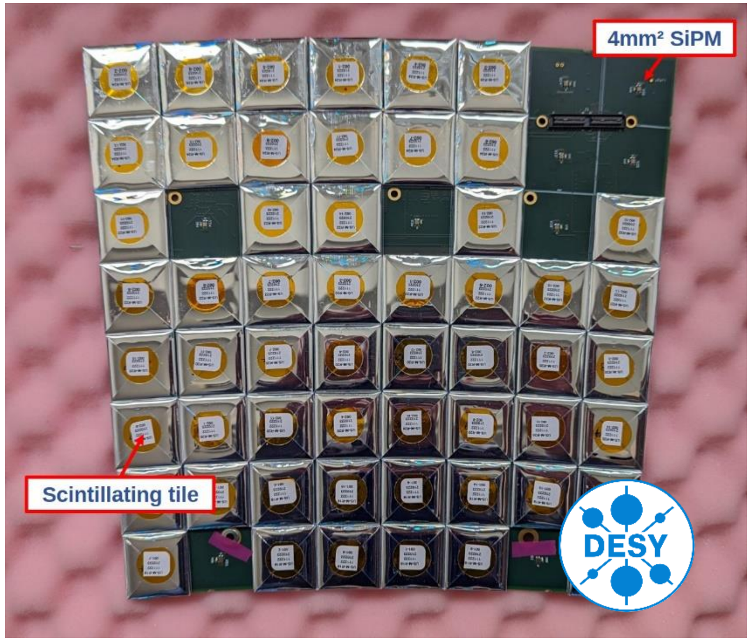


Figure 1.1: Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

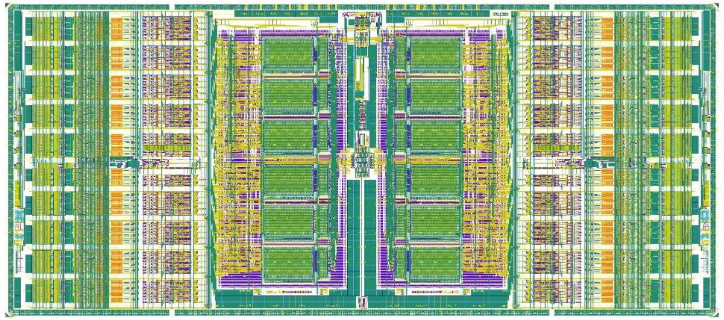
[2]

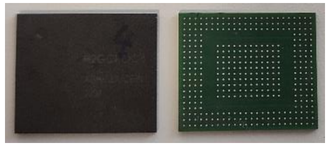


H2GCROC: SiPM version. Requirements

Requirements for H2GCROC (The SiPM version of the ASIC):

- Charge dynamic range : **160 fC to 320 pC**
- Timing accuracy **< 100ps for pulses above 3 MIPs (4.5pC)** for a $C_{det} = 100pF$
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**
- **Input DAC** to tune the overvoltage

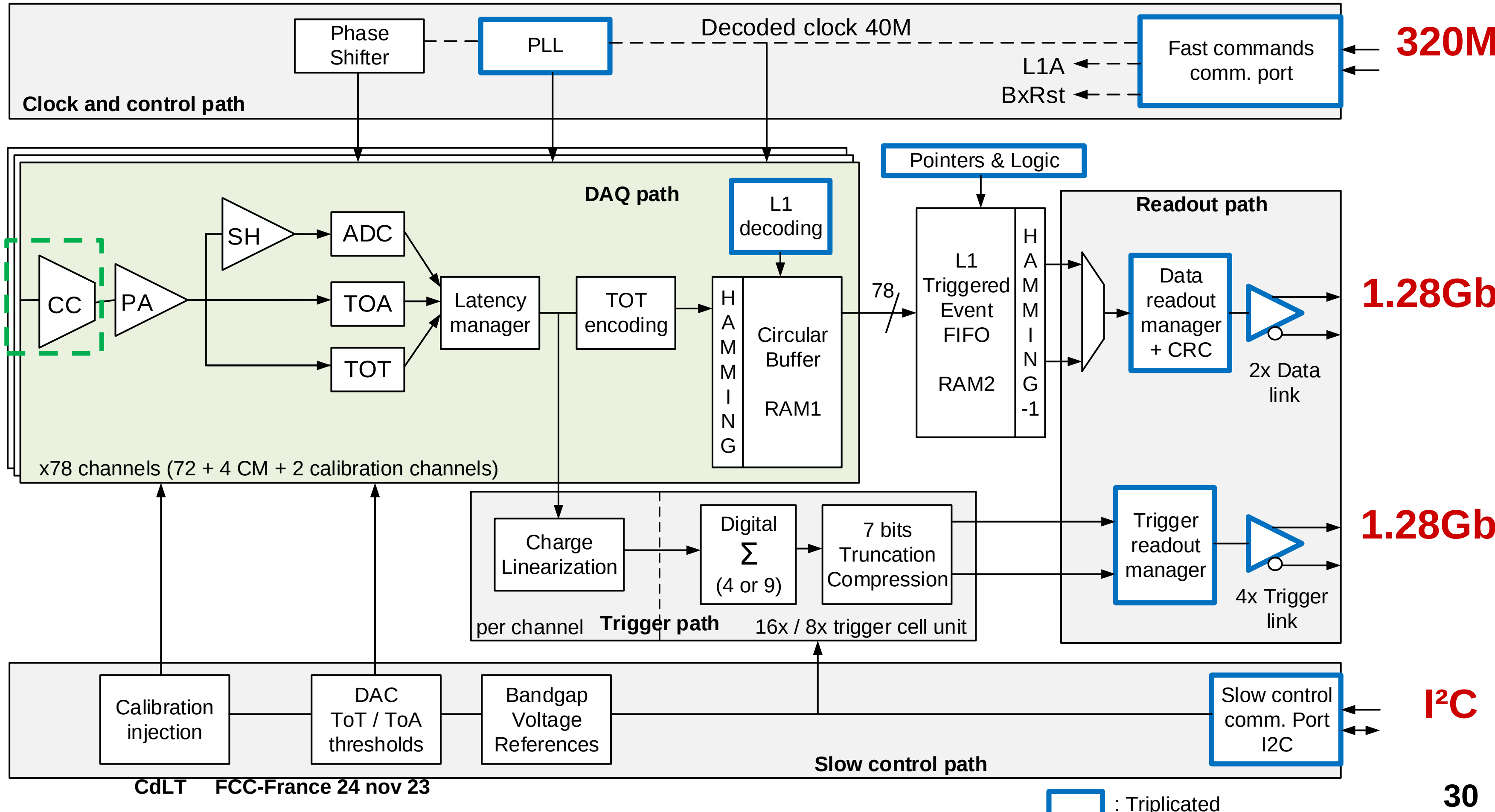




Current Conveyor based on KLAUS chip from Heidelberg UNI.

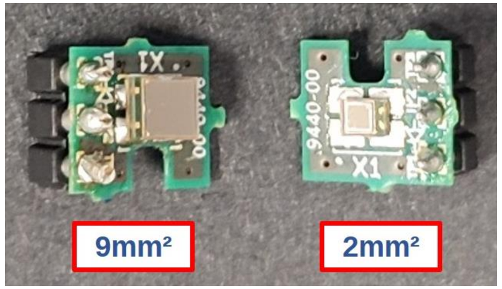
Attenuates the current at the input with 4 bits.

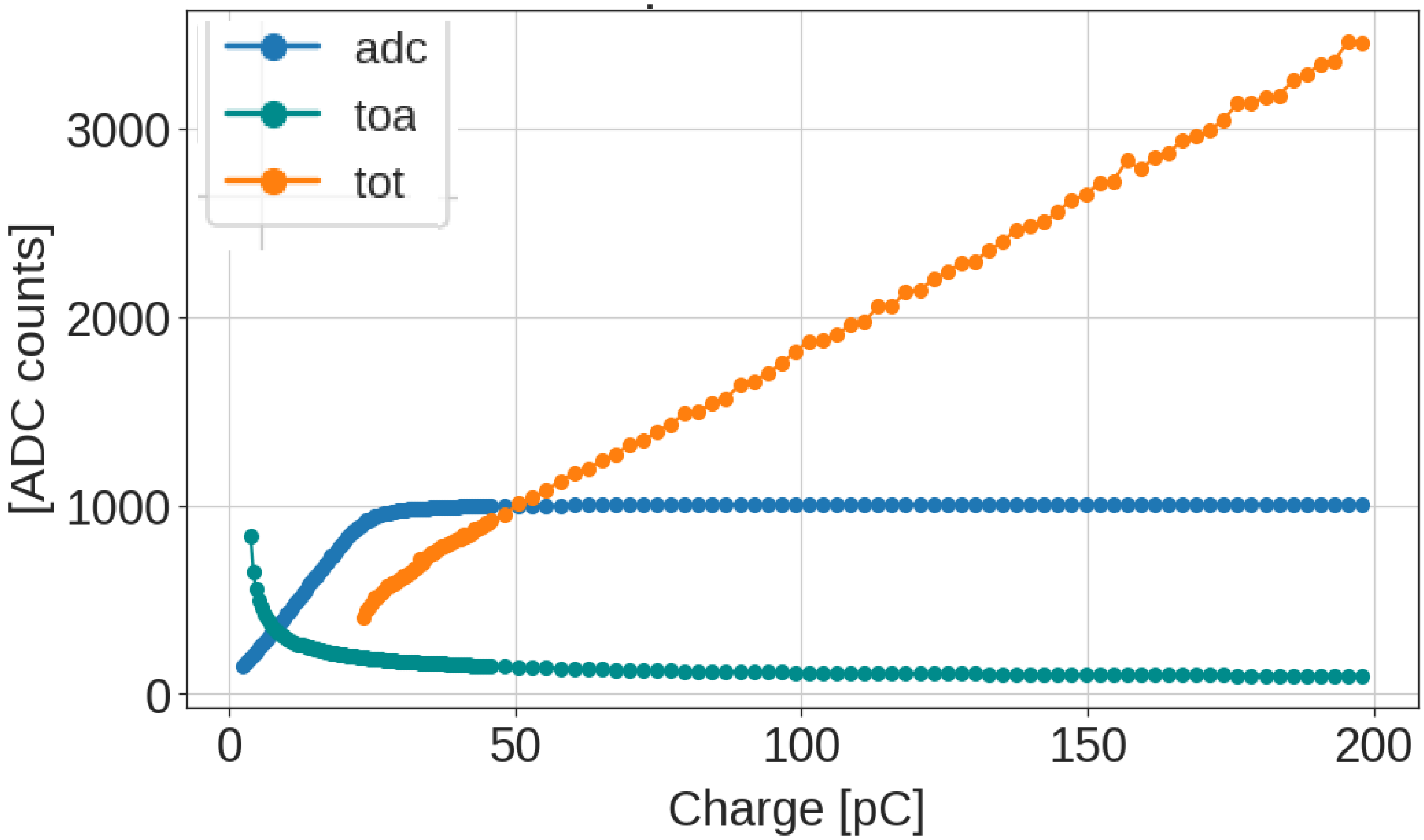
CC gain:
0.025 to 0.375
(step 0.025)



ADC and TOT readout

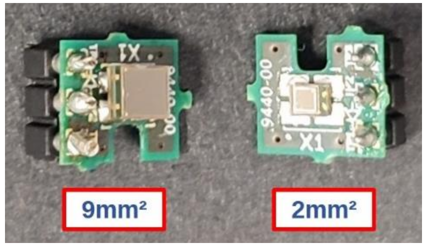
- 16bit dynamic range split in 10 bit ADC and 12 bit ToT
- Tests with 2 sizes of SiPM : 2mm² (120 pF) and 9 mm² (560 pF)



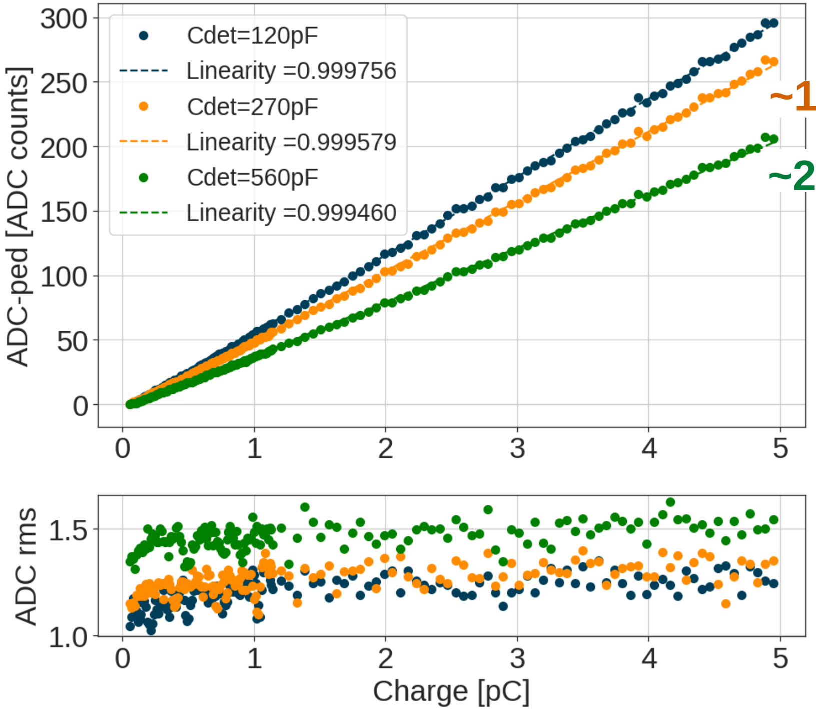


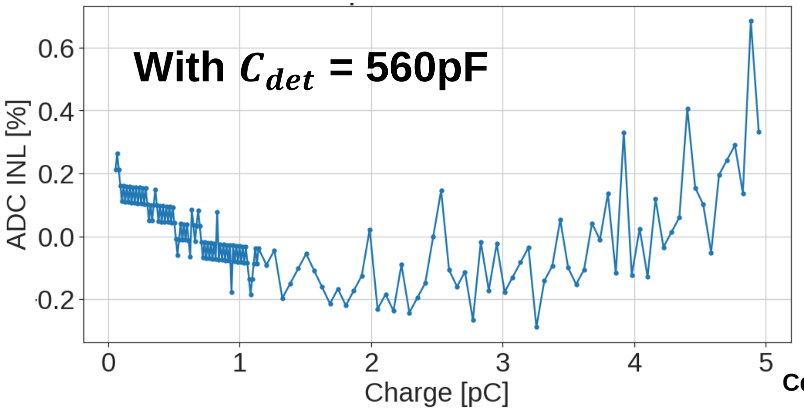
Physics mode : test pulse injection

- ~ 60 fC minimum detectable charge efficiently, up to 320pC

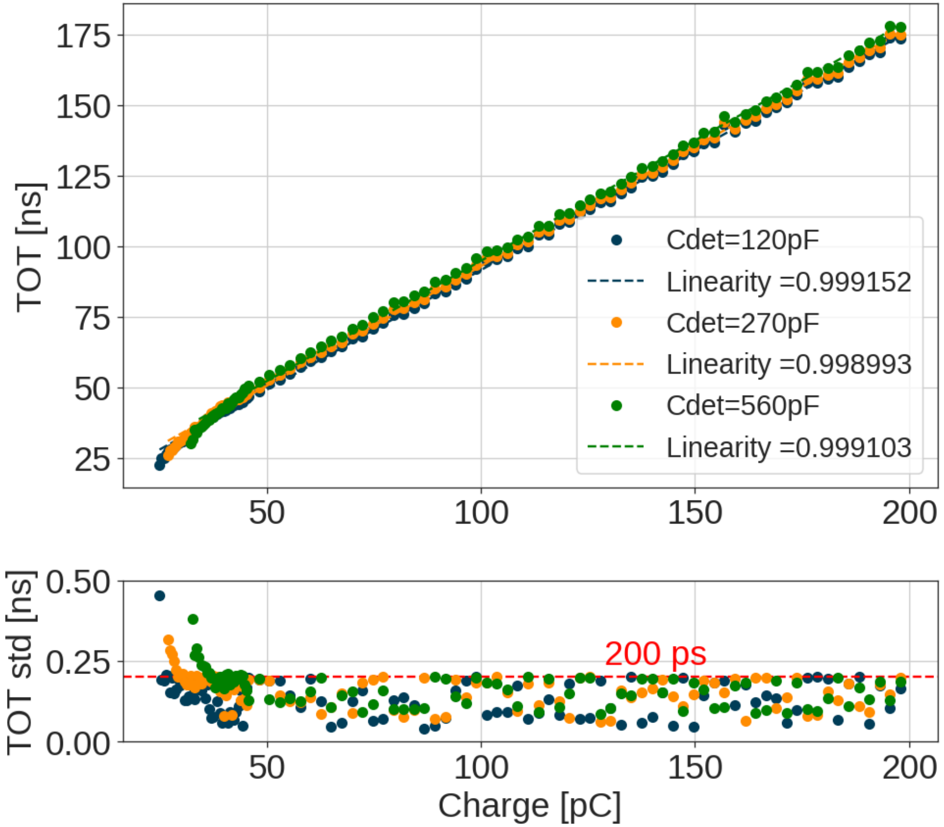


Low range injection (ADC):





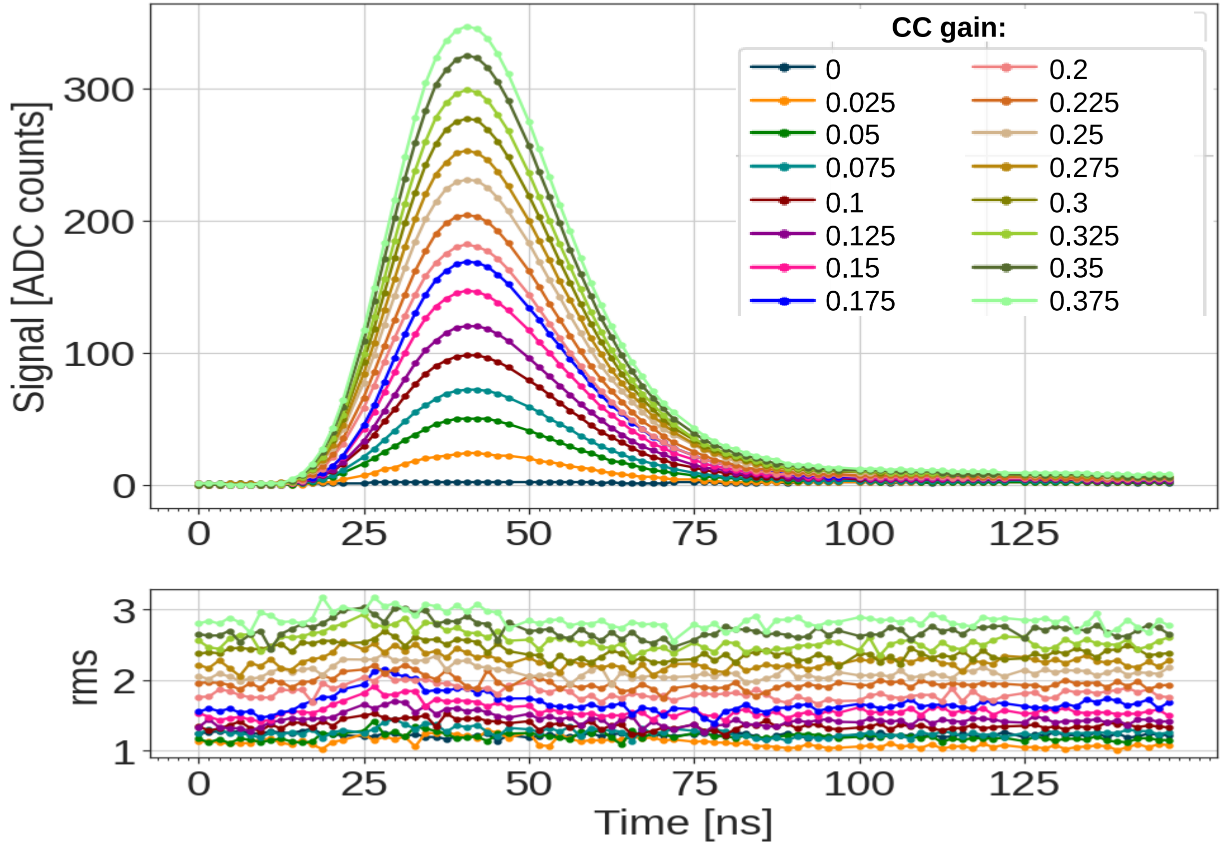
High range injection (TOT):



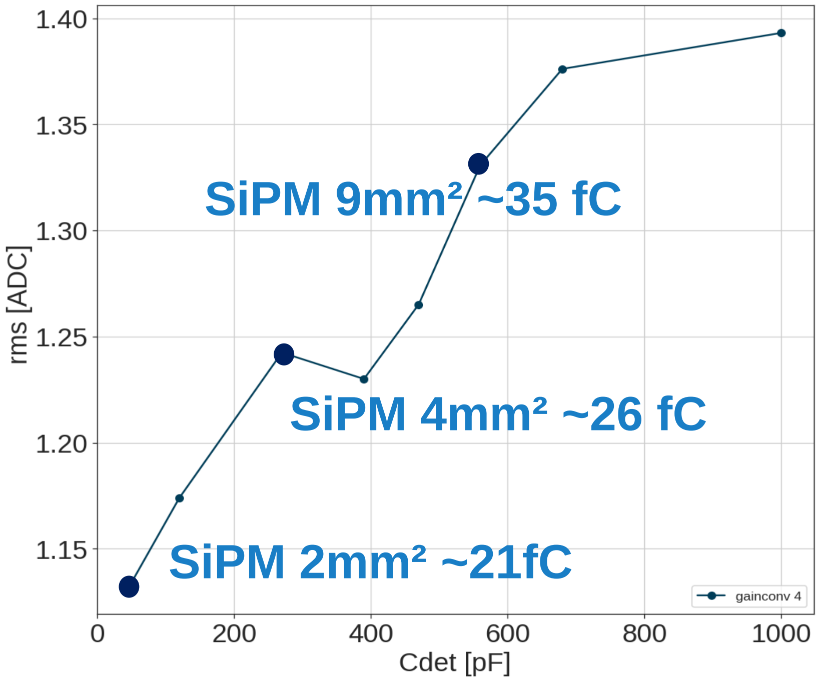
- The CC gain has good performance in linearity.

- The increment in noise is due to the gain configuration and the detector capacitance of the SiPM.

CC gain scan:

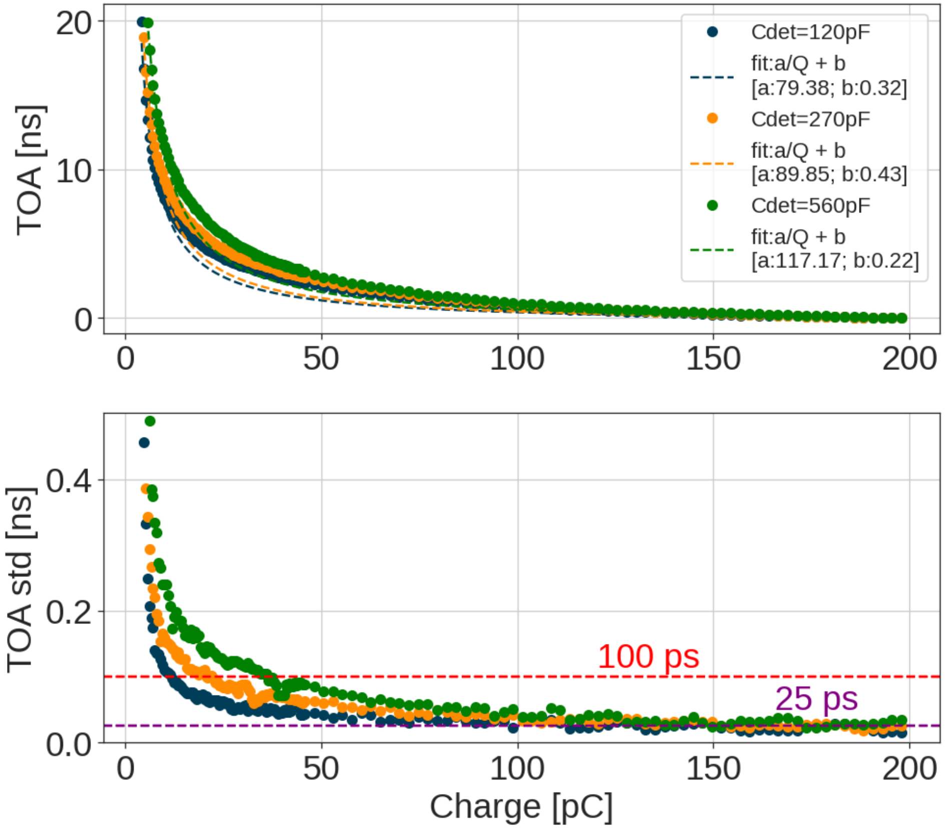


Noise vs C_{det}:



Physics mode : ToA

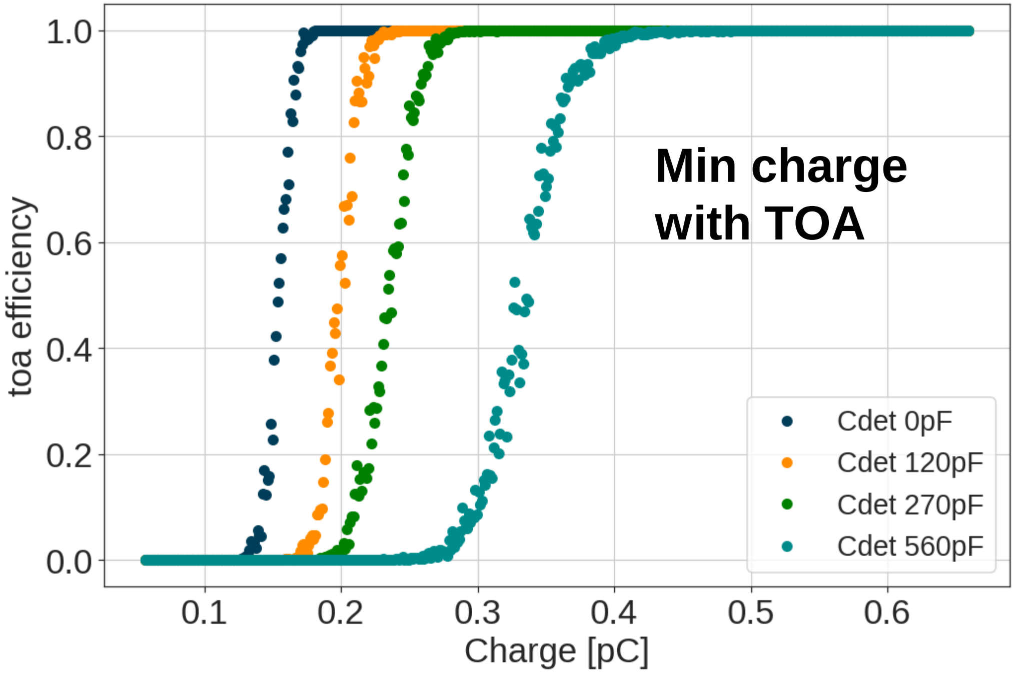
Time of Arrival (TOA) :



- The increase in noise due to larger C_{det} shifts the minimum charge associated with TOA data.
- The thresholds can be adjusted channel-wise for a uniform performance.

Effect of C_{det} on TOA:

- Larger C_{det} produce larger time walk due to the duration of the signal.
- Increasing C_{det} delayed the achievement of a 100ps resolution in charge injection.



Calibration mode: Single-photon-spectrum

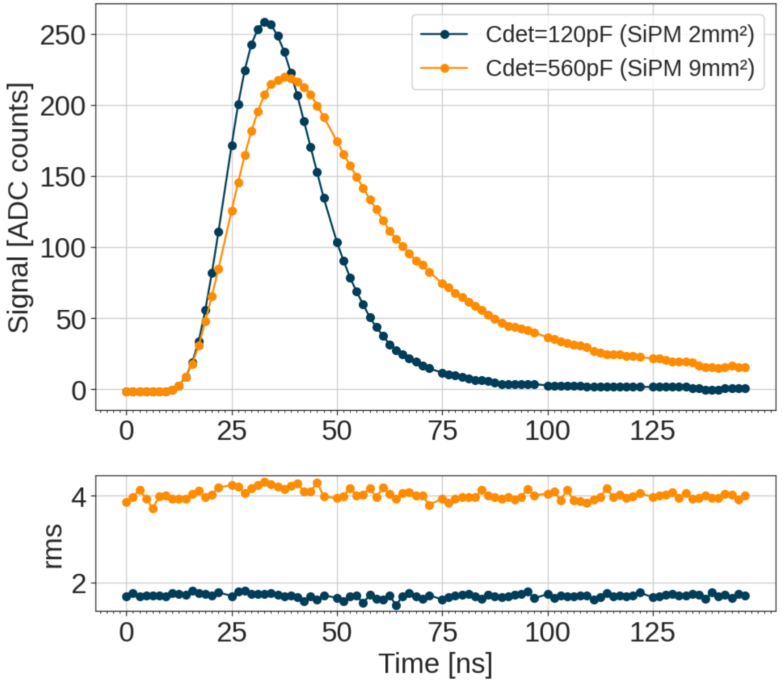
Also a different configuration of the ASIC is necessary to increase the SNR.

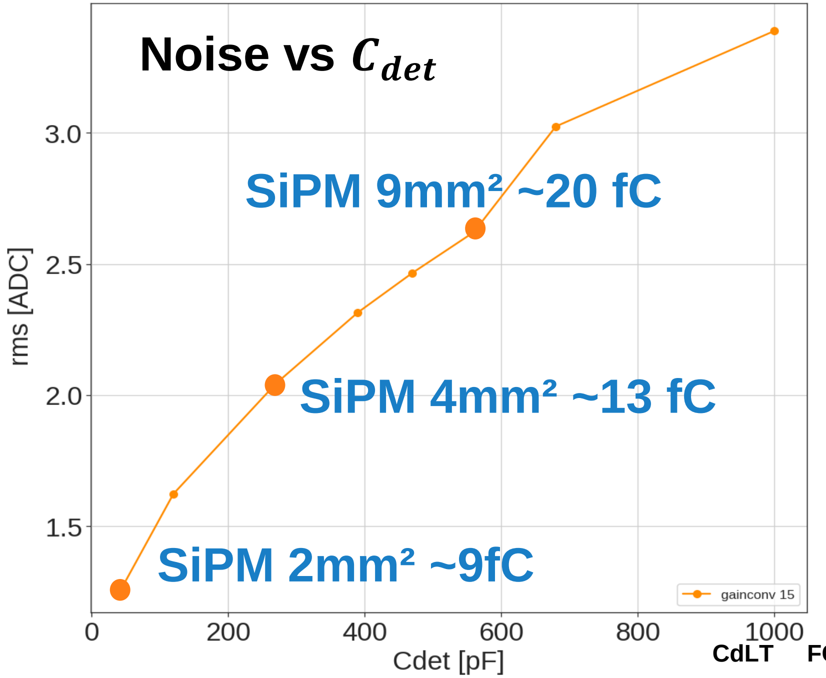
2mm²:

- CC gain attenuation = **0.3**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = 600fF\ (C_f + C_{fcomp})$

9mm²:

- CC gain attenuation = **0.375**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = \mathbf{300fF}$ (To make the pulse shorter)



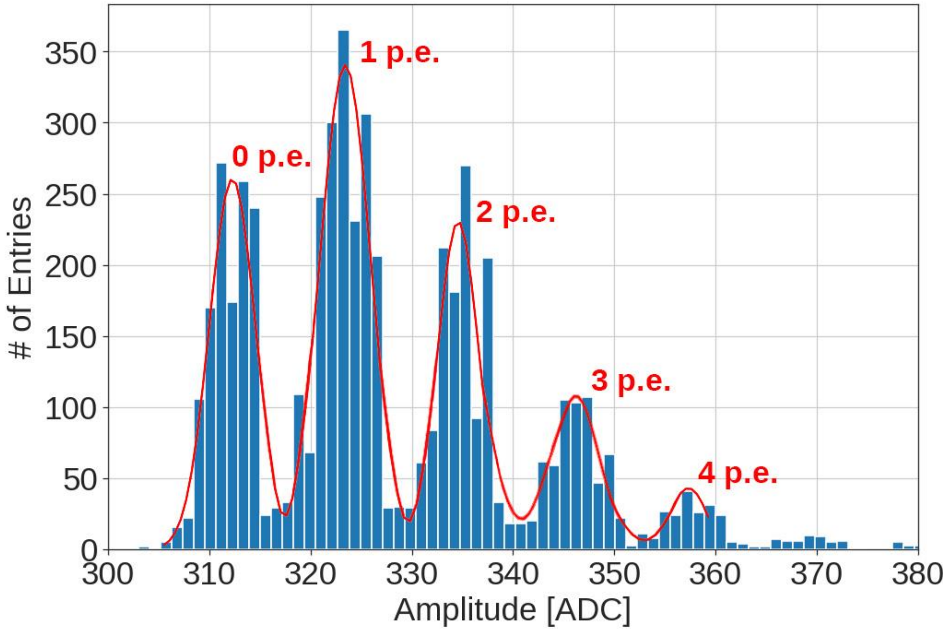


*Noise measured with the same configuration parameters for all $\boldsymbol{C_{det}}$.

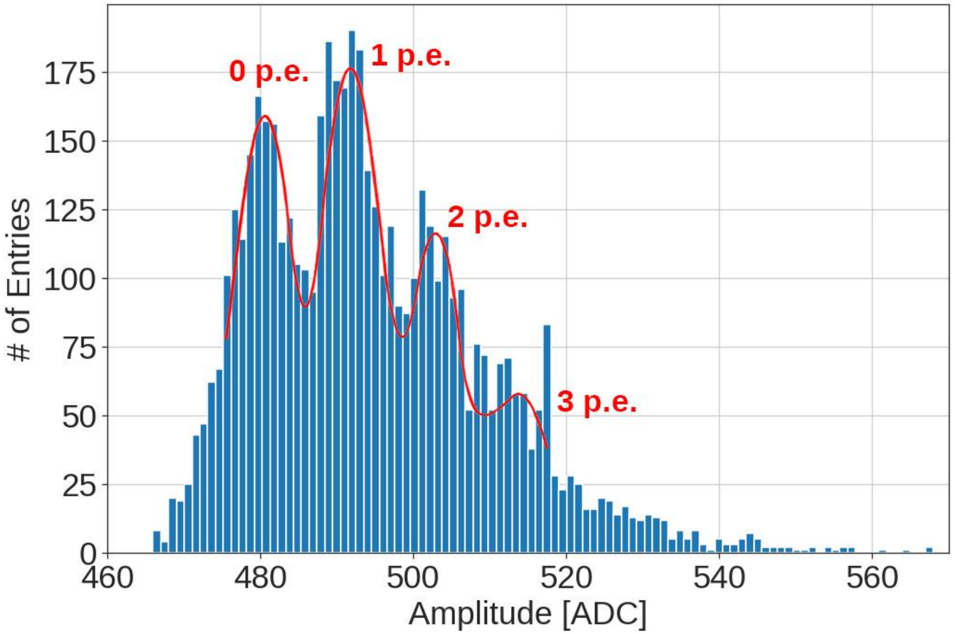
- The increment in noise is due to the detector capacitance of the SiPM.
- SNR can be improved with the gain configuration.

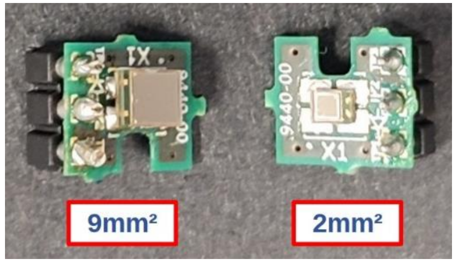
Calibration mode: Single-photon-spectrum

- **2mm²:**



- **9mm²:**



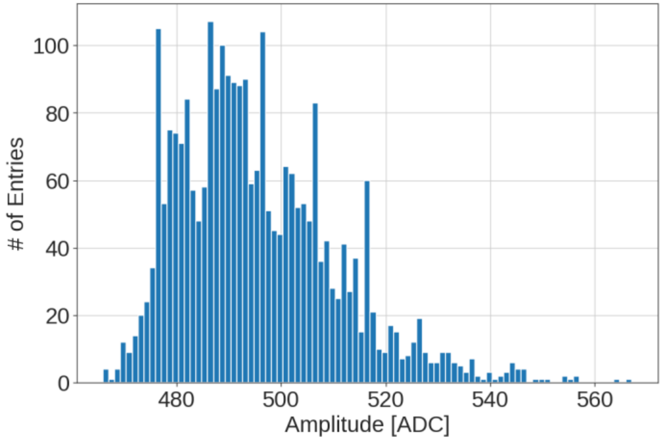


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

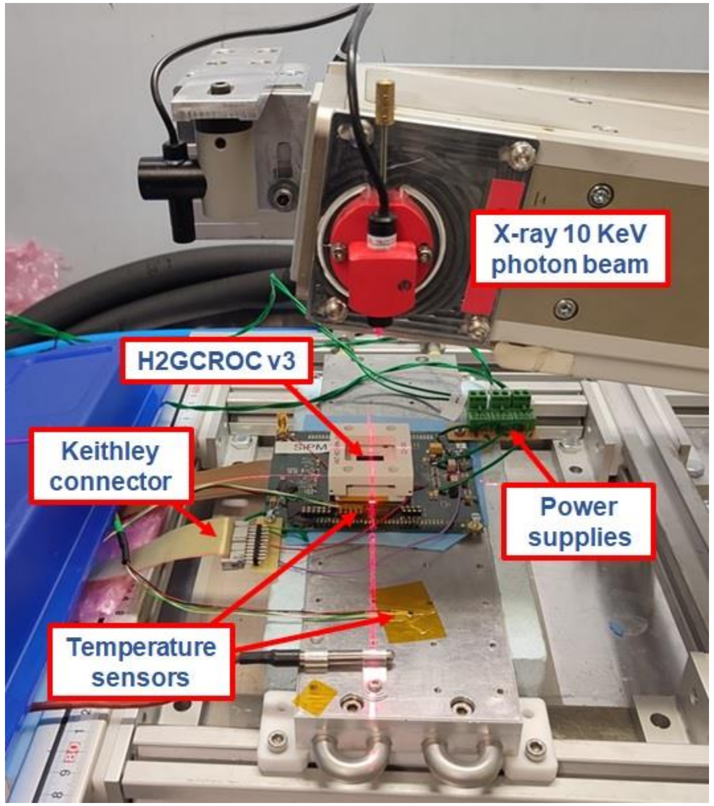
The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:

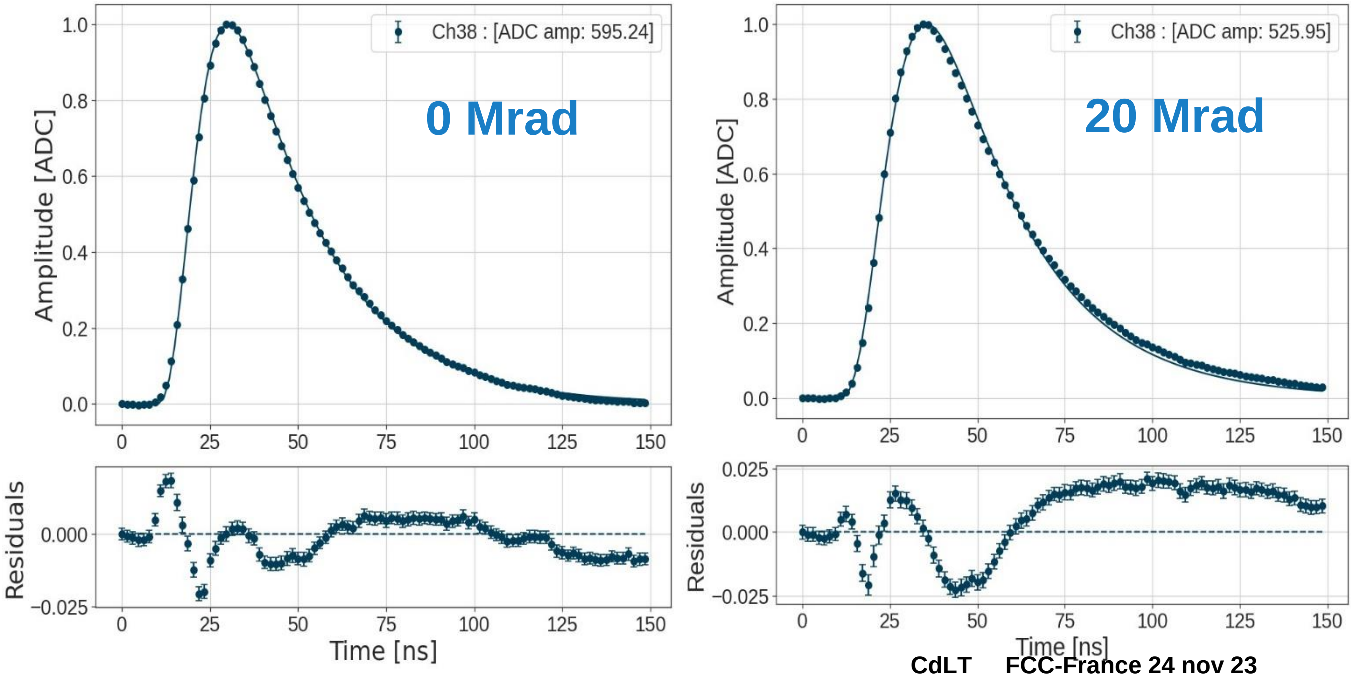


Irradiation campaigns

- Power consumption, ADC & TDC performance, noise, links stability, etc. tested during irradiation
- **TID irradiation tests in both ASIC versions.**
- **Heavy ion and Proton irradiation in the Si version of the ASIC**
  - Increase on triplicated parts for HGCROC3b

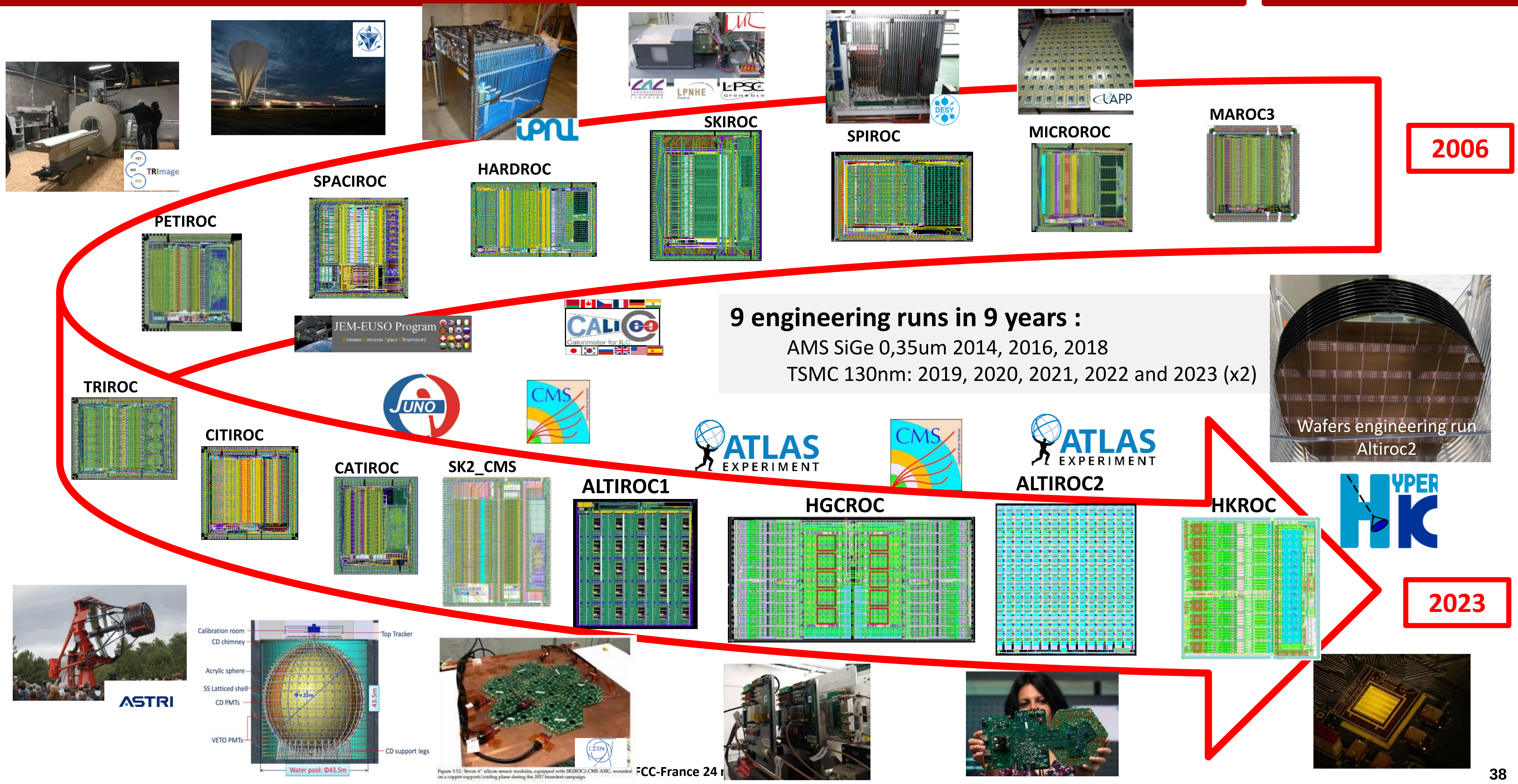


Stability of ADC measurements after 20Mrad:



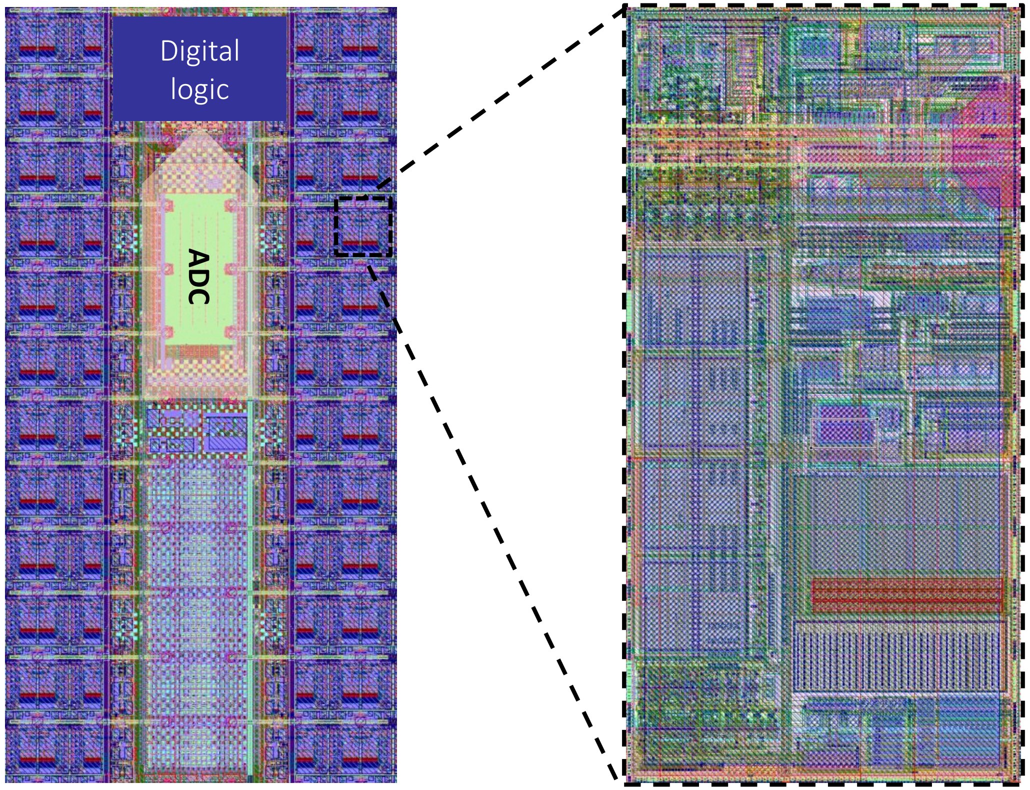
- **H2GCROCv3** has proven to be **radiation tolerant up to 20 Mrad** at room and -5°C with good ADC, TDC and PLL measurements.

ASICs produced and installed on detectors



Dynamic gain switching : Pixel matrix [SLAC]

600x1200 µm

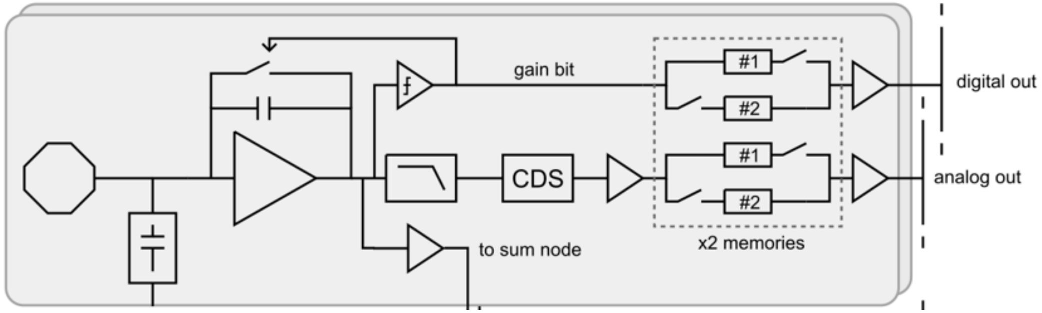


Cluster

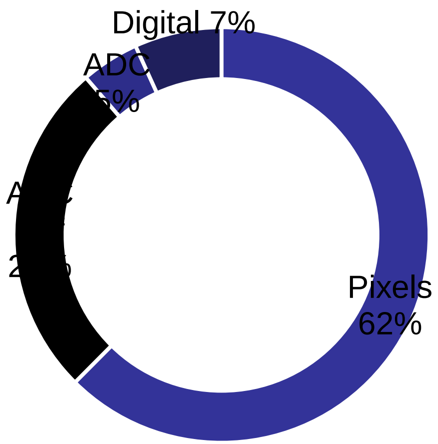
- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

Pixel

- Operates at 100 kHz – 1 MHz
- Si sensor: 100x100 μm^2
- ASIC: 50x100 μm^2



Pixel analog front-end block diagram



Power consumption of different blocks in matrix
(power density: 0.94 W/cm^2)