SiW-ECAL for FCC-ee

Vincent Boudry & many others...

Institut Polytechnique de Paris

LLR

FCC France
23/11/23 @ IPHC, Strasbourg

Forewords

ILD is one of the detector concepts for the ILC

in the process of adapting the design to the FCC conditions → ILD'

- Plans → Roman's (ILD(') & CLD) presention
  - Inner detectors ⇒ see Daniel's presentation
  - 'French' Calorimeters:
    - **SiW-EVAL** ⇒ see here
    - **T-SDHCAL** ⇒ see Imad's presentation

CALICE is a R&D collaboration working on PFA 'imaging' calorimeters [proto and methods]

SiW-ECAL work in transition to DRD6 T1.1 (Sandwich Calorimeters)

- Work Package 1: Sandwich calorimeters with fully embedded electronics
  - Task 1.1: Highly pixelised electromagnetic section
    - Subtask 1.1.1: A Silicon-Tungsten Electromagnetic Calorimeter SiW-ECAL

Particle Flow Approach

Full Reconstruction of single particles

- Charged almost exclusively from trackers
  - Cluster removal by spatial matching *only* (idealy)
- Neutrals only from calorimeters

Large Tracker

- Precision and low X_0 budget
- Pattern recognition

High precision on Si trackers

- Tagging of beauty and charm

Large acceptance

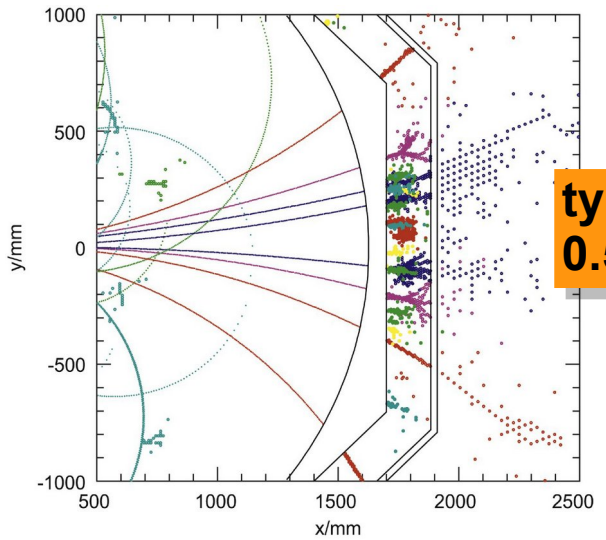
HG Imaging Calorimetry

Particle Flow Algorithms :

- Jets = 65% charged Tracks + 25% γ ECAL + 10% h^0 E+HCAL
- TPC $\delta p/p \sim 5 \cdot 10^{-5}$; VTX $\sigma_{x,y,z} \sim$ 10 µm

+ timing

H. Videau and J. C. Brient, "Calorimetry optimised for jets," (CALOR 2002)



typical size : 0.5 – 3 cm

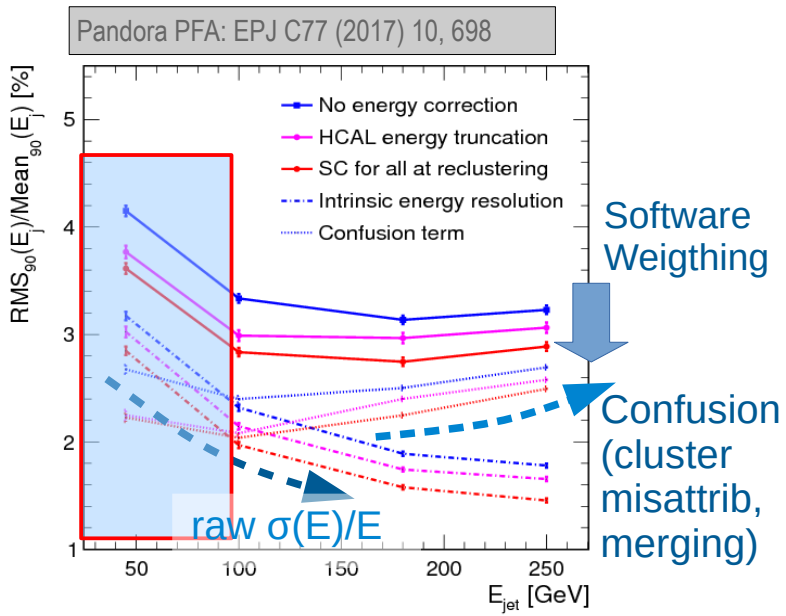
Reconstruction & Optimisation

Performances: (for a given configuration of detectors)

- Will depend on the Reconstruction SW (ex. PandoraPFA, ARBOR, APRIL, SW compensation, ML, ..)
- *and* it's proper tuning (~ generic ? not universal)
  - JER for HET physics, τ reconstruction, b physics, …

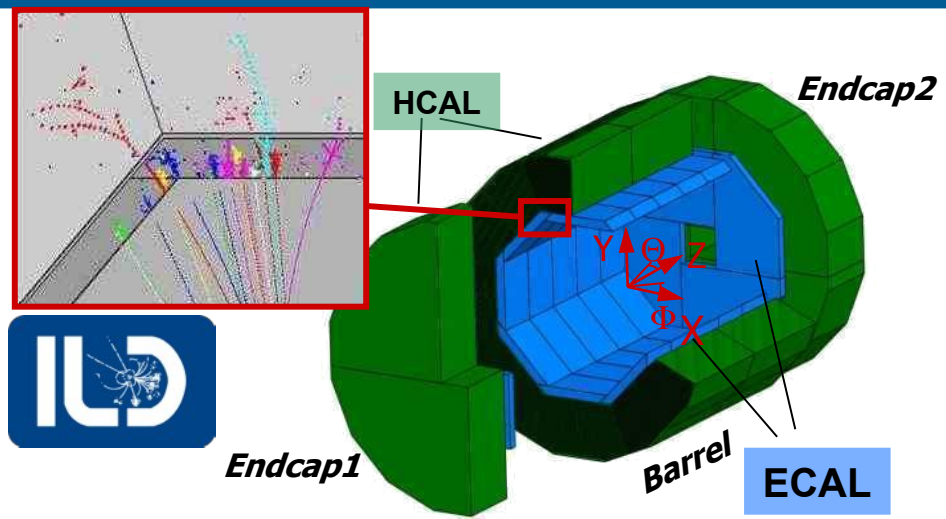
Optimisation (best configuration):

- on **simulation,** needs:
  - proper HW description
  - proper Electronics description (Digitization)
- needs the tuning o the Reconstruction SW for each



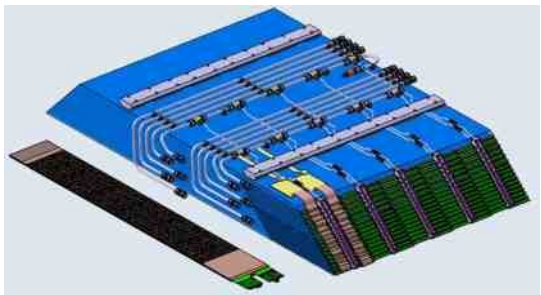
Low E jets ⇒ where PFA brings most

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (E, (θ,φ), t)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)

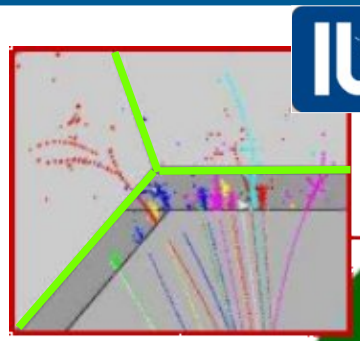


SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design: Sensor+RO≤2mm
  - Allows for ~any pixelisation
  - Robust technology
  - Excellent signal/noise ratio: ≥10
  - Intrinsic stability (vs environment, aging)
  - Albeit expensive…
- Tungsten–Carbon alveolar structure
  - Minimal structural dead-spaces
  - Scalability

To be assessed by prototypes

Modular & Transverse Constraints



HCAL

Endcap2

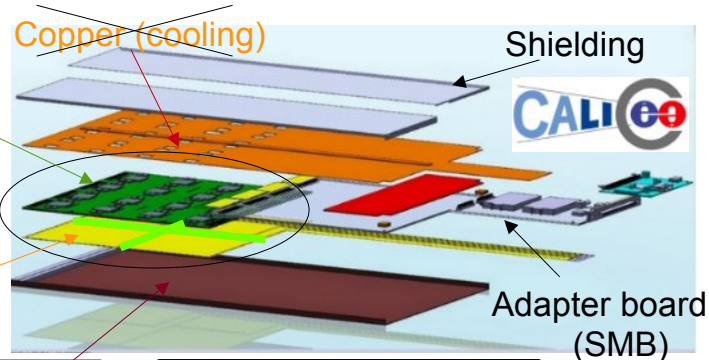
Endcap1

Barrel

ECAL

B = 2– 3.5 T

PCB (FeV)
16 SK2 ASICs
1024 channels
ASU
Wafer (4)

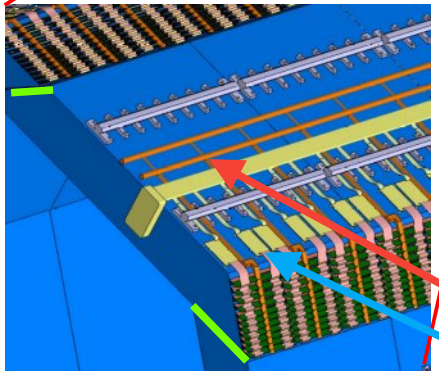


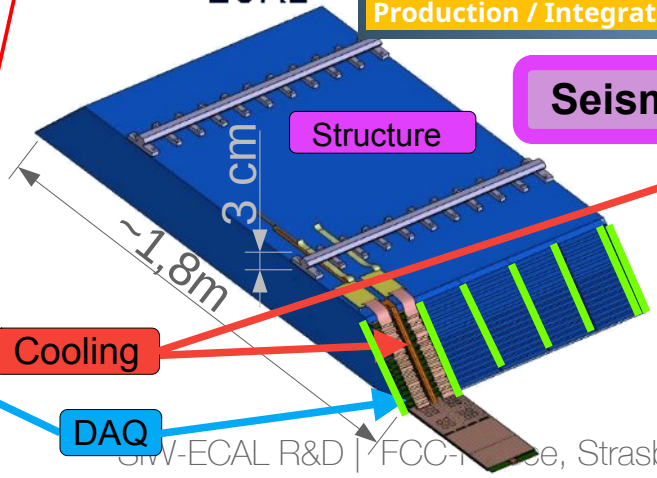
Carbon+W

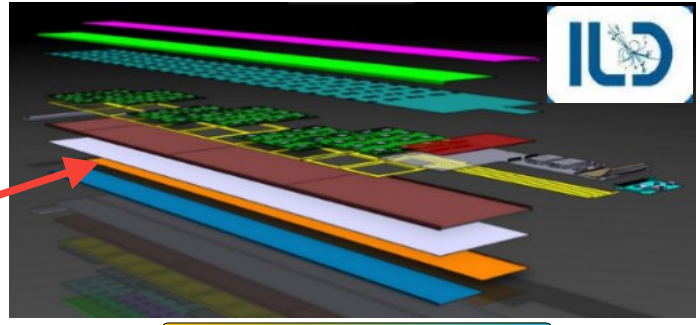
U layout of a **short slab**

Physical
Instrumental
Electronics
Mechanical
Thermal
Production / Integration

Seismic







U layout of a **long slab**

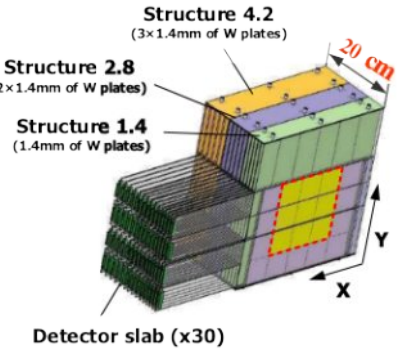
+ timing

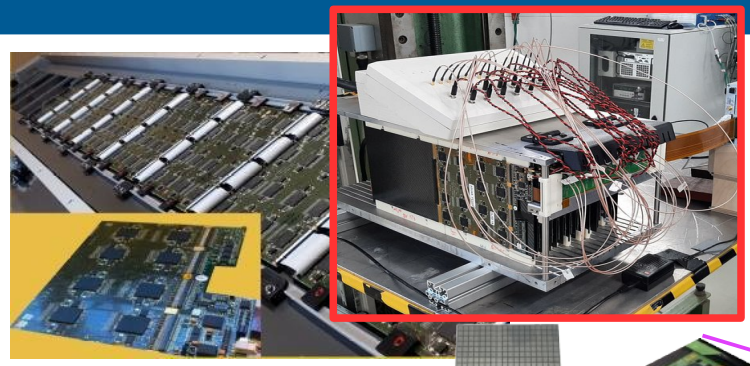
Cooling

DAQ

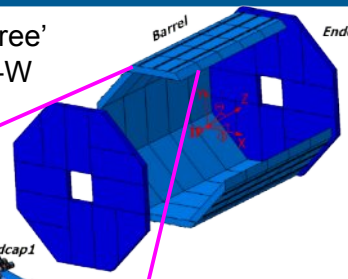
PP ↔ Cont

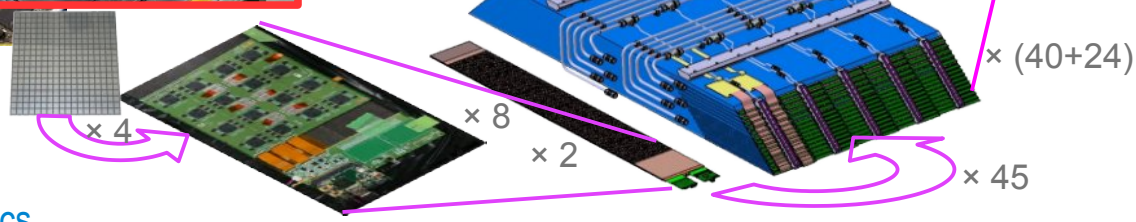
Timeline of SiW-ECAL Prototypes





'dead space free'
Carbon Fibre-W
Structure





Physical (2005-11)

- 1×1 cm² on 500µm 6×6 cm² Pad glued on PCB Floating GR
- × 30 layers (10k chan).
- External readout
- Proof of principe

Technological (now)

- Embedded electronics
  - Power-Pulsed, Auto-Trig, delayed RO
  - S/N = (MPV/σ_{Noise}) ≥ ~12 (trig)
- Compatible w/ 8+ modules-slab
- 5×5 mm² on 320–650m 9×9 cm² × 26–30 layers
  - 8k (slab) ~ 30k (calo) channels

We are here

Pilote ➡ Full Detector

- 1M ➡ 70M channels
- on 725µm 12×12 cm² 8" Wafers ?
- Pre-industrial building
- Full integration (⊃ cooling)
- Final ASIC

Linear → Circular Collider's Conditions

Linear (ILC, HL-ILC…)

- 250 GeV (ZH), 365 GeV (tt), 500 GeV (ZHH) + [1000 GeV], $\mathscr{L}$ ~ cst.
- Power pulsing : 5 [10–15]Hz × 1 [2] ms Power ~ $\mathscr{L}$.

More diverse et stringent conditions:

- 90GeV × 10^7 fb × $5{\cdot}10^{36}$ cm^{-2} s^{-1} (qq × 20,000 ILC @ 250)
- 150 GeV (WW) + 250 GeV (ZH)+ 365 GeV (tt)
  ~10^4 fb × $5{\cdot}10^{35}$ cm^{-2} s^{-1} (qq × 5–10 ILC @ 250)

From Pulsed to Continuous operation

- Power = cst + convertion+RO × local rates (P_{Conv}+P_{RO} ~ 40% P_{ACQ})
- ASIC, Power/Cooling, DAQ, *Granularity, Precisions (E, t)*, New ideas…

HL-ILC:

- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : τ_{Train} : 1 → 2 ms
- f_{rep} ×2 (3): 5 → 15 Hz

Dominated by ACQ time:
P(~25μW/ch) × 6

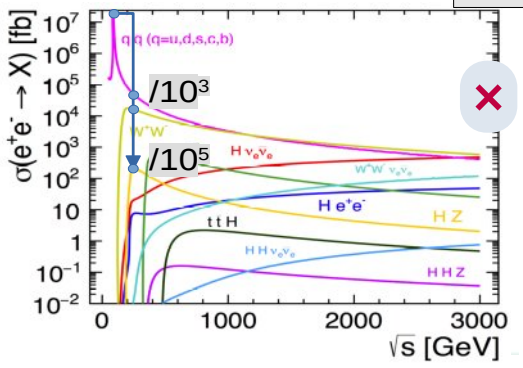
HL-CLIC:

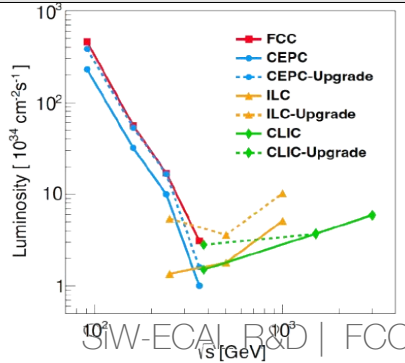
- $\mathscr{L}$ × 2
- $N_{bunches}$ → : τ_{Train} : 176 ns
- f_{rep} ×2 : 50 → 100 Hz

Dominated by Set-up & Conversion time: P (~82μW/ch) ×2

FCC-ee parameters		Z	W⁺W⁻	ZH	ttbar
√s	GeV	91.2	160	240	350-365
Luminosity / IP	10^{34} cm^{-2} s^{-1}	230	28	8.5	1.7
Bunch spacing	ns	19.6	163	994	3000
"Physics" cross section	pb	35,000	10	0.2	0.5
Total cross section (Z)	pb	40,000	30	10	8
Event rate	Hz	92,000	8.4	1	0.1
"Pile up" parameter [μ]	10^{-6}	1,800	1	1	1

Status of the CEPC, October 2022 J. Guimarães da Costa





Experimentally, Z pole most challenging

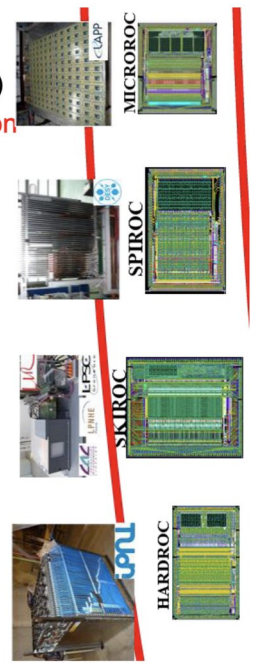
- Extremely large statistics
- Physics event rates up to 100 kHz
- Bunch spacing at 20 ns
  - "Continuous" beams, no bunch trains, no power pulsing
- No pileup, no underlying event …
  - …well, pileup of 2 x 10^{-3} at Z pole

https://indico.cern.ch/event/1064327/contributions/4893208/
Mogens Dam @ FCC Week, 10/06/2022

New ASIC:

DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - ⇒ allows common DAQ and facilitates combined testbeam
- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch
  - Allows better granularity or LAr operation
  - Extend to LAr (cryogenic operation) and MCPs (PID)
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts
- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL



CdLT : future chips DRDI 10 jul 23 8

See Christophe's presentation Friday

Low Power

- Timing ?

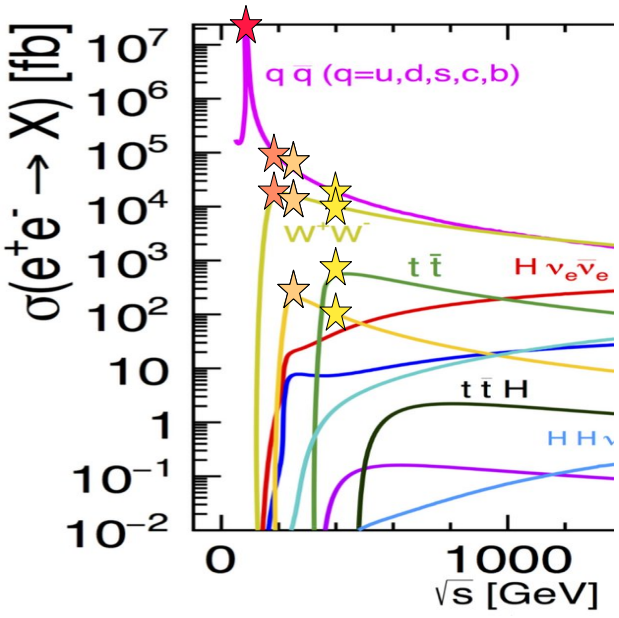
Low occupancy

- Self-trigger
- Less memory
  - if continuous readout

Optimized dynamic range (silicon)

Enough ?

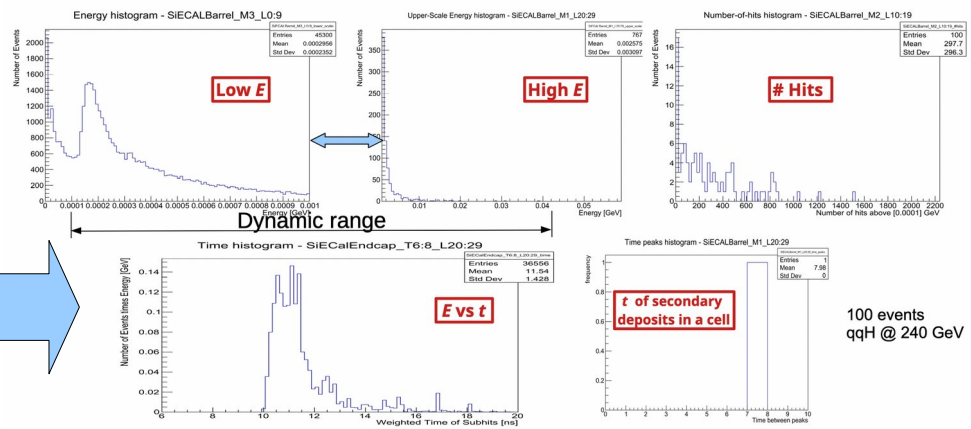
Fluxes in calorimeters



Processes: min. bias

- All
  - ee → qq
  - ee → $\mu\mu$, $\tau\tau$
  - ee → ee (⊃ Bhabha)
  - $\gamma\gamma$ → VV
  - Machine background (ee pairs)
- $E_{CM} \geq 160$ GeV
  - ee → WW
- ($E_{CM} \geq 240$ GeV)
  - ee → HZ
- ($E_{CM} \geq 360$ GeV)
  - ee → $t\bar{t}$

Full simulation ➞ statistics per region



× $\mathscr{L}$ + **Machine background**

➞ Fluxes of hits, data, per region

➞ Power with ASIC assumptions

See pres. this afternoon

Detector Parameters: scaling rules

- Cell lateral size
  - Shower separation (EM~2×cell size)
  - Cell time resolution (1 cm/c ~ 30 ps)
    - Time performance for showers
      - » ParticleID, easier reconstruction
- Longitudinal segmentation
  - sampling fraction
    - E resolution (ECAL ~15%/√E)
  - shower separation/start
- ECAL inner radius; Barrel Z_{Start}
- ECAL–HCAL distance
- Barrel–Endcap distance
- Dead-zones sizes (from Mechanics, Cooling)

Number of cells ↗ ⇒ Cost ↗ (1/size²)
Cell density ↗ ⇒ Power consumption ↗

Time resolution ↘ ⇒ Power ↗

threshold, passive vs active cooling
dead-zones ↗

BEING FULLY RE-EVALUATED (→ ILD, CLD)
for EW region with realistic ASIC hypothesis

Inner Radius ↗ ⇒ Tracking performance ↗
Cost ↗² (⊃ Magnet, Iron)

Gaps ↗ ⇒ PFlow performances ↘
↳ ⊃ *Active cooling*

Review of physical implication (from TeV): see Linear collider detector requirements and CLD, F. Simon @ FCC-Now (nov 2020)
Physics Requirement studies @ 250 GeV: see Higgs measurements and others, M. Ruan @ CEPC WS, (nov 2018)

Detector optimisation for Higgs Factories

Continuous running ≠ Pulsed runnning

- Power × 100 !

Low energy (90 GeV)

- Lower energy – less focused jets
  - Lower granularity needed (1–2 cm OK ?)
  - Lower dynamic range
- Other criterions ? Tagging

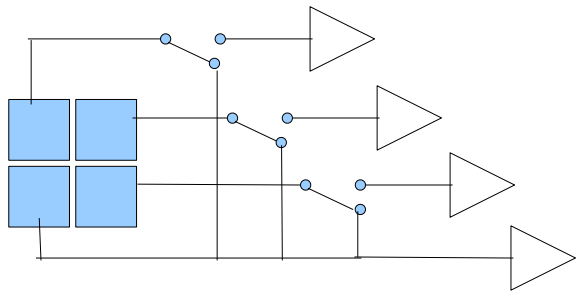
… but not so for the rest (≥ ~250 GeV)

Reduce the number of layers + thicker sensors

- See “Small ILD” model
- 6’’×500µm wafers ➡ 8’’ × 725 µm (resolution $1/\sqrt[5]{d}$)

One size fit all ?

- Have a dynamic granularity ?



- Have a semi-digital readout ?
  - Hit counting for low energy
  - E measurement for high energies

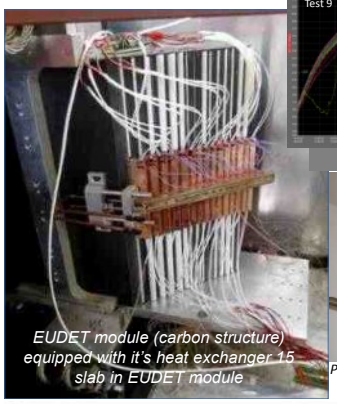
R&D

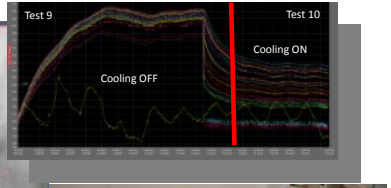
Current status

	TRL1	TRL2	TRL3	TRL4	TRL5	TRL6	TRL7	TRL8	TRL9
Sensor									✔
ASIC							✔		
PCB (FEV)			✔						
ASU		✔							
SLAB		✔	✔	✔					
Structure		✔	✔	✔					
DAQ									✔
Power			✔						
Cooling							✔	✔	✔
Design		✔							
Prototypes			✔						

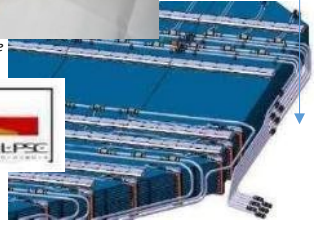
Leakless Water cooling system

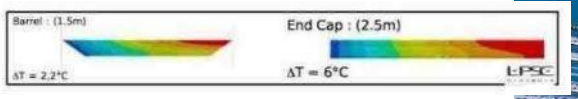
Thermique/Intégration

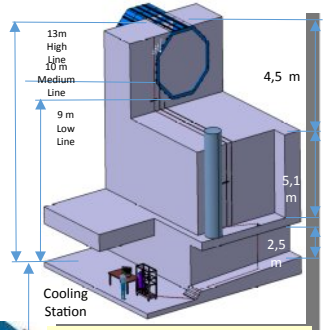

EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module




Passive cooling ramp example







LPSC cooling test area with a drop of 13 m


Cooling station

Buts:

- Heat evacuation at end of slabs
- Caloduc compatible with ECAL–HCAL spacing (3 cm)
- Leakless (depression)

Modèle : sur module pilote

Maquette 1: 1:1

- simple circuit

Maquette 2: 3:4

- heat model in C-W structure

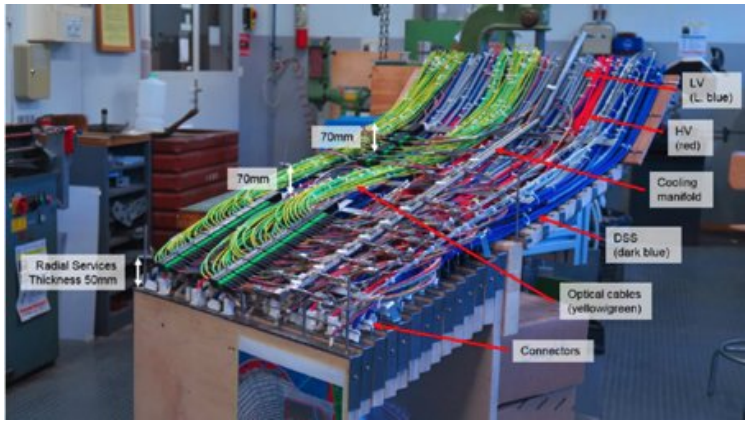
To Do:

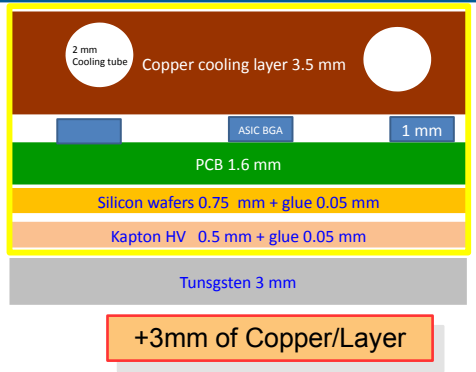
- **Test sur on a full ECAL module**

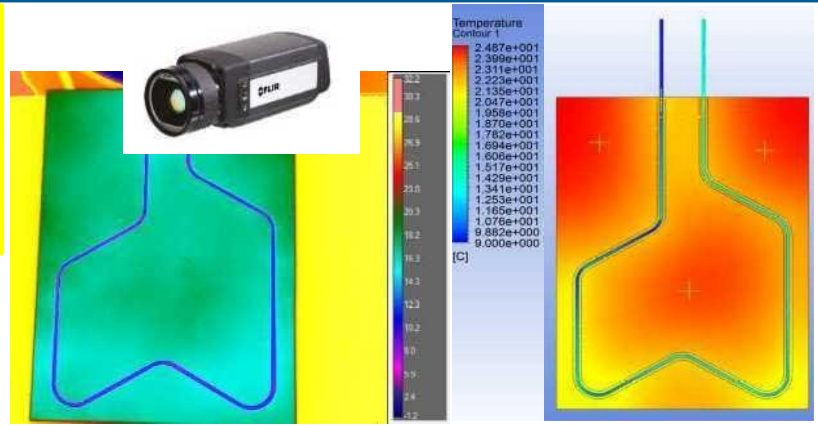
For FCC-ee:

- 1) Dimensioning for continous working, if possible, without active cooling
- 2) if not, include a active cooling CO_2 (in Cu or W)

Services: integration & cooling

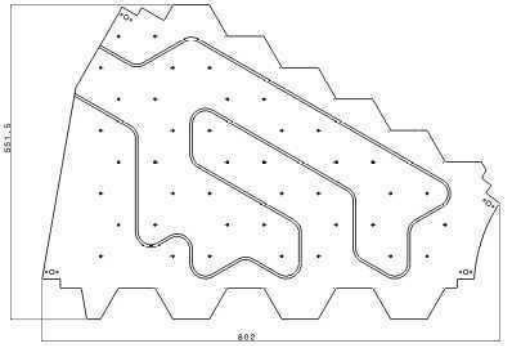


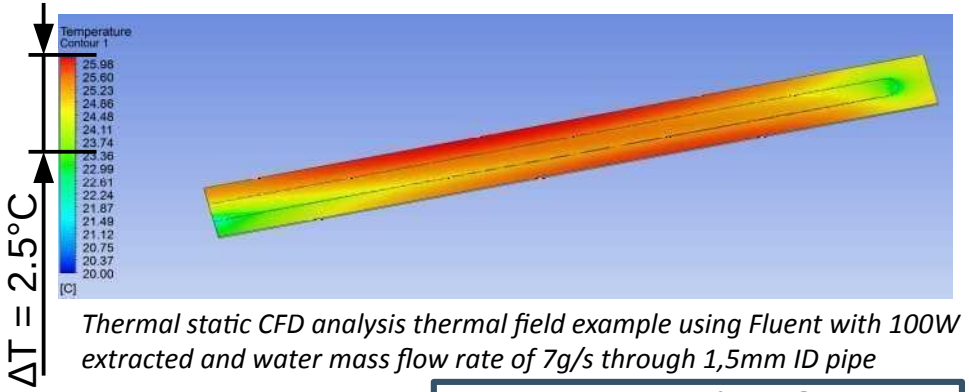




Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling

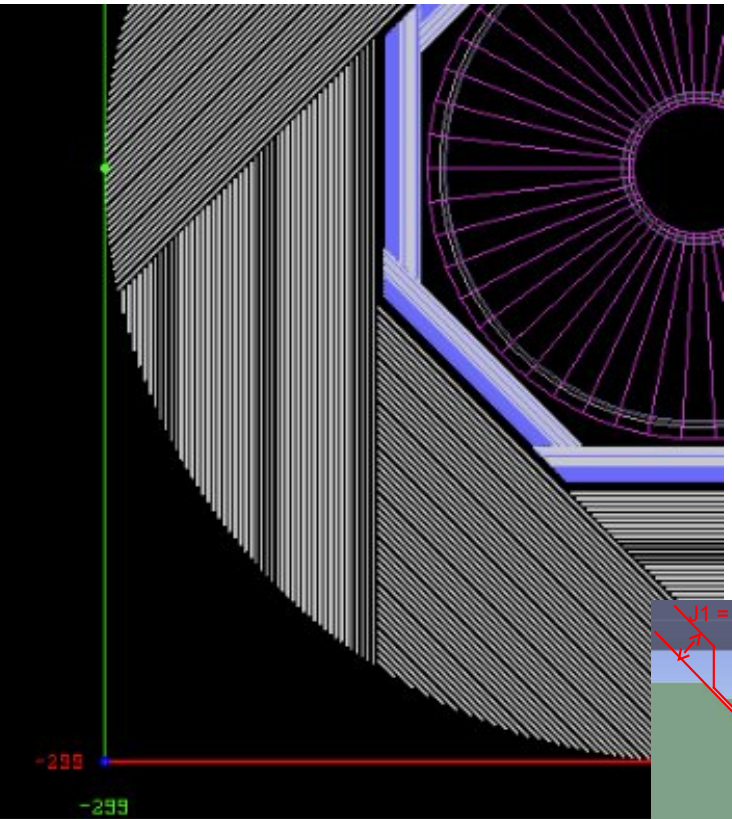


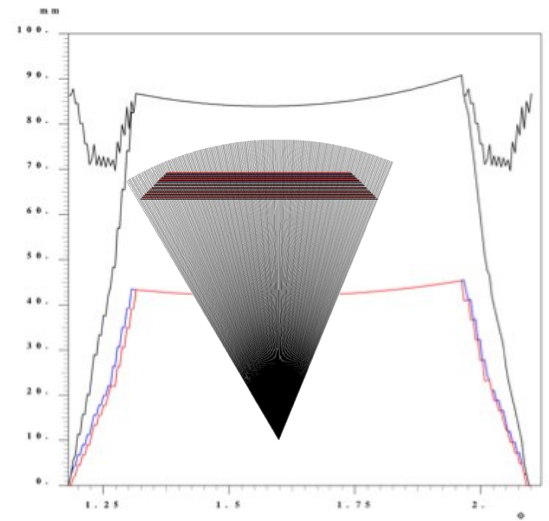


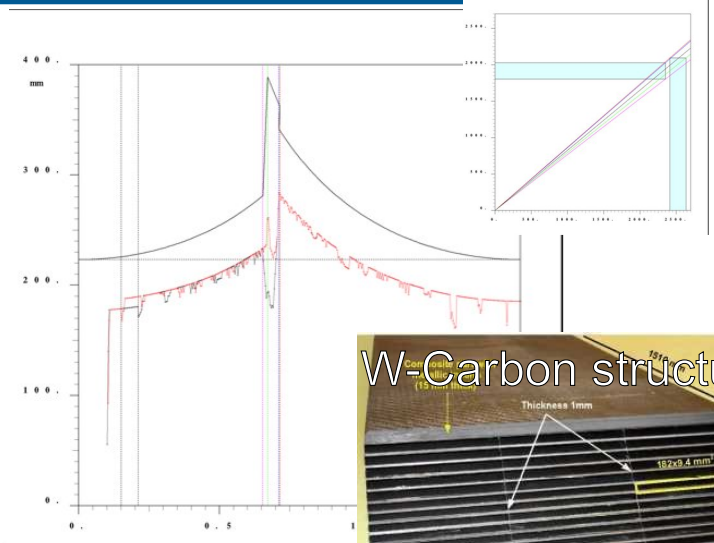
Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

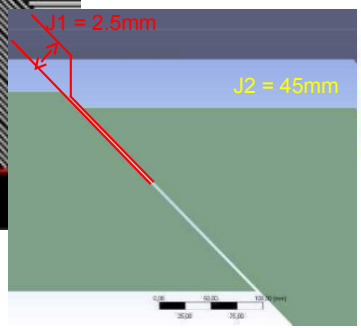
= 2× cont. operation of a SLAB

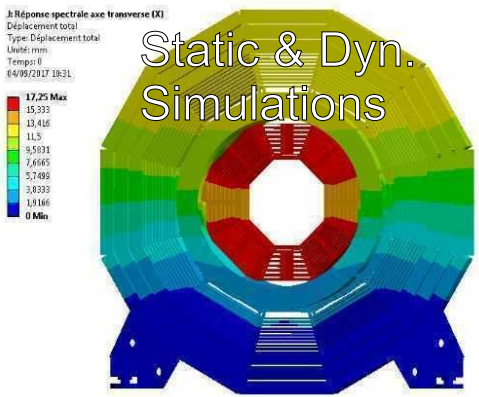
Mechanics : A crack-less ECAL geometry











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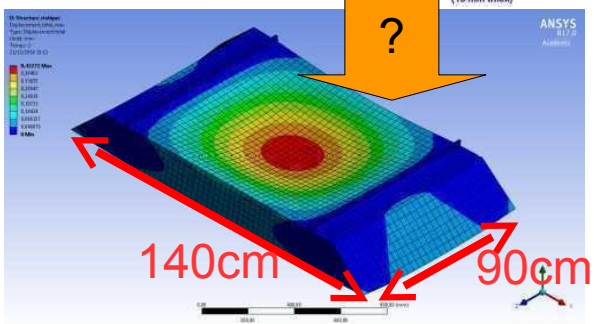
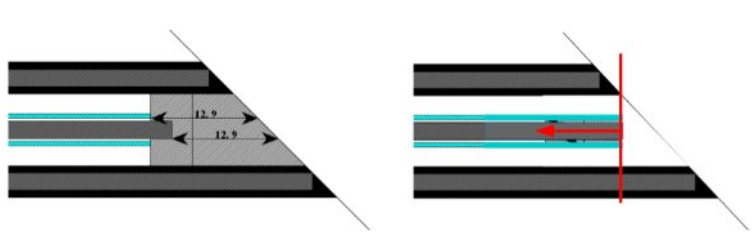
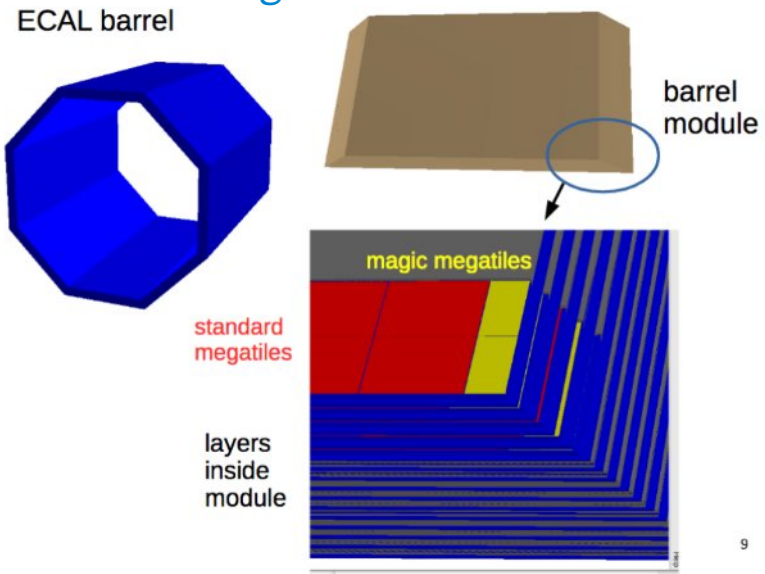


Simulation



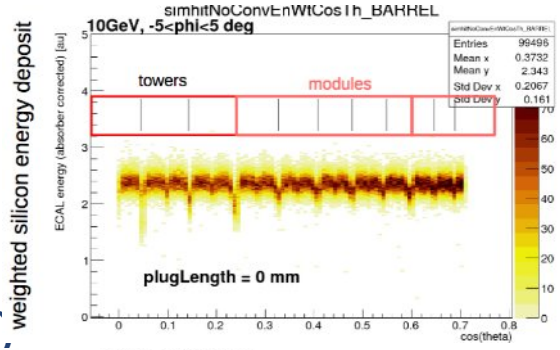
ECAL driver used in ILD models has been largely re-written (Mokka → DD4HEP)

- more modular code:
- less duplication Barrel & Endcap
- more configurable…

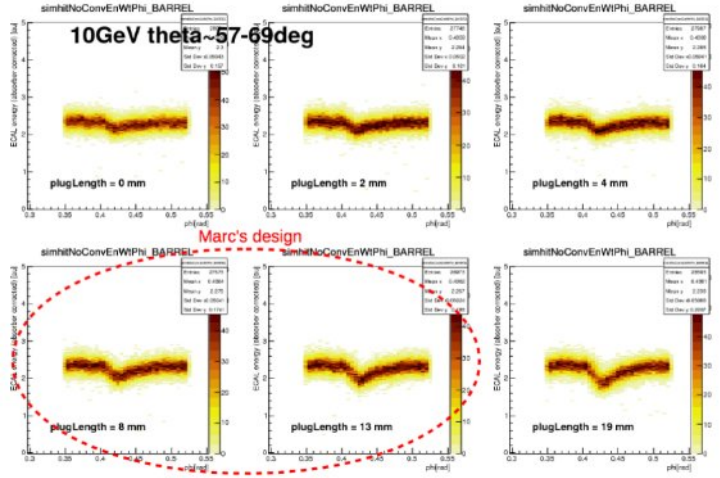


Effect of cracks [RAW= no correction at all!!]

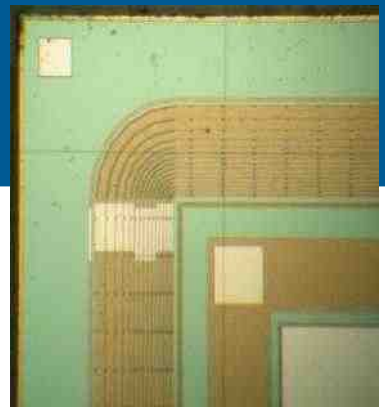
- Drop ~ 15%

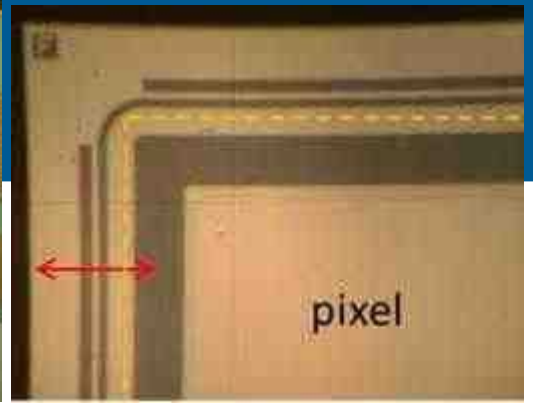


Effect of plug (missing in previous simulations)



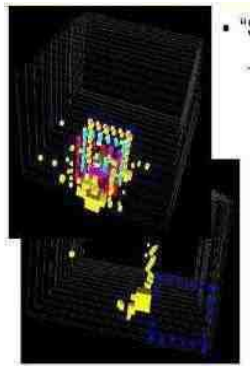
Silicon Sensors

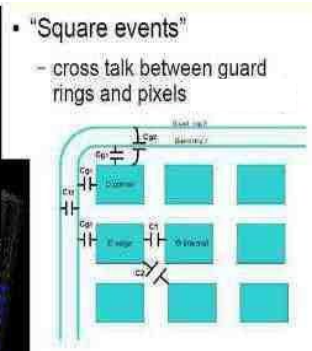




Cost driver

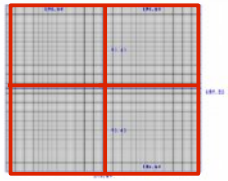
- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction(**CALIIMAX program**)
- Decoupling of Guard Ring (Square Events).
- new design of ILD detector

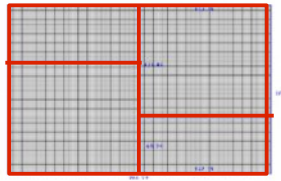


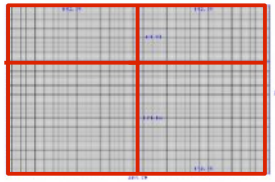


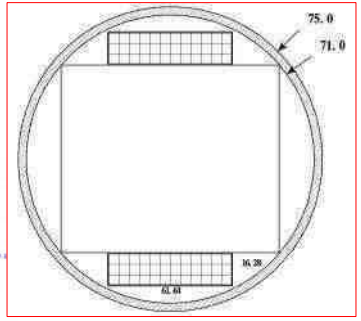
Command Sensors (@ Hamamatsu)

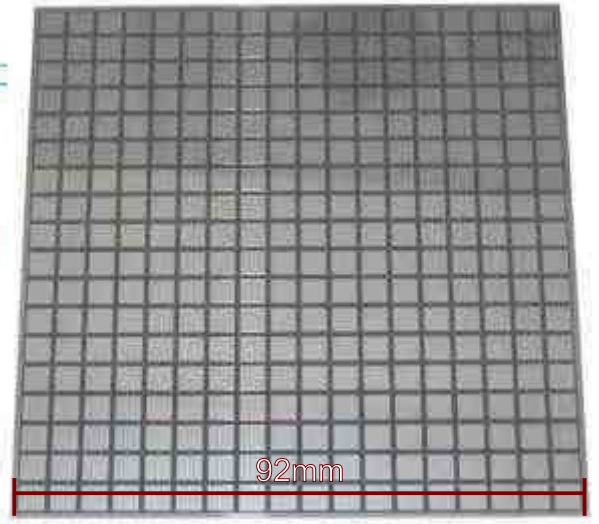
- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8'' in 186mm alveola 320 →











'quantum unit' of ILD dimensions (here 6'' wafer)

Going from 30 to 26 Layers: performances

Going from 30 to 26 layers

- Reduction of cost; increase of Energy resolution
  - keep 24X_0 (84mm) of Tungsten

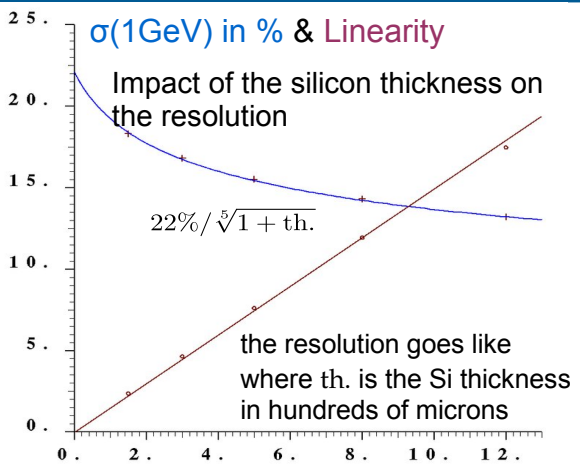
Increasing the Si thickness to 725µm

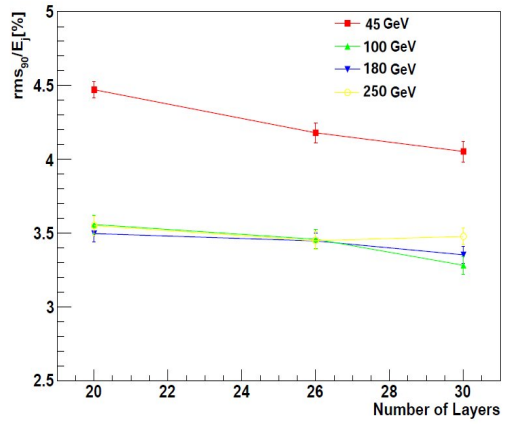
- GR width ↗ ⇒ go to 8" wafers, new design

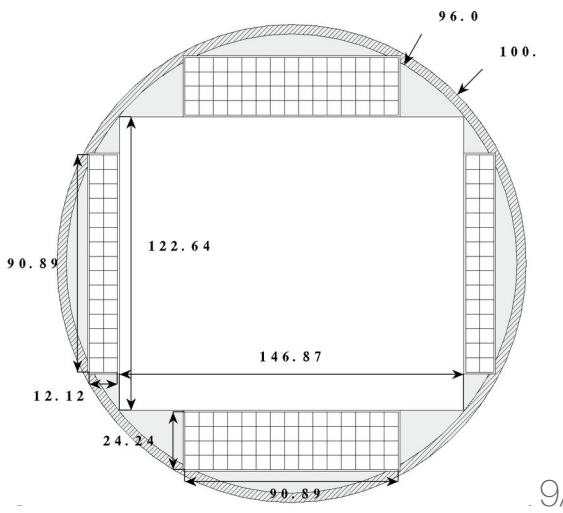
Energy resolution σ(E)/E:

- for 26 layers w.r.t. 30: ↗ +8.5%
- with 725µm w.r.t 500µm : ↘ –6.6% (-8.7% wrt to DBD 300µm)

near compensation



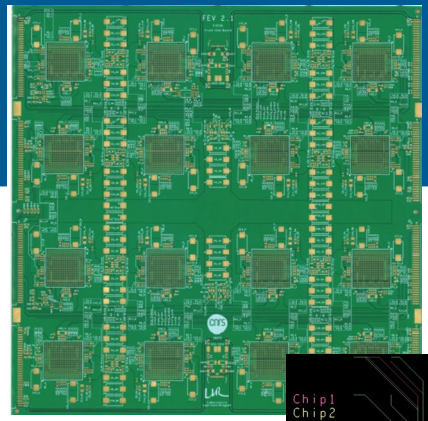


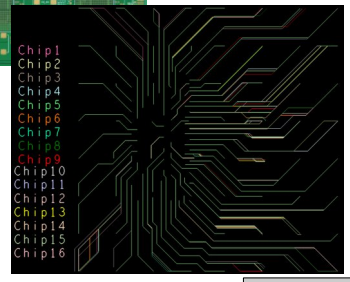


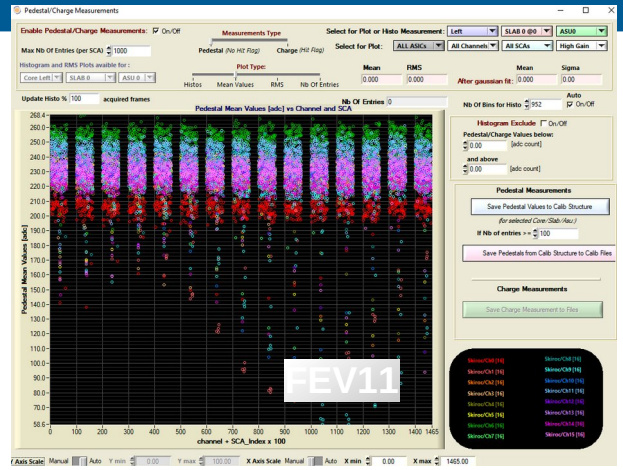
Study needed on dead zones (larger GR...), separation, resolution and efficiency performances at low energy.

- eg: JER : $\sigma(E_J)/E_J$ +6% for 26 layers (500 µm) to be redone...
  Shown @ 6th ILD Optim meeting (16/07/2014) [link]

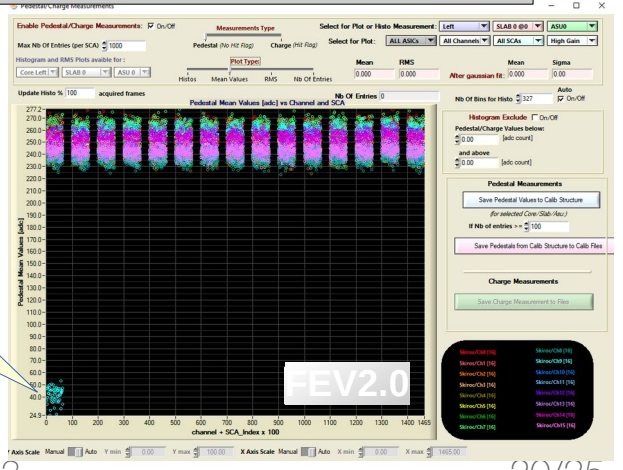
New FE boards







Pedestal measurements vs. Ch# + Mem#×100)



SIngle channel → the fault on the ASIC/packaging

Improvements:

- Power distributions
  - Local power regulation: LDO's
  - Local High Voltage filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing

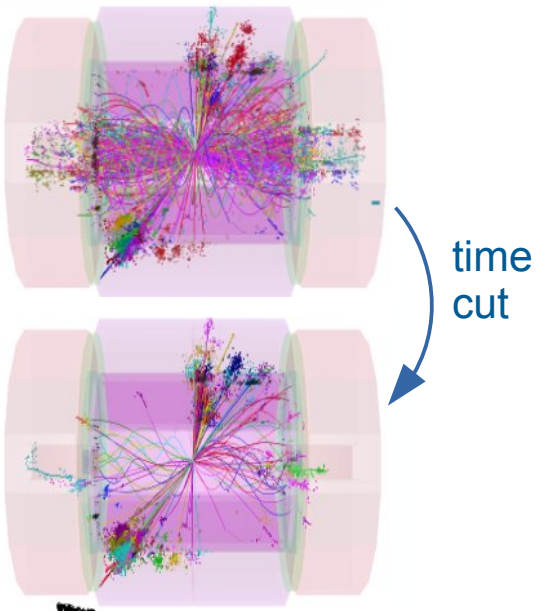
Status:

- pre-version 2.0 tested, minor corrections needed
  - Noise uniformity dramatically improved (ex: outliers in thr. / 20 !)
- version 2.1 produced, … in metrology
  - before cabling, 2nd metrology, gluing, …
  - All material available : ASICs being tested

Timing in Calorimeters: 0.1–1 ns range

1 cm/*c* = 30 ps

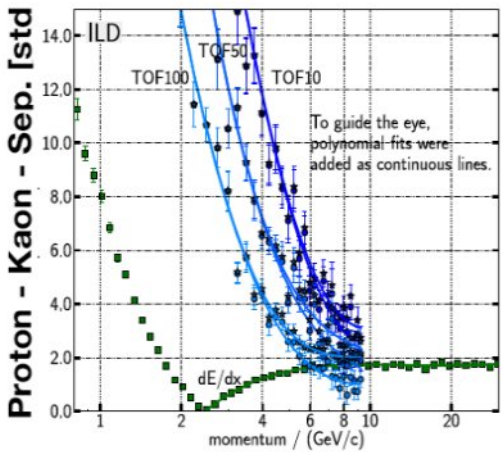
Cleaning of Events



[CLIC CDR: 1202.5940]
adapted from L. Emberger

Particle ID by Time-of-Flight

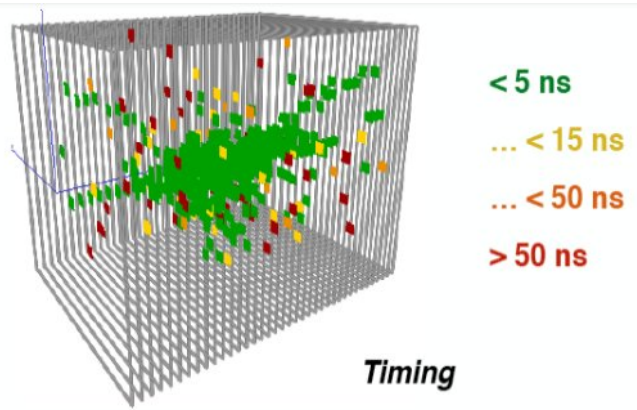
- Complementary to dE/d*x*
  - here with 100 ps on 10 ECAL hits



S. Dharani, U. Einhaus, J. List

Ease Particle Flow:

- Identify primers in showers
- Help against confusion
  better separation of showers
- Cleaning of late neutrons & back scattering.
- Requires 4D clustering

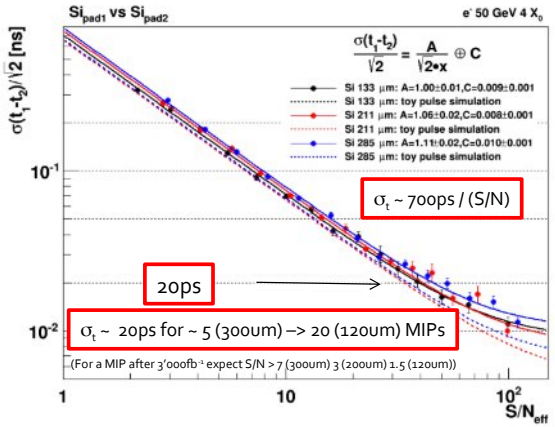


Ch. Graf

Timing Studies

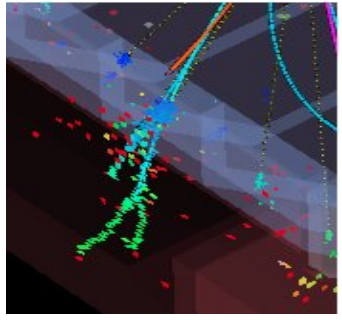
2015 CMS HGCAL CERN timing test beam

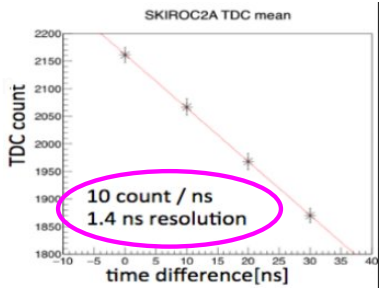
– Time resolution vs S/N ratio

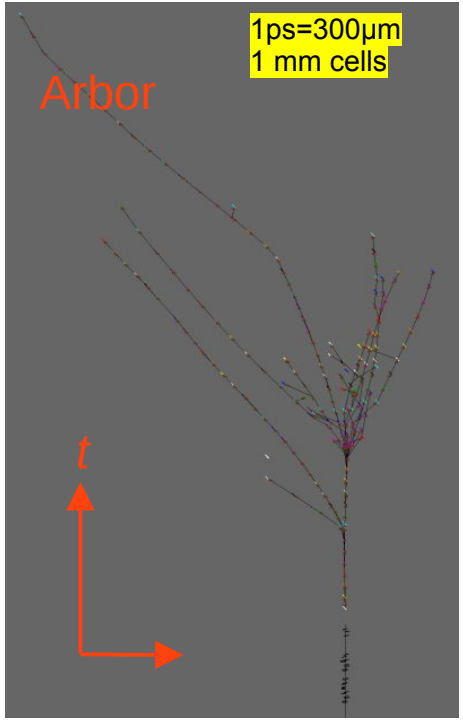


Transparent cells => no timing
Solid cells = > timing information ~50ps

Option 1) Bulk Timing





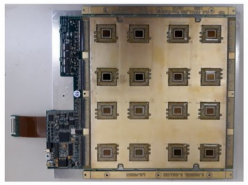


Option 2) Dedicated layers with fast sensors (LGADs, MAPs, …)

Technological Prototype beam test at DESY & CERN

FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014

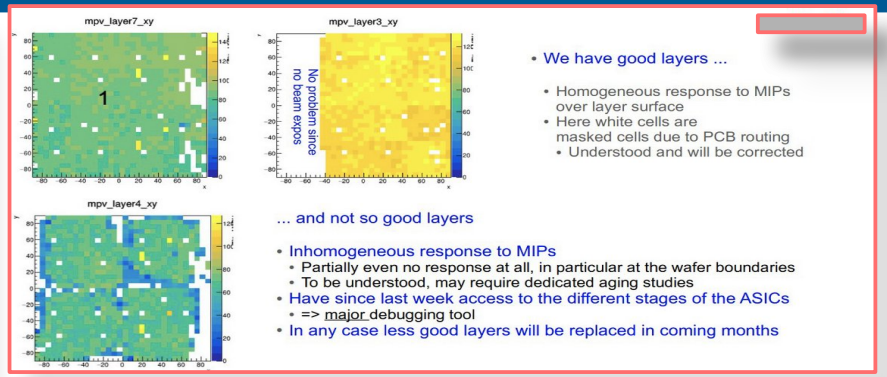


FEV-COB

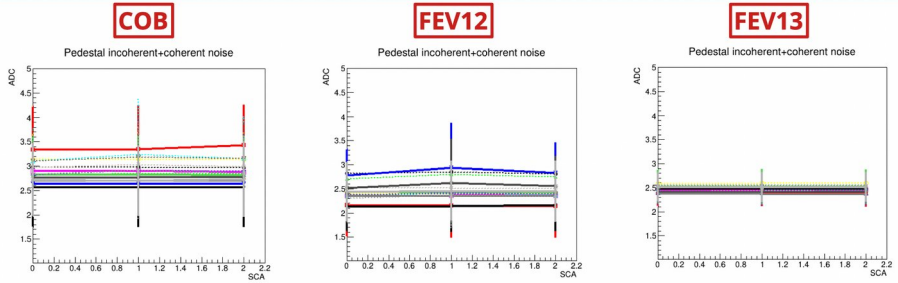
- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

FEV13

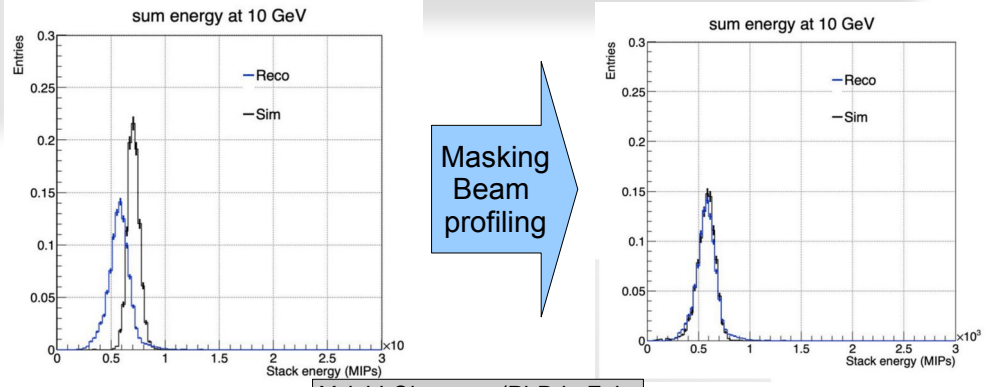
- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity



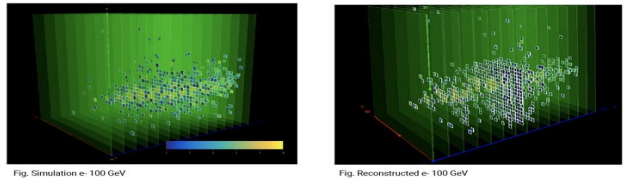
Pedestal widths, 1st memory cells, per asic



- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors



Yuichi Okugawa (PhD in Feb.



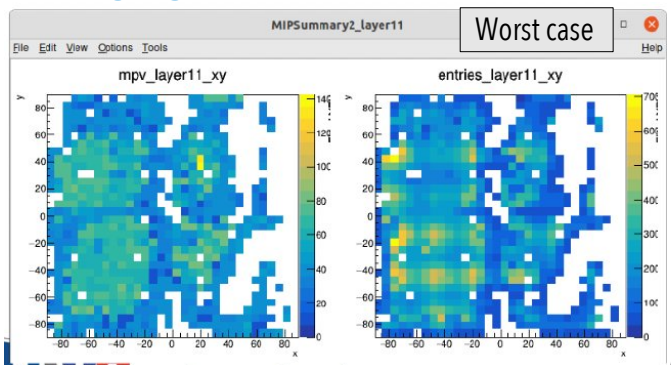
→ Homogenous prototype

Goal:

- 15 layers of FEV2.1 with 500µm wafers
  - Uniform and more perfornant electronics
  - Could be used for LUXE and Dark Photons exp's.
- All material available

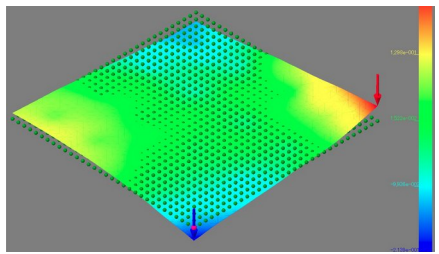
Main issue: contact PCB–Sensor

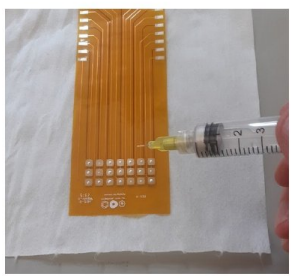
- Conductive glue dots of ∅2–3mm
- Aging, mechanical stress, manipulations, ...

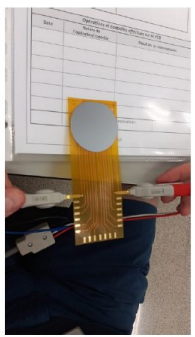


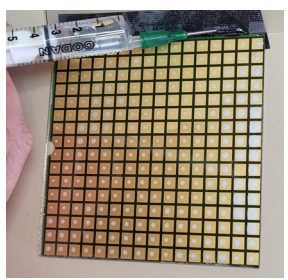
Revisiting gluing (IFIC, IJClab, LPNHE)

- PCB metrology
  - Bef. & After curing & soldering
- Glue formula & preparation
- Gluing methods
  - Robot
  - Stencil
- Reenforcement
  - Filling glue
  - Adhesive films









Conclusions

SiW-ECAL technological prototypes

- **2022:** Heterogeneous 15 layers
  - 1st full calorimeter working [DESY22, CERN22]
    - Shower seen, Detailled simulation ready
    - Analysis on-going → resolutions, ...
  - Numerous emerging issues
    - gluing, HV filtering at high energy
- **2024:** Uniform 15 layers
  - → New VFE boards
    - Cleaner PS & Clock distributions; more uniform
  - Gluing being revisited
  - Material available.
  - To be tested in 2024
    - → Provide reference sample for GEANT4
    - → With funding → "full" LUXE

SiW-ECAL design for HET factories

- **2023–26:** Power budget & performances to be re visited
  - Occupancy, power, data fluxes (on-going)
    - → Granularity; Passive or Active cooling
    - → new ASIC attributes
  - 2024–26: PFA & Timing & Physics performances

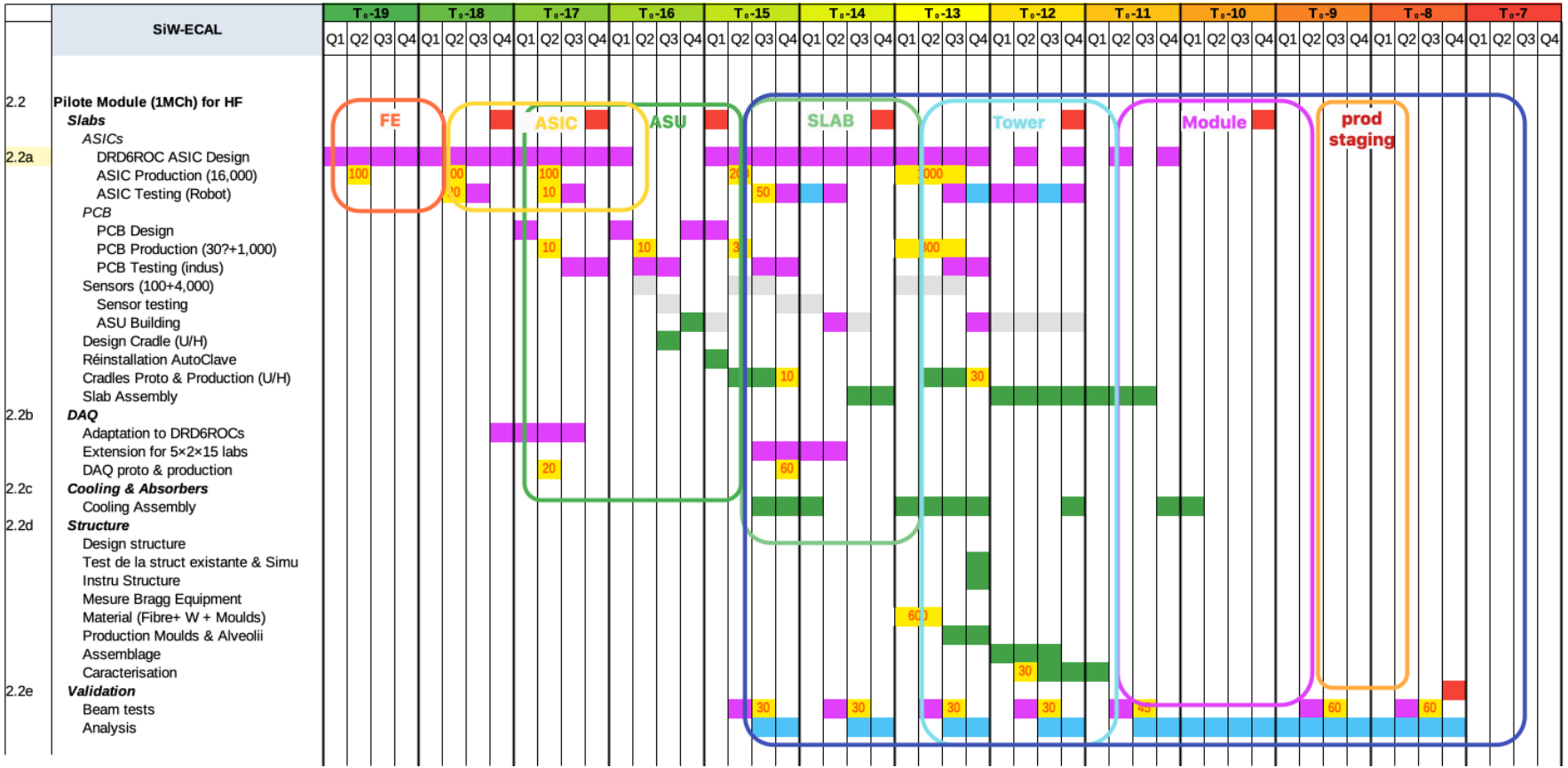
ANR

2025–26: Blue-print for a SiW-ECAL detector for the next ee collider

➡ planning for a pilote module @ T_0 collider-8y -5y (1 Mch, 1/60th of real detector)

semi-industrial, quality, ASICs, ...

Planning towards a pilot module… *just in case*



	T_0
FCCee	2045–48 ?
CEPC	2035 ?
ILC	2040 ?

Bonuses

Detector Parameters

- Cell lateral size
  - Shower separation (EM~2×cell size)
  - Cell time resolution (1cm/c ~ 30 ps)
    - Time performance for showers
      - ParticleID, easier reconstruction
- Longitudinal segmentation
  - sampling fraction
    - E resolution (ECAL ~15%/√E)
  - shower separation/start
- ECAL inner radius; Barrel Z_{Start}
- ECAL–HCAL distance
- Barrel–Endcap distance
- Dead-zones sizes (from Mechanics, Cooling)

Number of cells ↗ ⇒ Cost ↗
Cell density ↗ ⇒ Power consumption ↗
Time resolution ↘ ⇒ Power ↗

thr. passive vs active cooling
dead-zones ↗

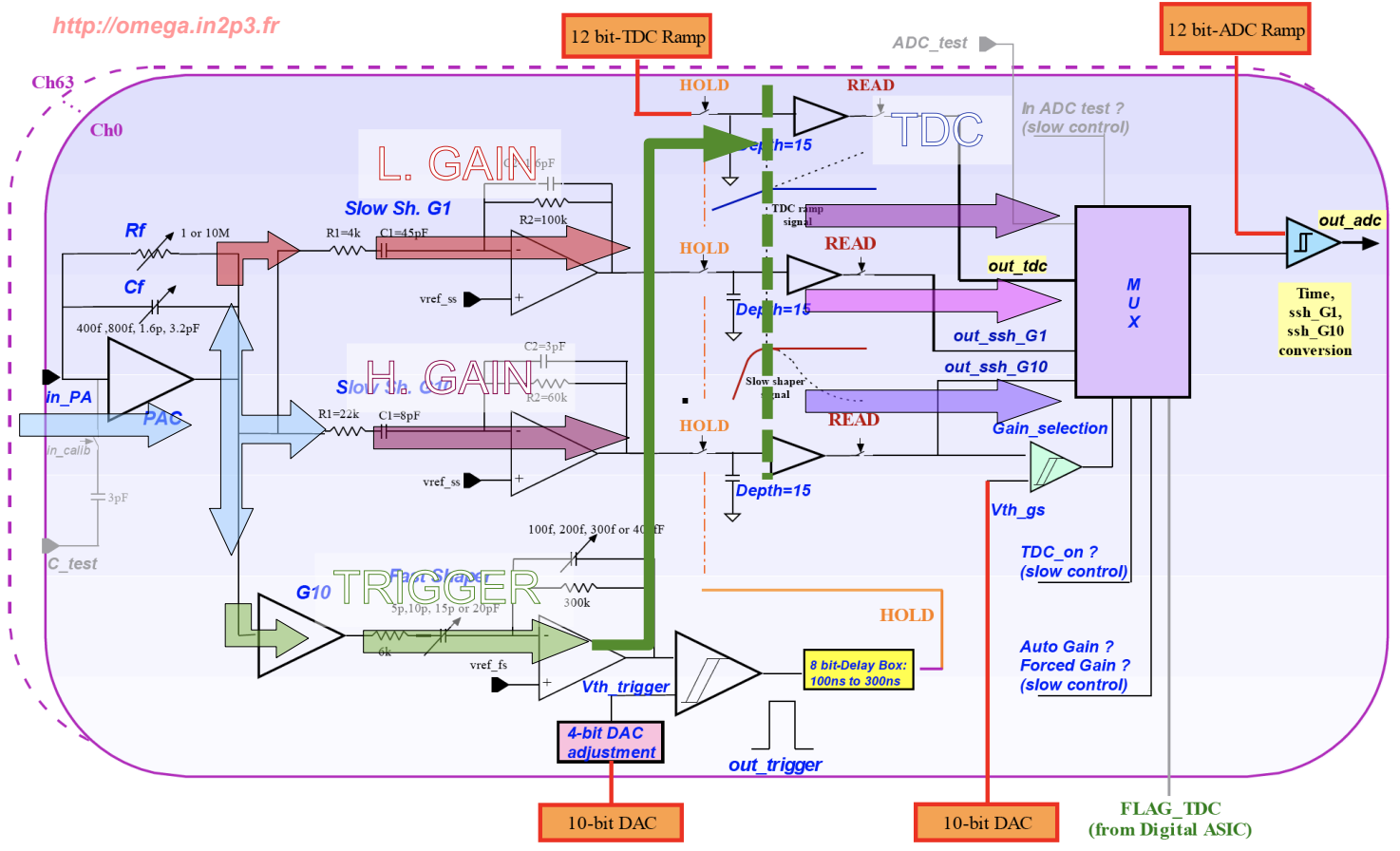
Inner Radius ↗ ⇒ Tracking performance ↗
Cost ↗² (⊃ Magnet, Iron)
Gaps ↗ ⇒ PFlow performances ↘

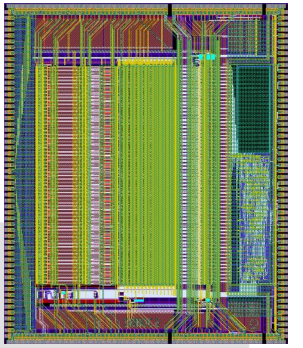
NEED TO BE FULLY RE-EVALUATED

Review of physical implication (from TeV): see Linear collider detector requirements and CLD, F. Simon @ FCC-Now (nov 2020)
Physics Requirement studies @ 250 GeV: see Higgs measurements and others, M. Ruan @ CEPC WS, (nov 2018)

ΩMEGA Microelectronics

http://omega.in2p3.fr





- **64 channels**
- **Auto-triggered**
  - per cell adj.
  - 1 cell triggers all
- Preamp
  + **2 Gains** + Auto-select
  + **TDC** (~1.4ns)
- 15 (×2) analogue memories
- Dyn range 0.1 ~ 2500 mips
  - mip in 320 µm (4 fC)
  - 12 bits ADC's
- *616 config bits*
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-Pulsed

Implication of HL schemes

Higher $\mathscr{L}$ ⇒

- Occupation / bunch train ↗
  - More memory for events
    - But large margins

Higher repetition rates × longer bunch

- Power = $f_{rep} \times \sum P_{ASIC\_part} \times \tau_{spill\_part}$
  - $\tau_{spill} = \tau_{Ramp\text{-}up} + \tau_{Train} + \tau_{Conv}$
    $= \mathcal{O}(\mu s) + \{ \ldots \} + \mathcal{O}(100's\ \mu s)$
    - $\tau_{Train} = \Delta T_{bunches} \times N_{bunches}$
    - $\tau_{Conv} \propto$ (occupancy + Noise ≥ thr.)

Critical also for Power budget

⇒ Full ZERO suppr. needed

HL-ILC:

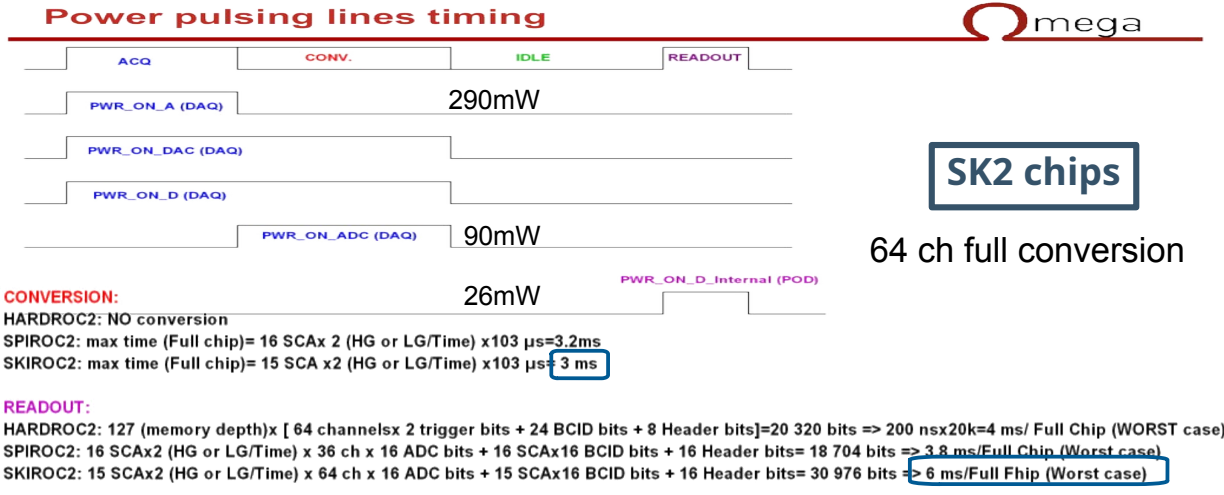
- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : τ_{Train} : 1 → 2 ms
- f_{rep} ×2 (3): 5 → 15 Hz

Dominated by ACQ time:
P(~25µW/ch) ×

HL-CLIC:

- $\mathscr{L}$ × 2
- $N_{bunches}$ → : τ_{Train} : 176 ns
- f_{rep} ×2 : 50 → 100 Hz

Dominated by Set-up &
Conversion time: P (~82µW/ch) ×2



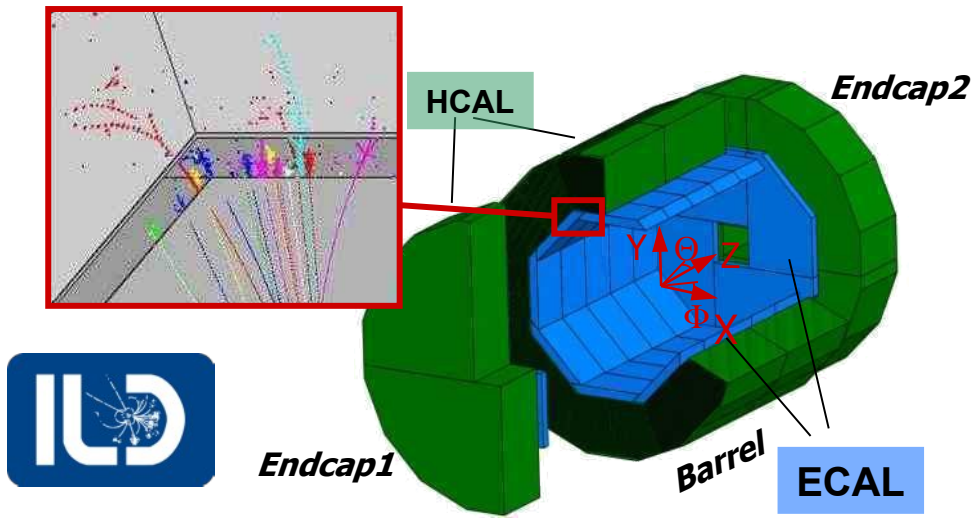
SK2 chips

64 ch full conversion

ILD Rationale & Adaptation

ILD high granularity calorimeters

- Designed for ILC
  - Power pulsing, low occupancy
- Marginaly adapted for CLIC and CLD
  - Physics : number of layers ↗ 40 (ECAL)
- Partially adapted for CEPC
  - Lower granularity (2×2 cm² ECAL)
- Needs strong adaptation for EW physics and continuous operation
  - Rates, Heat, Electronics



ECAL: 30 layers

- SiW-ECAL": 0.5×0.5 cm³ Si cells
- ScECAL: 0.5×5 cm² Scint strips

10–100M channels

HCAL: 48 layers

- AHCAL: 3×3 cm³ scint. cells
- ScECAL: 1×1 cm² RPC cells

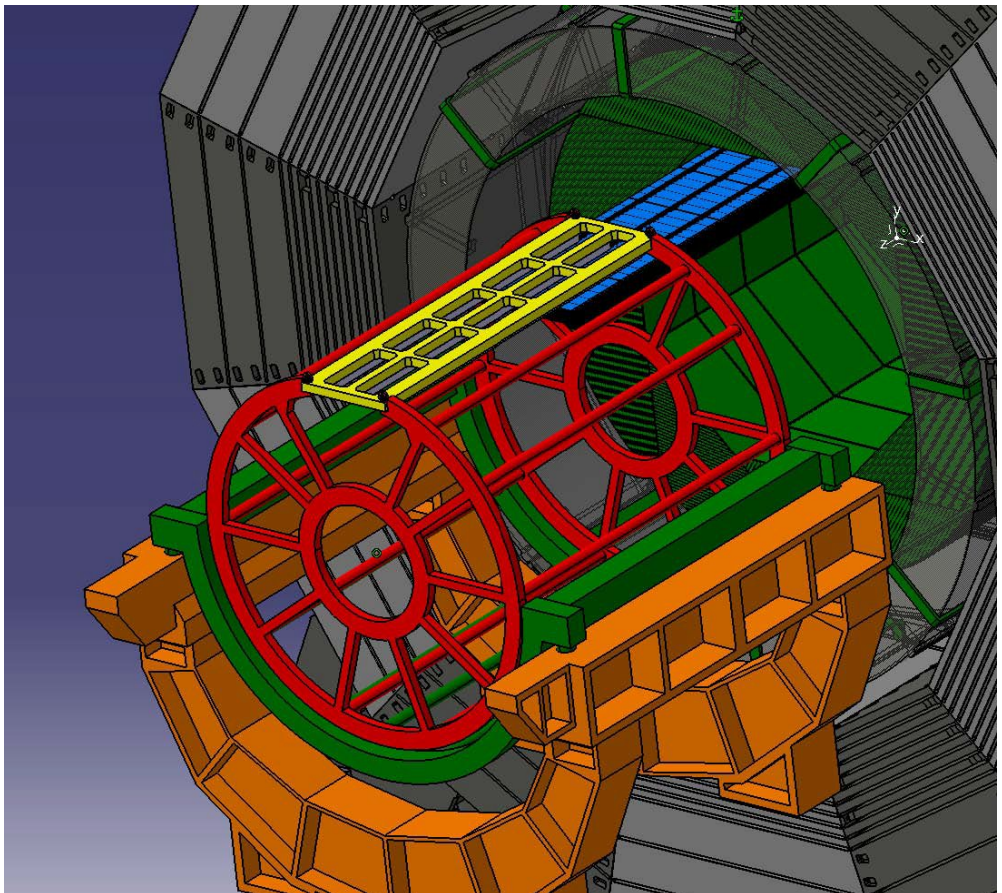
10–70M channels

Building tools and procedure

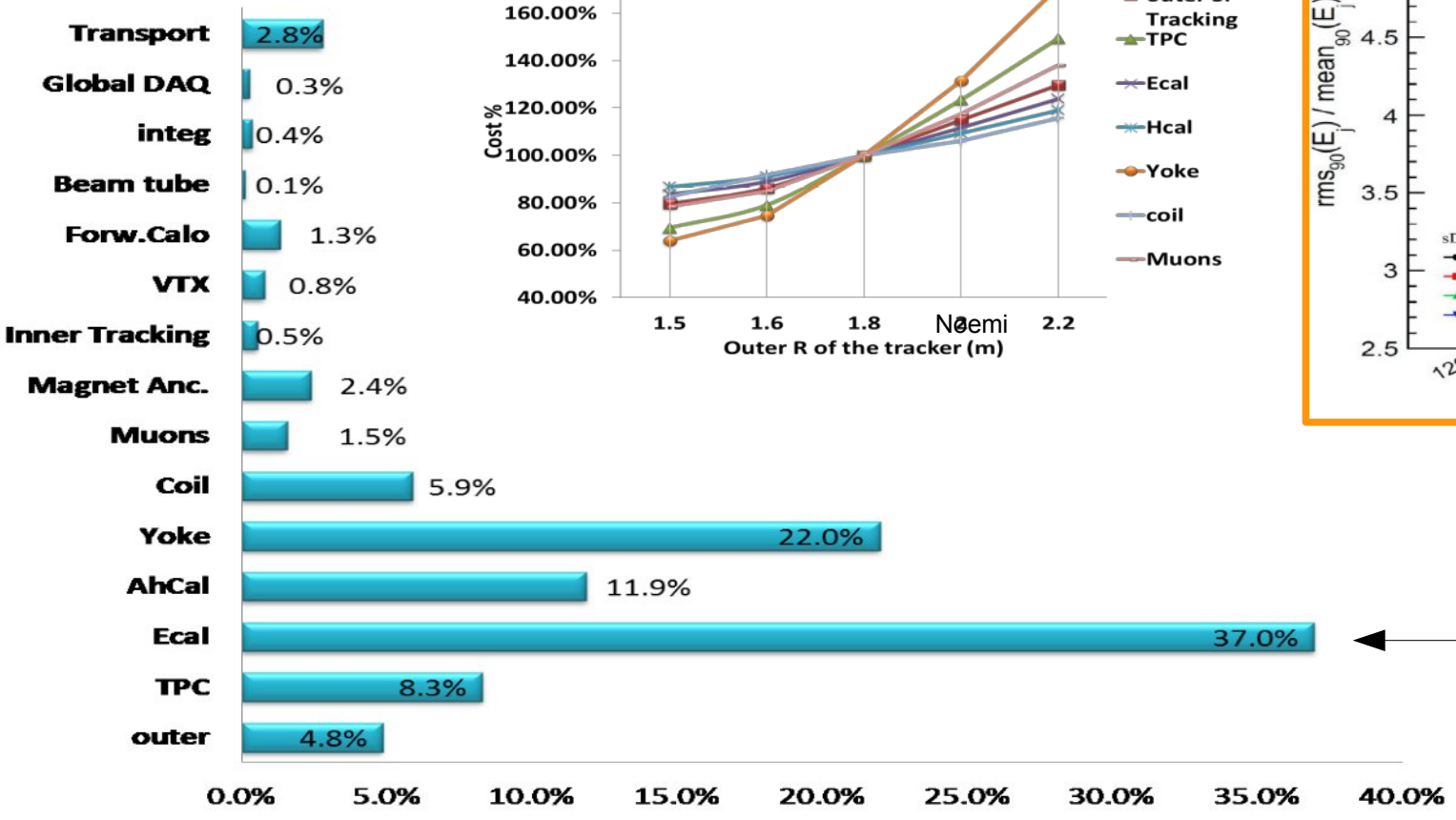
Documented for ILD

– incuding space and manpower estimations

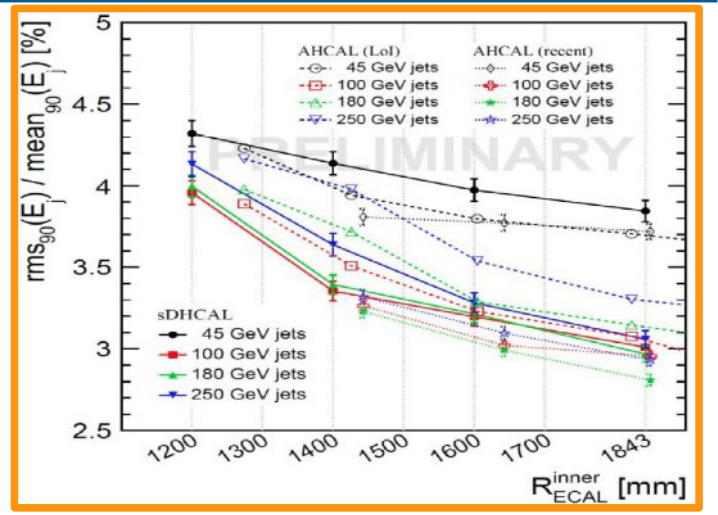
Handling and positioning tool for integration & tests



Cost Structure of ILD

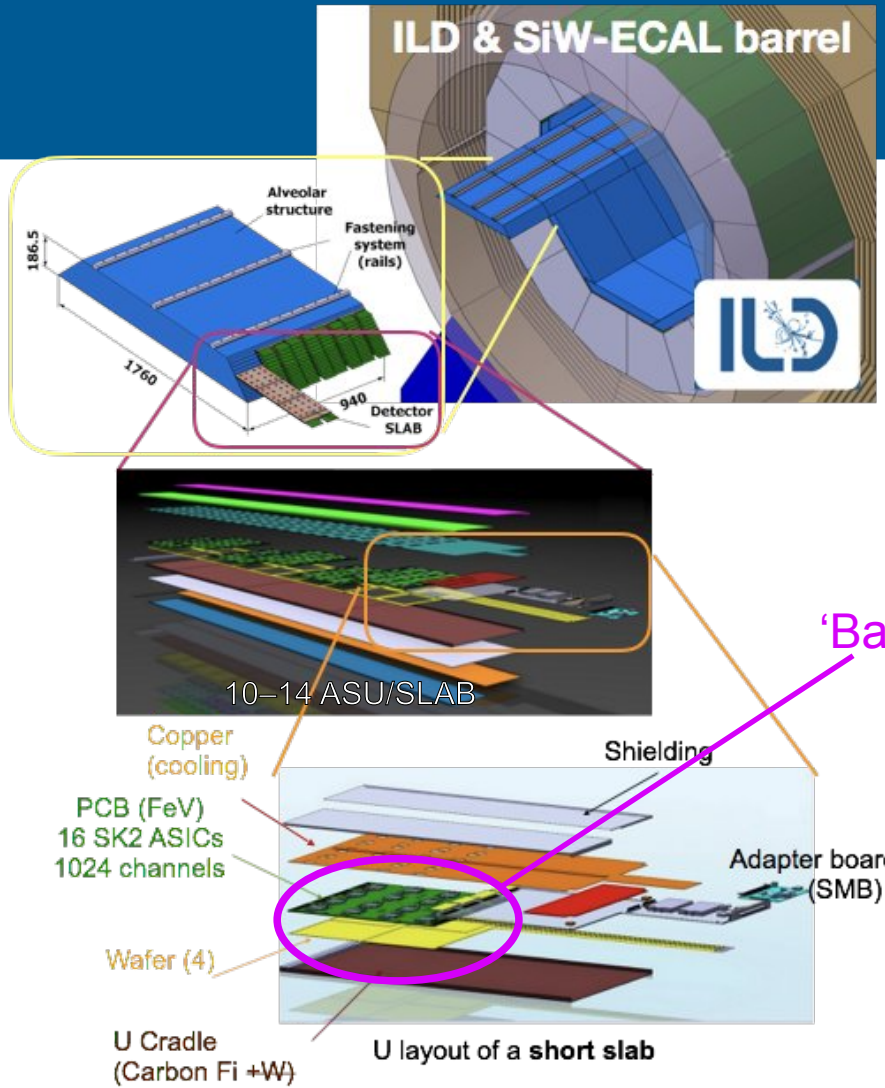


Noemi



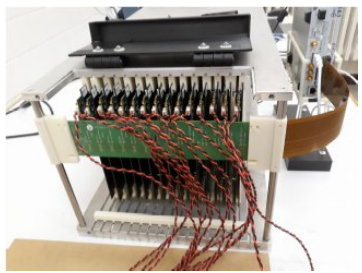
Full Silicon option

Large Scale Building : CALICE ECALs



ILD ECAL

	Prototyped*
~10,000 SLAB's	~0.1
100,000 ASU's	~20
400,000 Wafers	~350
1,600,000 ASIC's	~1000
100,000,000 channels	~20000
	*incl.



SiW-ECAL
0,5×0,5 cm²
×15 couches +W

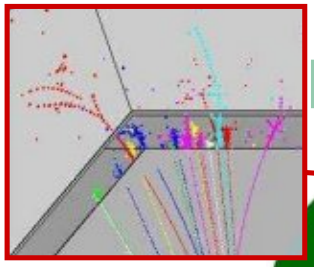
ScW-ECAL
0,5×4,5 cm²
×30 layers + SS

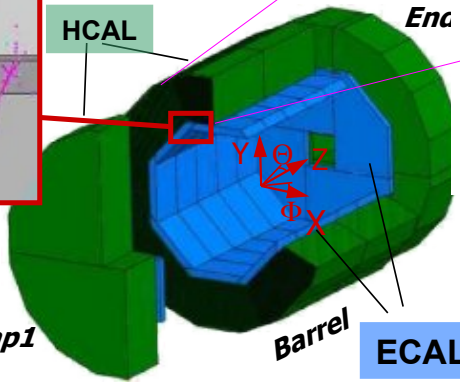
See Adrian's presentation

Geometries & Services

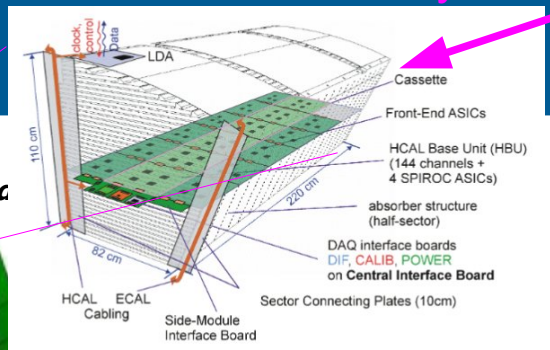
HCAL elec ‘accessibilty’

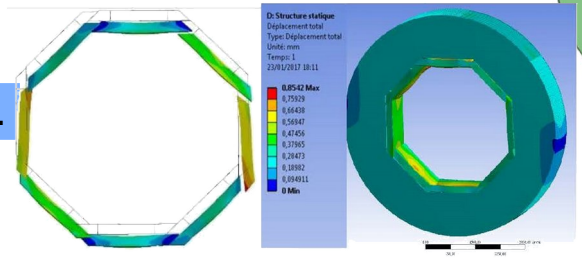
Prism vs diapragm

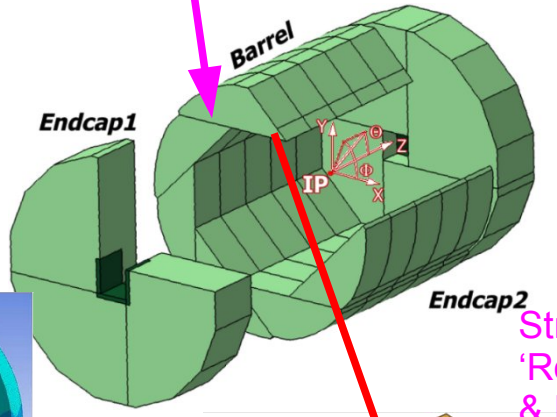




(SiD = 12 fold)







Structural ‘Robusteness & Precision’