



# CMOS TPSCo 65 nm technology R&D

Motivations

ALICE ITS-3

R&D with CE65 prototypes

Future R&D & plans

# CMOS-MAPS for charged particle detection

## Main features

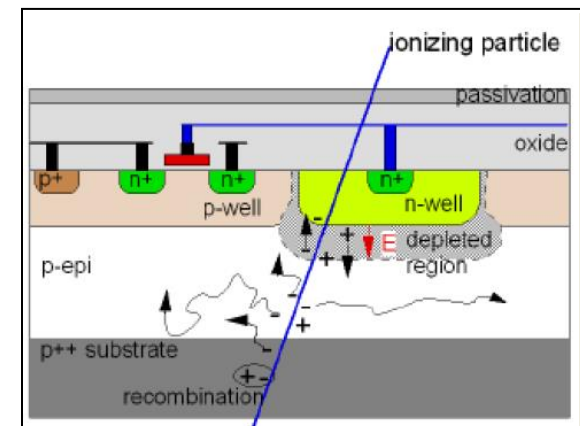
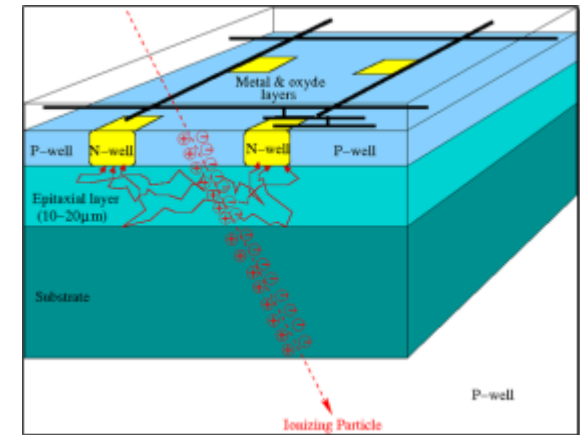
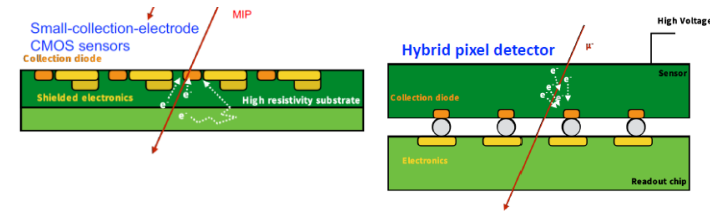
- ✓ Monolithic, p-type Si
  - Signal created in low doped thin epitaxial layer  $\sim O(10) \mu\text{m}$
  - $\sim 80 \text{ e}^-/\mu\text{m} \Rightarrow$  total signal  $\sim O(1000 \text{ e}^-) \Rightarrow$  low noise electronic
- ✓ Charge collection: diffusion of  $\text{e}^- \Rightarrow$  N-Well diodes
  - Partial depletion  $\Rightarrow$  Charge sharing  $\Rightarrow$  resolution
  - Possible full depletion  $\Rightarrow$  Higher S/N & rad. tol.
- ✓ Continuous charge collection

## Main advantages

- ✓ Granularity
  - Pixel pitch down to  $10 \times 10 \mu\text{m}^2 \Rightarrow$  spatial resolution down to  $\sim 1 \mu\text{m}$ )
- ✓ Material budget
  - Sensing part  $\sim 10\text{-}20 \mu\text{m} \Rightarrow$  whole sensor routinely thinned down to  $50 \mu\text{m}$
- ✓ Signal processing integrated in the sensor
  - Compacity, flexibility, data flux
- ✓ Flexible running conditions
  - From  $\leq 0^\circ\text{C}$  up to  $30\text{-}40^\circ\text{C}$  if necessary
  - Low power dissipation ( $\sim 150\text{-}250 \text{ mW}/\text{cm}^2$ )  $\Rightarrow$  material budget
  - Radiation tolerance:  $>\sim \text{MRad}$  and  $O(10^{13\text{-}14} \text{ n}_{\text{eq}}) \Rightarrow f(T, \text{pitch})$
- ✓ Industrial mass production
  - Advantages on **costs**, yields, fast evolution of the technology,
  - Possible frequent submissions
  - Smaller feature size, adapted epitaxial layers, doping profile to enhance depletion

## Main limitations

- ✓ Industry addresses applications far from HEP experiments concerns
  - Different optimizations on the parameters on the technologies
  - **R&D costs**
- ✓ High expertise needed (from design to tests & characterizations)
- ✓ Long R&D needed for a given application



# Synergies

K. Jakobs, FCC Physics Workshop, Feb 2022

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. **ECFA supports a series of workshops** with the aim to **share challenges and expertise, to explore synergies in their efforts** and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).

Goal: bring the entire  $e^+e^-$  Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge



Important similarities between FCCee requirements & Heavy ions experiments (ALICE ITS3, ALICE3, EIC, etc.)

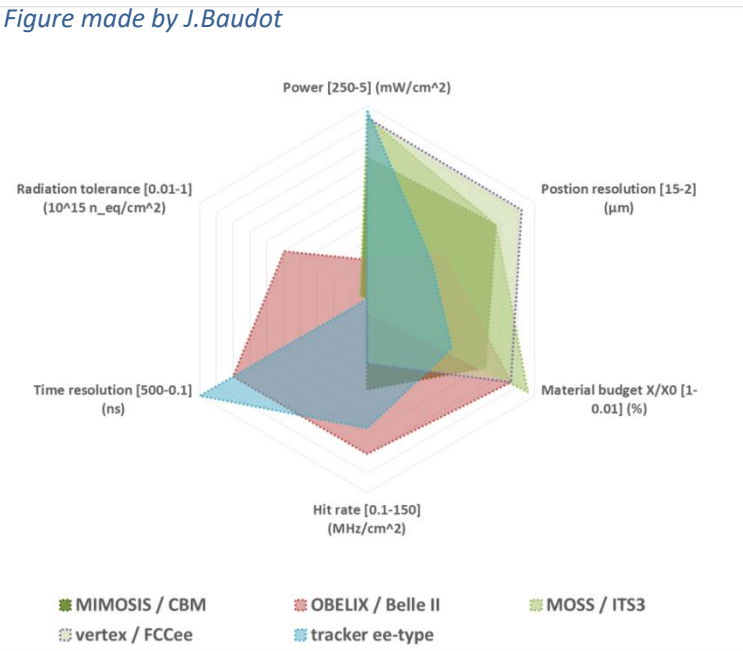
- Spatial resolution < 5  $\mu$ m
- Low material budget ( $\sim 0.15\%$   $X_0$ /layer)
- Low Power (<100 mW/cm<sup>2</sup>)

● Must happen or main physics goals cannot be met   
 ● Important to meet several physics goals   
 ● Desirable to enhance physics reach   
 ● R&D needs being met

# Pixel detector requirements

	past		present				future					
	MIMOSA28 STAR	ALPIDE ITS2	MIMOSIS CBM	OBELIX Belle II	MOSS ITS3 ALICE	ITK R&D ATLAS	Vertex ALICE3	vertex FCCee	Tracker ALICE3	tracker ee-type	Up. Tracker LHCb	Tracker hh-type
Power (mW/cm <sup>2</sup> )	170	35	70	200	20	200,0	20	20	10	10	100	100
Position res. (μm)	4	5	5	9	5	10,0	2.5	3	10	5-10	10	15
Mat. budget X/X <sub>0</sub> (%)	0,37	0,3	0,3	0,15	0,05	1,0	0,05	0,15	0,5	0,5	0,3	1
Hit rate (MHz/cm <sup>2</sup> )	0,1	1	70	120	10	120,0	35	50	0,005	10-100	200	200
Time resolution (ns)	200000	5000	5000	100	5000	25,0	100	500	100	1-500	1	0,1
Rad. tolerance (10 <sup>15</sup> n <sub>eq</sub> /cm <sup>2</sup> )	0,001	0,05	0,05	0,5	0,05	2,0	1	0,0011	0,01	0,001-1	3	9
Sensor size (cm <sup>2</sup> )	4,6	4,5	5,4	5,7	300,0	5,0	300,0	6,0	100,0	100,0	6,0	100,0

Figure made by J.Baudot



« high granularity vertex »  
(MIMOSIS, ALICE ITS-3, FCCee vtx, ALICE3 vtx)

GRAM Master project



« outer trackers »  
(Belle-II trk, ALICE-3 trk, FCCee trk)

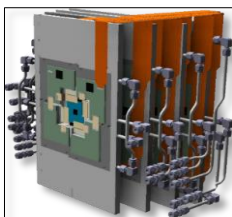
DEPHY Master Project



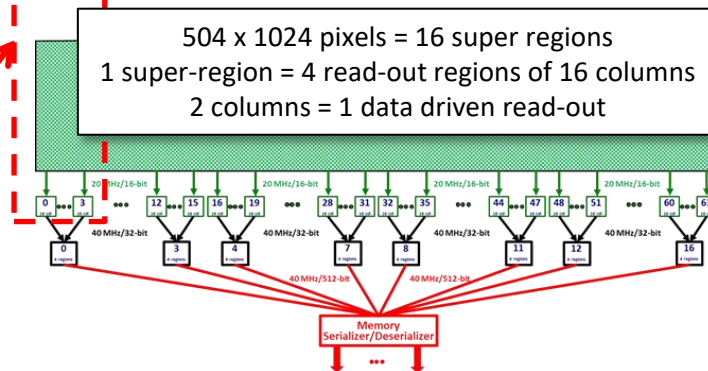
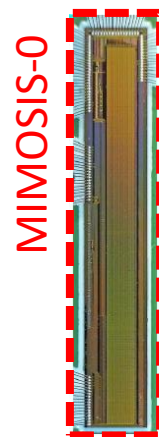
« high flux & rad. tol. »  
(ATLAS, LHCb upgrades, FCC hh)



# 180 nm: MIMOSIS roadmap



Physics parameter	Requirements
Spatial resolution	~ 5 $\mu\text{m}$
Time resolution	~ 5 ns
Material budget	0.05% $X_0$
Power consumption	< 100 – 200 mW/cm <sup>2</sup>
Operation temperature	- 40 °C to 30 °C
Temp gradient on sensor	< 5K
Radiation tol* (non-ion)	~ 7 x 10 <sup>13</sup> n <sub>eq</sub> /cm <sup>2</sup>
Radiation tol* (ionizing)	~ 5 MRad
Data flow (peak hit rate)	@ 7 x 10 <sup>5</sup> / (mm <sup>2</sup> s) > 2 Gbit/s



## MIMOSIS-0:

- ✓ Tests (2018-2019)

## MIMOSIS-1: 1<sup>st</sup> full size prototype

- ✓ Elastic buffer, SEE hardened
- ✓ Fabricated in 2020
- ✓ Intense test campaign in 2021-22
  - Lab and beam tests
  - Irradiations
  - Latchup tests

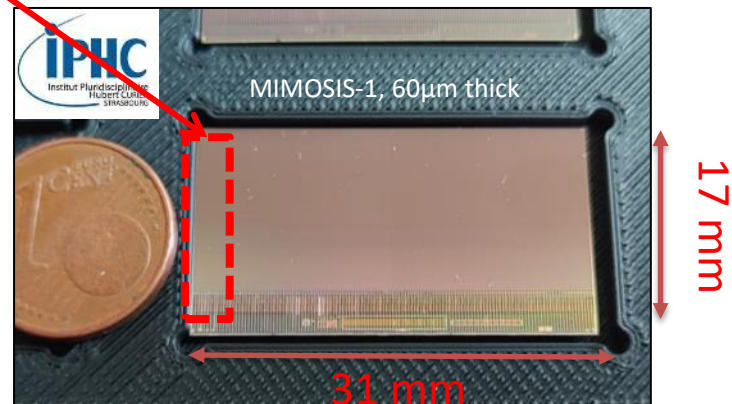
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	~ 25 $\mu\text{m}$
Epi layer resistivity	> 1k $\Omega\text{cm}$
Sensor thickness	60 $\mu\text{m}$
Pixel size	26.88 $\mu\text{m}$ x 30.24 $\mu\text{m}$
Matrix size	1024 x 504 (516096 pix)
Matrix area	~ 4.2 cm <sup>2</sup>
Matrix readout time	5 $\mu\text{s}$ (event driven)
Power consumption	40-70 mW/cm <sup>2</sup>

## MIMOSIS-2:

- ✓ On-chip clustering
- ✓ Triplication added
- ✓ Back from foundry Q2 2023
- ✓ Issues  $\Rightarrow$  resubmission of MIMOSIS 2.1 Q4 2023

## MIMOSIS-3: final pre-production sensor

- ✓  $\geq 2025$



$\Rightarrow$  architecture adaptable to a fast sensor for a future e<sup>+</sup>e<sup>-</sup> collider vertex detector

$\Rightarrow$  Know-how maintained for large scale sensors

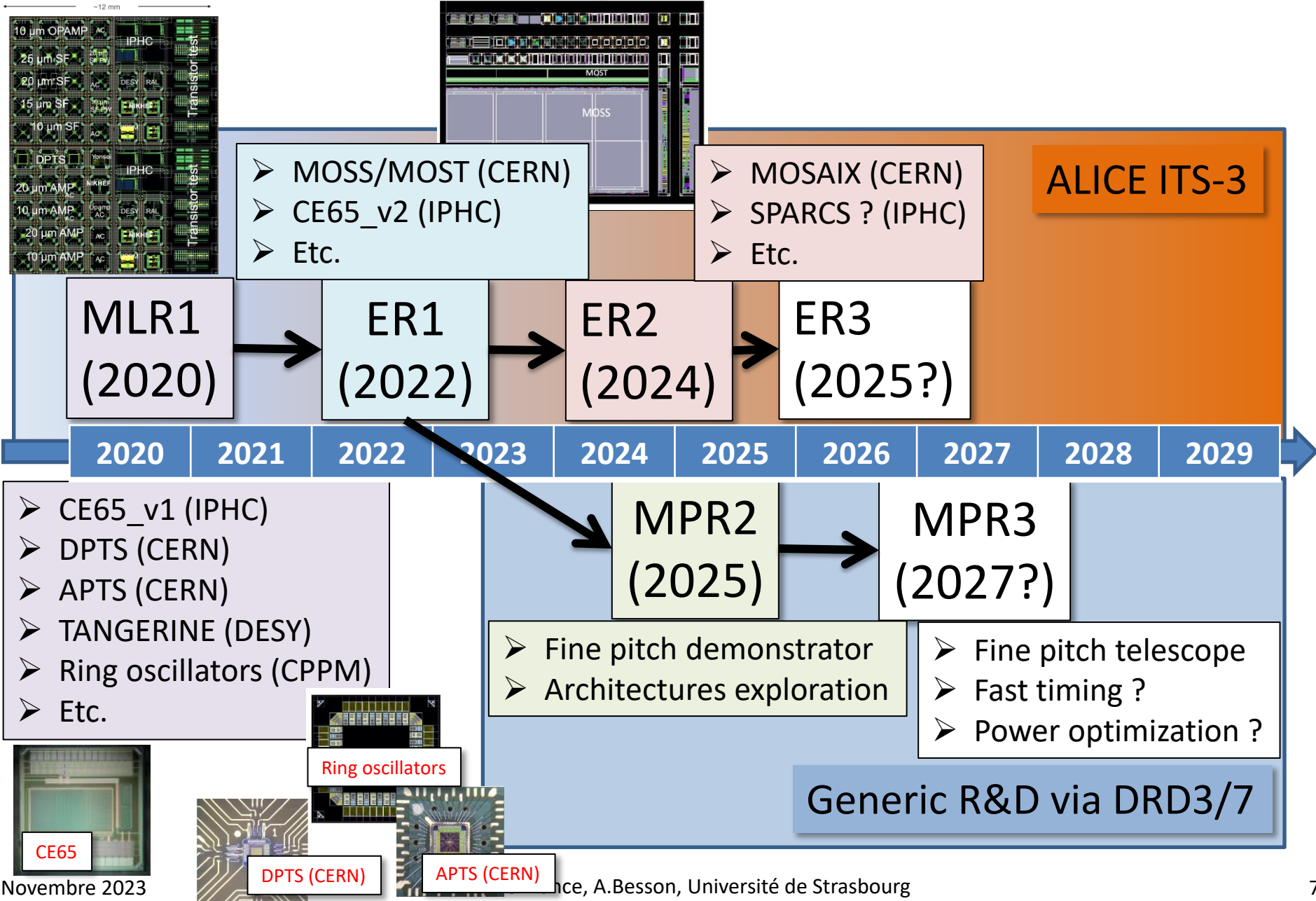
$\Rightarrow$  Opportunity to study different designs/options

# Moving from 180 nm to 65 nm

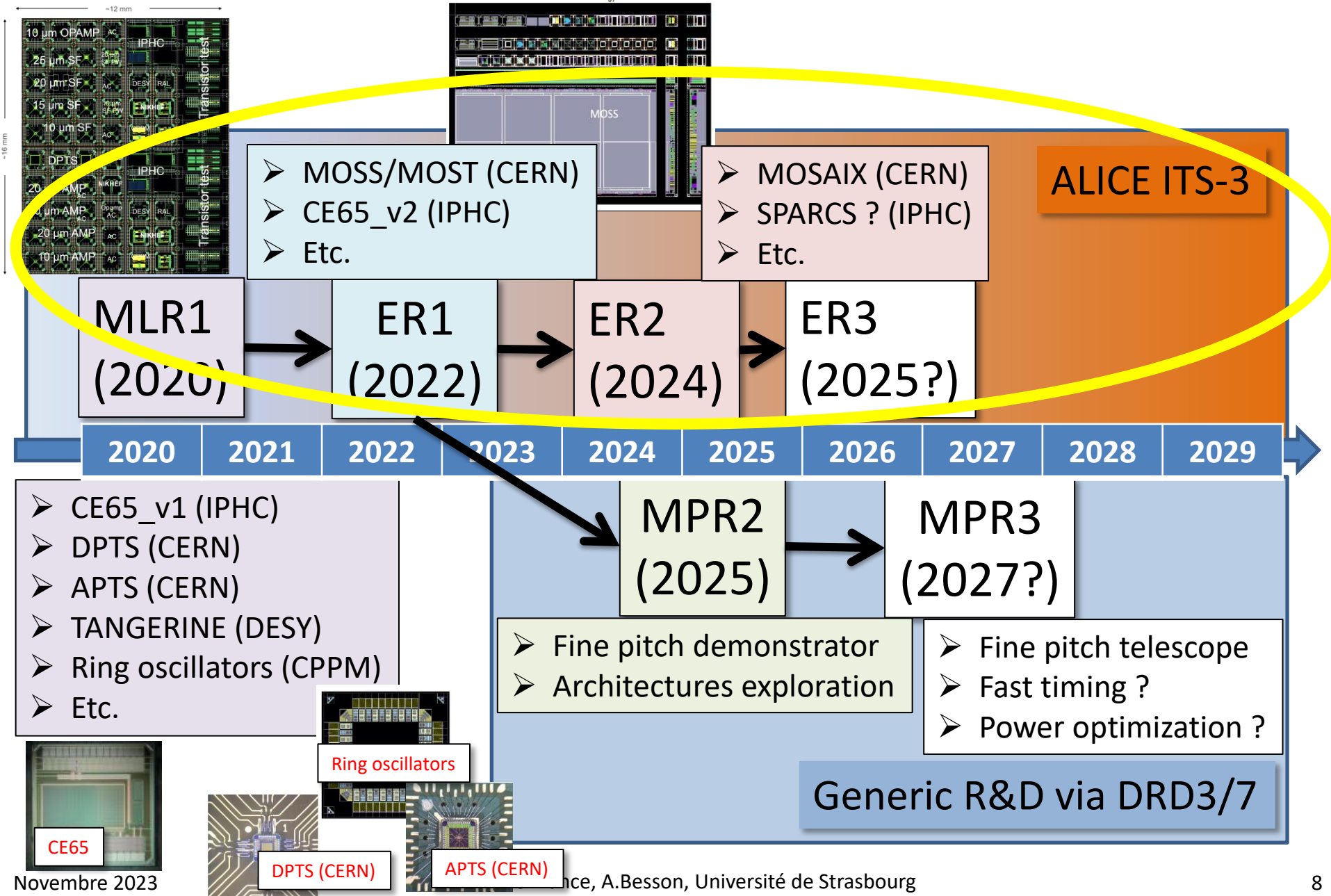
Technology	TowerJazz 180 nm	TPSCo 65 nm
Available since	2013 ( mature technology)	2020 (access through CERN)
Large surface projects	<ul style="list-style-type: none"> <li>• ALPIDE for ALICE ITS-2</li> <li>• MIMOSIS for CBM-MVD</li> <li>• OBELIX for Belle-II upgrade</li> </ul>	<ul style="list-style-type: none"> <li>• MOSAIX for ALICE ITS-3</li> <li>• DRD3/7 R&amp;D ?</li> </ul>
Price	affordable	More expensive
Wafer	<ul style="list-style-type: none"> <li>• 8 inches (20 cm)</li> </ul>	<ul style="list-style-type: none"> <li>• Larger: 12 inches (30cm)</li> </ul> ⇒ stitching + bent sensors
Epitaxial layer thickness	<ul style="list-style-type: none"> <li>• 18/25/30/40/50 <math>\mu\text{m}</math></li> </ul>	<ul style="list-style-type: none"> <li>• 10</li> </ul>
Process options	<ul style="list-style-type: none"> <li>• « standard »</li> <li>• « modified », « gap »</li> </ul>	<ul style="list-style-type: none"> <li>• « standard »</li> <li>• « modified », « gap »</li> </ul>
Technology	<ul style="list-style-type: none"> <li>• Feature size (180 nm)</li> <li>• V (1.8V)</li> <li>• 6 Metal Layers</li> </ul>	<ul style="list-style-type: none"> <li>• Feature size (65nm)</li> <li>• Lower V (1.2 V)</li> <li>• 7 Metal layers</li> </ul> ⇒ Pitch reduction, power saving, more fonctionnalites, etc.

⇒ Strong motivations to switch to a smaller feature size to increase the performances space

# TPSCo 65nm Submissions

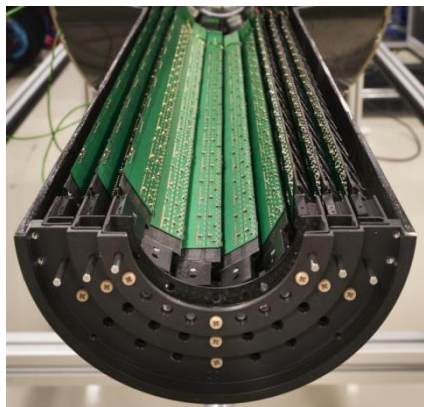
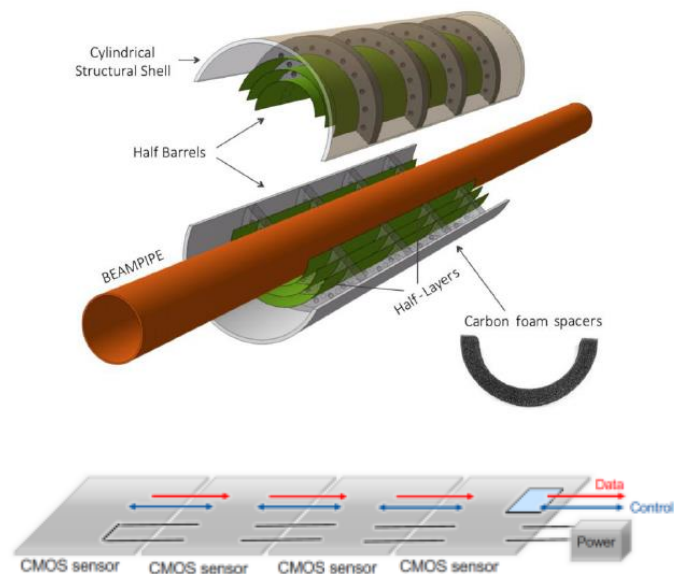
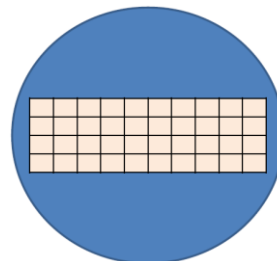
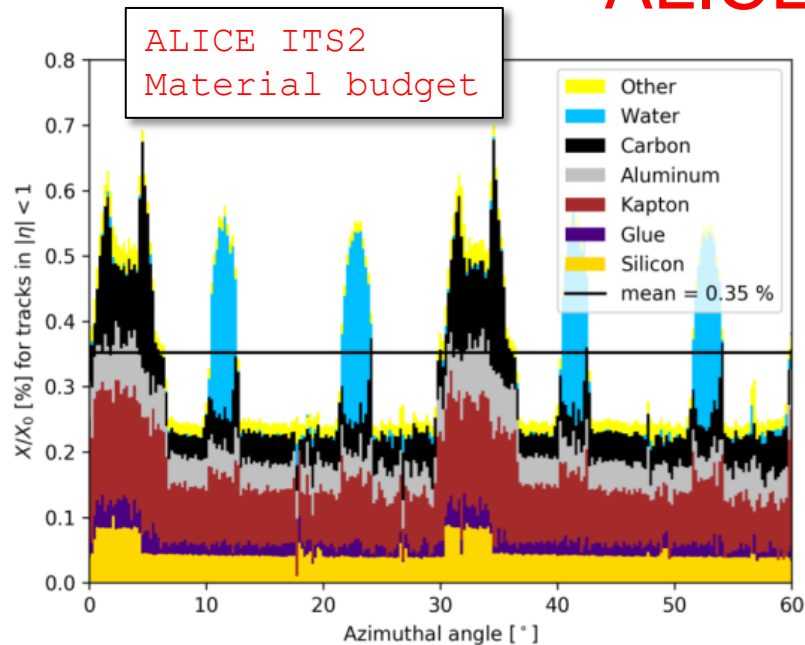


# TPSCo 65nm Submissions



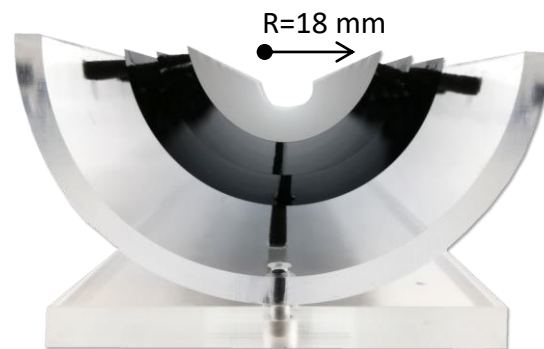


# ALICE ITS-3 (Run4)



## ITS2:

- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size:  $27 \times 29 \mu\text{m}^2$
- Water cooling
- **0.3 %  $X_0$  / inner layer**



## ITS3:

- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to  $27 \times 9$  cm
  - Thickness 30-40  $\mu\text{m}$
  - No FPCs
  - Air cooling in active area
- **0.05 %  $X_0$  / inner layer**

⇒ ALICE ITS-3 paves the road for the stitched sensor approach

# How to adapt ITS-3 approach to FCCee ?

ALICE-ITS3/CERN drives the R&D on stitching + bent sensors:

- ✓ Sensor part ~15% of total material budget
- ✓ Sensors thinned down to 50  $\mu\text{m}$  or less ?
  - Tests performed by ALICE
- ✓ Minimizing overlapping regions,
- ✓ minimizing minimal radius around the beam pipe

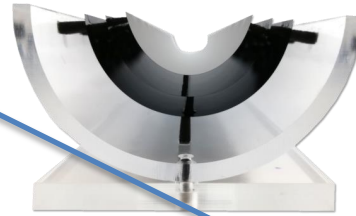


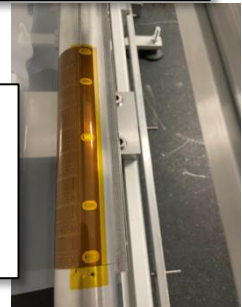
Figure 4.42: Setup for the bending strength measurements.

Challenges and caveats (for  $e^+e^-$  colliders)

- ✓ Mechanics ? Bonding ? Air cooling only ?
- ✓ Design: Minimizing peripheral circuits (Fill factor ~90%)
- ✓ Bent sensor performances ? Yield ? Radiation hardness ?
- ⇒ design rules constraints the minimal pitch (~22  $\mu\text{m}$ )
- ✓ ITS-3 do not have disk (chip periphery adds Z position constraint)
- ✓ Approach validated in a limited radius range ( $R > 18\text{mm}$ ) ?
  - Trials performed by ALICE down to  $R = 10\text{mm}$

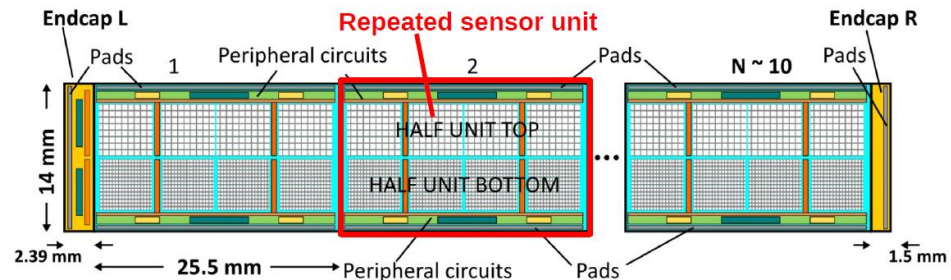
Questions potentially addressed by GRAM with MIMOSIS

1st bending tests by C4PI microtechnics

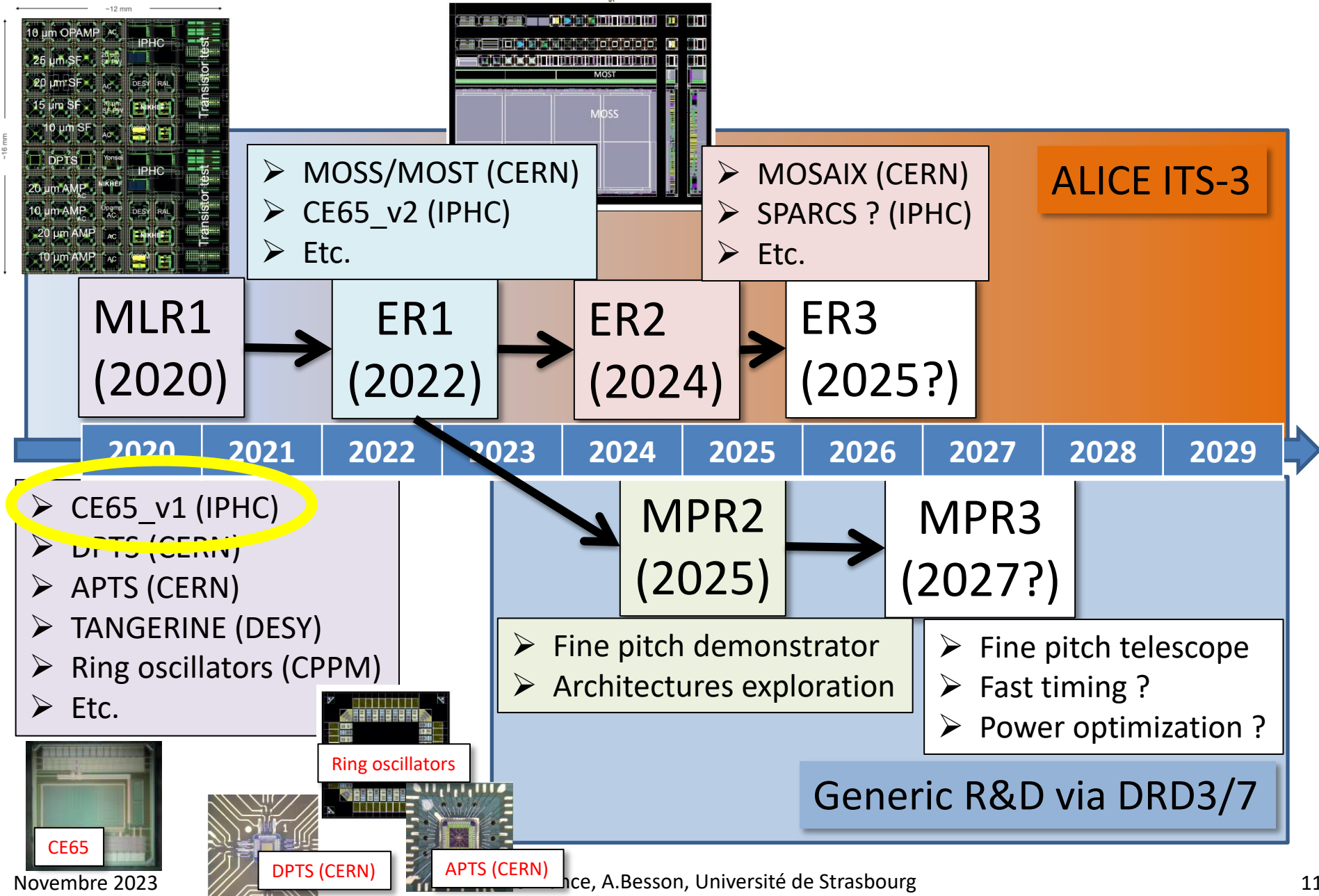


ALIC ITS-3 Significant contributions from IPHC (C4PI, ALICE, PICSEL)

- ✓ MOSS
  - Read-out line
  - Standard cells designs
  - DACs
- ✓ MOSAIX
  - Feasibility studies
  - Matrix assembly (pixel analog + digital + readout)
  - Column read-out in the matrix
  - Digital & Analog pixel (driven by CERN)
  - Standard cells with low leakage current
  - Biasing blocks (DACs)



# TPSCo 65nm Submissions



# CE\_65v1 (MLR1 submission)

- ✓ prototype designed @ IPHC
- ✓ Analog output, various designs (pitch, amplification)

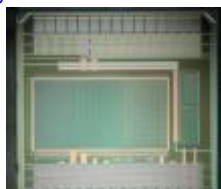
# CE65\_v1



PICSEL



C4PI-Platform



CE-65 (IPHC)

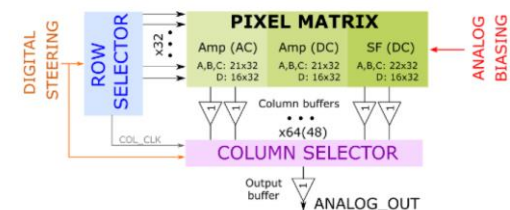
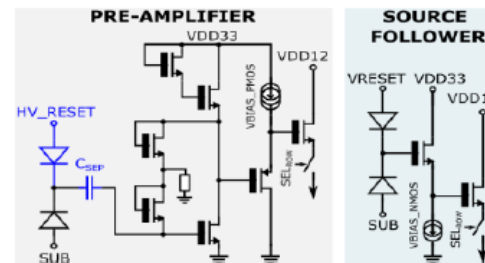


# CE\_65v2 (ER1 submission)

- ✓ 18/22  $\mu\text{m}$  pitch, hex design
- ✓ Test beam next week @ DESY

More results: [PSD13, Oxford, El Bitar](#)

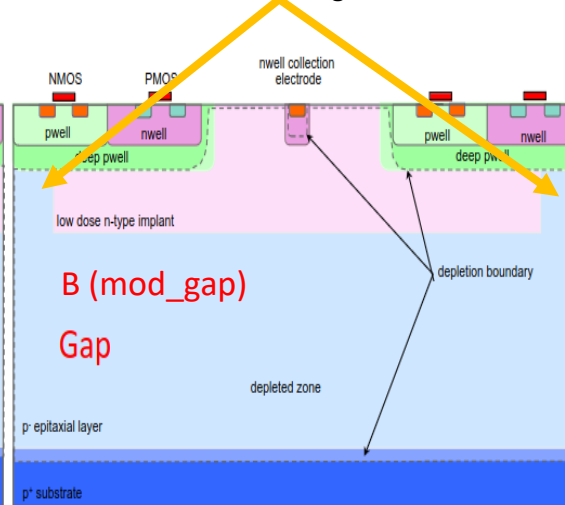
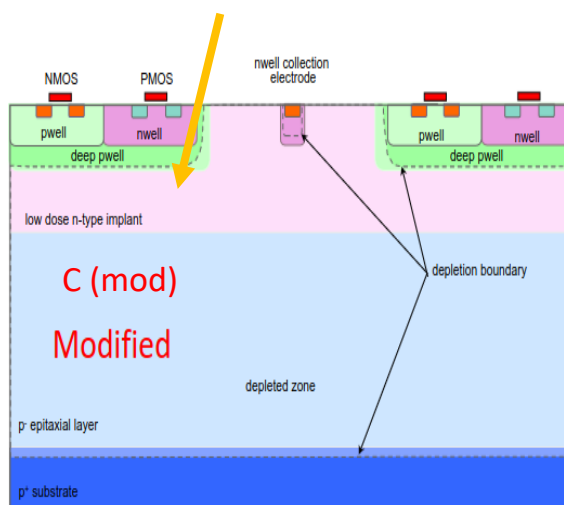
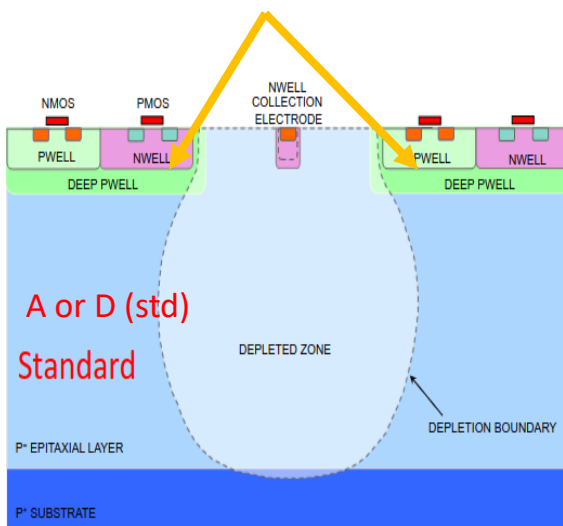
Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15 $\mu\text{m}$	64x32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15 $\mu\text{m}$	64x32	AC/21, DC/21, SF/22
CE65-C	mod	15 $\mu\text{m}$	64x32	AC/21, DC/21, SF/22
CE65-D	std	25 $\mu\text{m}$	48x32	AC/16, DC/16, SF/16



Prevent circuitry's nwells from collecting charge

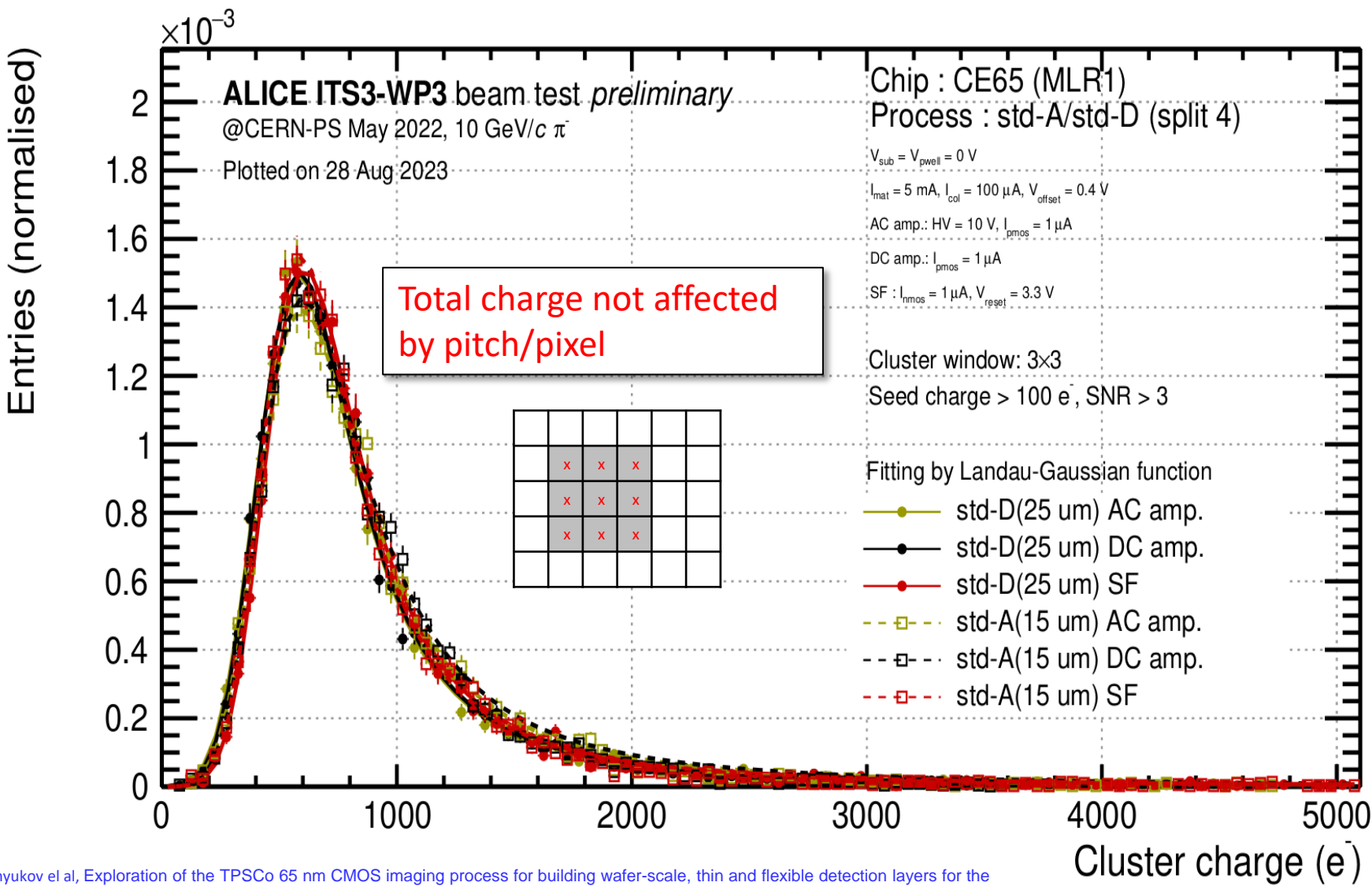
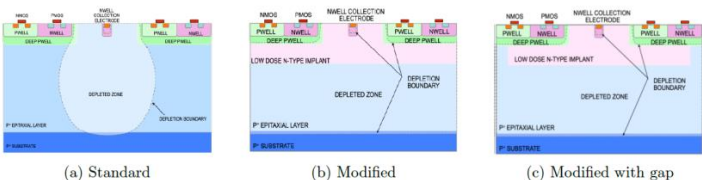
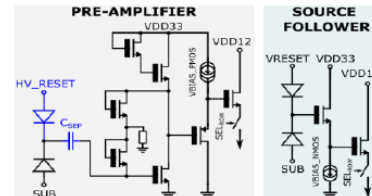
To obtain a full depletion

To overcome the weak electric field near the edges





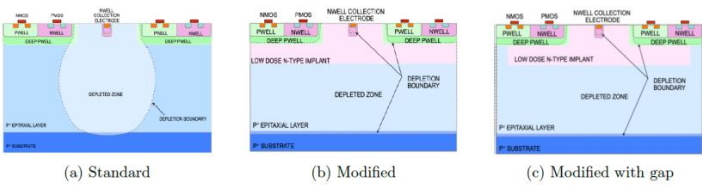
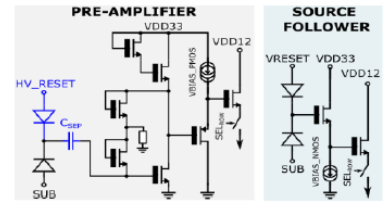
# Comparing the processes



Serhiy Senyukov et al, Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE Inner Tracking System upgrade (ITS3), IWORID 2022 <https://indico.cern.ch/event/1120714/>



# Comparing the processes



Entries (normalised)

$\times 10^{-3}$

**ALICE ITS3-WP3 beam test preliminary**  
 @CERN-PS May 2022, 10 GeV/c  $\pi^-$   
 Plotted on 21 Jun 2022

Chip : CE65 (MLR1)  
 Process : std/mod\_gap (split 4)

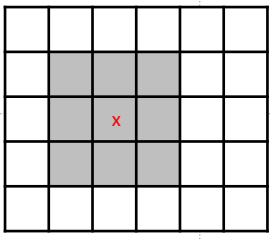
$V_{sub} = V_{pwell} = 0 V$   
 $I_{mat} = 5 mA, I_{col} = 100 \mu A, V_{offset} = 0.4 V$   
 AC amp.: HV = 10 V,  $I_{pmos} = 1 \mu A$   
 DC amp.:  $I_{pmos} = 1 \mu A$   
 SF :  $I_{nmos} = 1 \mu A, V_{reset} = 3.3 V$

Cluster window: 3x3  
 Seed charge > 100  $e^-$ , SNR > 3

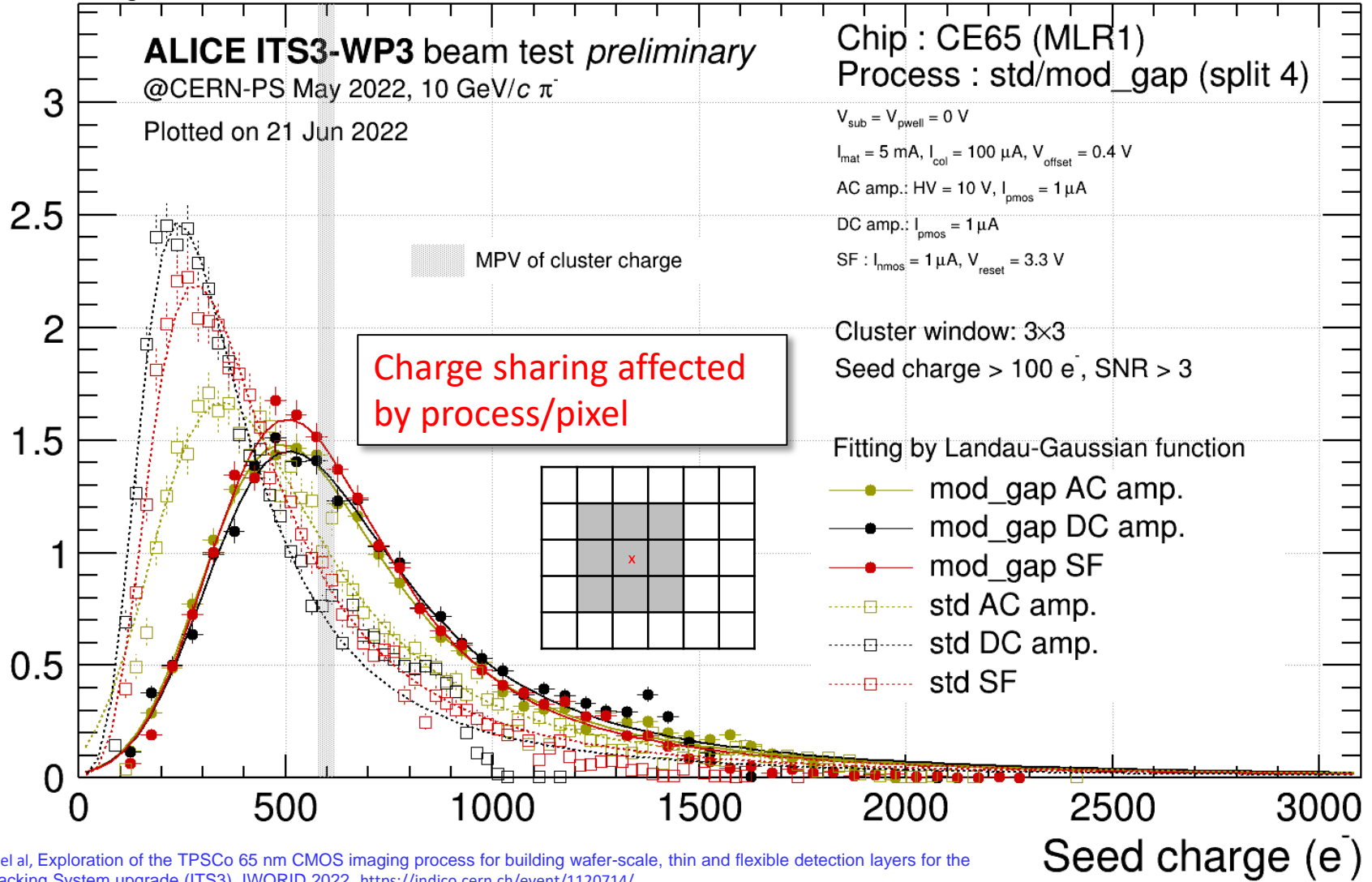
Fitting by Landau-Gaussian function

- mod\_gap AC amp.
- mod\_gap DC amp.
- mod\_gap SF
- - -□- - - std AC amp.
- - -□- - - std DC amp.
- - -□- - - std SF

Charge sharing affected by process/pixel

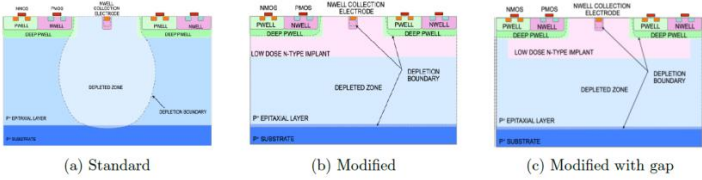
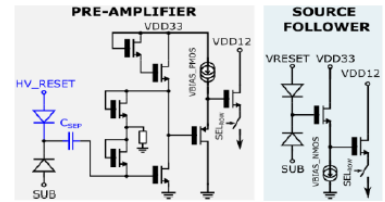


MPV of cluster charge



Serhiy Senyukov et al, Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE Inner Tracking System upgrade (ITS3), IWORID 2022 <https://indico.cern.ch/event/1120714/>

# Comparing the pitch/pixel

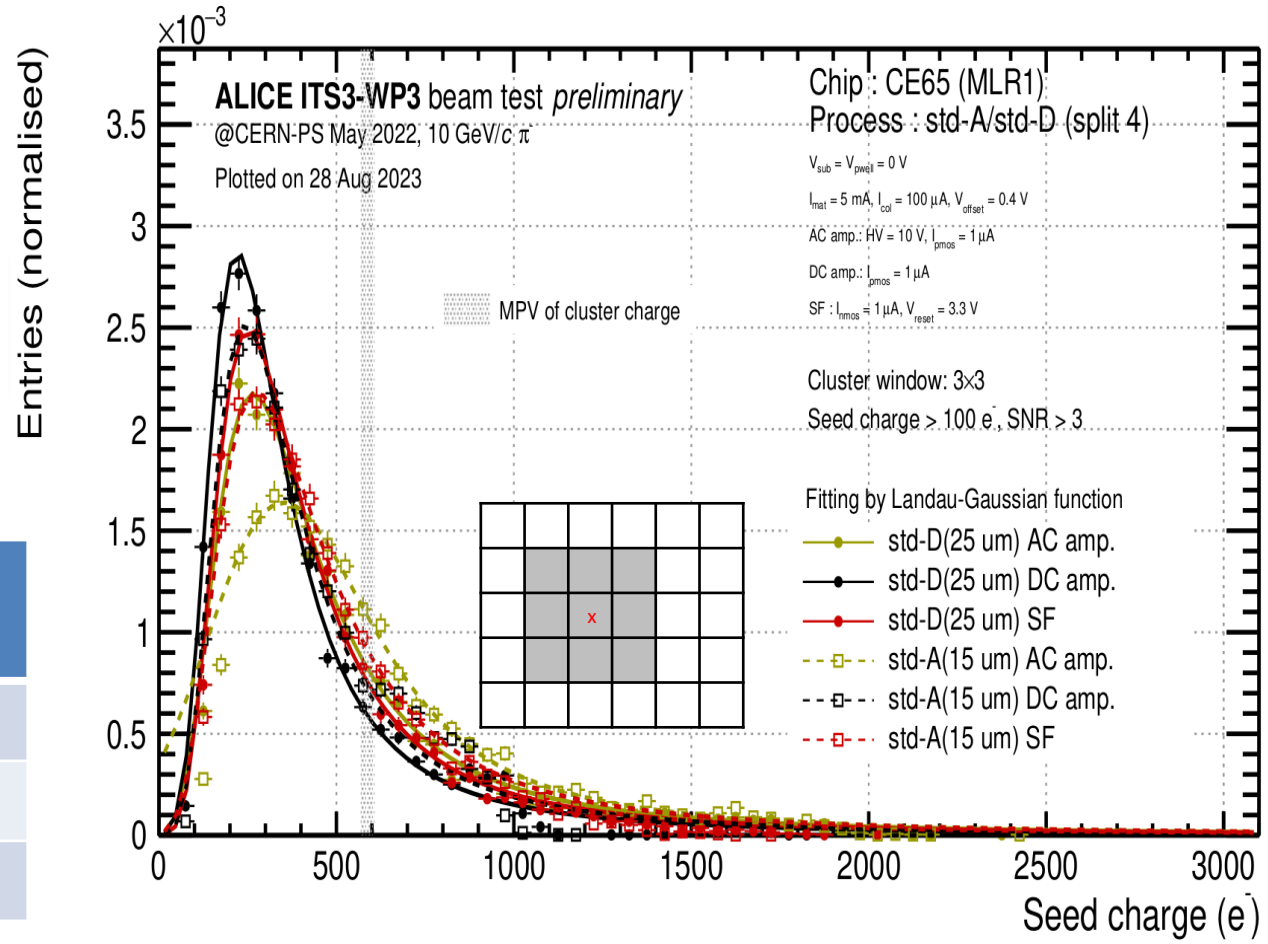


Charge sharing affected by pitch/pixel

Charge sharing increase

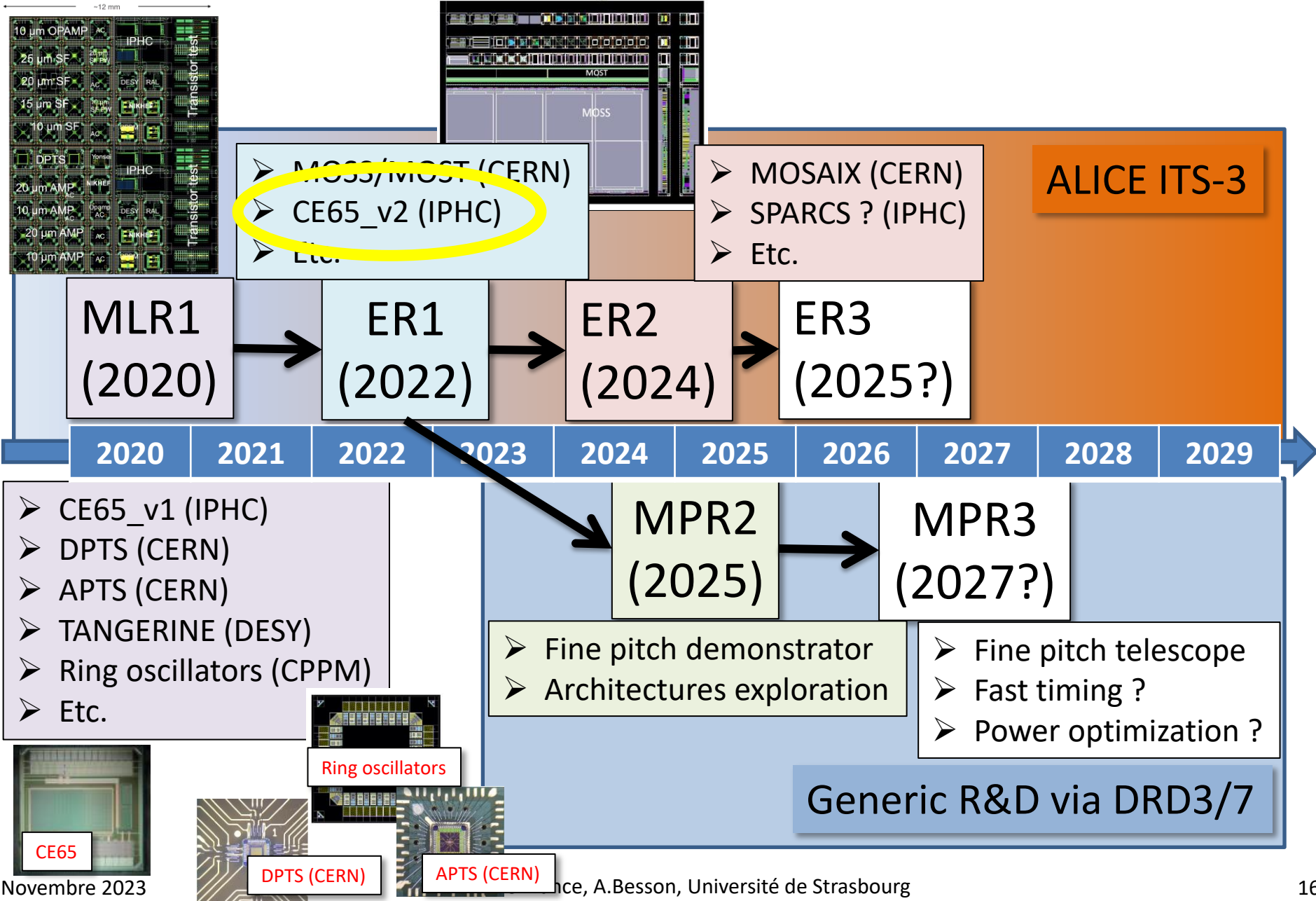
Charge sharing increase

	A4-std 15 um	D4-std 25 um
AC	311	284
SF	297	269
DC	261	232

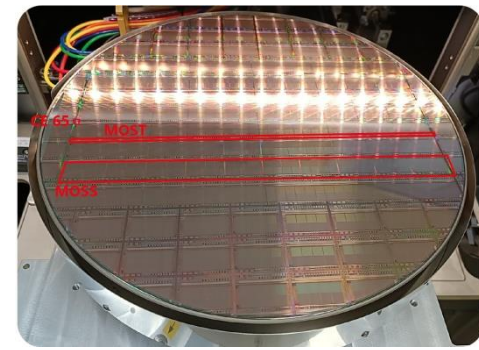


Serhiy Senyukov et al, Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE Inner Tracking System upgrade (ITS3), IWORID 2022 <https://indico.cern.ch/event/1120714/>

# TPSCo 65nm Submissions

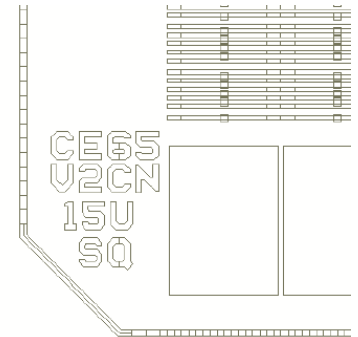
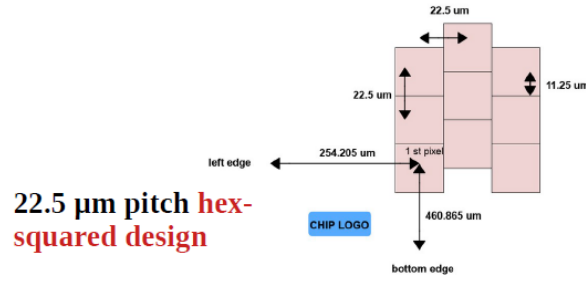
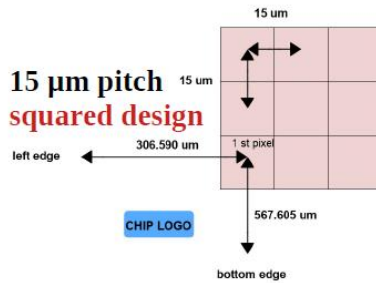


# CE65\_v2 (ER1 fabrication)

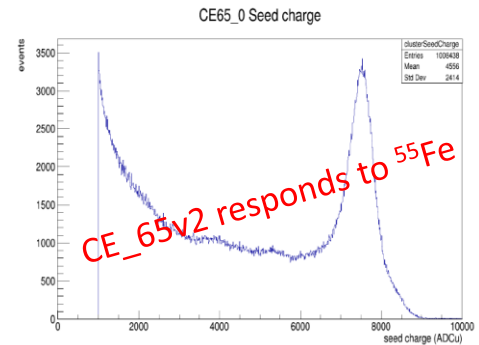
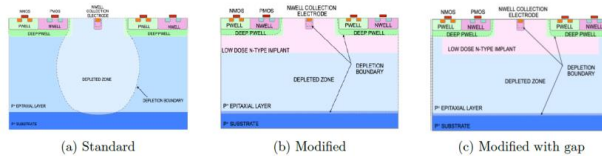


## New variants (x 15 !)

- ✓ Back from foundry summer 2023
- ✓ 48 col x 24 rows = 1152 pixels
- ✓ 5 pixel geometries :
  - 15  $\mu\text{m}$ , 18  $\mu\text{m}$  squared & hexagonal, 22.5  $\mu\text{m}$  squared & hexagonal



## ✓ 3 process options (« standard », « Blanket », « Gap »)



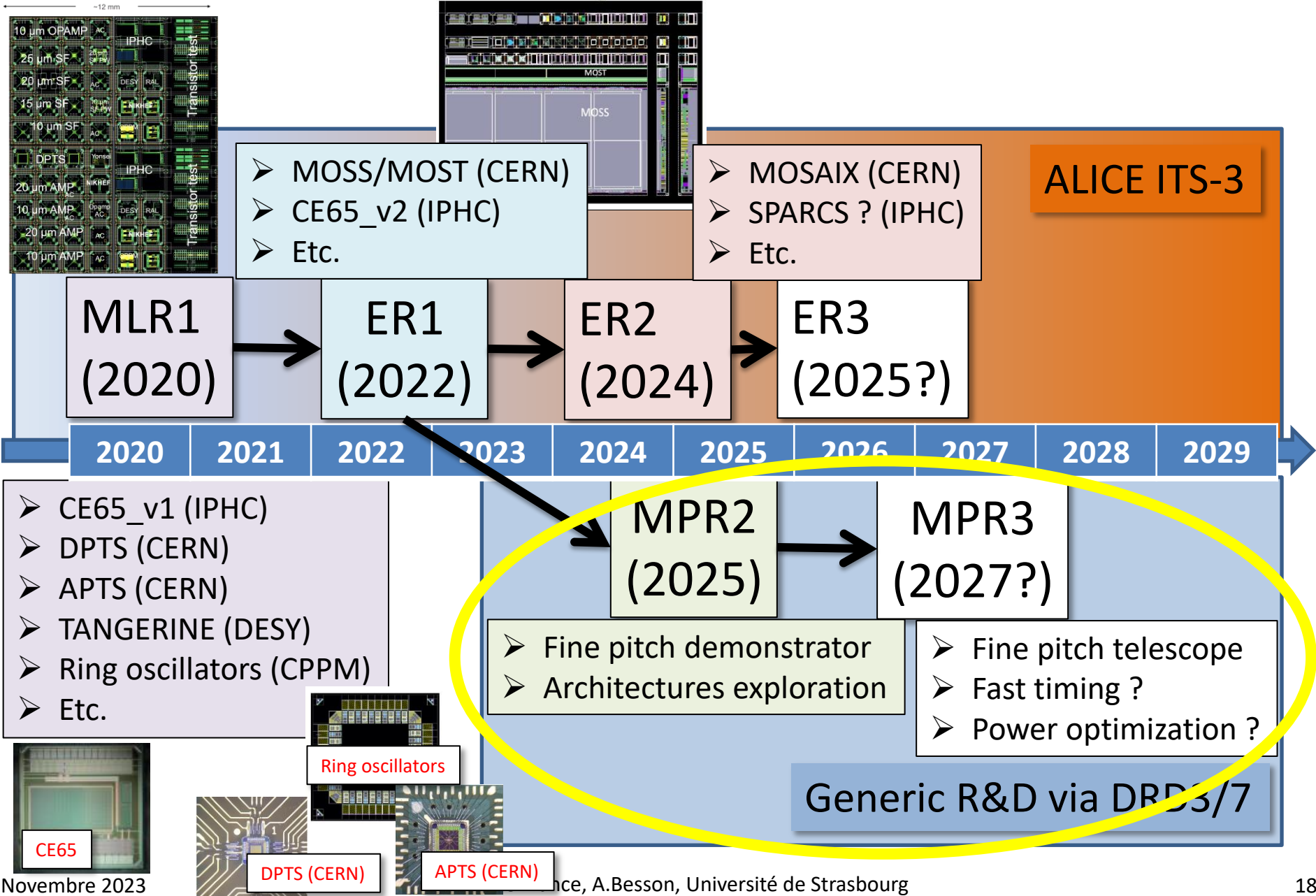
## First beam test next week (5 GeV e<sup>-</sup> @ DESY)

- ✓ ALPIDE telescope (DPTS trigger)

## Added value of CE65\_v2: Charge collection model, resolution, efficiency, etc.

⇒ Deep understanding of the charge collection allows pixel optimization for various applications

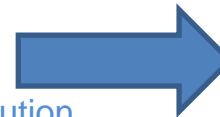
# TPSCo 65nm Submissions





# CMOS 65 nm submissions and connexion with DRD3/DRD7

- 2 lines of submissions
  - ✓ Submissions dedicated to ALICE ITS-3 (ER2 & ER3)
  - ✓ Submissions for generic R&D, supported by CERN EP R&D WP1.2 (« MLR2 » and beyond)
    - Motivations to gather the Higgs factory community
- Solid state detector R&D framework = DRD3/7
- Generic R&D possible contributions
  - ✓ One expression of interest submitted with future e+e- collider vertex detectors as the main driver
    - Goal: gather groups to reach a critical size
    - Targets 3  $\mu\text{m}$  spatial resolution, improved time resolution (5-500 ns), controlled Power ( $< 50 \text{ mW}/\text{cm}^2$ ), data flow (10-100 MHz/cm<sup>2</sup>) and low material budget (50  $\mu\text{m}$  thickness)
    - Demonstrator to equip new generation beam telescope
    - Proposing Institutes: CERN, DESY, IPHC, APC, etc.
    - Open to other participations
  - ✓ Other projects in discussion (tracking, timing, calorimeters)
- MLR2 submission model ?
  - ✓ R&D submissions: ~ end 2025 (another expected > 2027)
  - ✓ Cost to be shared between EP R&D WP 1.2 and participating projects
  - ✓ Multi-year plan needed to allow significant contributions to the targeted submissions



DRD project: Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments

DRD technology area  
DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.

Proposing participants

Institute	Contact	Foreseen main areas of contribution
APC Paris	M. Bomben	Simulations, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Hynds	Testing, simulations
Zurich University	A. Macchiolo	Testing, DAQ, simulations

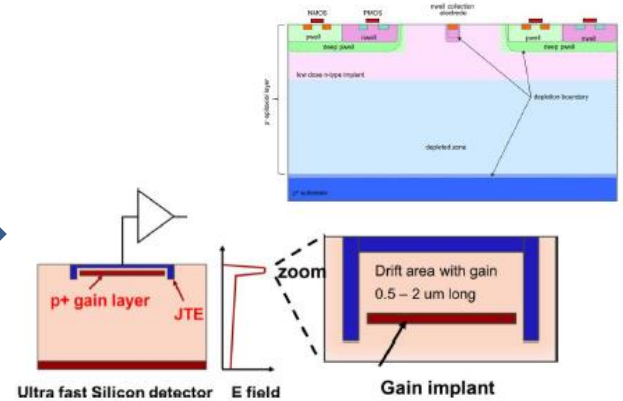
# Other R&Ds

- Generic R&D

- ✓ if fully generic  $\Rightarrow$  C4PI is the key player

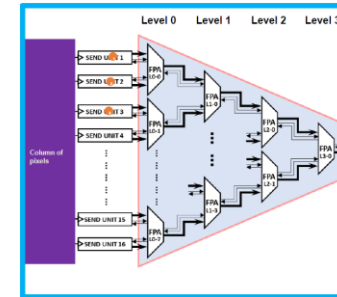
- CMOS with Pre-amplification

- ✓ Carried by C4PI & ANR APICS 2023 (J. Baudot, CPPM/IPHC/ICUBE)
  - ✓ Interest: amplification of primary charges in the sensitive layer  $\Rightarrow$  Spatial resolution, Fast time resolution & Power optimization



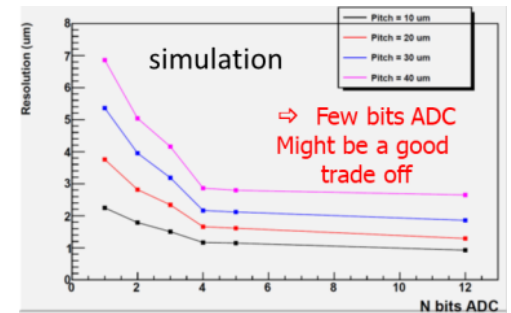
- Asynchronous read-out

- ✓ Carried by C4PI/ICUBE + PhD
  - ✓ Interest: power, fast read-out architecture & increased bandwidth
  - ✓ Challenge: make it compatible with small pitches
  - ✓ Goal : compare the performances with other architectures



- In pixel ADCs

- ✓ with APC
  - ✓ Interest: optimize the spatial resolution vs pitch figure of merit



- Fast timing (ToF via TDC)

- ✓ with IP2I/APC
  - ✓ Interest:  $\Rightarrow$  MAPS with 4D measurements

ANR 4D MAPS submitted in 2023 (IPHC/APC/IP2I, Bomben)

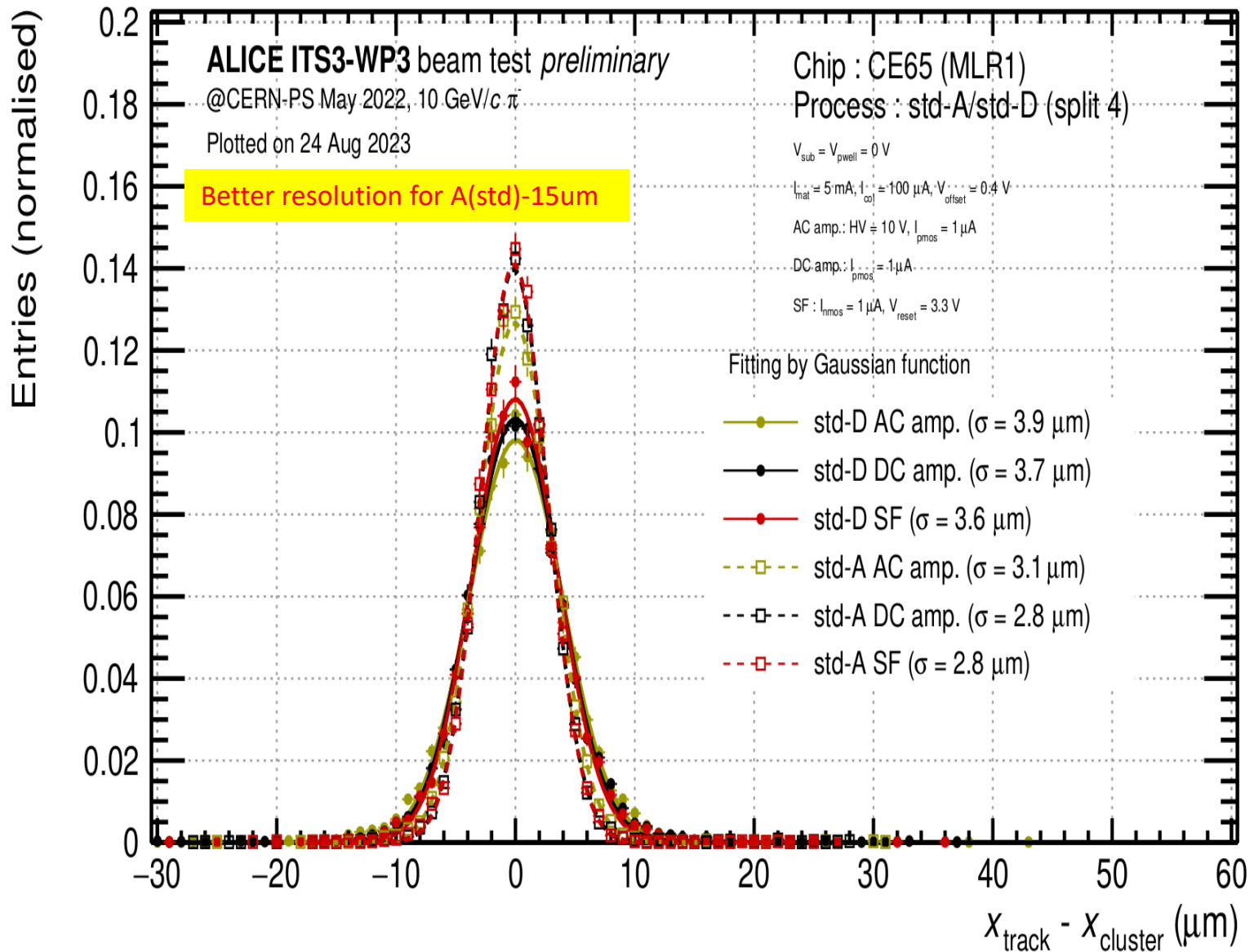


# CMOS R&D for FCCee: Summary

- CMOS-MAPS technology:
  - ✓ After 20 years of R&D, the technology has reached a level of maturity which allows it to be widely used in HEP
  - ✓ The technology has not yet reached its full potential
- Scientific goals:
  - ✓ Exploit fully the potential of the technology, targeting future Higgs factory (FCCee) and any applications where granularity is a leading requirement
- Strategy definition:
  - ✓ Synergies: Mid-term projects are still the way to go
    - Carried by GRAM : MIMOSIS OR carried by other MPs: ALICE ITS-3, Belle-2 upgrade (Obelix)
    - Provides invaluable milestones, maintains/develops the know-how for full size chips
  - ✓ Leading technology: 65nm TPSCo R&D
    - Supported by CERN and DRDs
- Strategy implementation:
  - ✓ Local:
    - Crucial role of C4PI (e.g. R&D strategy coordination between GRAM & C4PI, manpower)
    - Strategy for Higgs factories/ALICE-ITS3/Belle II endorsed by IPHC scientific council (2023), HCERES.
  - ✓ National:
    - GRAM extended to emerging activities (IP2I, APC) and to other applications (e.g. outer trackers)
    - Complementarity of the 2 master projects : GRAM / DEPHY
    - Complementarity with projects carried by experiments (ALICE ITS-3, Belle-II) (e.g. technical coordinator of ITS-3 @ in2p3)
    - Continue to strengthen the community targeting FCCee (e.g. ANR submitted (Bomben, APC/ IP2I/IPHC)
    - Find the right balance between generic R&D and specific requirements & mid-term vs long term
    - Develop simulations & physics studies dedicated to FCCee
  - ✓ International:
    - DRD3/DRD7 and program of submission in 65 nm technology
    - Exploit synergies and maintain the network of partners (CERN, DESY, KEK, Zurich, etc.)

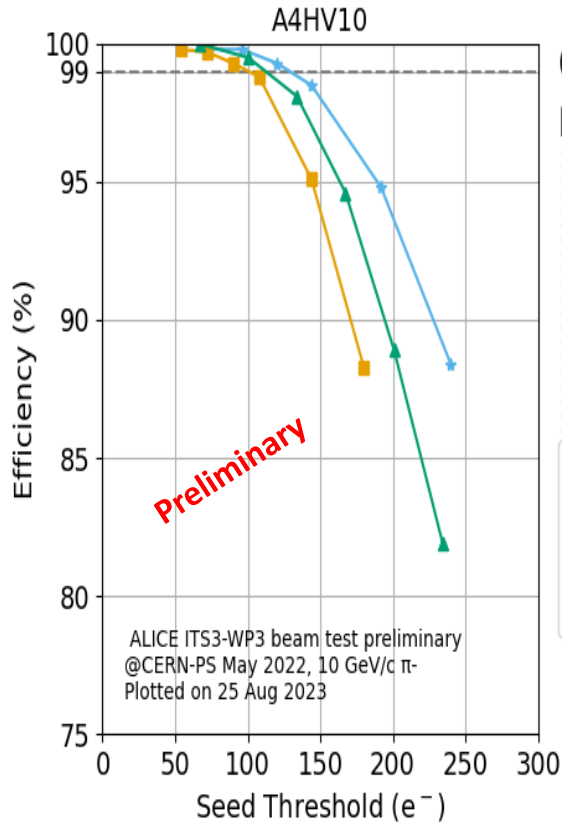
Back up

# Residual



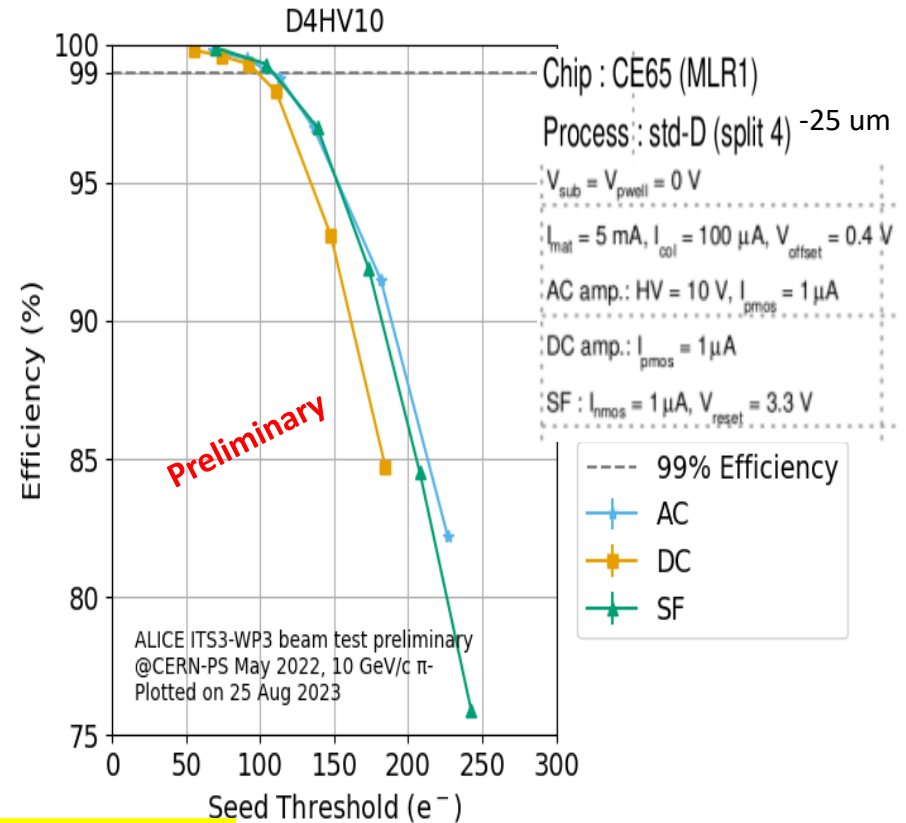


# Detection efficiency



Chip : CE65 (MLR1)  
Process : std-A (split 4) -15  $\mu\text{m}$   
 $V_{\text{sub}} = V_{\text{pwell}} = 0 \text{ V}$   
 $I_{\text{mat}} = 5 \text{ mA}, I_{\text{col}} = 100 \mu\text{A}, V_{\text{offset}} = 0.4 \text{ V}$   
AC amp.: HV = 10 V,  $I_{\text{pmos}} = 1 \mu\text{A}$   
DC amp.:  $I_{\text{pmos}} = 1 \mu\text{A}$   
SF :  $I_{\text{nmos}} = 1 \mu\text{A}, V_{\text{reset}} = 3.3 \text{ V}$

--- 99% Efficiency  
+ AC  
+ DC  
+ SF

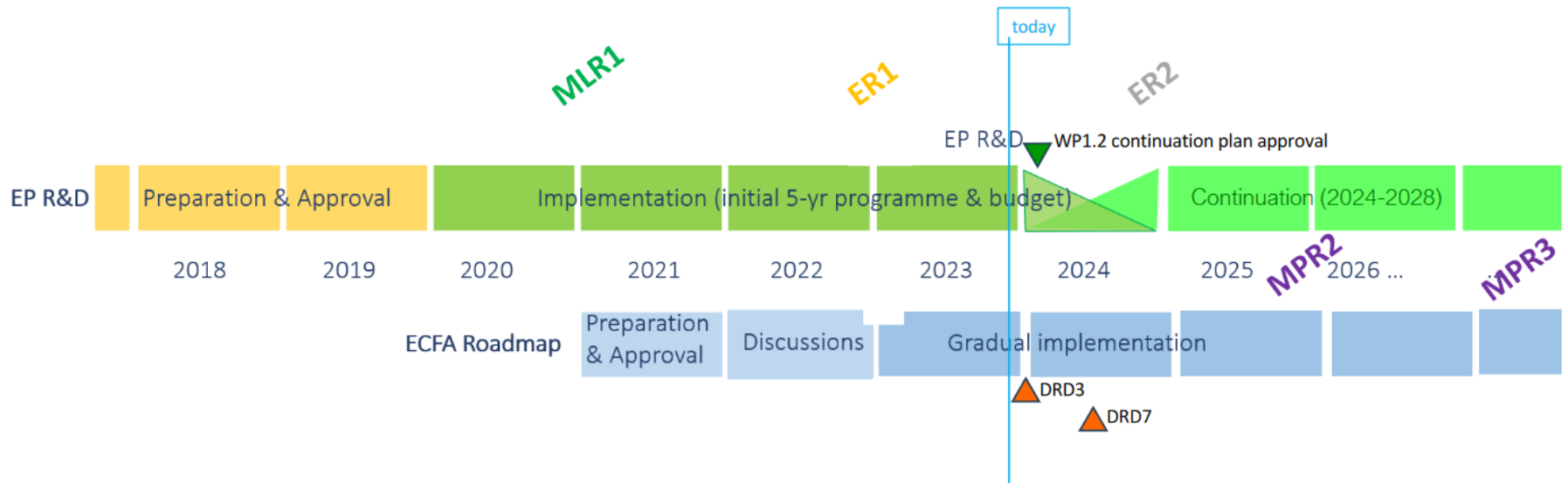


Chip : CE65 (MLR1)  
Process : std-D (split 4) -25  $\mu\text{m}$   
 $V_{\text{sub}} = V_{\text{pwell}} = 0 \text{ V}$   
 $I_{\text{mat}} = 5 \text{ mA}, I_{\text{col}} = 100 \mu\text{A}, V_{\text{offset}} = 0.4 \text{ V}$   
AC amp.: HV = 10 V,  $I_{\text{pmos}} = 1 \mu\text{A}$   
DC amp.:  $I_{\text{pmos}} = 1 \mu\text{A}$   
SF :  $I_{\text{nmos}} = 1 \mu\text{A}, V_{\text{reset}} = 3.3 \text{ V}$

--- 99% Efficiency  
+ AC  
+ DC  
+ SF

Charge sharing reduce efficiency

# CERN WP 1.2



<https://indico.cern.ch/event/1339888/>