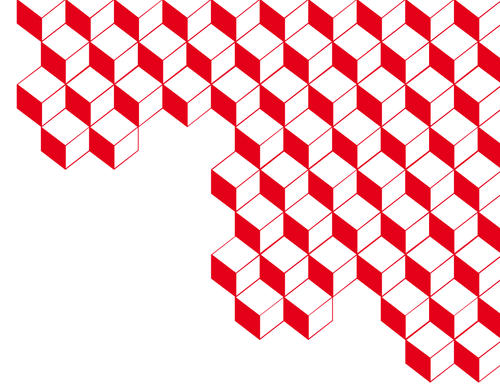

Timing with Monolithic CMOS
Potential applications to FCC

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Monolithic CMOS and DRD3

WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n$_{eq}$/cm^2 NIEL and 500 MRad

- Ambitious research goals
- Agressive timeline
- Quite some technologies/foundry processes under consideration → no clear choice yet, very likely one given technology will not reach all goals

DRD3 WG1 Monolithic CMOS		**Assess technology performance for each RG – handle technical solution options for strategic programs of LS4 time scale**			
Research Goals	**Timeline**	**2024**	**2025**	**2026**	**2027**
	Technologies	**Foundry submissions and Milestonses (MS)**			
	TPSCo (TJ) 65 nm	design MPW1.1	submit MPW1.1 mid-2025 design MPW1.2	evaluate MPW1.1 submit MPW1.2 Q4-2026	evaluate MPW1.2
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	design MPW1.1 submit MPW1.1 Q4-2024	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q1-2026	
RG1 Position precision	**TPSCo (TJ) 65 nm**	electrode size/shape/pitch, process variants 12" ER splits, thin epitaxial layer, stitching optimized for high channel density (low pitch)		MS1 establish position precision versus technology, channel configuration and readout mode MS2 establish time precision versus technology, channel configuration MS3 establish performance of readout variants for power consumption MS4 establish radiation tolerance provide guidlenies for choice of substrates select/merge MPW1.1 features add new technology features submit configurations for Vertex Detector, Central Tracking, Timing Layers, HGCAL	MS5 handle technical solutions for Vertex Detector (ALICE-3, LHCb-2, Belle-3, CMS/ATLAS) 1) high radiation tolerance/rate technlogies > 65 nm 2) high channel density, sitching TPSCo 65 nm MS6 handle technical solutions for Central Tracking (ALICE-3, EIC, LHCb-2, Belle-3), Timing Layers (ALICE-3, ATLAS, CMS) with stitching TPSCo 65 nm MS7 handle technical solutions for low power w/o and w/ precision timing, at medium and high rates
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	electrode size/shape/pitch, wafer type/thickness, process variants 8" ER or MLM splits			
RG2 Timing precision	**TPSCo (TJ) 65 nm**	similar to RG1 optimized for fast signal collection speed and high S/N			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	similar to RG1 optimized for fast signal collection speed and high S/N including gain layer option			
RG3 Readout architecture common with DRD7	**TPSCo (TJ) 65 nm**	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium rates power distribution and control in large size stitched matrix			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium and high rates			
RG4 Radiation tolerance	**TPSCo (TJ) 65 nm**	process features in splits			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	variants of substrates (Cz, epitaxial), resistivity, p-type and n-type			

Timing sensor basic ingredients

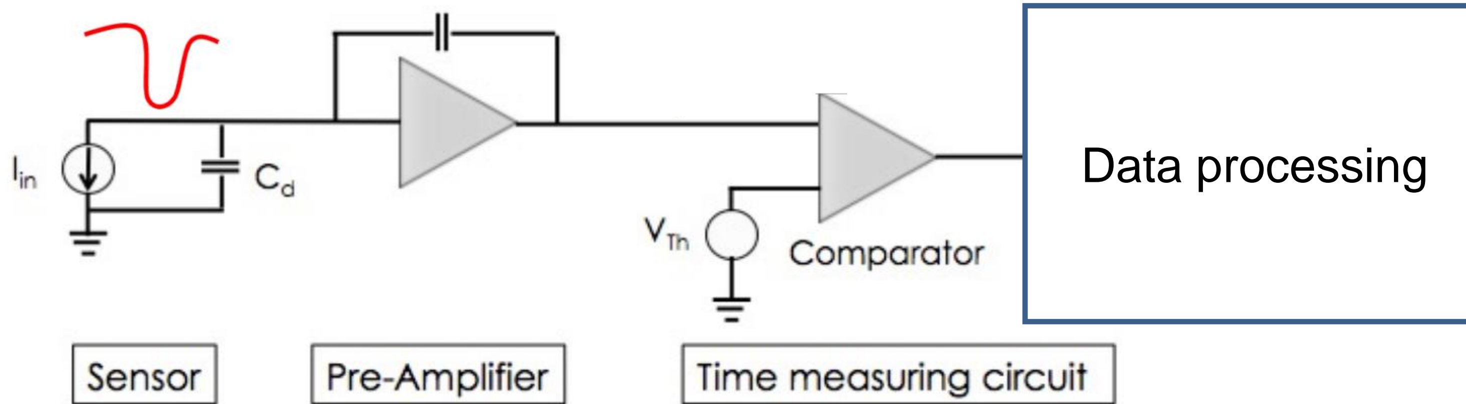


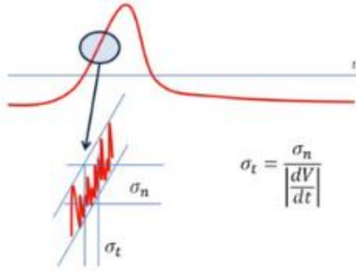
Illustration taken
From N. Cartiglia
(VCI 2022)

- Monolithic sensors : Analog Front-End, Time measuring electronics (typically LE discriminator)
- Data processing (TDC, serializers, PLL, sparsification) can ideally also be on same chip,

but actual development not easy (risk of analog/digital couplings)

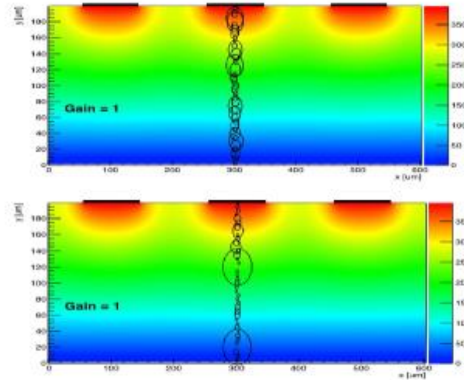
Time resolution

$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$



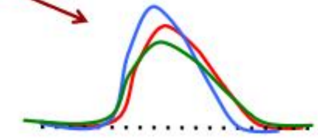
"Jitter" term

Small noise → choice of technology, small detector capacitance
High dv/dt →
High electric field (but Vd saturates around 1 V/μm)
Intrinsic amplification (LGADs)



Amplitude variation → Timewalk, corrected offline

Non-homogeneous energy deposition → cannot be corrected, minimized by design



Signal shape is determined by Ramo's Theorem

$i \propto qvE_w$

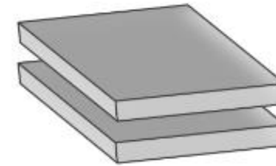
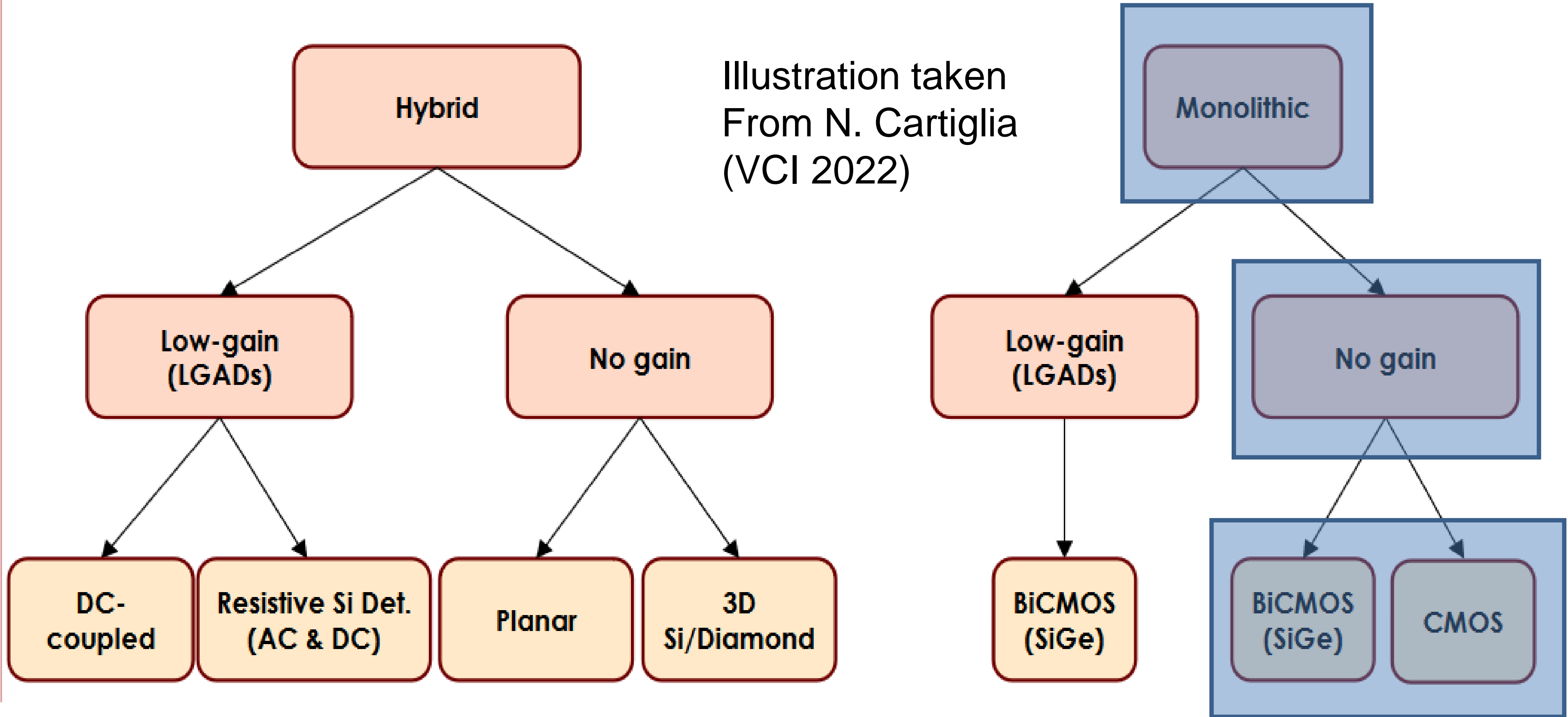


Illustration taken From N. Cartiglia (VCI 2022)

Saturated drift velocity in sensor volume → Uniform weighting field

Parallel plate geometry, easier for big pixels

Timing oriented sensor families

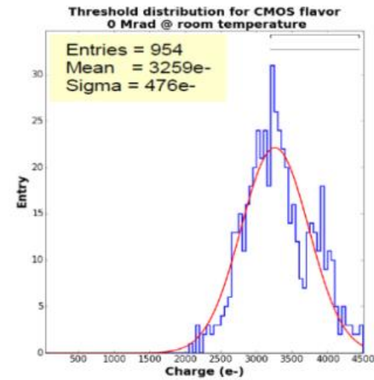


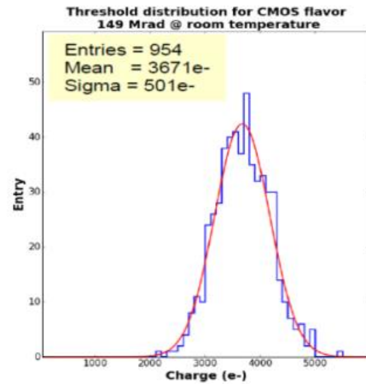
Features of monolithic CMOS sensors

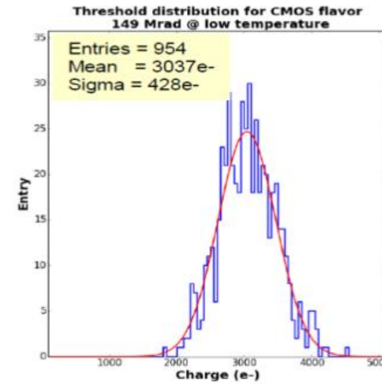
- (Relatively) cheap high volume industrial technology
  - 2-3 k euro/8'' wafer, post-processing and dicing included → bare sensor cost for 100 m2 : 7-11 M euros
  - Bump bonding operation not needed for fully monolithic architecture
- Stable and easy operation
- HV-HR wafers available, allows charge collection by drift and not only by diffusion → favorable for fast collection and for radiation hardness
- Can be designed as a complete SoC, from sensor to DAQ interface
- Presently available technologies are known to be rad-hard up to a few 10^{15} 1 MeV neq/cm2
- Can be thinned down to < 100 µ

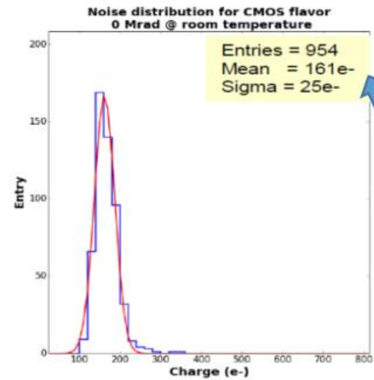
LF15A radiation hardness

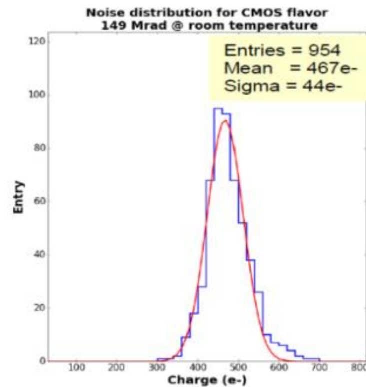
0 Mrad @Room Temp **149 Mrad @Room Temp** **149 Mrad @Low Temp -15°C**

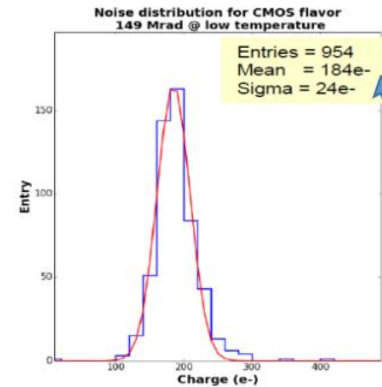


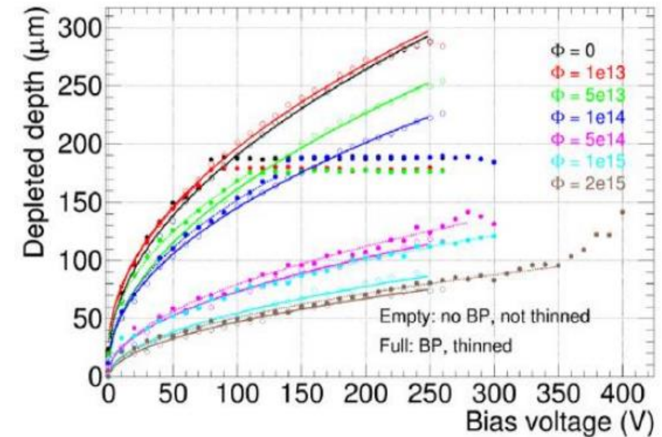












[I. Mandic et al. NIM A 903, 2018]

→ Radiation tests at CERN-SPS with **proton** beam on **LF-CPIX** chip (**CPPM**)

→ 14% increase of noise after irradiation with cooling

Leading-edge technology: IHP SG13G2

130 nm process featuring SiGe HBT with

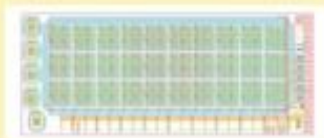
- Transistor transition frequency: $f_t = 0.3\ THz$
- DC Current gain: $\beta = 900$
- Delay gate: 1.8 ps

2016

200ps

- 1 and 0.5 mm² pixels
- Discriminator output

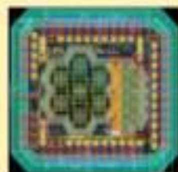
2017



110ps

- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

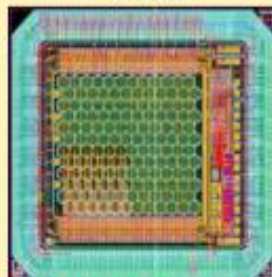
2018



50ps

- Hexagonal pixels 65µm and 130µm side
- Discriminator output

2019

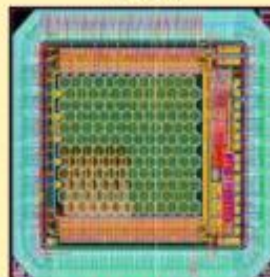


ATTRACT noGAIN

36ps

- Hexagonal pixels 65µm side
- 30ps TDC +I/O logic
- Analog channels

2021

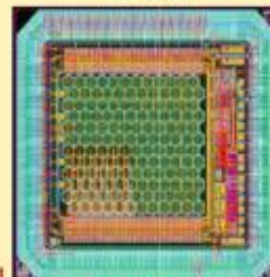


PicoAD p0

24ps PRELIMINARY

- Same pixel/Electronics of ATTRACT

2022

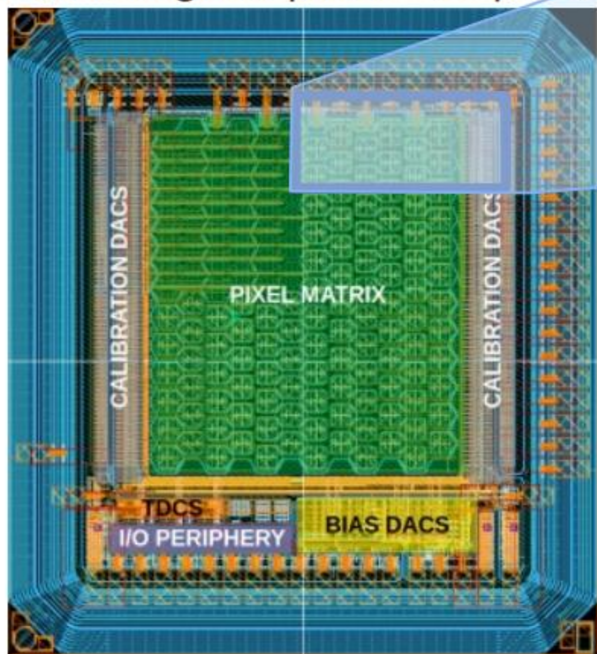


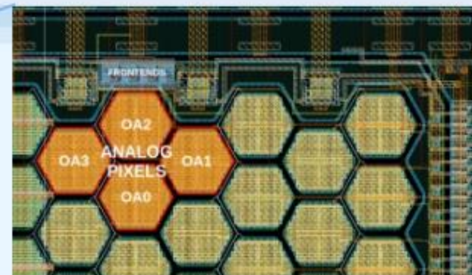
PicoAD p1

- Hexagonal pixels 65µm side
- 1ps TDC +I/O logic
- New FE, target 10ps

ATTRACT prototype

100µm pitch hexagonal pixels - 25 µm depletion

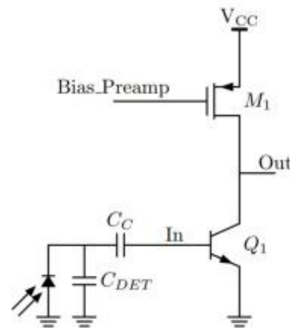


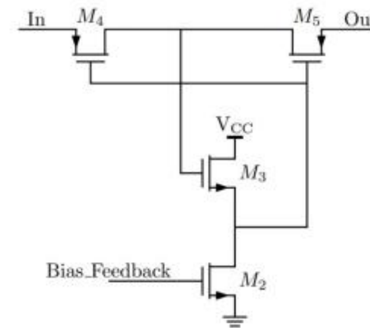


UNDER TEST HERE

Analog Channels:

HBT preamp + two HBT Emitter Followers to 500Ω Resistance on pad.





MPW submission in 2019 funded by H2020

G. Iacobucci et al 2022 JINST 17 P02019

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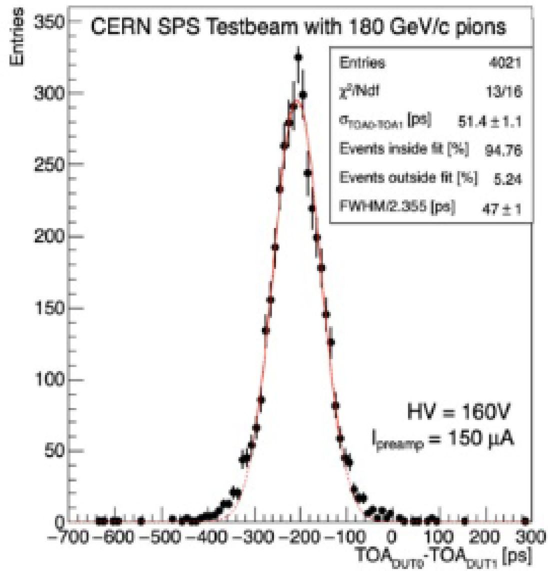
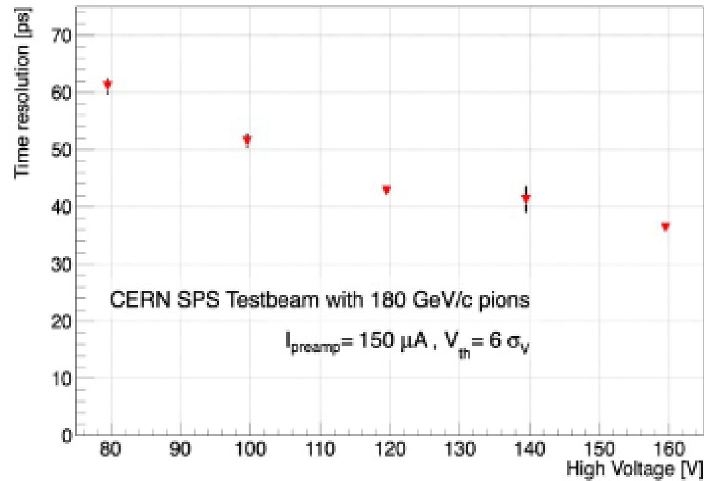
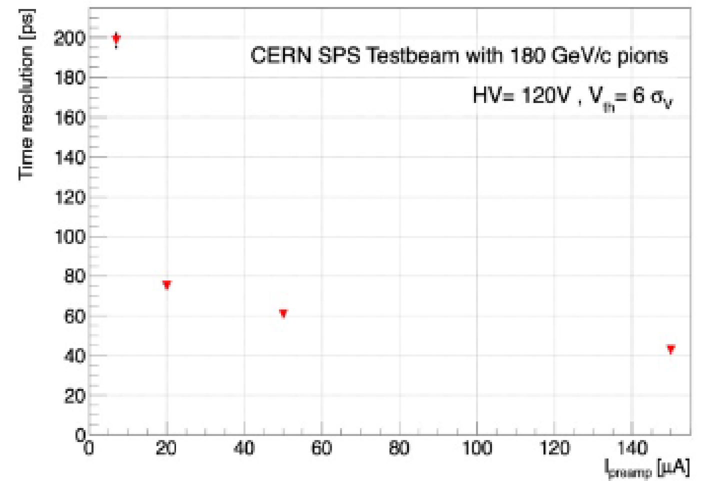
Department of Nuclear and Particle Physics

ATTRACT prototype – Time Stamping



Time of flight between DUT0 and DUT1





- 57 ps after 10^{16} 1 MeV neq/cm2
- can be brought back to 40 ps, with HV and LVPS increase :

Arxiv : 2310.19398

$$\sigma_t = \frac{\sigma_{TOA0\text{-}TOA1}}{\sqrt{2}} = (36.4 \pm 0.8)\text{ps}$$ without gain structure

24 ps with gain layer (but complicated manufacturing → mass scale production ???)

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Fastpix (CERN) : sub-ns timing with TJ180

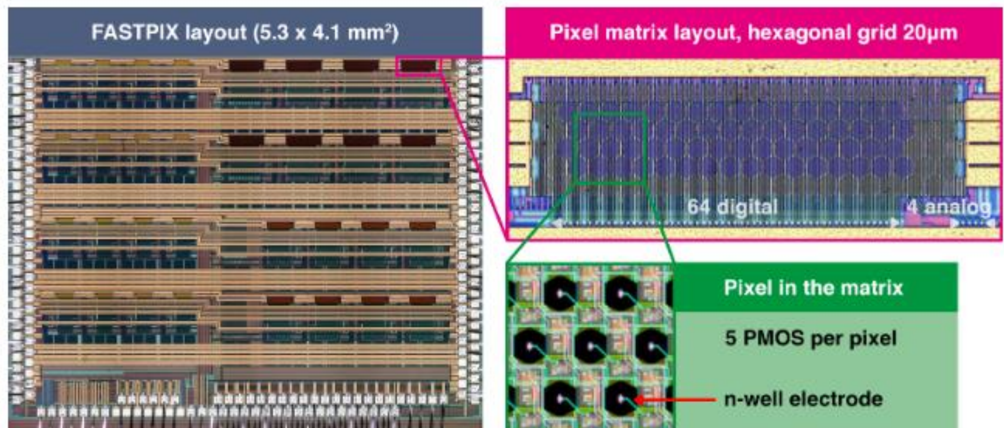


Figure 2. FASTPIX layout (5.3 mm × 4.1 mm) with details of the 20 µm pitch hexagonal grid zoom on 7 pixels.

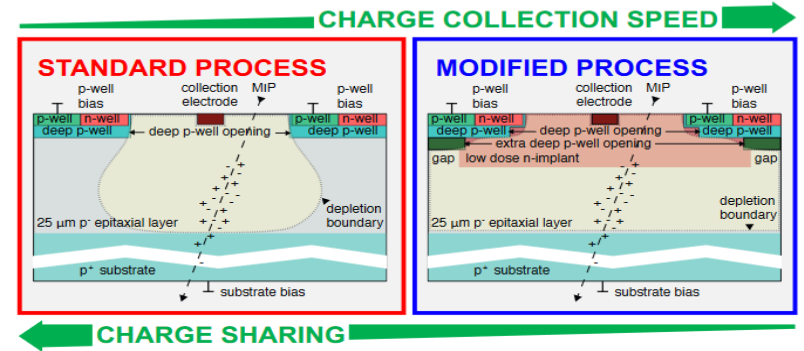


Figure 2. Wafer production process variants for FASTPIX represented by schematic cross-sections of the pixel unit cells, showing a cut perpendicular to the sensor surface. The standard 180 nm CMOS imaging process (left) and the modified process variant (right) with added low-dose n-type implant and optimizations such as a gap in the n-implant, retracted deep p-well and additional extra-deep p-well implant.

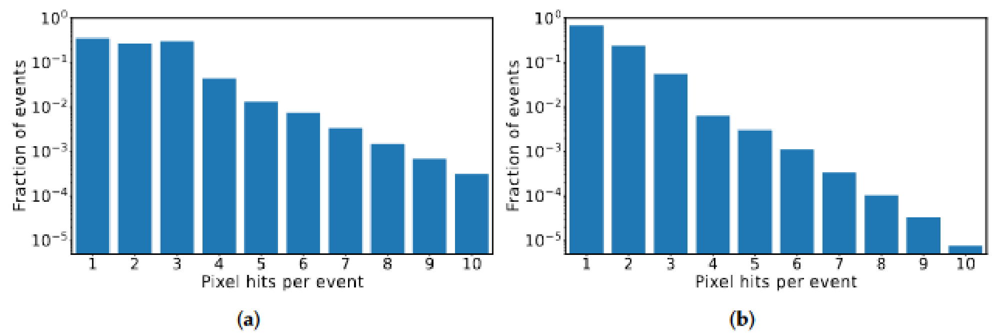


Figure 8. Number of pixel hits per event for the 10 µm (a) and 20 µm (b) pitch matrix.

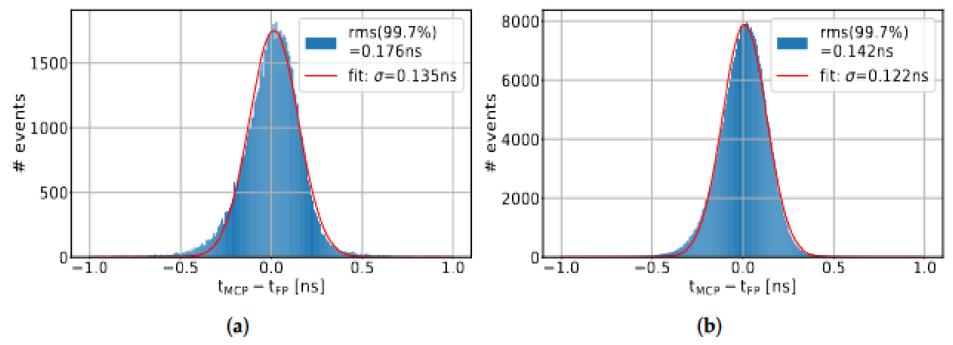


Figure 14. Seed-pixel time residuals after timewalk correction for the inner region of the 10 µm (a) and 20 µm (b) pitch matrix.

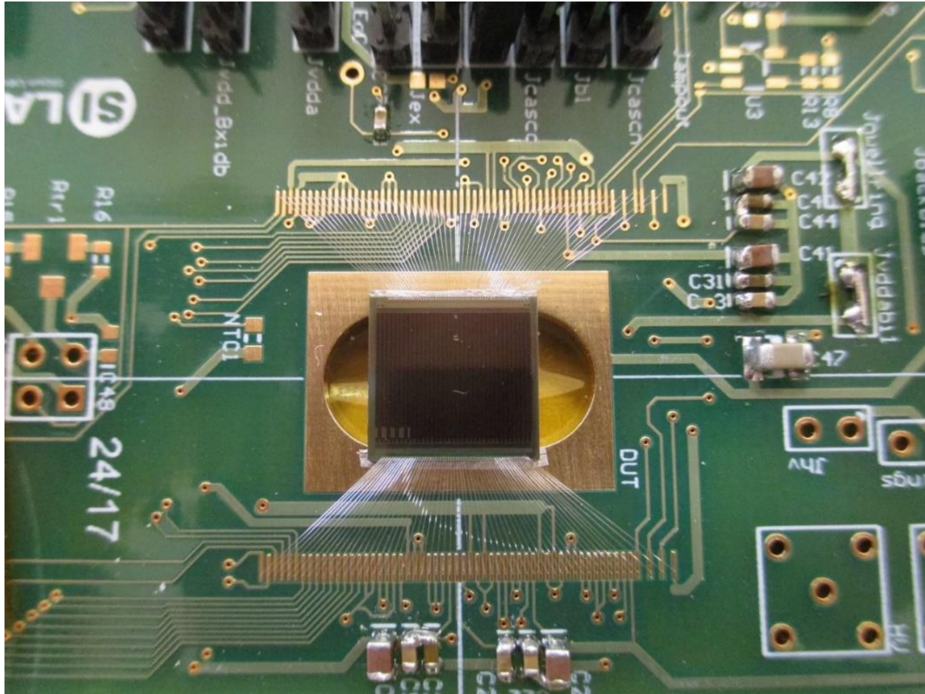
Plan to port and test the concept on TPSCo 65 technology, but small pixels → beware of drift field inhomogeneity !

Cactus (Irfu) : A bit of History

We started around 2017 after being involved into LF-CPIX and MONOPIX strip detector for ATLAS-ITK outer layers (possible backup solution)

At that time, 2 possible applications for sub-100ps timing detectors:

- ATLAS High η muon tagger (upstream forward calorimeter)
- HGTD in front of ATLAS-LAr



First try with CACTUS:

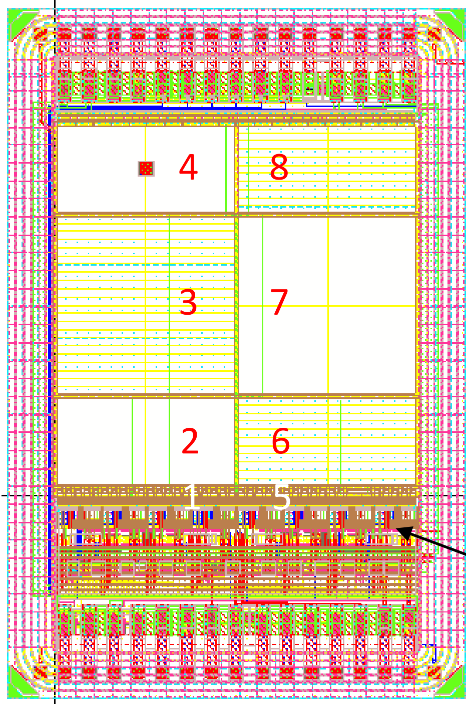
- Yield correct, High break down voltage, homogenous charge collection, deep depletion depth
- Main problem with CACTUS: underestimation of parasitic capacitance → bad S/N

-Also coupling between analogic and digital part → ringing of digital pulse

→ modest timing performance ~500ps

https://arxiv.org/abs/2003.04102

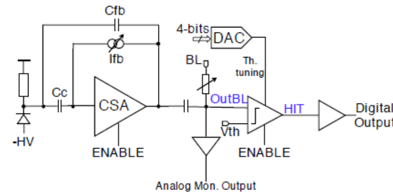
→ Version 2 of CACTUS called Mini-Cactus



Layout of MiniCACTUS chip

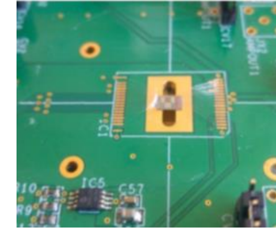
MINICACTUS PROTOTYPE CHIP

- **MiniCACTUS** is a small detector prototype designed in order to address the *low S/N issue* of the larger size CACTUS
- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive
- FE parameters programmable through on-chip Slow Control
- 2 digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns

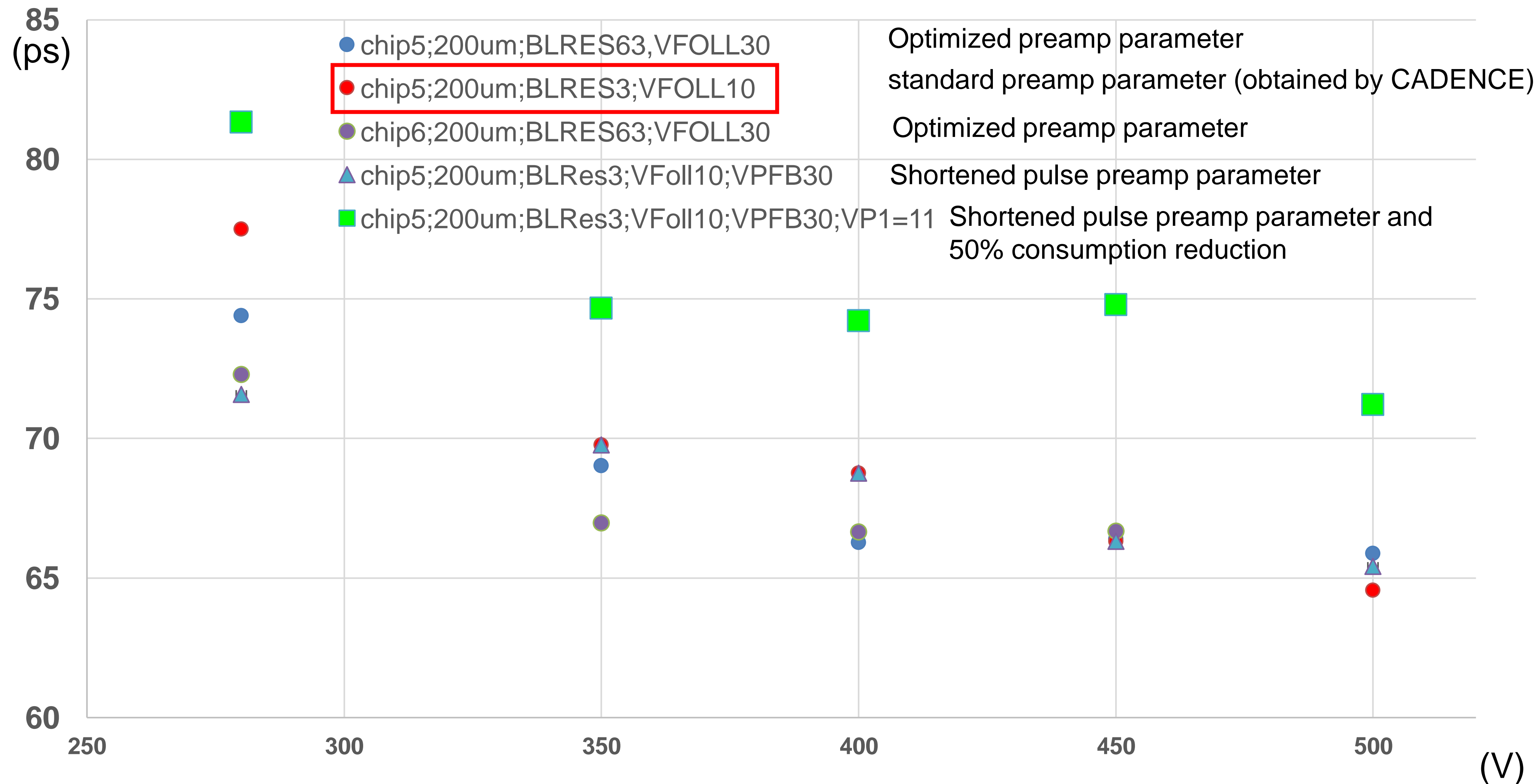


FE (1/pixel)

Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel



- **Front-end mostly optimized for 1 mm² pixels** with peaking time of 1-2 ns @ 1-2pF (Ibias_total=800µA → P ≈ 150mW/cm²)
- Small pixels can be seen as test structures to study charge collection (no power optimized FE available)
- Some detectors thinned to 100µm/200µm/300µm and than post-processed for backside polarization after fabrication



Pixel 8;200 µm; Resolution versus HV
85
(ps)
80
75
70
65
60
250
300
350
400
450
500
(V)
chip5;200um;BLRES63,VFOLL30
chip5;200um;BLRES3;VFOLL10
chip6;200um;BLRES63;VFOLL30
chip5;200um;BLRes3;VFoll10;VPFB30
chip5;200um;BLRes3;VFoll10;VPFB30;VP1=11
Optimized preamp parameter
standard preamp parameter (obtained by CADENCE)
Optimized preamp parameter
Shortened pulse preamp parameter
Shortened pulse preamp parameter and
50% consumption reduction

MiniCactus Next steps

- Non amplified HV CMOS MiniCactus v1 sensor reaches 65 ps time resolution on MIPs, power consumption 0.3 W/cm^2
- A new iteration of MiniCactus has been submitted (May 2023), expected back December 2023
  - Improved front-end : better discriminator, programmable analog filtering
  - Altiroc-inspired Front-end designed and studied by IFAE, improvements in jitter and shorter signal expected
  - Irradiated MiniCactus v1 chips (10^{14}, 10^{15}, 10^{16} 1 MeV neq/cm^2) under test, test setup has been modified to run at -15°C
- TCAD simulations support the possibility to implement a gain layer without modifying LF15A process
  - To be tested in an MPW run in 2024

Global trade-offs : time resolution is not everything

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm^2	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm^2	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm^2	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm^2	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm^2	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm^2	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm^2	~~~ 90~~ 65 ps	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm^2	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm^2	~ 25	40

50 ps @ 0.1W/cm2

Table from N. Cartiglia (VCI 2022)

Trade off to be found between

- Space resolution,
- time resolution
- power consumption

Conclusions

- A lot of activity underway on monolithic CMOS timing oriented sensor developments
  - Many technologies are being evaluated

- Present performance not far from what could be needed for a timing layer or a TOF detector

- Integration in an actual experiment needs :
  - Careful trade off evaluation between timing performance, space resolution, power dissipation
  - A lot of work to integrate digital data processing in a fully monolithic design