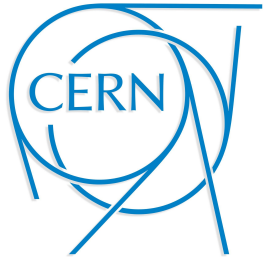

# Control, Operation, Run-in and Performance of the LAr calorimeter Ph-1 Upgrade electronics on the ATLAS Detector

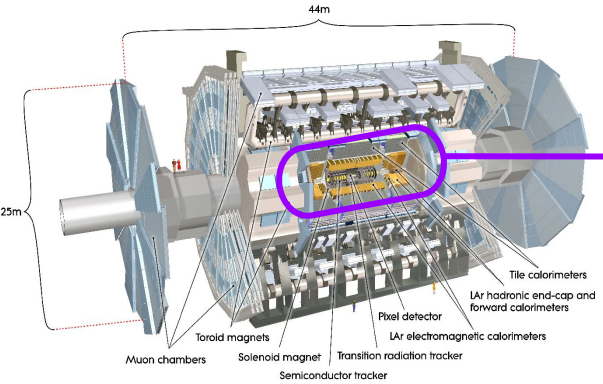


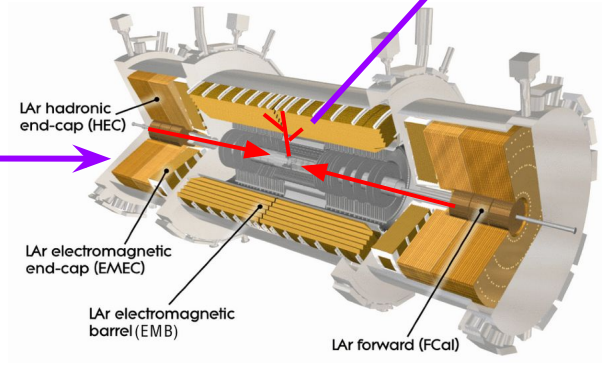


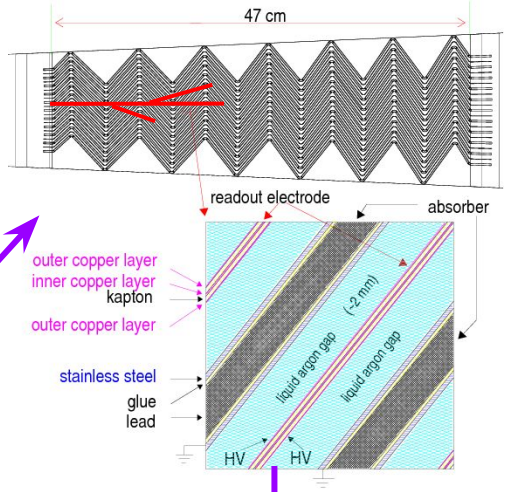
3rd Year PhD Student Presentations
04-12-2023
Florent Bernon

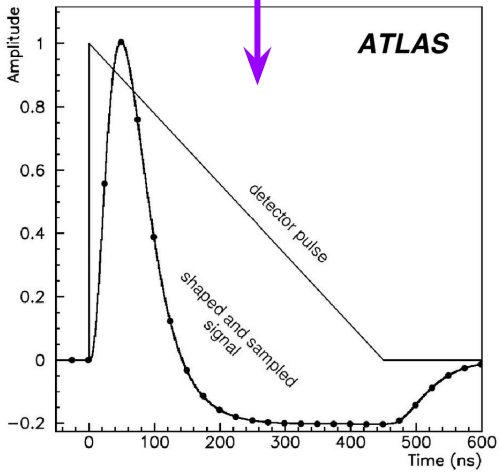
# ATLAS Liquid Argon Calorimeter

- Used to measure the energies of electromagnetic particules (photons, electrons) and hadronic particules in forward region
- Provides signals of triggering
  - 40 million events per second
  - Electromagnetic shower ionised the liquid Argon
  - Induces triangular electric signal in electrode



# LHC to HL-LHC

Increase in luminosity in two phases in 2022 and 2029 to reach the HL-LHC

- Run 3 μ = 50
- Run 4 μ = 200

Requires an upgrade of the detectors

- The triggering system for the ATLAS Liquid Argon Calorimeter (LAr) was replaced during phase-I

# Phase-I of the LAr upgrade

A new LAr trigger system for high pile-up environment with a total of 34048 SCs.

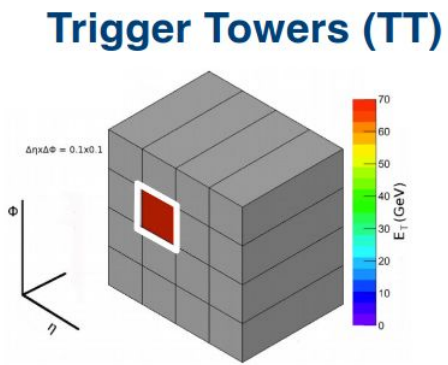
- Finer granularity than Trigger Towers.
- Better trigger energy resolution.
- Higher efficiency in selecting physics objects.

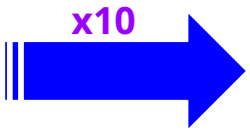
**Trigger Tower (TT)**

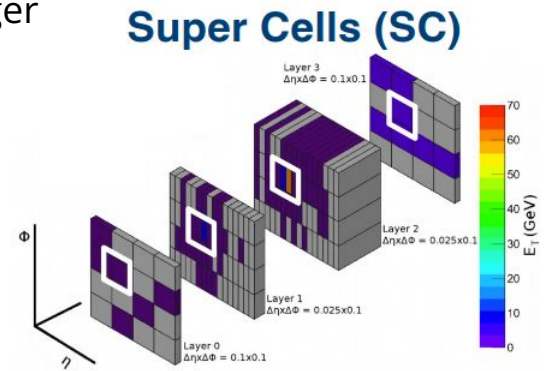
- No longitudinal segmentation
- Fixed size in Δη × Δφ = 0.1 × 0.1
- Up to 60 cells from 4 layers
- Only ~5.4k TT from 180k cells
- Analog trigger

**Super Cells (SC)**

- Lateral & longitudinal segmentation
- Increased granularity in Front and Middle to Δη × Δφ = 0.025 × 0.1
- Up to 8 cells from 1 layer
- ~34k SC from 180k cells
- Digital trigger



# New electronics for Phase-I

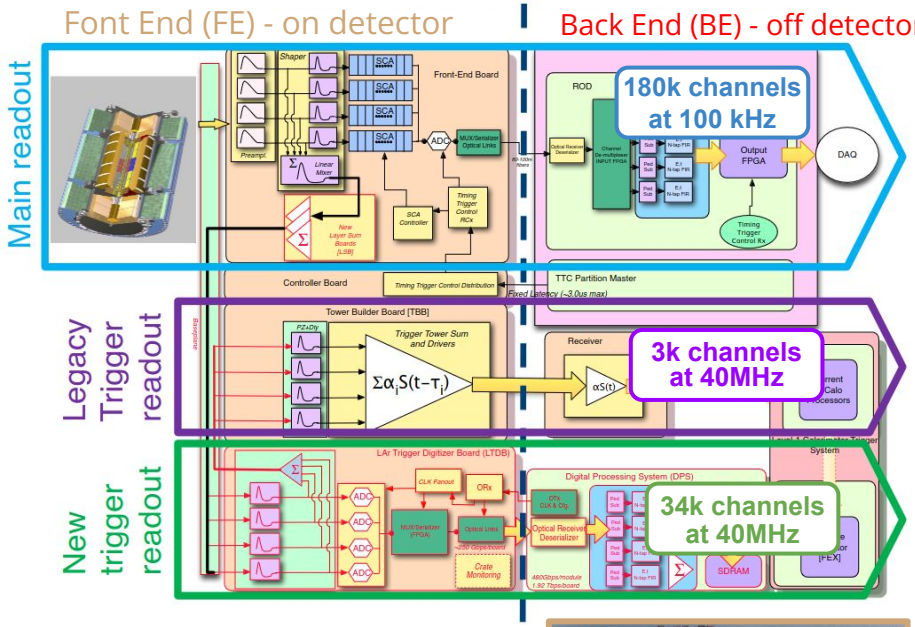
The entire readout system is affected by this upgrade

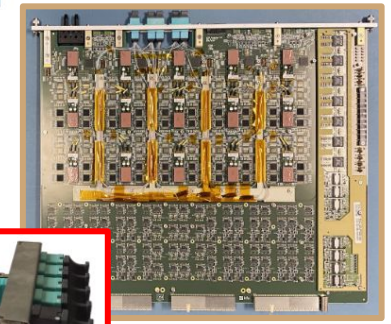
The front end electronics of the legacy trigger was dismantled then reassembled, some components replaced:

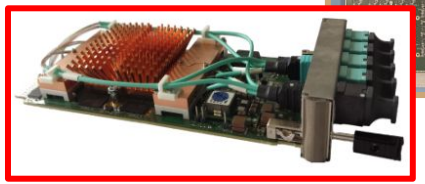
- Baseplane
- Front End Board
- Layer Sum Board

New cards added for the digital trigger

- LAr Trigger Digitizer Board
  - Send analog signals to Tower Builder Board, digitize analog signals, and send digital signals to the back-end. A total of 124 LTDBs are installed
- LAr Digital Processing System
  - LAr Carrier
  - LAr Trigger prOcessing MEzzanine
    - Receives ADC counts from a LTDB via 40 optical fibers with the speed of 5.12 Gbps for each fiber, computes energy and pulse timing in a FPGA and sends energy to Feature Extractors.
      116 LATOMEs are installed.





# Scientific purpose

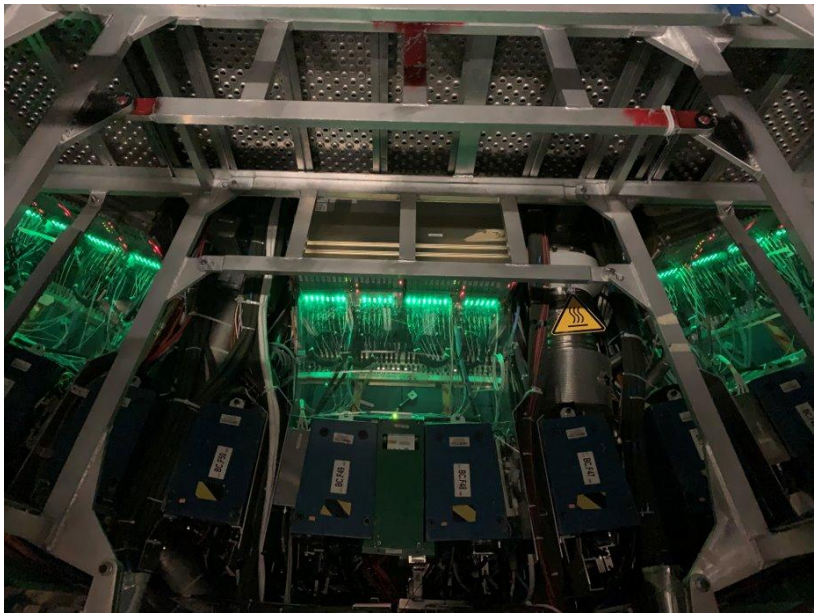
**Thesis subject:** Implementation and performance of the reading and triggering system for the Liquid Argon Calorimeter of the ATLAS experiment

Installation and validation of LTDBs completed by early 2022
All LTDBs operational for the start of data collection in March 2022

Digital trigger activated on EM objects in May 2023
Analog trigger remains active on other objects.

Trigger digital will be the only trigger in early 2024

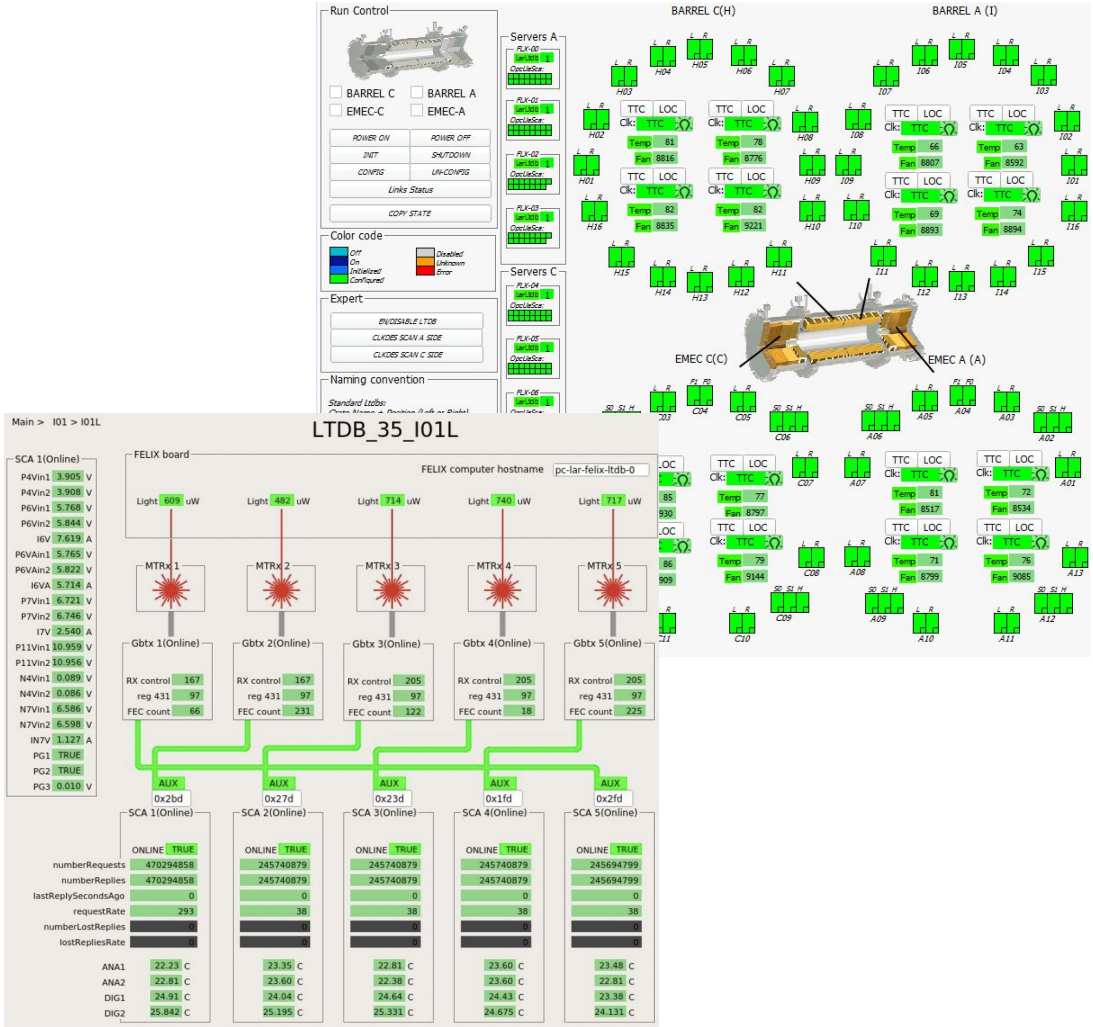
- Continue to monitor and control LTDBs
- Target 100% of LTDBs operational
  - Study and understanding of problems
- **System performance assessment**



# DT front end slow control & monitoring

LTDB 124 boards

- Control:
  - Configuration of all the boards
  - Calibration
  - General status
- Monitoring:
  - Optical power of the control fiber
  - Tension/current
  - Fan speed
  - FPGA temperature
  - SCA temperature/register
  - Data fiber status



# LTDB phase selection

To be able to decode the data received by the LATOME from the LTDB

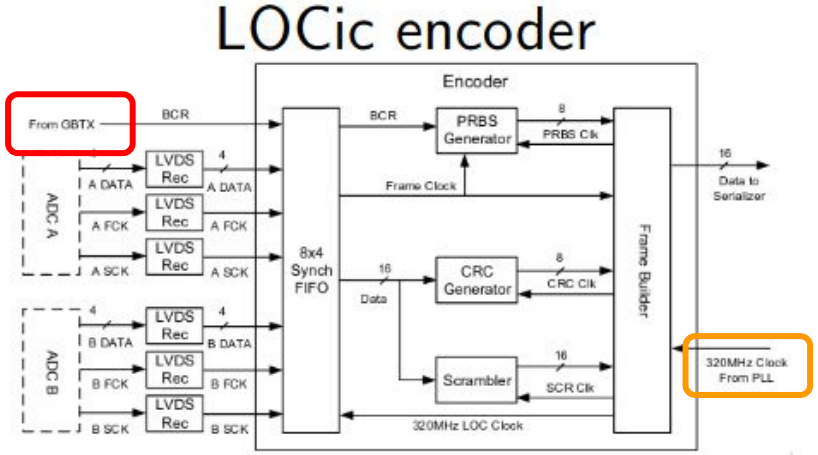
- Clk from PLL and GBTx clk should not be in phase

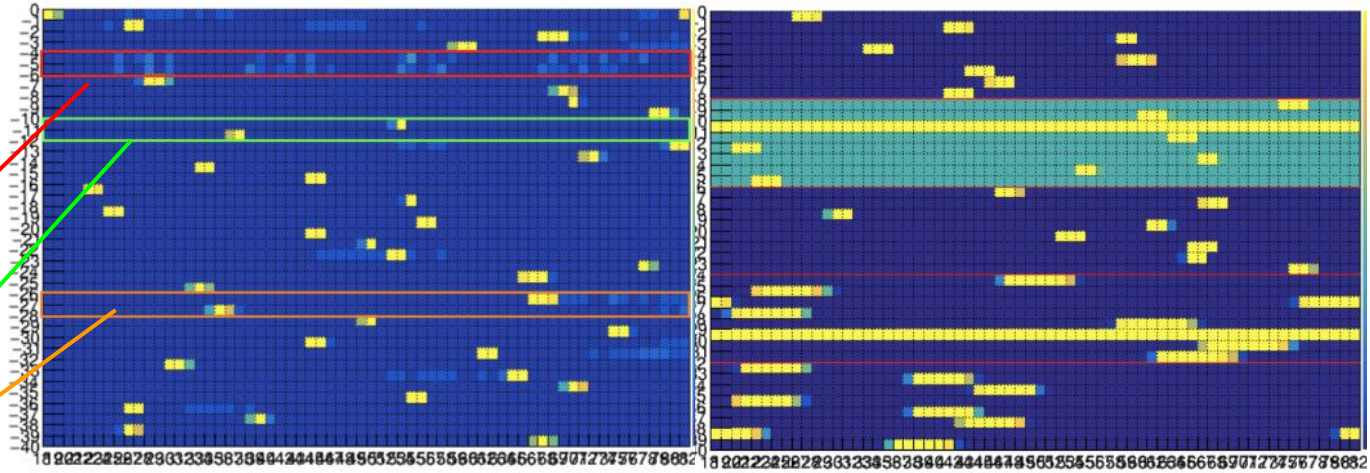
Develop a calibration to choose the delay between the 2 phases:

- Works per pair of fibers (1 LOCx2)
- 64 delays in total
- For each delay → look at the number of errors received by the LATOME
  - If errors are received → delay is tagged as wrong
- Should be done after each power cycle
  - Was very instable
  - Was done more often (~1/week)

Solution found:

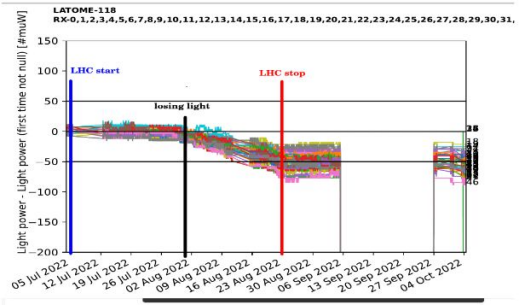
- GBTx reset
- LATOME transceiver reset

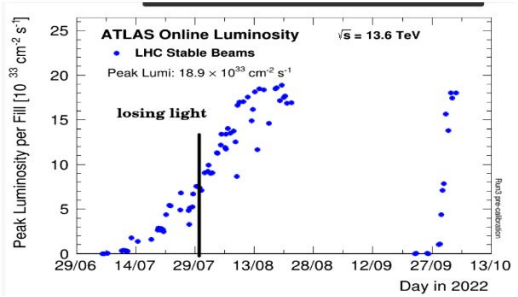


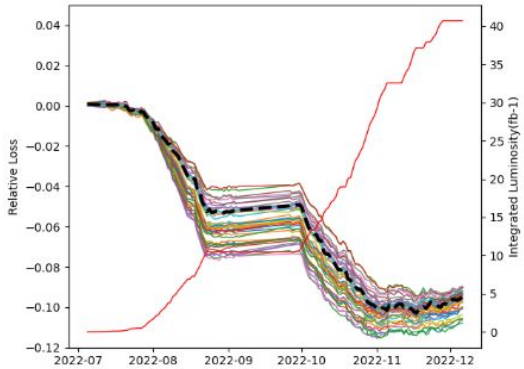



0 peak or severals
1 peak only
1 peak and values outsides

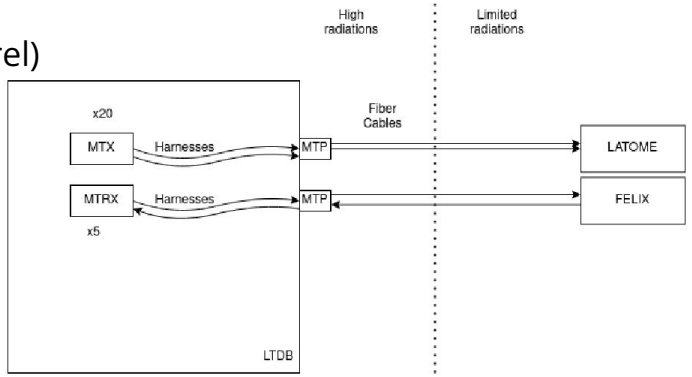
# Loss of light optical power




- Phenomenon observed on EMB (barrel)
  Slight effect on EMEC (end-cap)
- Seen on control and data fibers
- Correlated with LHC luminosity

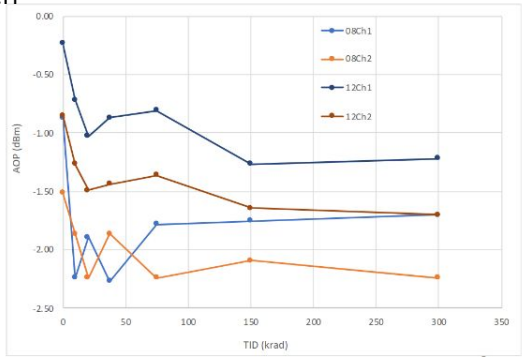



Results :

- Fiber:
  - No phosphorus found in fibers
  - Radiation test on a non-irradiated harness -0.1dB/kGy
- MTx(optical transmitter):
  - Production test → A decrease in light then stabilization after a high dose of radiation
    - Corresponds to the problem observed on the system
  - Origin of the problem: a transistor in the LOCic circuit is sensitive to irradiation
  - Effect known and in agreement with spec but forgotten

Setting optical power alarms

For LTDBs with very low optical power optical power: replacement at the end of the year



# Study on time shifting

Observation of a time shift (TAU) during a calibration run

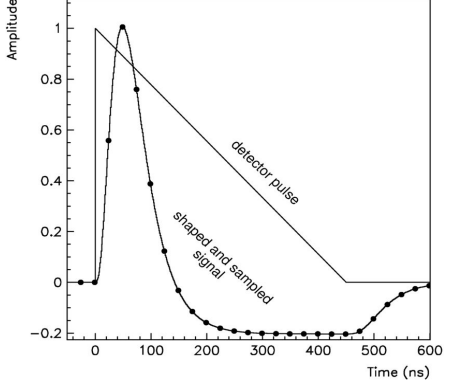
- TAU = 0 ns → max amplitude of the LTDB ADC pulse
- TAU ≠ 0 ns → energy transmitted to the LATOME and not optimal

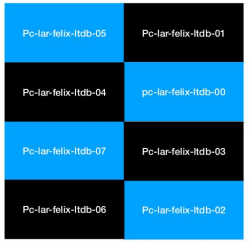
The aim of my study is to identify the source of the problem and quantify the loss in performance caused by this timing shift

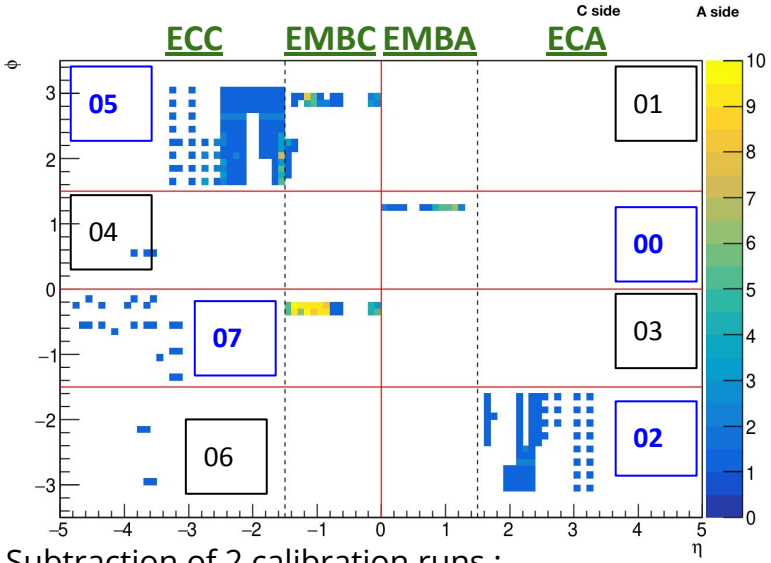
- Timing shift occurs when FE FELIX LTDB machines are power cycled
- It is of the order of -5 ns to 5 ns
- Appears within an LTDB, but not on the entire LTDB
  - All SCA/GBTx channels shift in the same way

List of tests that do not induce a time shift :

- LTDB GBTx reset
- Switch off clock signal at FELIX input
- Deactivate/activate FELIX uPOD light
- Reload FPGA FW



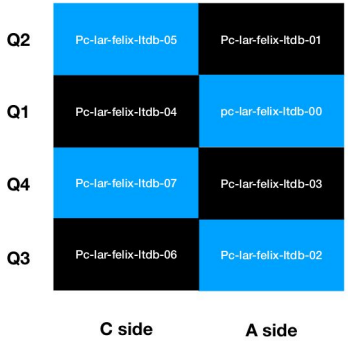




Subtraction of 2 calibration runs :

- power cycle run - reference run
- All Super Cells with Tau > 3ns

# Study on time shifting

- 8 pc-lar -felix-ltdb-XX
  - 2 boards FLX 712/pc
    - 2 device
      - max 4 LTDBs/device
        - 5 elinks/LTDB

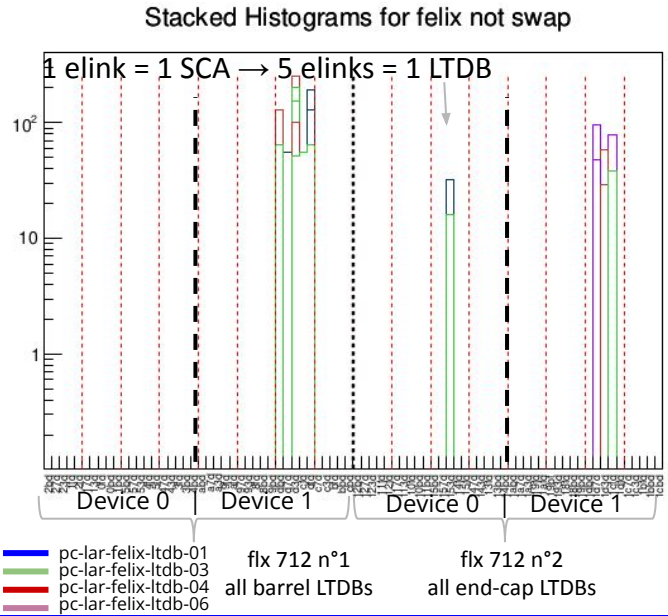



TAU/elink distribution for the 8 pc-lar-felix-ltdb-xx over 12 calibration runs

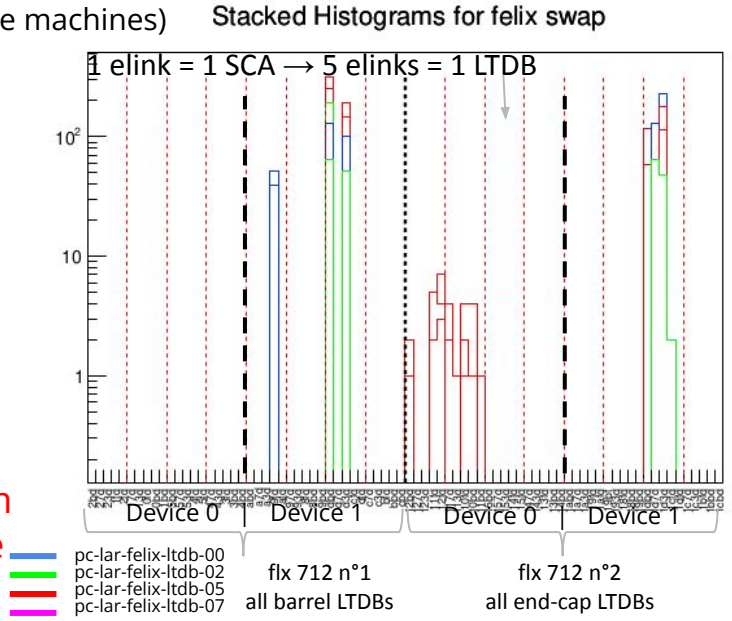
- Power cycle on blue and black machines
- Timing shift appears mainly on the last elinks of device 1 on FELIX boards

Procedure:

- Swap cable on 4 machines (blue machines)
- Power cycle on all FELIXs
- Calibration run
- Power cycle on all FELIXs
- Calibration run
- …




The timing shift persists on the same elink despite moving the LTDBs, confirming that the problem originates on the FELIX side



# Performance evaluation

Performance of a specific calibration run:

- Pulse simultaneously on all supercells
- Then shift the 32 samples of the 1ns pulse
- Shift up to +24 ns.

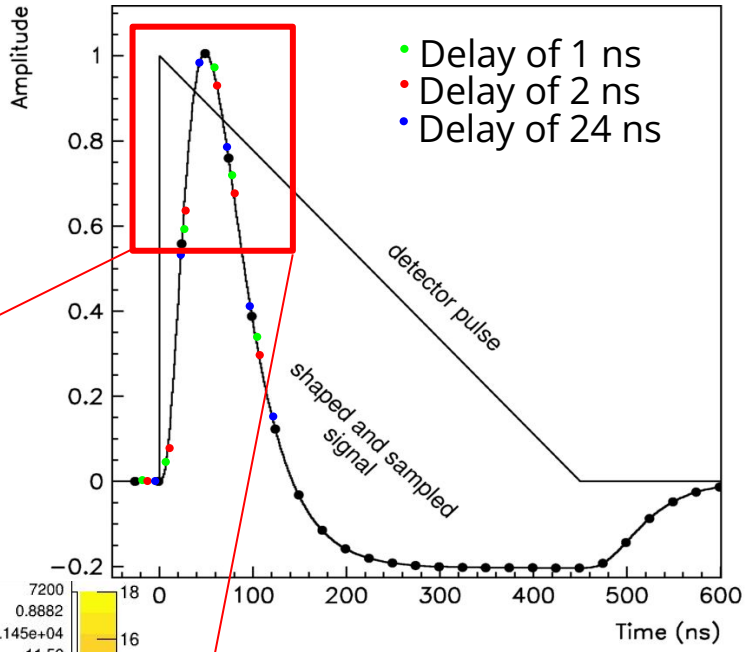
This gives a complete scan of the ADC pulse from 0 ns to 25 ns, for the 34,048 supercells

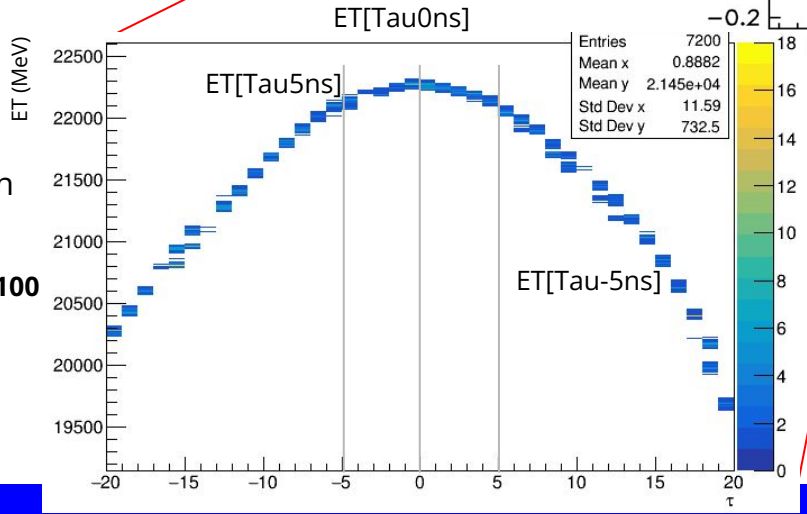
For each SCs:

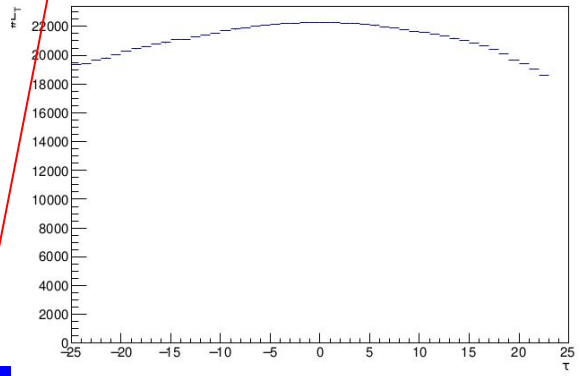
- Compute the average energy
  - TAU 0ns
  - TAU 5ns
  - TAU -5ns
- Calculate the ratio as a function of the energy a TAU0

**Ratio = (1- ET[Tau5ns] / ET[Tau0ns]) x 100**

SC 956410880
- EMB
- Middle layer



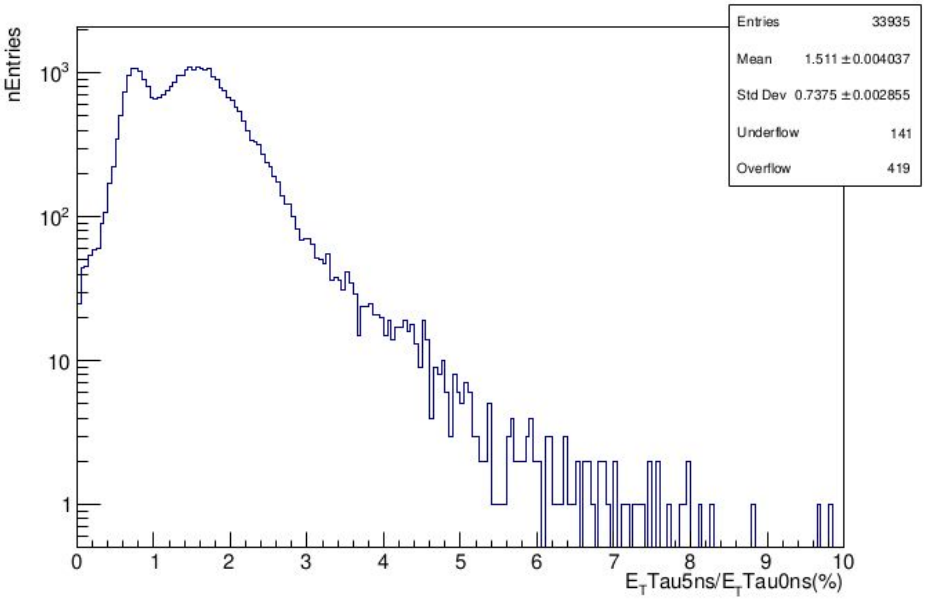
# Distribution of lost energy in % for all SCs

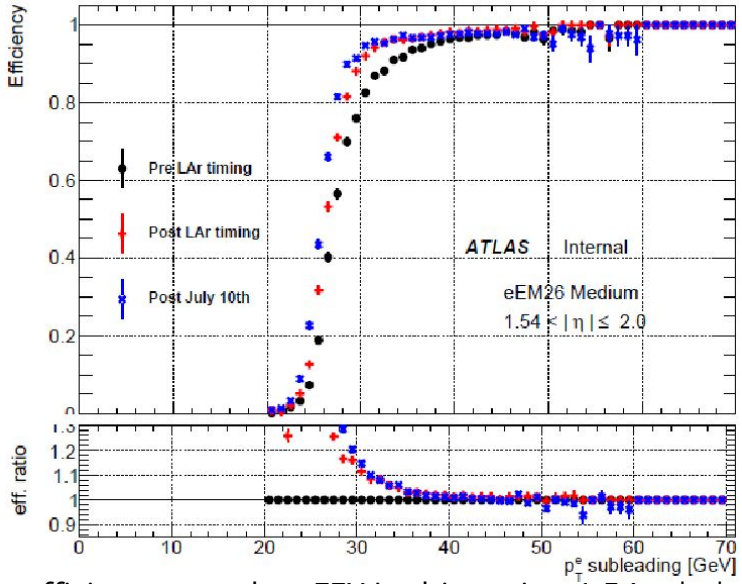
Energy lost when TAU = ± 5ns

- EMB → 1%
- EMEC → 1.5%
- HEC → 1.1%
- FCAL → 3.4%

Overall Timing shift have a small impact on the SCs energy reconstruction

Trigger efficiency clearly impacted by this timing shift

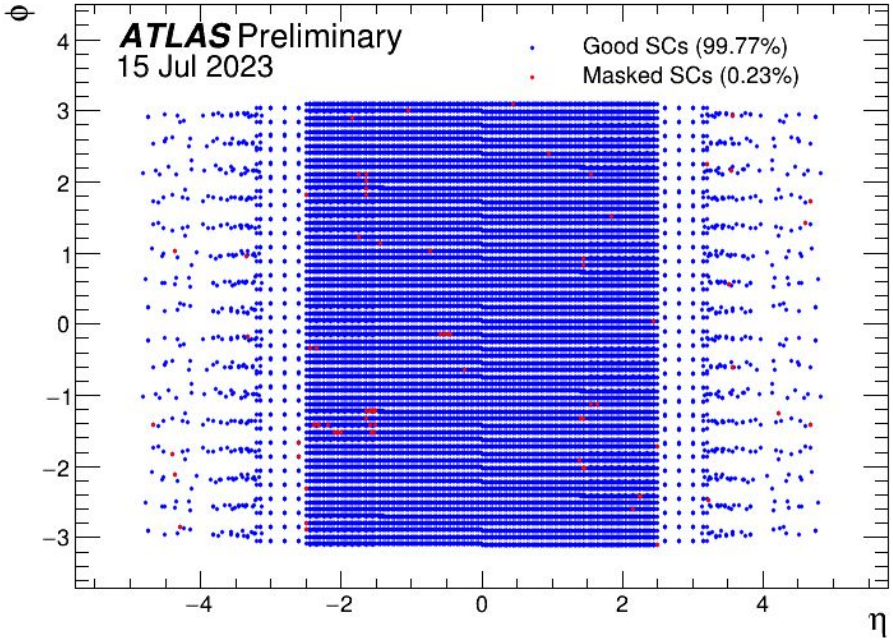



Trigger efficiency seen by eFEX in this region 1.54 < |η| =< 2.0

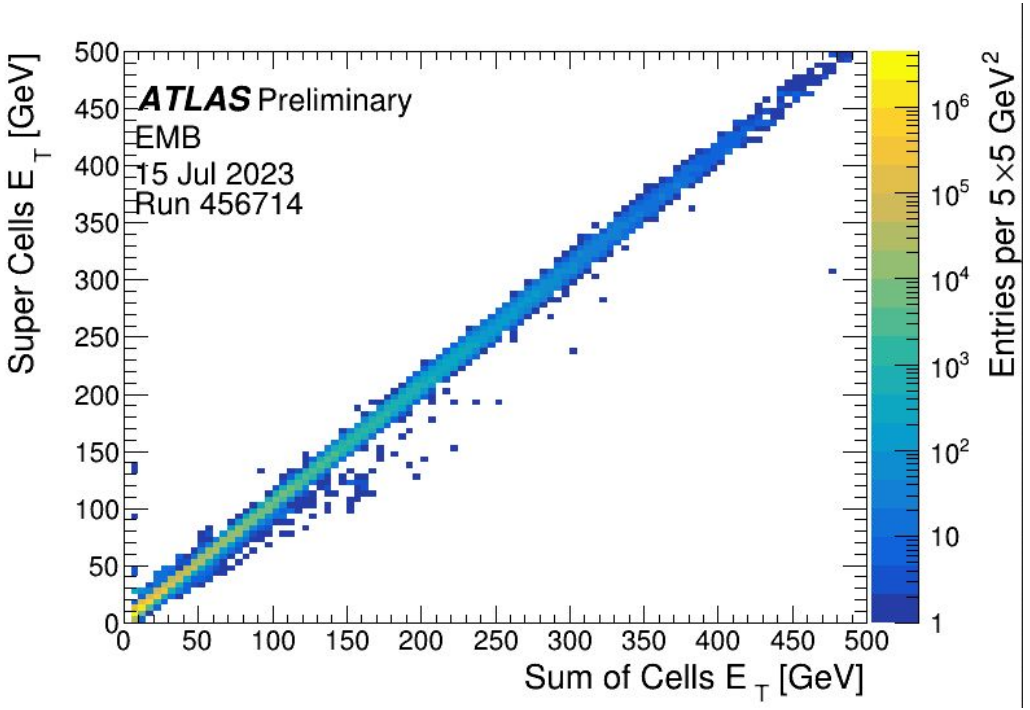
# Digital Trigger status

- SC status reported on 15 July 2023 for a pp collision run at √s = 13.6TeV
- 99.7% of SCs (33970 out of 34048) show (in blue) have no issues and return the expected timing and energy
- 78 SCs (in red) are dead, it comes from known problematic Digital Trigger Front End Board channels (LTDBs or with known calibration issues)



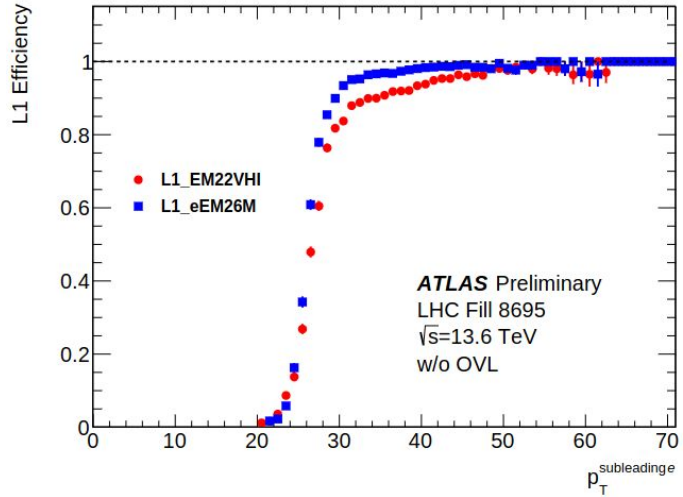
# Energy comparisons DT - main readout

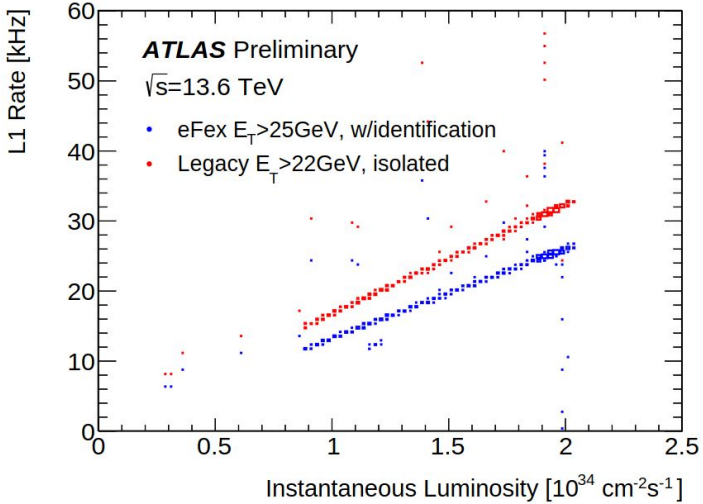
- Supercells transverse energies ($E_T$) are compared to the sum of the corresponding LAr cells in the main readout
- The data from the run with the pp collision at √s = 13.6 TeV on 15 July 2023 is used for the comparison
  - Bad SCs are not included
  - **A good agreement is observed between the two readouts**



# Phase-I trigger performance

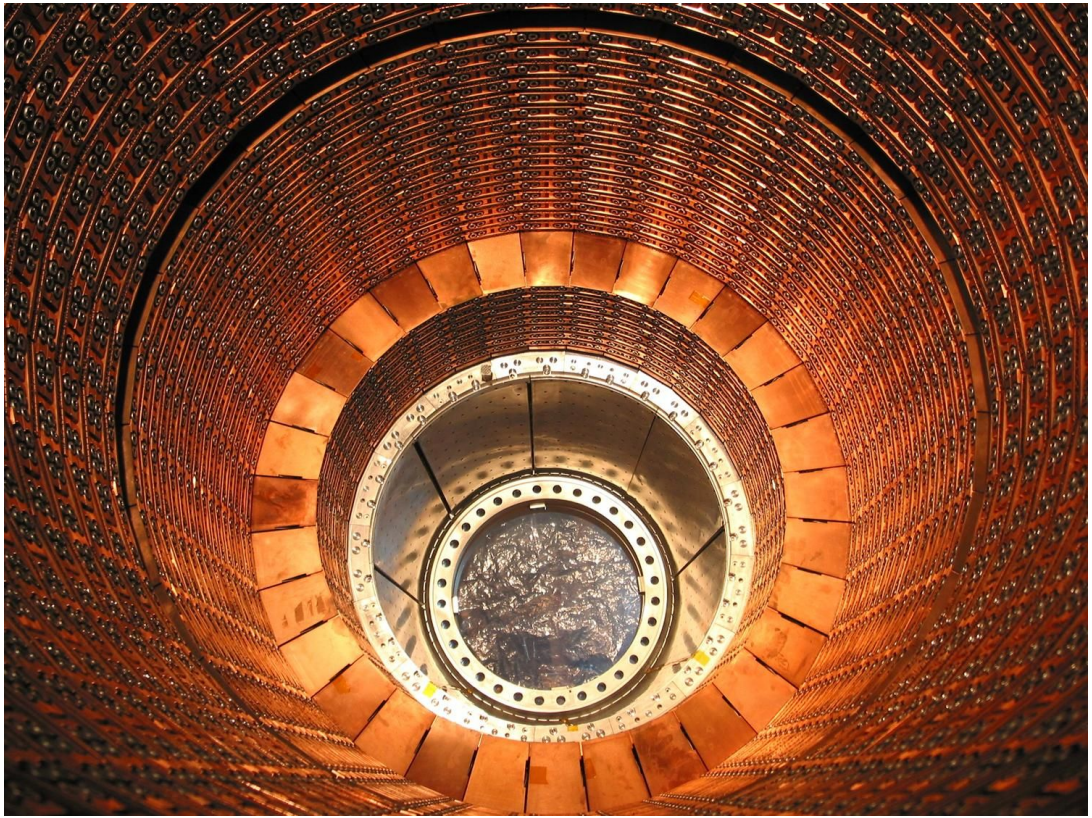
- Cell energies correspond well between calorimeter cells and SCs
- The single electron triggers for the legacy system and the Phase-I system are compared
- Phase-I EM trigger item shows better performance:
  - Sharper efficiency turn-on curve
  - Lower trigger rate (~80% of legacy EM item) at the same ET threshold
- Phase-I EM items used as primary trigger now
- Plan to turned on the rest of the phase-I system beginning of 2024



# Thank you for your attention

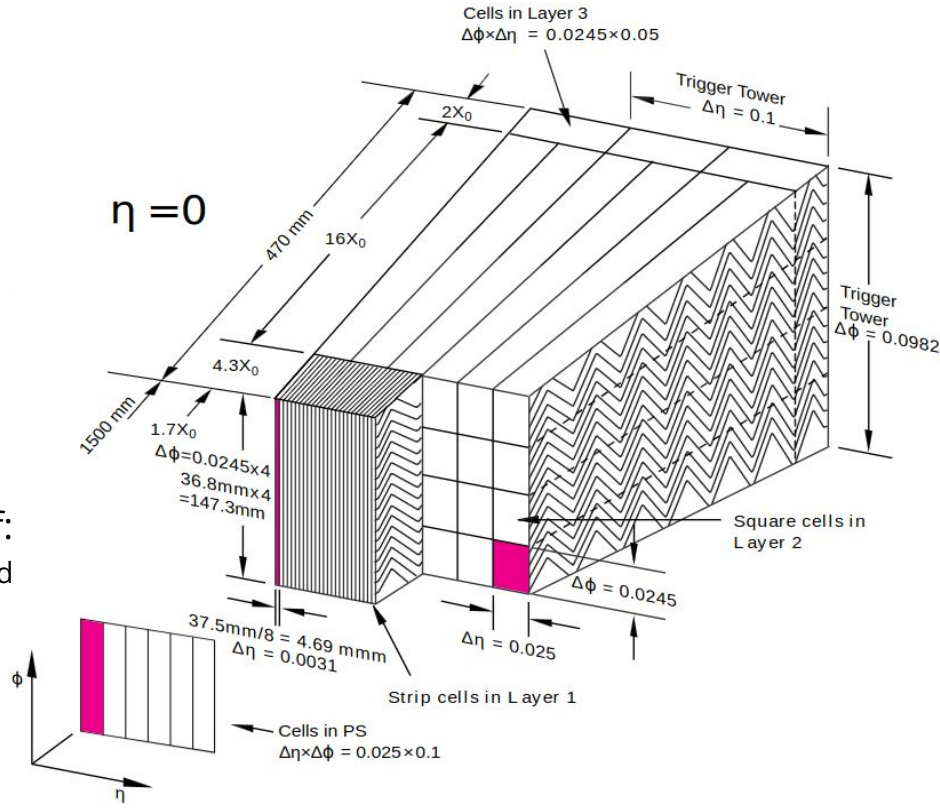
Any questions ?



# BACKUP

# LAr calorimeter layers

- LAr cells are the readout units with the finest granularity
  - The size of LAr cells is varying in different parts of the calorimeters
  - In total there are **182418** LAr cells
- The readout units for the trigger are composed of the sum of LAr cell signals call trigger tower
  $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$
  - A new trigger system was introduced in Run 3 with a smaller units
- The barrel electromagnetic calorimeter consists of:
  - **Presampler**: correction of the energy loss caused by dead material
  - **Front layer**: fine granularity along η
  - **Middle layer**: most of energy deposit
  - **Back layer**: recovery of e/γ longitudinal energy leakage



# Legacy readout electronics

The readout system is composed of front-end (on detector) and back-end (off detector) electronics.

Front-end:

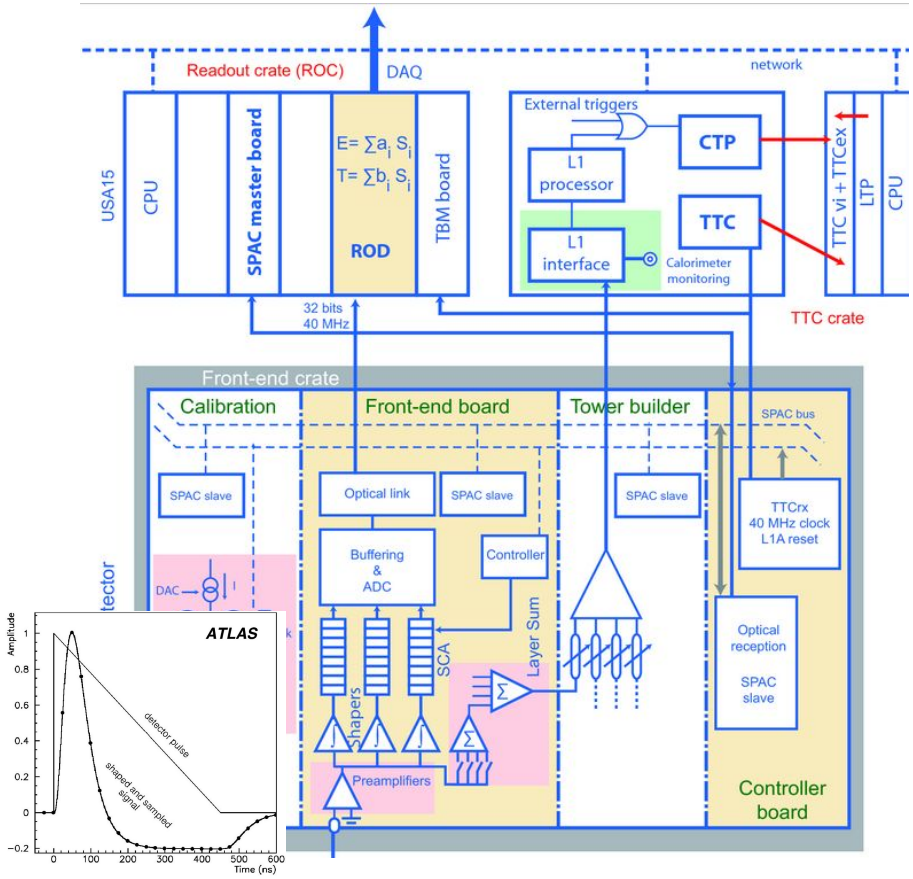
- **Front End Boards (FEBs):**
  - Analog signals from LAr cells are amplified, shaped to bipolar analog signals, and digitized using 12-bit ADC.
  - **Layer Sum Boards** (LSB) on FEBs sum the analog signals.
- **Tower Builder Boards (TBBs):**
  - Analog signal sums from LSB are received in TBB, which forms trigger towers with a granularity of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$

Back-end:

- **Read Out Drivers (RODs):**
  - RODs receive digital signals from FEBs and compute the energy, time phase, and quality of the signal.
- **Level-1 calorimeter (L1Calo) system:**
  - Analog signals from trigger towers are sent to L1Calo, which identifies physics objects and sends the results to the Central Trigger Processor (CTP).

Main readout: FEB → ROD

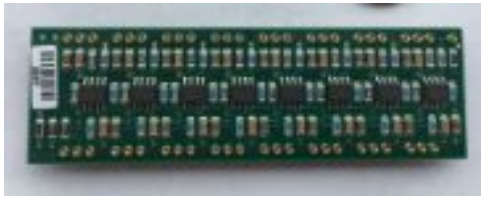
Legacy trigger: LSB → TBB → L1Calo

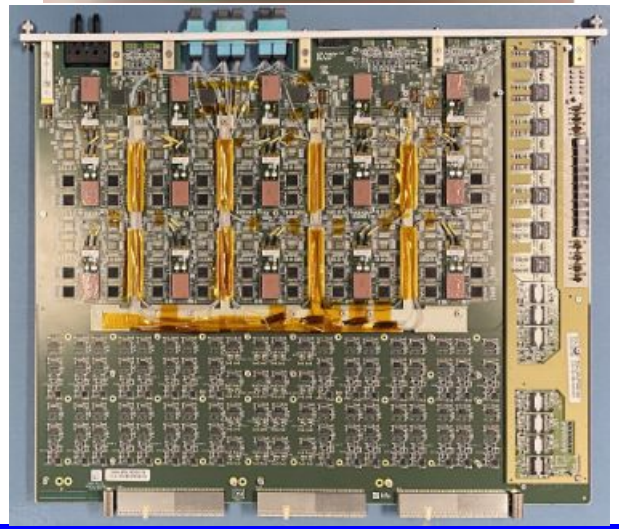


# Front-end electronics

**Baseplane:**
New baseplanes provide an additional slot for LTDB and distribute analog signals of SCs from FEBs to LTDB.

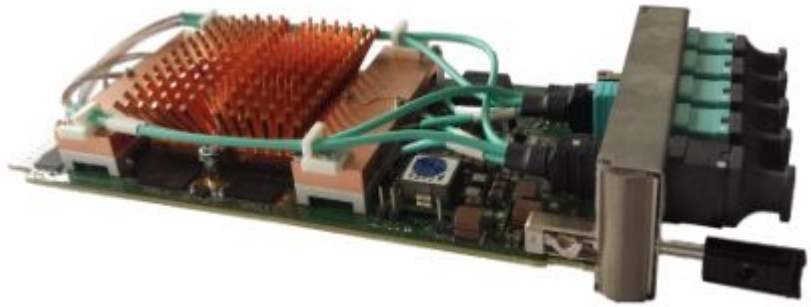
**Layer Sum Board (LSB):**
A plug-in card of the FEB provides a sum of analog signals for SCs. 2328 LSBs are replaced.





**LAr Trigger Digitizer Board (LTDB):**
Send analog signals to Tower Builder Board, digitize analog signals, and send digital signals to the back-end. A total of 124 LTDBs are installed

# Back-end electronics



**Intelligent Platform Management Controller (IMPC):**
Manage the power, cooling, and interconnect needs of intelligent devices.

**LAr Trigger prOcessing MEzzanine (LATOME):**
Receives ADC counts from a LTDB via 40 optical fibers with the speed of 5.12 Gbps for each fiber, computes energy and pulse timing in a FPGA and sends energy to Feature Extractors. 116 LATOMEs are installed.

**LAr Carrier (LArC):**
Transmit data from LATOMEs to the readout system, distribute clocks and trigger signals synchronized to the LHC beam clock. 30 LArCs are installed.

# LATOME firmware

Input: 5.12GHz/fiber
40 fibers

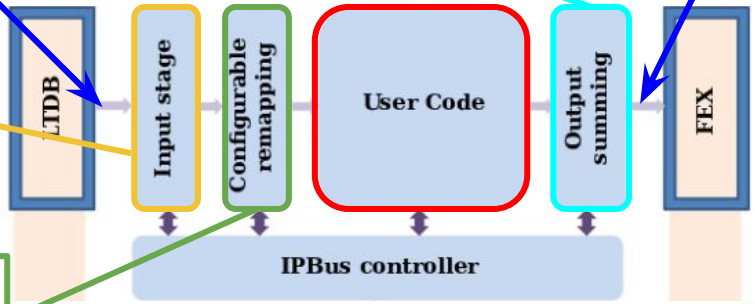
Output: 11.2GHz/fiber
40 fibers

Sum SCs for triggering

8 SCs x 16bit = 128 bit sent as 1 frame at 320MHz

Frequency is reduce to 240MHz
Mapping in function of SCs

Energy reconstruction
Bunch Crossing identification
Baseline correction
Saturation detection



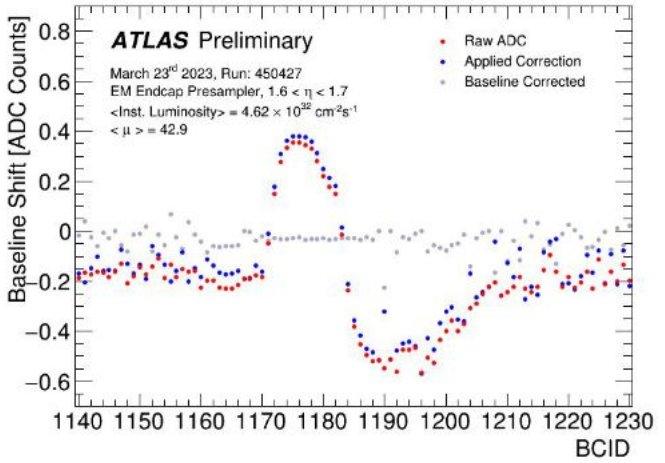


FPGA resource occupancy
- 91% of logic unit
- 95% of block memory

$$E_T = \sum_{i=0}^{3} \widetilde{A_i}(S_i - p - b)$$

$$E_T\tau = \sum_{i=0}^{3} \widetilde{B_i}\,(S_i - p - b)$$

Si ⟶ ADC samples from LTDB
P ⟶ Pedestal level (Cool DB)
b ⟶ Baseline correction
Ai and Bi ⟶ OFCs (Cool DB)



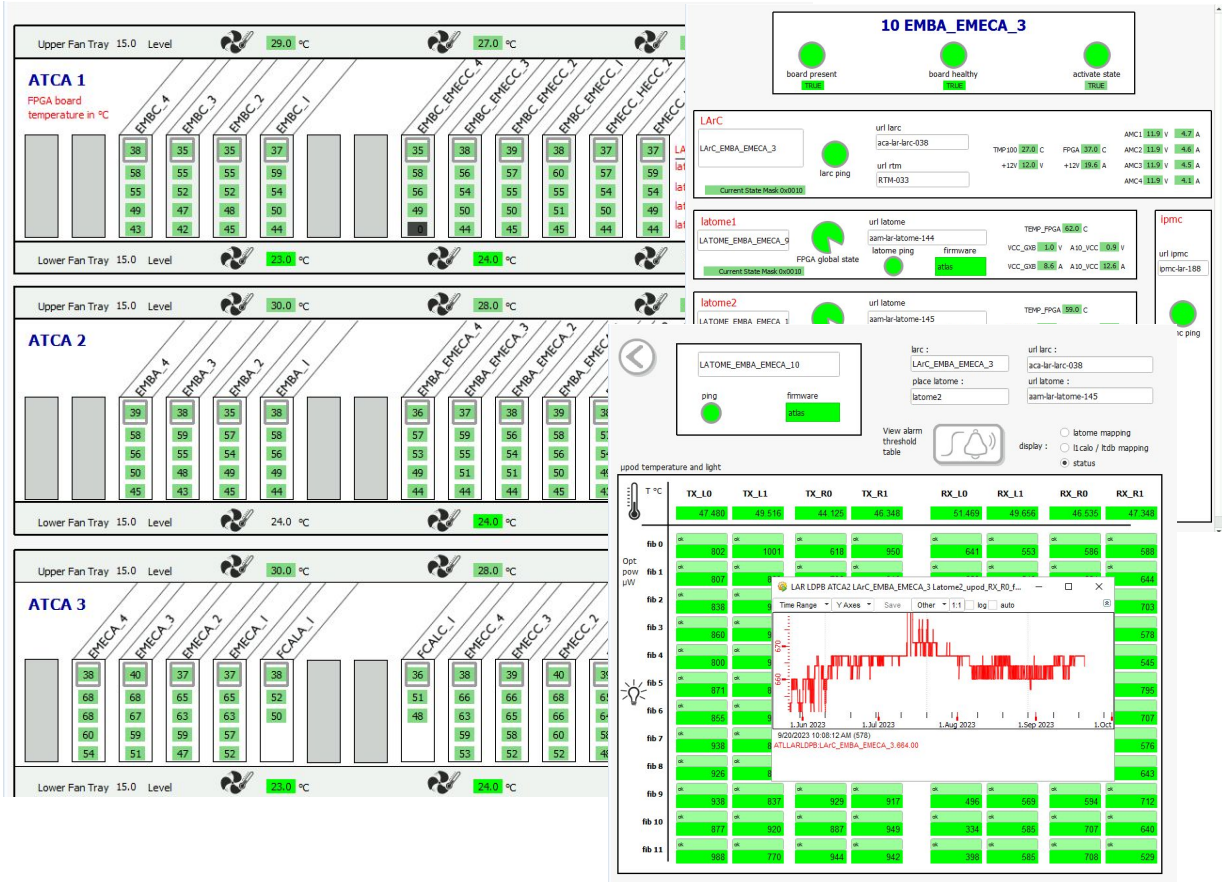
# Digital Trigger back end slow control & monitoring

## ATCA crate

- Fan speed level
- Region temperature (left, center, right)
- Rack temperature

## LDPB boards

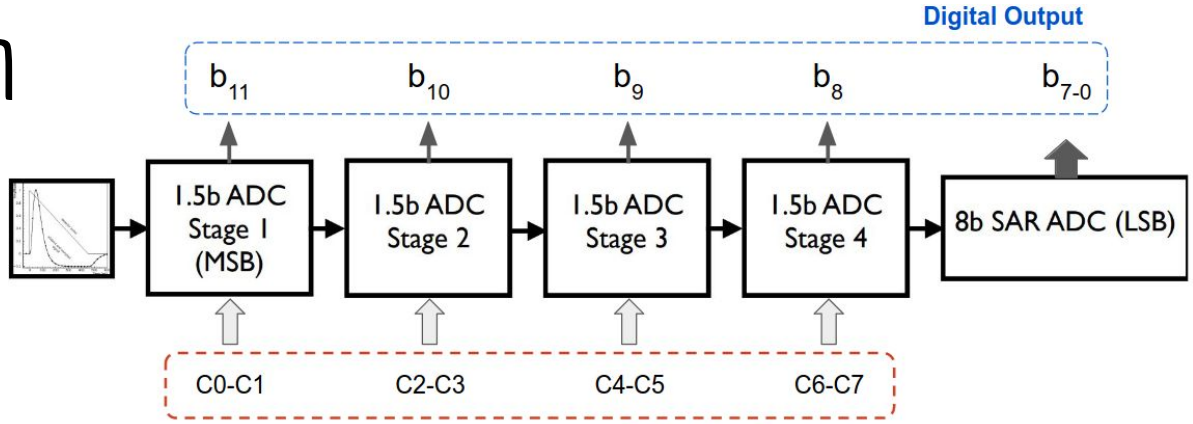
- Monitoring:
  - State
    - ID
    - Ping
    - Firmware
  - Tension/current
  - FPGA temperature
  - Optical power data fiber

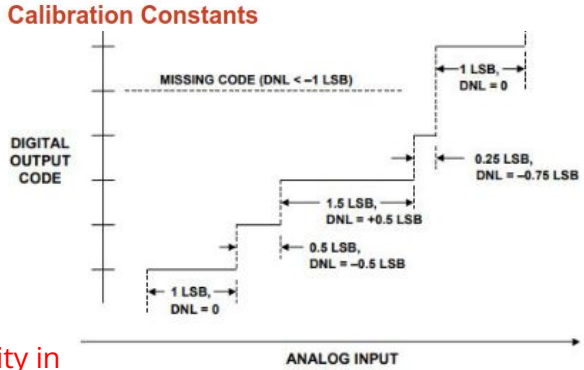


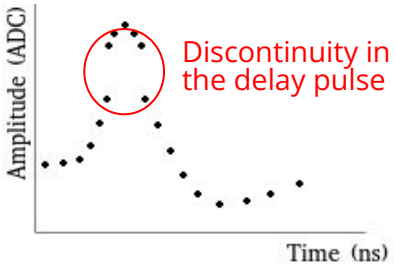
# LTDB ADC calibration

- NevisADC is a pipeline ADC
  - 4 stage of 1.5 bit MDACs
  - 8 bit SAR ADC
- Calibration constants are loaded in the MDAC units to account for gain errors
- Miscalibration can cause Differential Nonlinearity (DNL) errors → will be perceived as ADC jumps in the digitized signal
- DNL is nonlinearity of the code transitions of the converter
  It can be measured as the deviation of quantization steps from 1 LSB

**The new calibration constants solve all ADC jumps !**



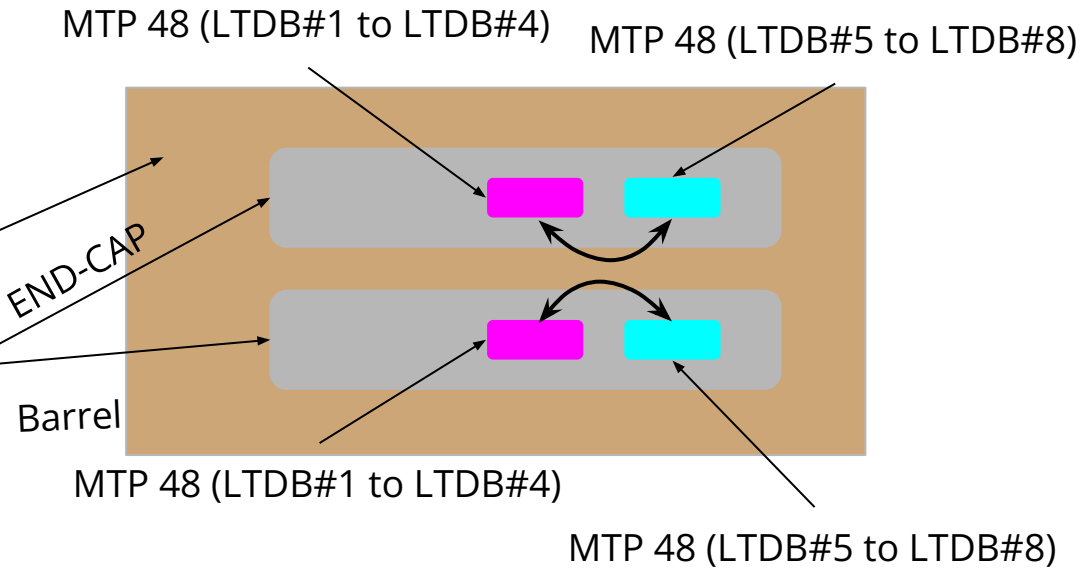



# FELIX swap fibers

pc-lar-felix-ltdb-00

FELIX-712 board




| | Barrel | END-CAP |
|---|---|---|
| | pc-lar-felix-ltdb-00 | pc-lar-felix-ltdb-00 |
| 1 | 35(I01L) | 132(A01L) |
| 2 | 31(I02R) | 127(A01R) |
| 3 | 14(I02L) | 120(A03L) |
| 4 | 27(I03R) | 116(A03R) |
| 5 | 23(I03L) | 141(A02Spe0) |
| 6 | 47(I04R) | 151(A02Spe1) |
| 7 | 21(I04L) ◆ | 179(A02HEC) ◆ |
| 8 | 22(I05R) ◆ | 187(A04F0) ◆ |

◆ Timing shift observed on these links

- Swap the blue connector with the pink one

Expected results:

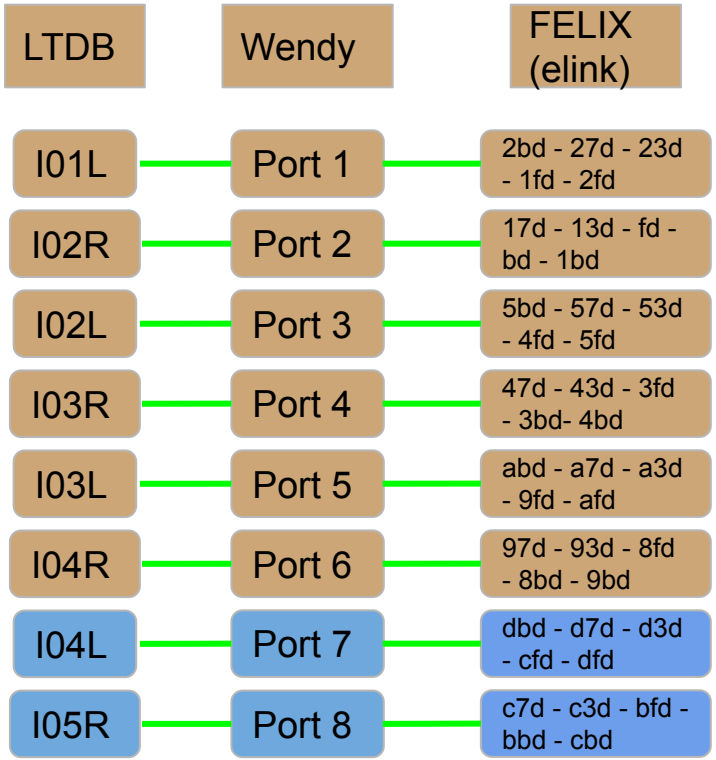
- If LTDB problem → time shift will move with LTDBs
- If FELIX problem → time shift stays on same elinks

# FELIX swap fibers

Example for
pc-lar-felix-ltdb-00 FELIX card 0

Standard cabling
Swap cabling

Observed timing shift
Timing shift if LTDB problem
Timing shift if FELIX problem




Hardware modification