Analysis of the 1st batch testing

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CALICE meeting
22/09/2023, SiW-ECAL tech meeting

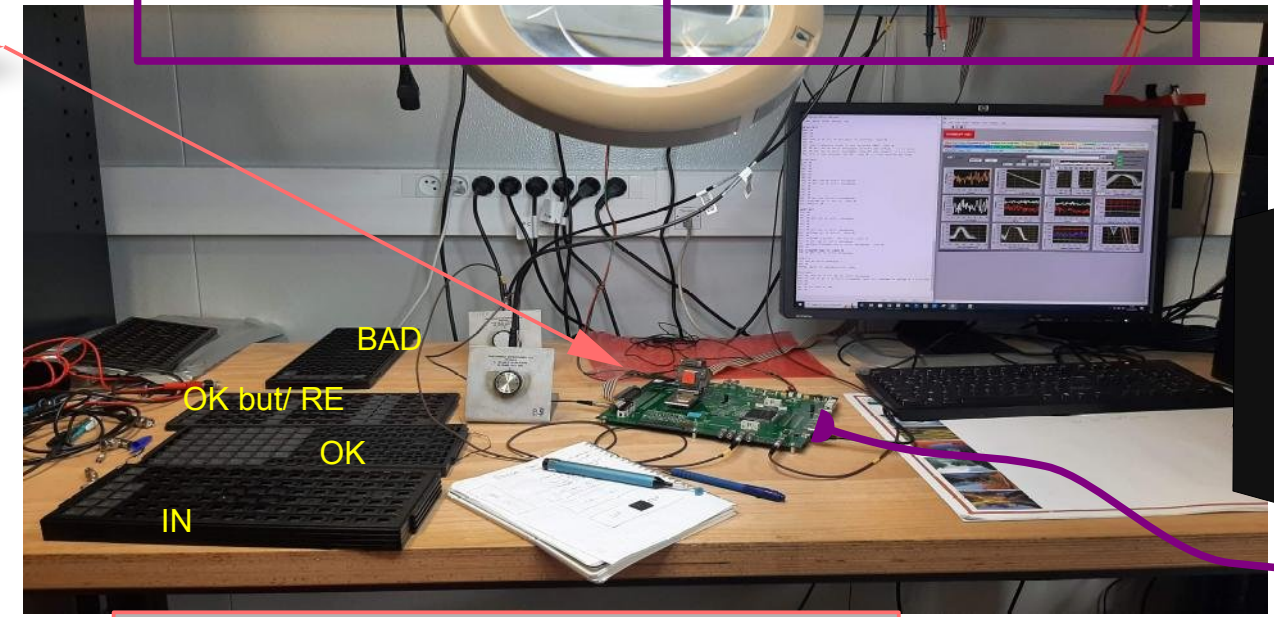
SKIROC2 test bench at Ωmega

LV power supply

WF Generator

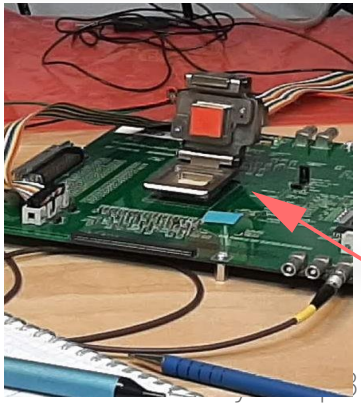
Keithley Multimeter

Test Card
(Ωmega+Kyushu)
- 1 Socket
- 1 FPGA
- 1 ADC
- Connectors
- USB R/O



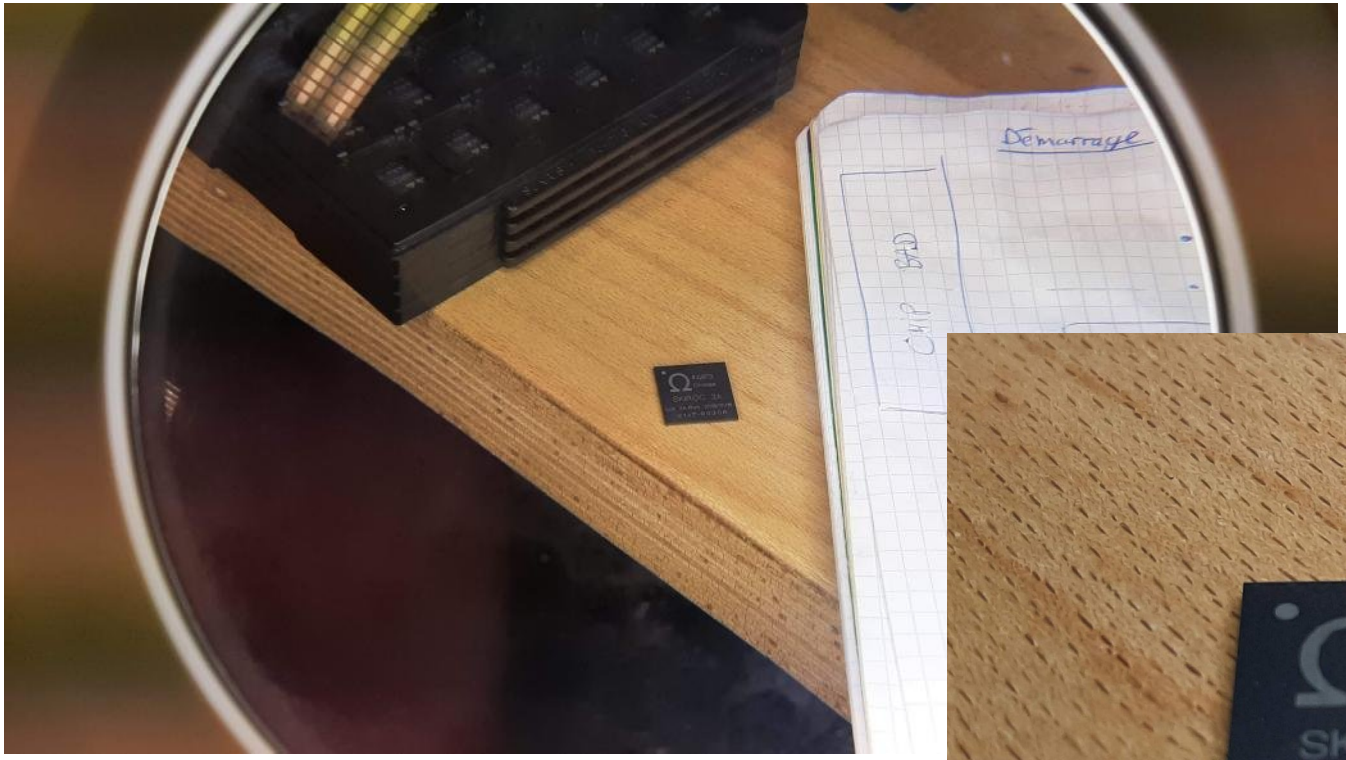
USB

PC



Socket
- IRONWOOD CBT-BGA-6036.
- Screw + paper buffers

NCAP packaging



- 460 pieces; 400 remaining
- Thinner
- Labelled

Measurements

LabView testing SW : Digital & Analogue probing 9 mins per ASIC (optim) © S. Callier

Powering

Fine Thr Adjust /ch

VDC Pre-Amp /ch

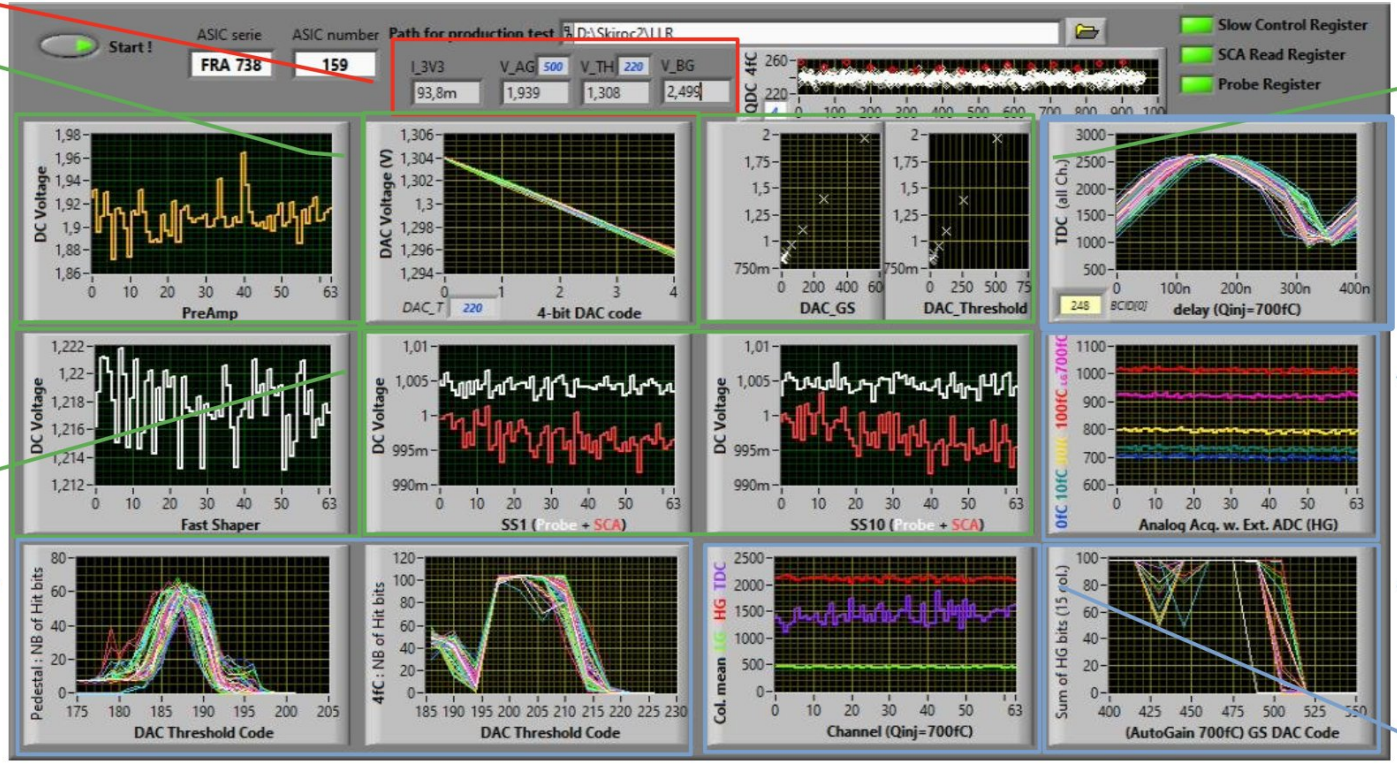
VDC Fast Shaper /ch

VDC Slow-Shaper /ch

- G1, G10
- Probe & SCA

DAC Thr scan / ch

- Pedestal
- MIP (4fC)



DAC Scan with probe:

- auto-gain (GS)
- Global Thr.

TDC Delay scan /ch

Analog Readout/ch

AutoTrigger delayed by FPGA

- HG : 0, 10, 30, 100 fC
- LG: 700 fC

AutoGain efficiency

(SCA 0–14) Qinj = 700fC

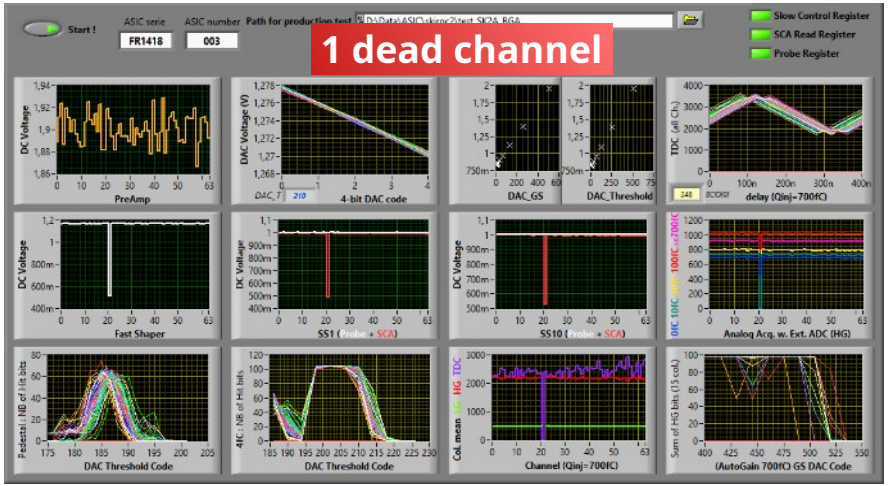
Eff. per Ch. vs Gain code

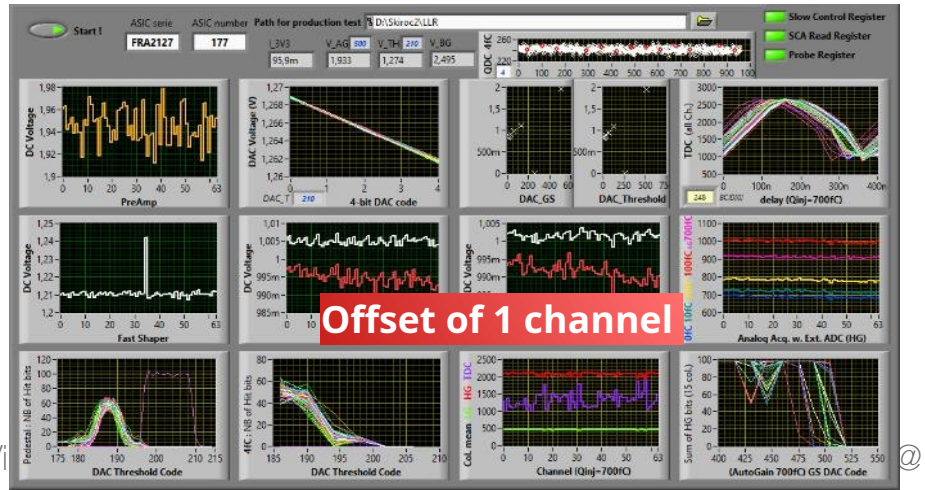
ADC ⟨SCA0–14⟩/ch

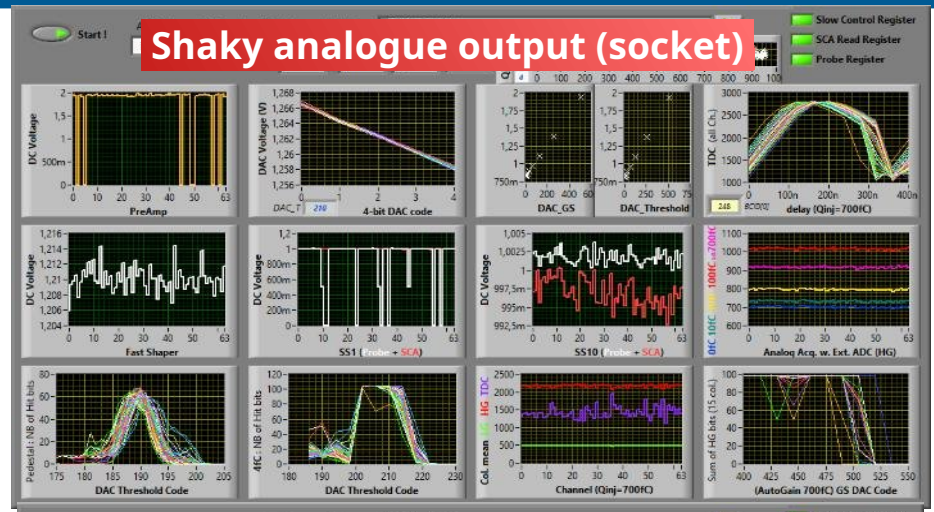
Qinj = 700fC

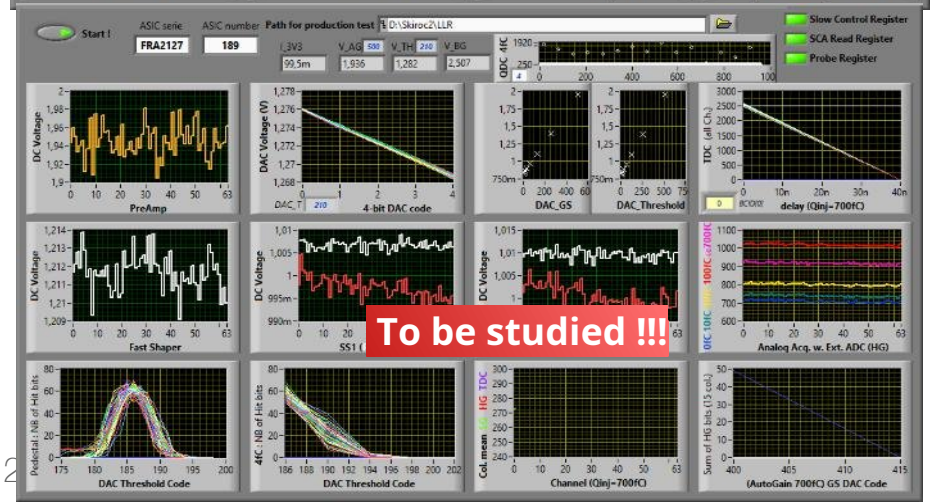
- HG, LG, TDC(SCA0)

Examples of errors









Novapac

46 chips tested

	Data	
Statut	Count - Statut	Count - Statut
BAD	8	17 %
OK	35	76 %
OK but	3	7 %
Total Result	**46**	**100 %**

Count - Rems	Statut			
Remarks	BAD	OK	OK but	**Total Result**
1 channel 60 (61e) with abnormal pedestal		1		**1**
Noisy (ERREUR alim 6.3V et -7V off)			2	**2**
Thr DAC not working	1			**1**
fine scan of DAC_GS not working		1		**1**
multi problems	2			**2**
no digital data (ADC); 23e voie off	1			**1**
No probe register V_BG = 1.873; I_3V3 = 695m !!!	1			**1**
pb preamp	2			**2**
pb probes; internals OK			1	**1**
pbm de probe reg. court circuit FS ? Conso 160mA; pbm SCA 8 ?	1			**1**
(empty)				
Total Result	**8**	**2**	**3**	**13**

NPAC

400 ASICs

- 105 tested

	Data	
Statut	Count - Statut	Count - Statut
BAD	3	3 %
OK	85	81 %
OK but	11	10 %
RE	6	6 %
Total Result	**105**	**100 %**

Count - Rems	Statut			
Rems	BAD	OK	OK but	RE
8mA de consommation		1		
Multiple problems; a étudier		1		
issue with DAC_GS ?			1	
Noisy (alim OFF so… normal) --> A re tester				4
low pedestal (~176)			1	
No analogue output		10		
OK mais pas de sortie analogique (alim OFF donc normal) --> A re tester				2
No digital output		1		
pas de TDC ni de sortie analogique (peut être problème de cablage de l'injection)			1	
problème injection + TDC voie 29			1	
problem ch 41			1	
problem ch 62			1	
problem ch 49			1	
quelques étrangeté sur la sortie analogique		1		
voie 12 plus bruyante (thr+20); Faire vérifier par Steph			1	
voie 36 avec un offset de 30mV à corriger avec le DAC 4bits		1		
voie 36 pb SS1; no auto gain; no injection			1	
voie 47 mauvaise valeur LG avec injection 700fC			1	
voie 6 pb shaper			1	
(empty)				
Total Result	**3**	**12**	**11**	**6**

Conclusions

FEV2.1 PCBs ready for measures (then cabling)

- All component for cabling now available

ASIC testing :

- **Previously** : only basic configuration and simple readout test were performed, WITHOUT any quality check ~ response to DAQ ✔
- **Now**: Quality control is performed on all stages for all channels ! Even on non used stages for analogue readout. We are ensuring that the response of each channel is identical.
- 1st learning phase
  - Socket: Mechanically hard to handle

SKIROC2a 1st Analogue Batch Tests :
~ 1/3 of available stock (~450).

- 2 packaging
  - NOVAPAC: 75% GOOD, but 15% BAD.
    Includes some already tested (only on config-data)
  - NPAC: 80% GOOD, but 3% BAD,
    some specific dysfunctions
    - Most errors affect only single channels
- Preliminary STAT, **worse** than reality.
  - standard settings → adjusments (e.g. thr.) possible
  - “OKbut” ASICs will be retested with tuned settings
  - requires better classification

Full Analysis (started)

Data has been recorded

- text format
- Example of paaremeters to be extracted

Granularity	Parameters	Rem
Set of ASIC's		
ASIC-wise	Temperature	optimal stabilisation time to be measured
	Power ×2 (VDD, VDD_PA)	V*I during measurement
	LG ADC Ped, σ	
	HG ADC pedestal, σ	
	⟨Ped⟩_thr, ⟨sigma⟩_thr	from channels
Channel-wise	Low Gain ADC Ped, Sigma	From non-triggered channels, from external triggers ?
	High Gain ADC Ped, Sigma	From non-triggered channels, from external triggers ?
	Trigger Ped, sigma adcc, σ	From S-Curve : single or two-sided ?
	Relative LG ADC linearity (adcc, σ vs Ampl)*n	From charge injection
	Relative HG ADC linearity (adcc, σ vs Ampl)*n	From charge injection
	TDC linearity (adcc, σ vs ns)*n	From charge injection ≠ Amplitudes ?
	Low Gain Mip response (adcc)	From Sensors
	High Gain Mip response (adcc)	From Sensors
	Threshold linearity (adcc vs DAC)	Threshold scan

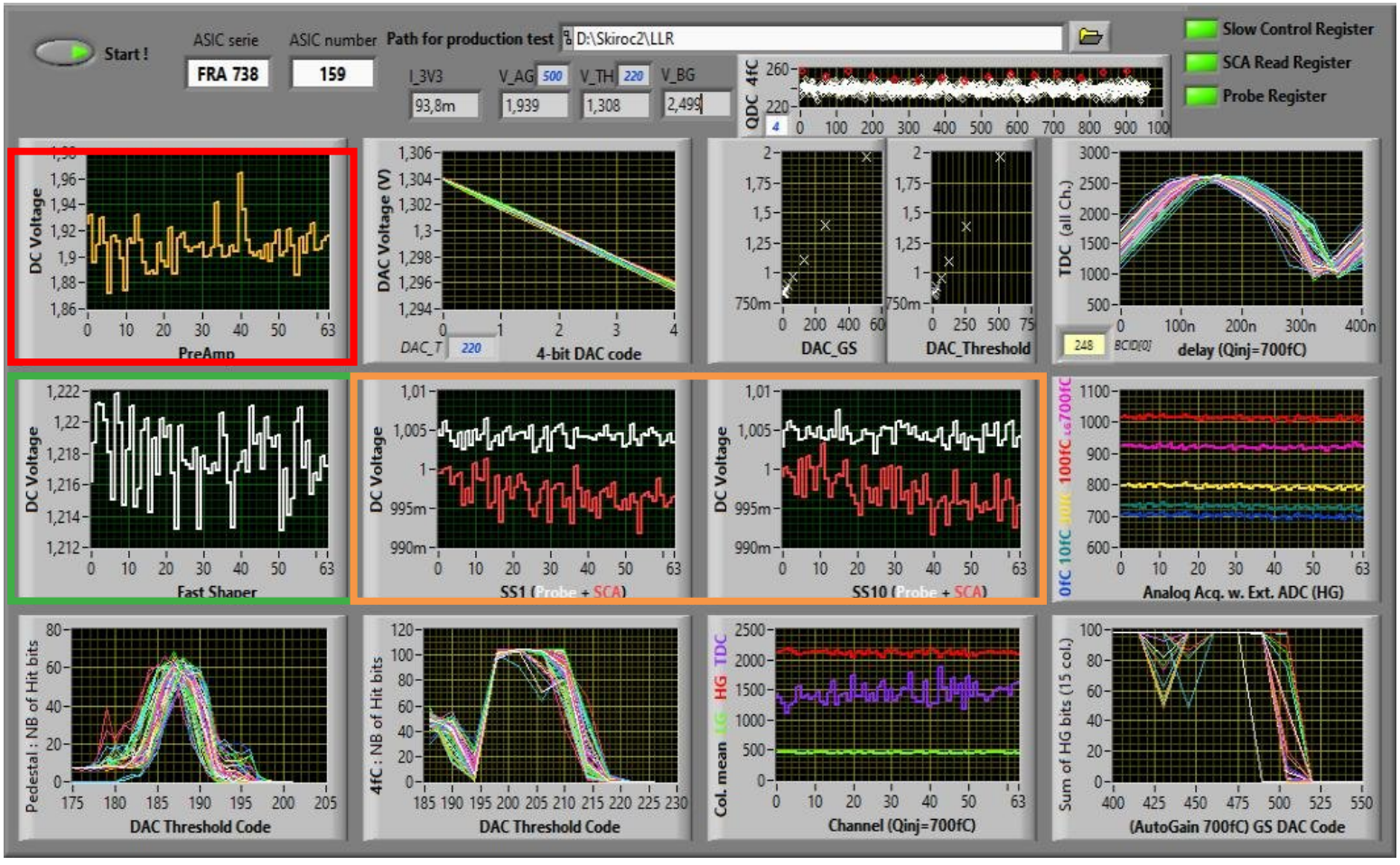
Retrieved data file: Chip # FRA 738-159

data > Test_SK2A_BGA_FRA 738-159.data

```
Slow_Control_Register       OK
SCA_Read_Register       OK
Probe_Register      OK

I_3V3   V_BG    V_TH    V_GS
0,0937976   2,4989200   1,3079803   1,9394339

VDC_FS
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
1,2161662   1,2186568   1,2211954   1,2211390   1,2201431   1,2180445   1,2150118   1,2218660   1,2199741   1,2147174   1,2182692   1,2210182

VDC_SS10
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
1,0028281   1,0049861   1,0061333   1,0052725   1,0049275   1,0038300   1,0038774   1,0053356   1,0045272   1,0041886   1,0052986   1,0039053

VDC_SS1
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
1,0049201   1,0042521   1,0060671   1,0047835   1,0035045   1,0028111   1,0046542   1,0024921   1,0047438   1,0031069   1,0049574   1,0038115

VDC_PA
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
1,9249406   1,9312833   1,8951288   1,9088952   1,9294705   1,9108778   1,8721739   1,9158122   1,9111444   1,8988010   1,8742716   1,9141055

VDC_SCA10
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
0,9991411   1,0001048   0,9995381   0,9989773   0,9967898   1,0012201   0,9964449   1,0015977   1,0000934   0,9974055   1,0004141   1,0032151

VDC_SCA1
0   1   2   3   4   5   6   7   8   9   10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35
0,9994429   0,9994854   0,9999536   1,0002390   0,9980254   0,9991362   0,9994906   0,9953494   0,9975675   0,9957655   1,0008029   0,9987904

DAC linearity   V_TH
0   1   2   4   8   16  32  64  128 256 512
0,8154298   0,8176452   0,8198520   0,8241404   0,8326749   0,8507235   0,8876501   0,9597801   1,1026122   1,3905303   1,9663821

DAC linearity   V_AG
0   1   2   4   8   16  32  64  128 256 512
0,8276091   0,8297366   0,8318541   0,8365022   0,8451735   0,8619108   0,8989854   0,9687146   1,1116212   1,3978217   1,9652133
```

Channel Scans:

- VDC Pre-Amp /ch
- VDC Fast Shaper /ch
- VDC Slow-Shaper /ch
  - G1, G10
  - Probe & SCA

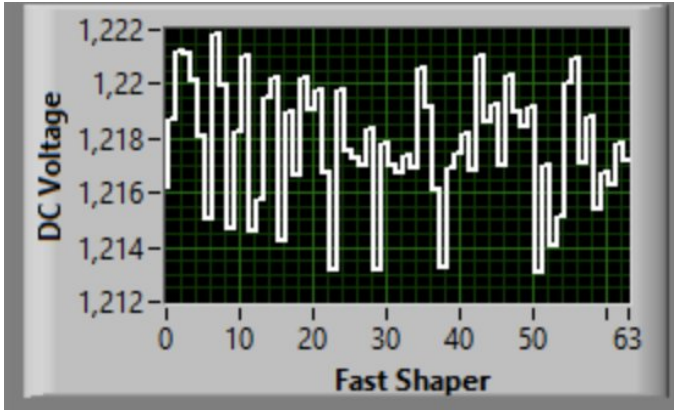


Channel Scans: Output csv files: stats and outliers

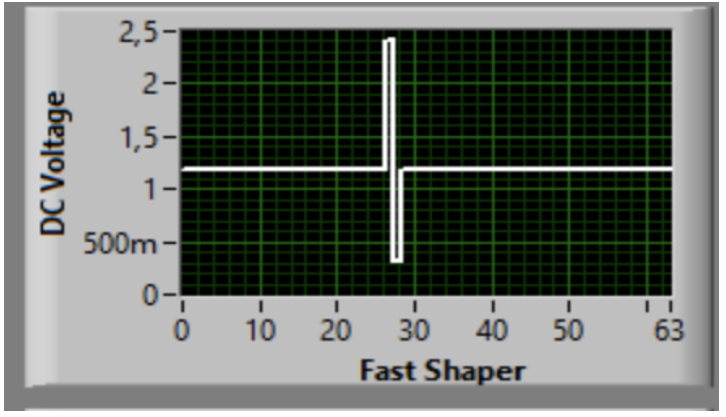
- single measurements from 64 channels
- Find mean and standard deviation
- Fit to Gaussian by MLE method, extract fitted mean and std

```
value_range = {'VDC_FS':[0.9,1.7], 'VDC_SS10':[0.5,1.5], 'VDC_SS1':[0.5,1.5],
               'VDC_PA':[1.6,2.4],'VDC_SCA10':[0.5,1.5], 'VDC_SCA1':[0.5,1.5]}
```

ASIC	number of valid channels	mean	std	fitted mean	fitted std
738-159	64	1.2177	0.002220	1.2177	0.002203



ASIC	number of valid channels	mean	std	fitted mean	fitted std
738-202	62	1.1851	0.001506	1.1851	0.001494



- Outliers (outside 3 std from the mean)

ASIC	channel	distance
738-261	34	3.4829

ASIC	channel	distance
2127-251	34	-3.4044

Distance = (value - mean)/std

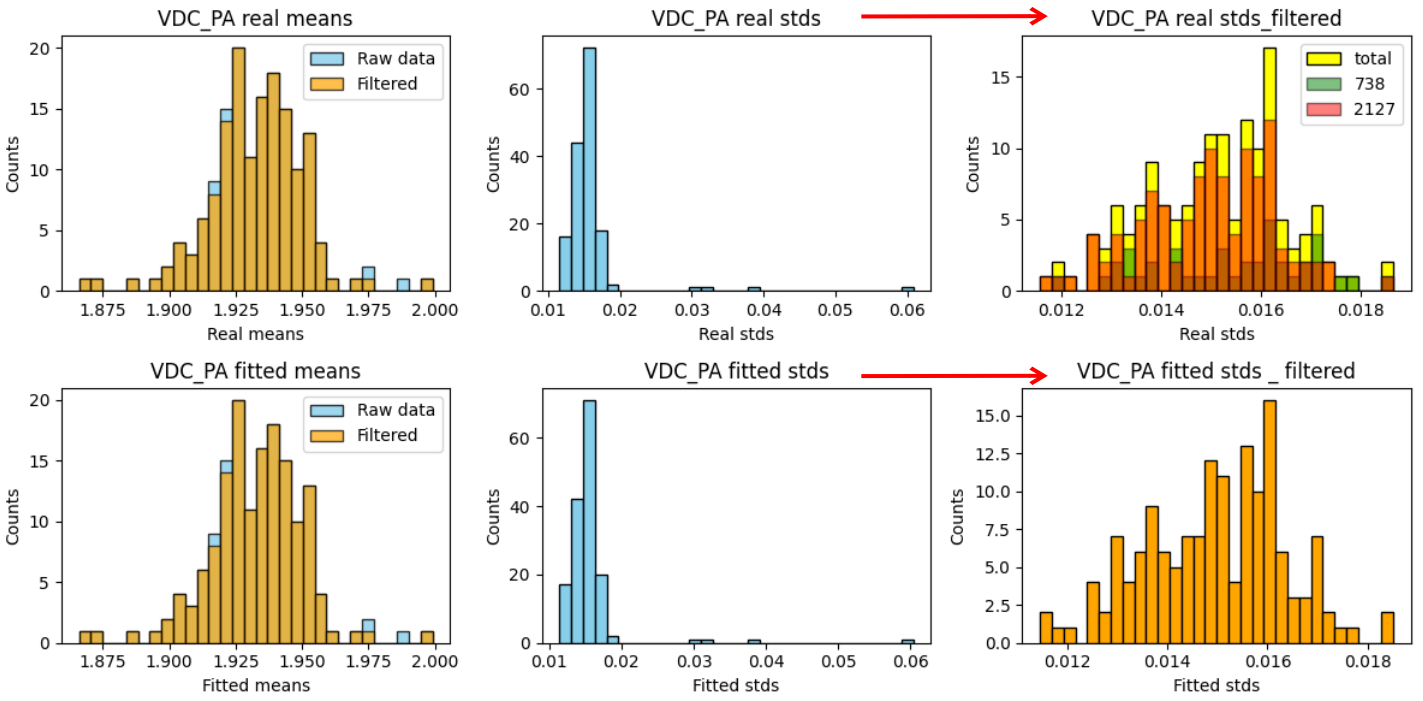
Channel Scans: Summary VDC_PA

- Filter by standard deviation

```
std_range = {'VDC_FS':[0,0.003], 'VDC_SS10':[0,0.002], 'VDC_SS1':[0,0.02],
             'VDC_PA':[0, 0.02],'VDC_SCA10':[0,0.004], 'VDC_SCA1':[0,math.inf]}
```

- Total no. of ASICs: 156
- valid ASICs: 152

```
ASICS of filtered std outliers:
         ASIC       std
27   2127-209  0.039015
55    738-264  0.029789
61   2127-178  0.031462
143  2127-264  0.060818
total no. of ASICs: 156
number of excluded ASICs: 4
number of valid ASICs: 152
```



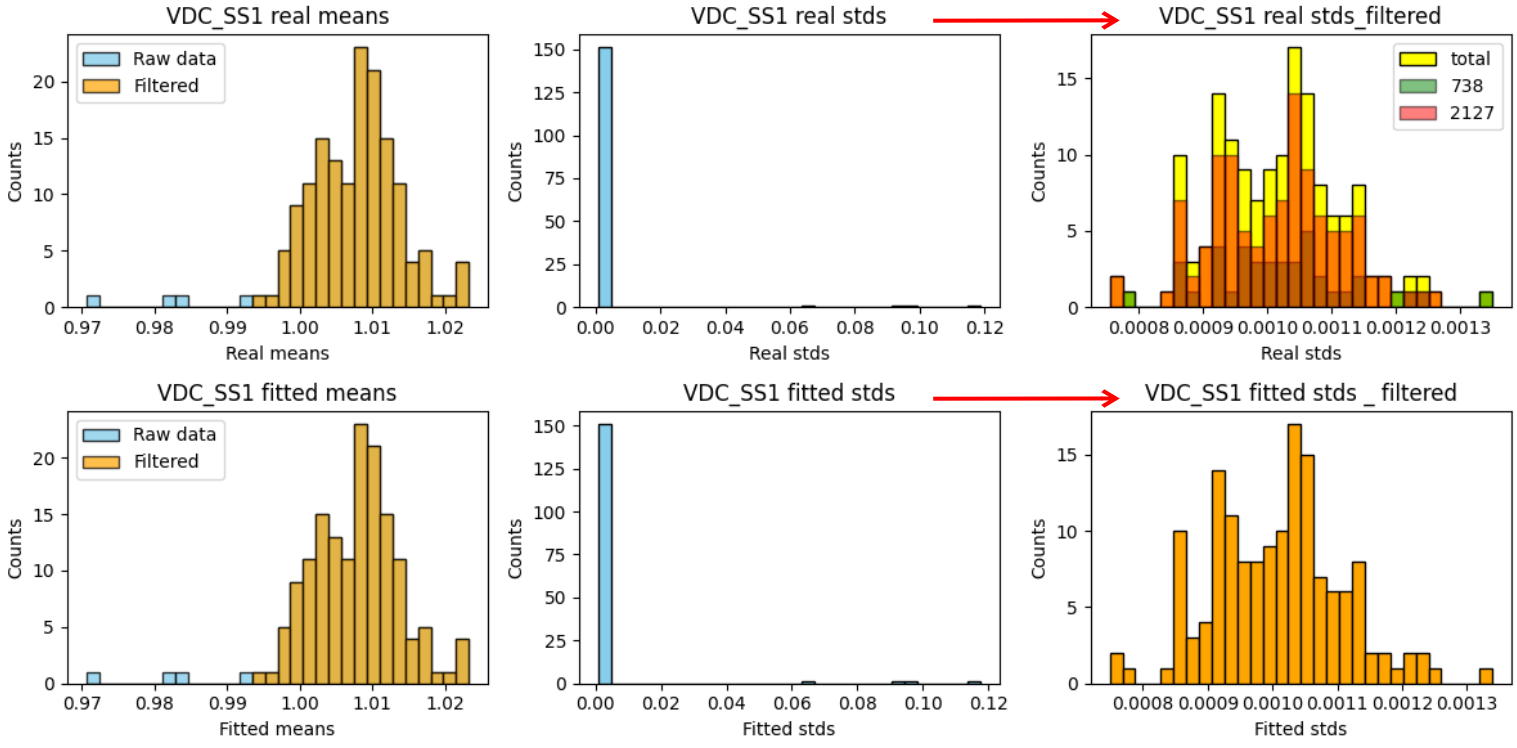
Channel Scans: Summary VDC_SS1

- Filter by standard deviation

```
std_range = {'VDC_FS':[0,0.003], 'VDC_SS10':[0,0.002], 'VDC_SS1':[0,0.02],
             'VDC_PA':[0, 0.02],'VDC_SCA10':[0,0.004], 'VDC_SCA1':[0,math.inf]}
```

- Total no. of ASICs: 155
- valid ASICs: 151

```
ASICS of filtered std outliers:
         ASIC       std
20     738-167  0.095356
87    2127-415  0.093840
114   2127-390  0.118829
150   2127-391  0.065169
total no. of ASICs: 155
number of excluded ASICs: 4
number of valid ASICs: 151
```



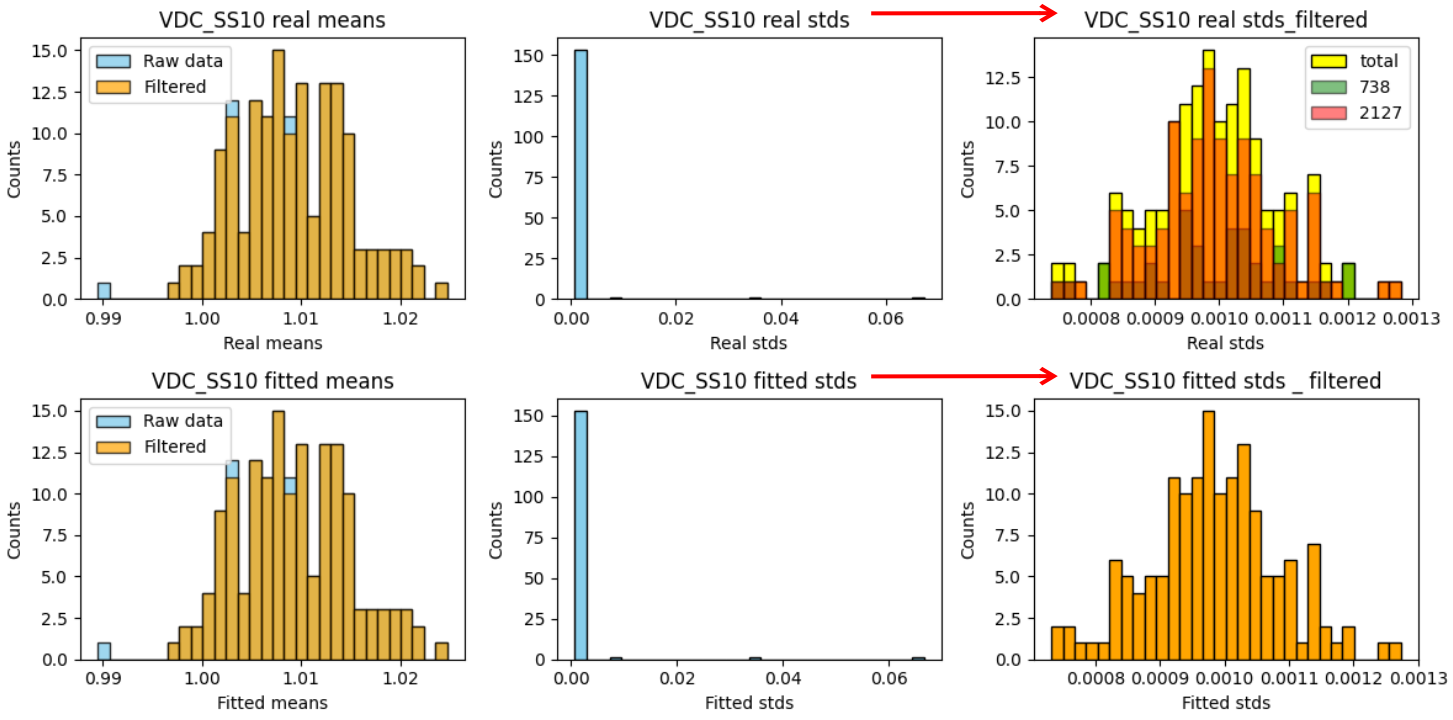
Channel Scans: Summary VDC_SS10

- Filter by standard deviation

```
std_range = {'VDC_FS':[0,0.003], 'VDC_SS10':[0,0.002], 'VDC_SS1':[0,0.02],
             'VDC_PA':[0, 0.02],'VDC_SCA10':[0,0.004], 'VDC_SCA1':[0,math.inf]}
```

- Total no. of ASICs: 156
- valid ASICs: 153

```
ASICS of filtered std outliers:
        ASIC       std
1    738-202  0.009274
34   738-15_  0.067224
142  738-264  0.035039
total no. of ASICs: 156
number of excluded ASICs: 3
number of valid ASICs: 153
```

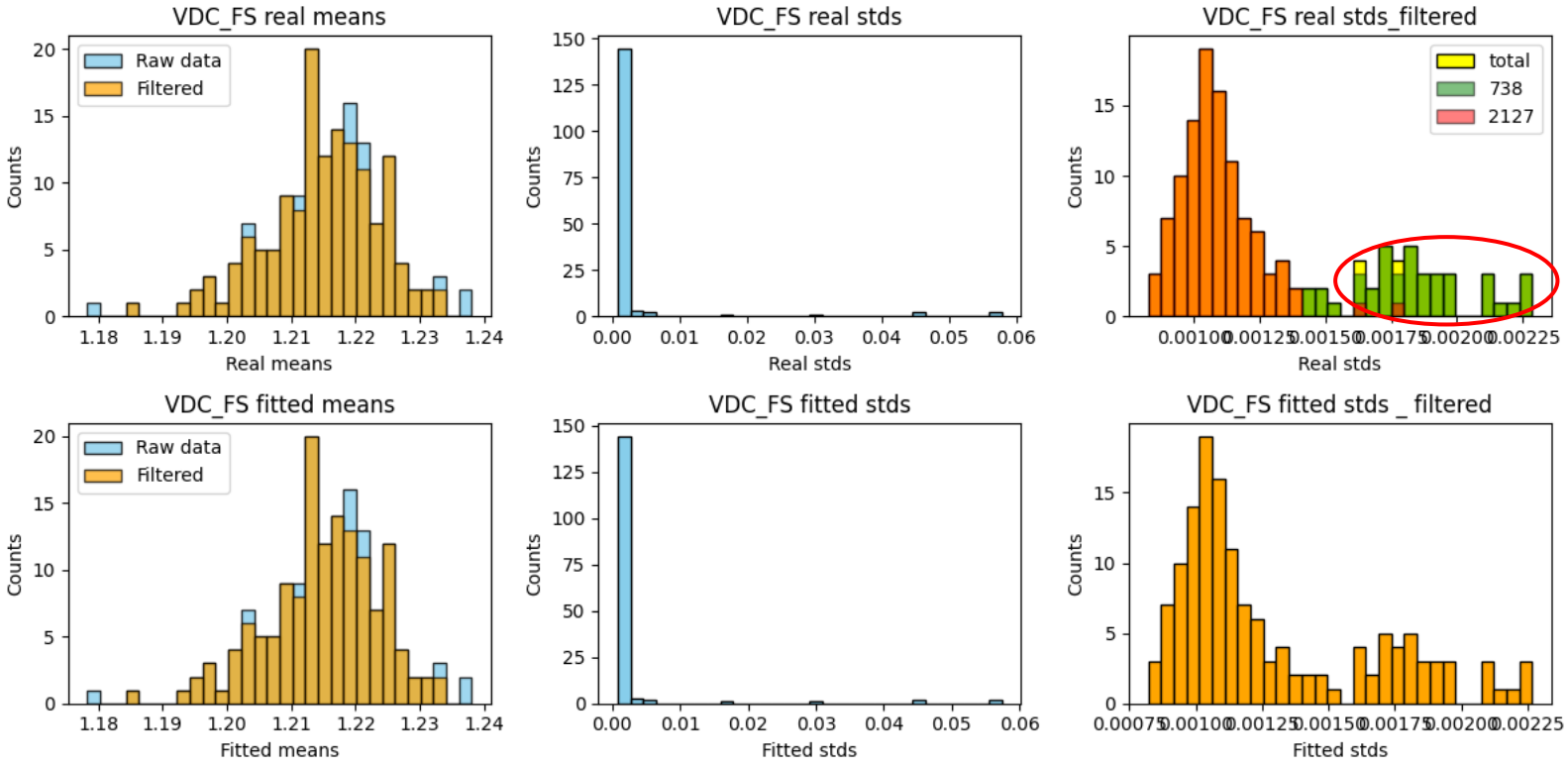


Channel Scans: dependence on packaging VDC_FS

- Particular VDC_FS
- 39 ASICs “outside” the Gaussian in filtered std
- Different packaging

- Total no. of ASICs: 155
- valid ASICs: 144

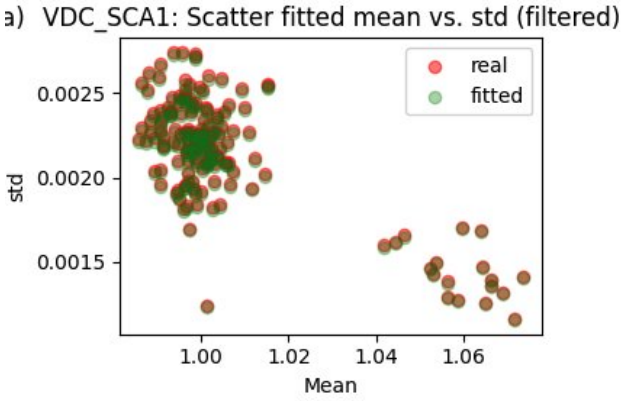
```
ASICS of filtered std outliers:
                ASIC       std
34   2127-254_chn62off  0.003949
37   2127-264_chn41off  0.045919
43            2127-282  0.005098
63             738-264  0.016618
70            2127-129  0.057840
80            2127-254  0.003949
85            2127-177  0.004103
94            2127-264  0.046293
103  2127-129_chn6off   0.057476
117           2127-262  0.030707
149           2127-256  0.006103
total no. of ASICs: 155
number of excluded ASICs: 11
number of valid ASICs: 144
```

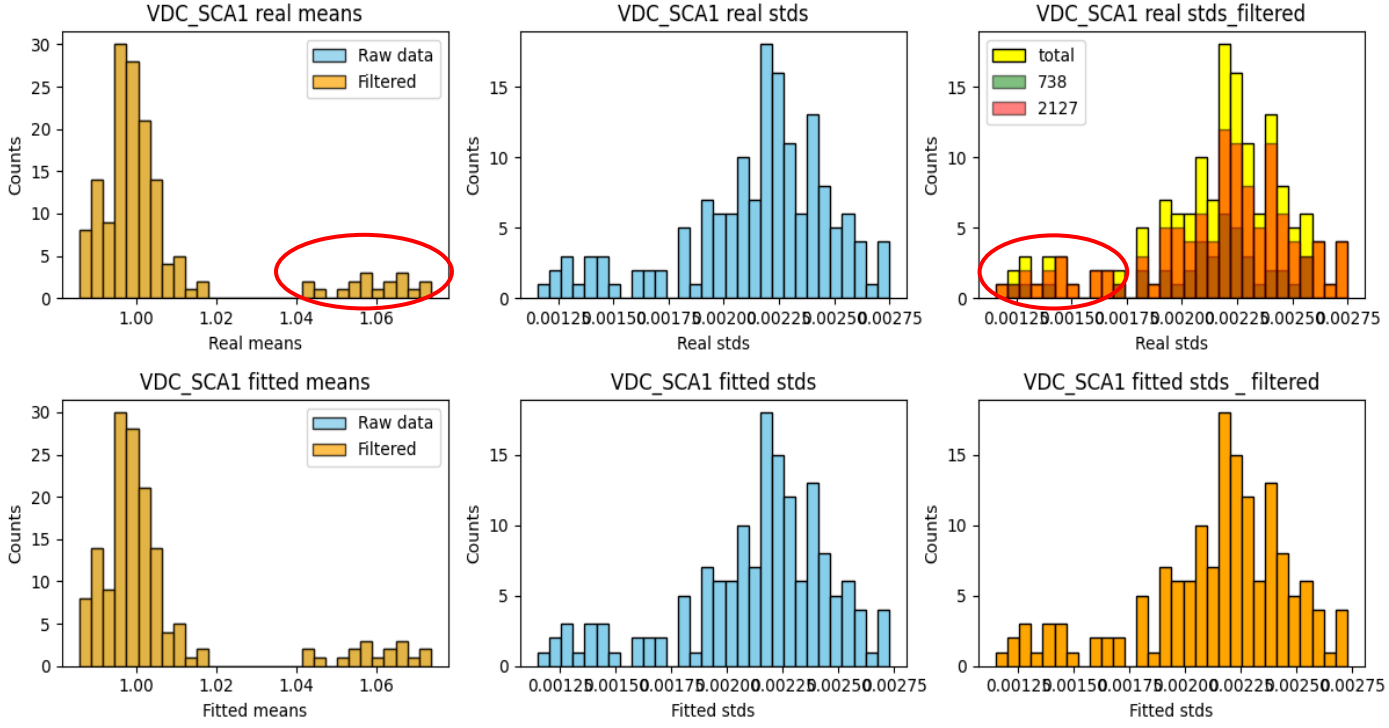


Channel Scans: 2 groups of mean data SCA1

- Notch of data that is “outside” Gaussian in mean and filtered std as in red circle
- Scatter plots show correlation between mean and std.

- Total no. of ASICs: 155
- valid ASICs: 155



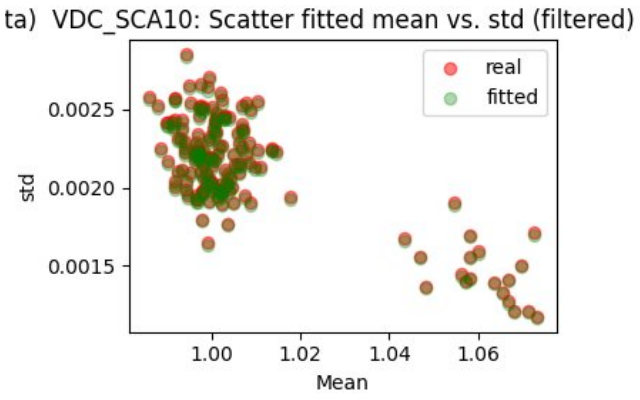


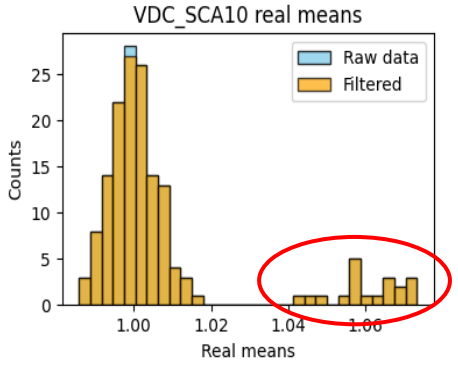
Channel Scans: 2 groups of mean data SCA10

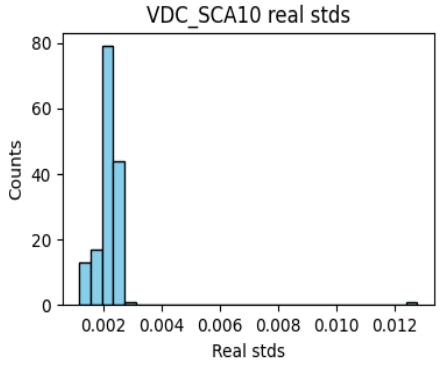
Notch of data that is “outside” Gaussian in mean and filtered std as in red circle

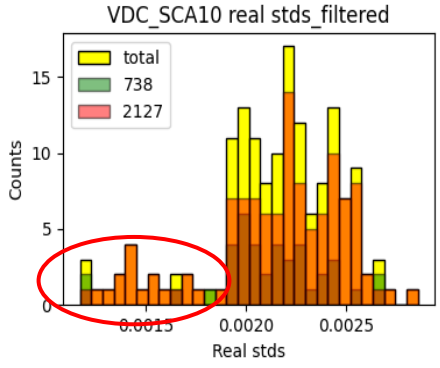
Scatter plots show correlation between mean and std.

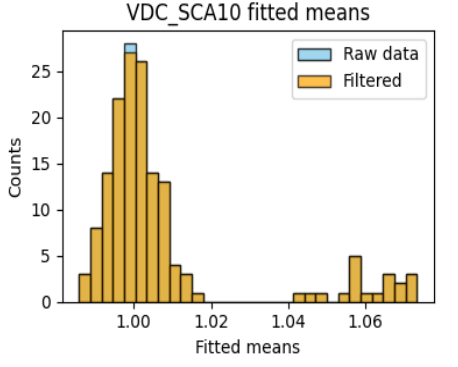
- Total no. of ASICs: 156
- valid ASICs: 155

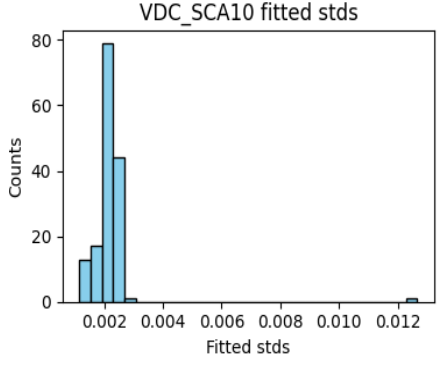


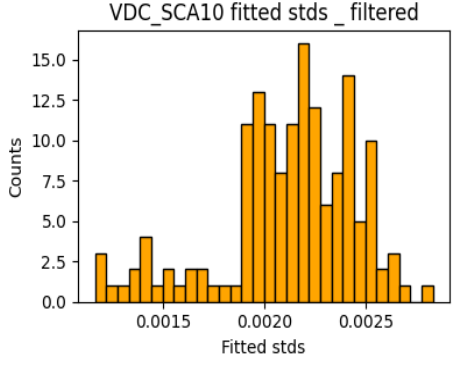




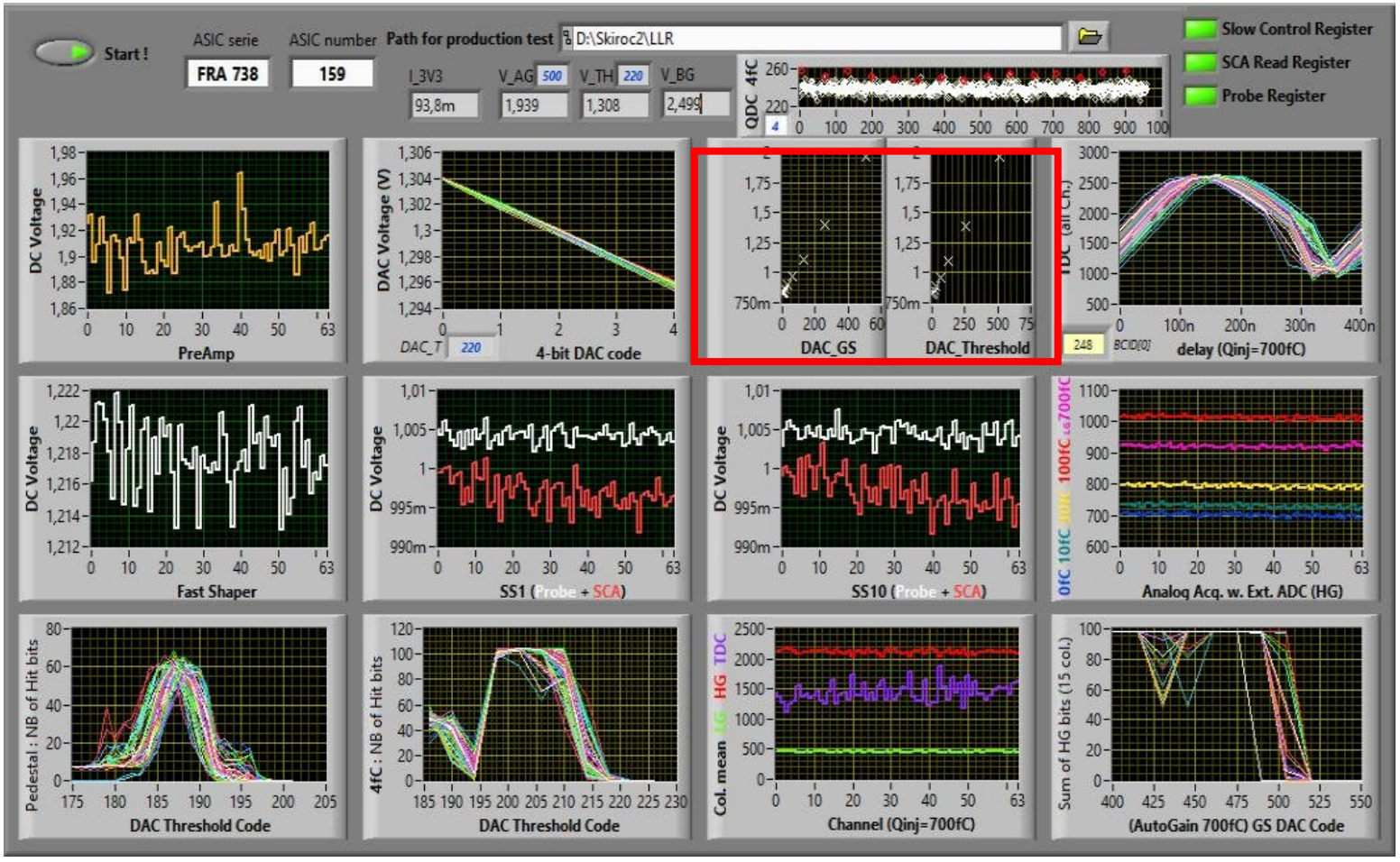








Parameter Scans:



DAC Scan with probe:

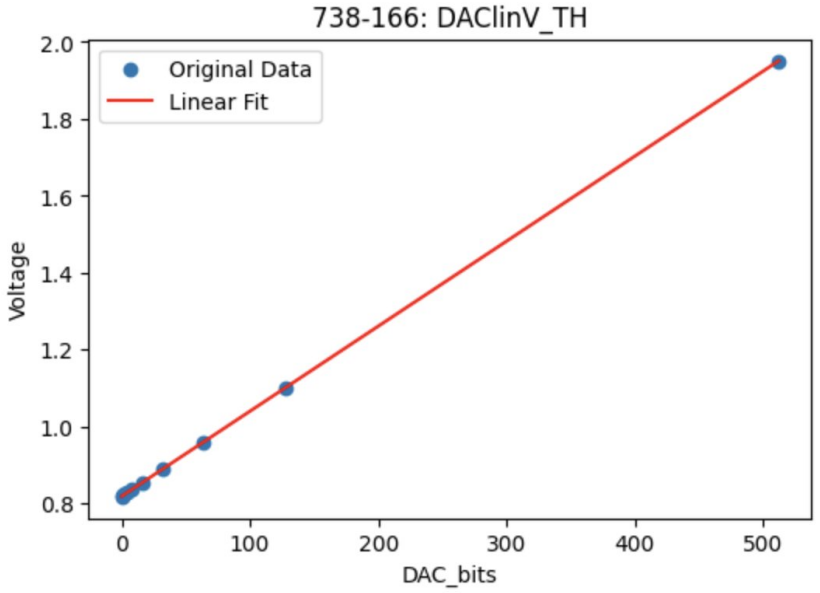
- auto-gain (GS)
- Global Thr.

Parameter scan: retrieved data file

```
DAC linearity   V_TH
0   1   2   4   8   16  32  64  128 256 512
0,8185536   0,8209090   0,8229595   0,8273524   0,8362206   0,8543637   0,8898767   0,9599614   1,1015056   0   1,9504651
```

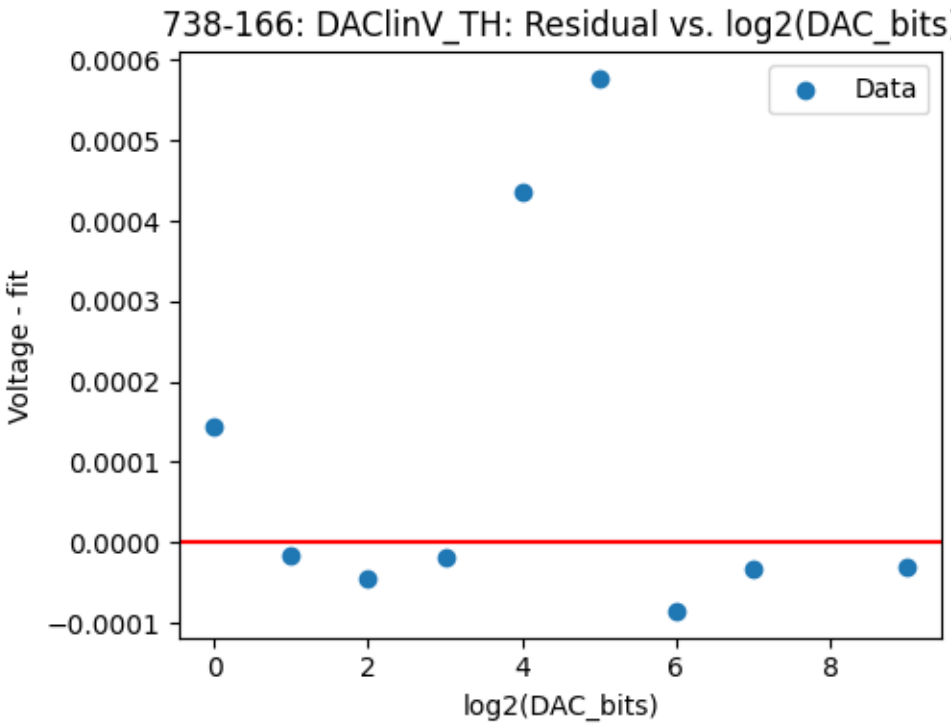
- Linear fit with y-intercept = voltage value at DAC = 0
- excluding zeros (if V0 = 0, extrapolate)
- Extract slope

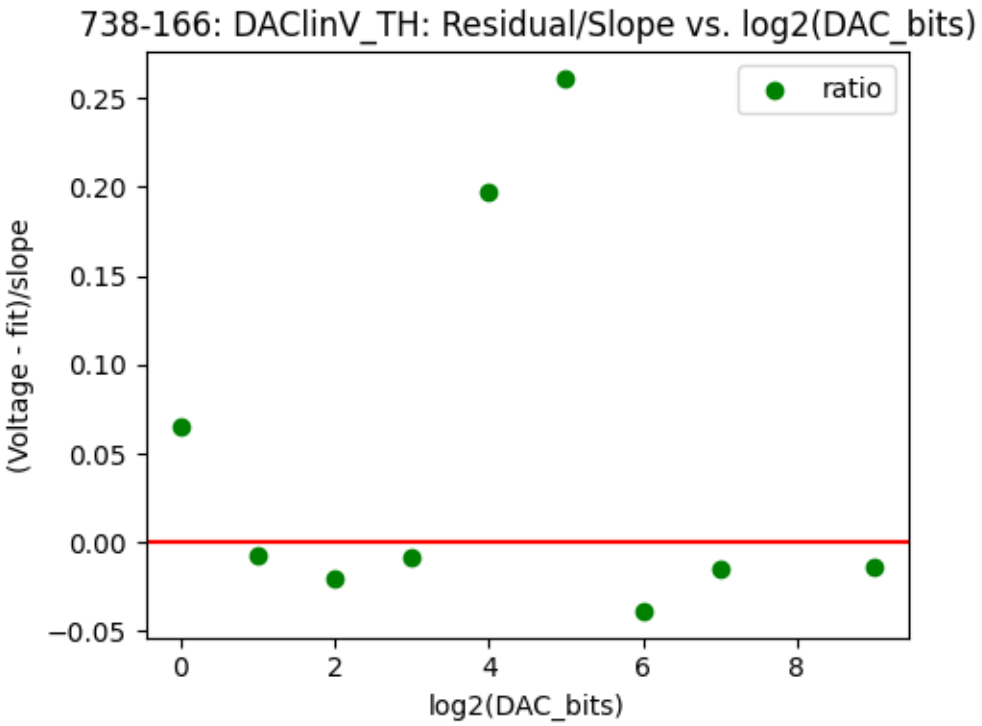
```
738-166: DAClinV_TH
Equation of the linear fit:
Voltage = 0.0022108238079647283 * DAC + 0.8185536
```



Parameter scan: Analysis of a single chip

- Ratio = residual/slope: how well the fit is
- slope = smallest step of voltage when changing DAC value





Parameter scan: output file

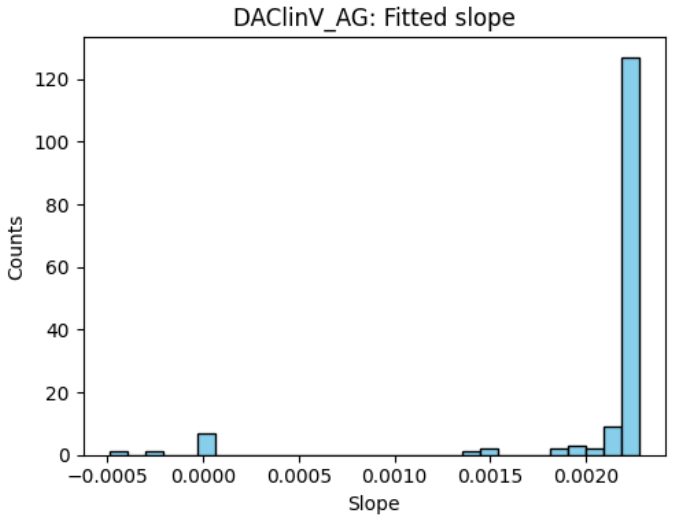
ASIC	V0 != 0	Fitted slope	Max abs. residual/slope ratio	V0(intercept)
738-159	TRUE	0.002247538	0.327114922	0.8154298

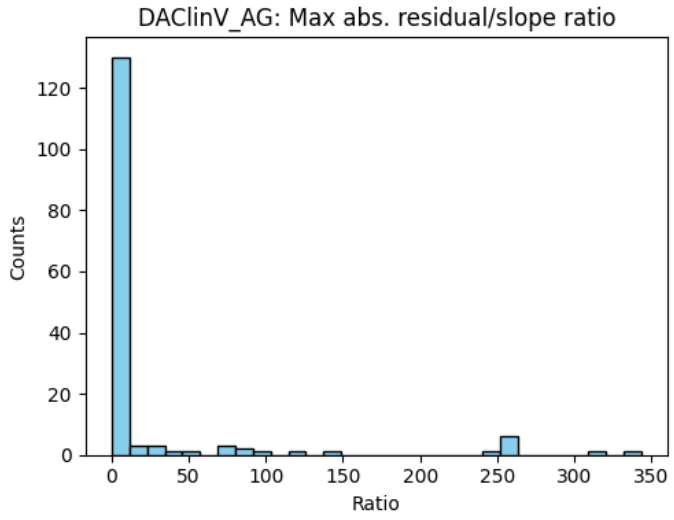
- Steps of

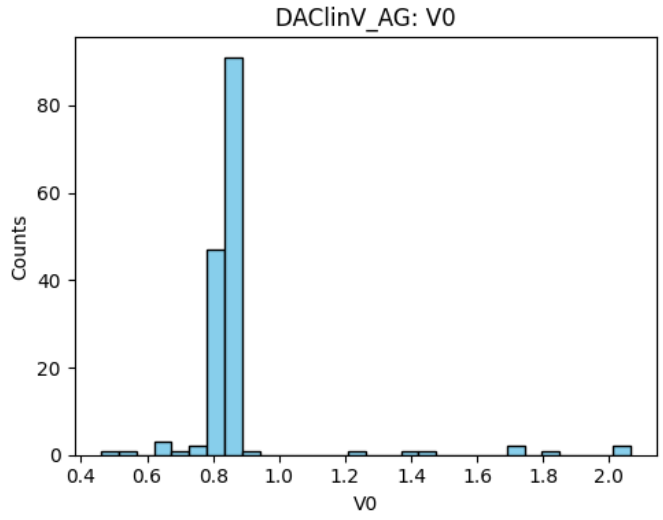
Step: V1-V0	Step: V2-V0	Step: V3-V0	Step: V4-V0	Step: V5-V0
0.0022154	0.0044222	0.0087106	0.0172451	0.0352937

Step: V6-V0	Step: V7-V0	Step: V8-V0	Step: V9-V0	Step: V10-V0
0.0722203	0.1443503	0.2871824	0.5751005	1.1509523

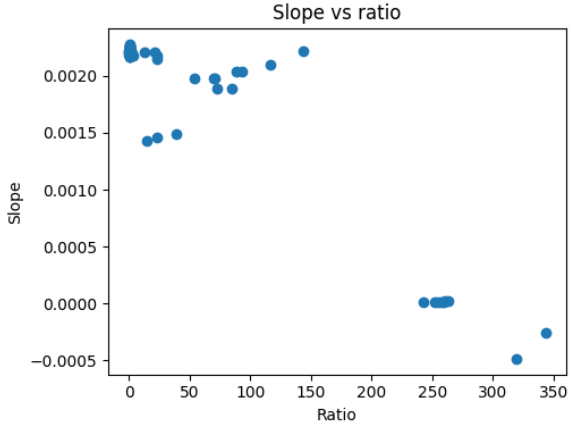
Parameter scan: Summary analysis of DAClinV_AG

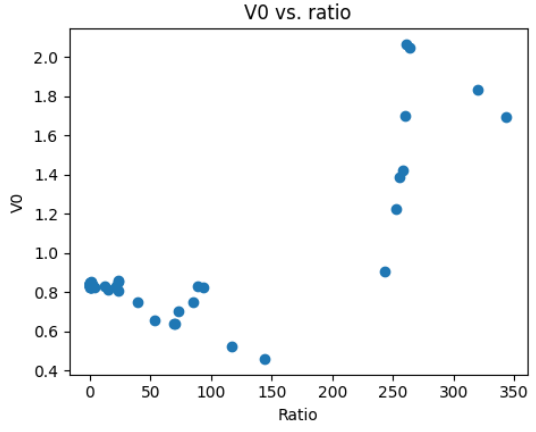




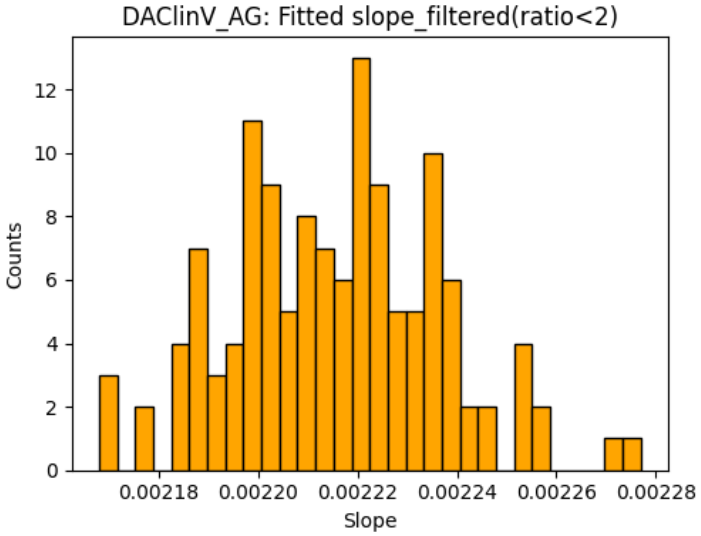


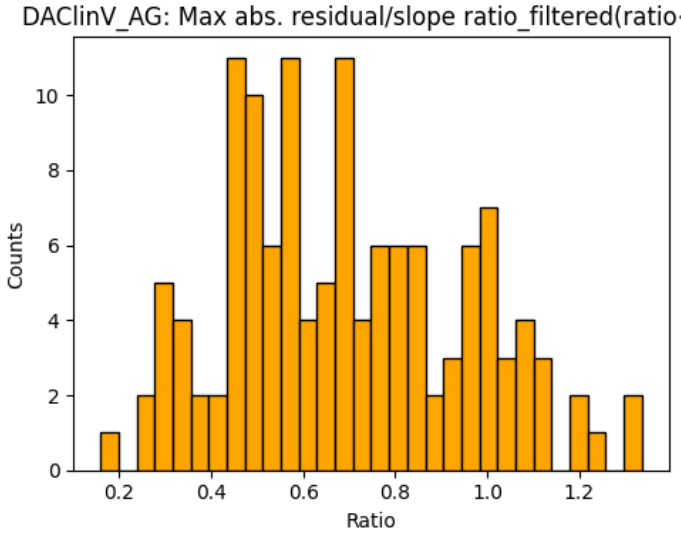
Scatter plot showing correlation of slope and V0 with ratio:

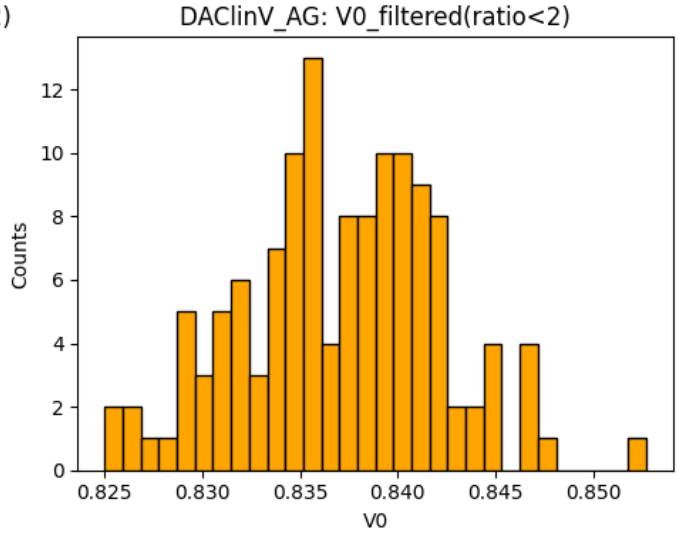




Parameter scan: Summary analysis of DAClinV_AG

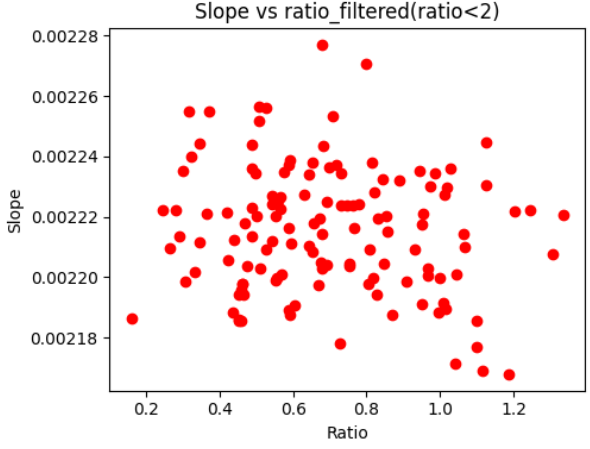


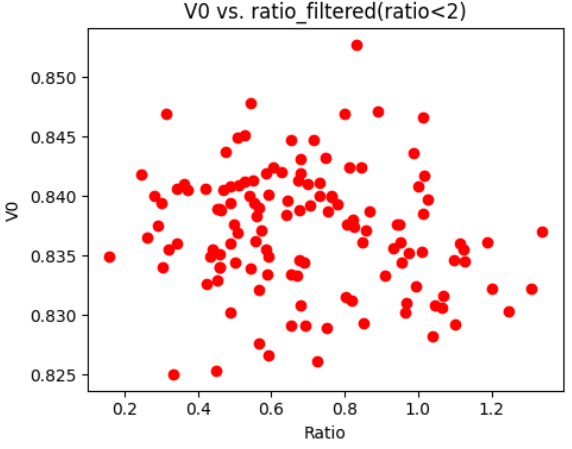




Filtered ratio < 2

```
total number of ASICs: 154
number of excluded ASICs: 25
number of valid ASICs: 129
```

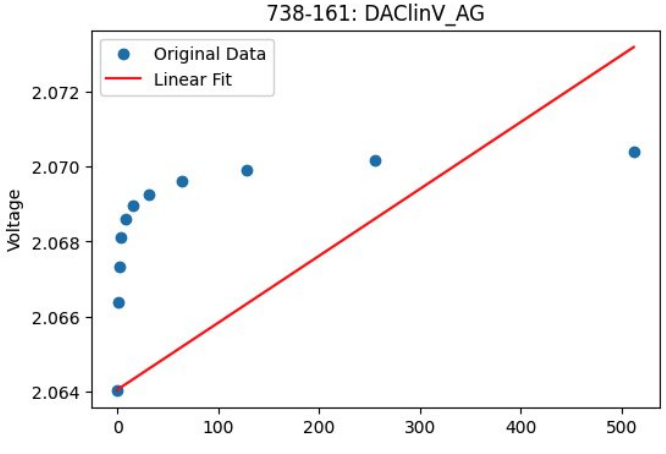


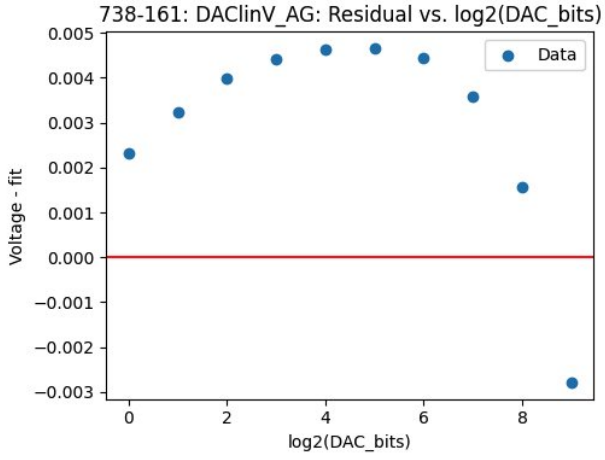


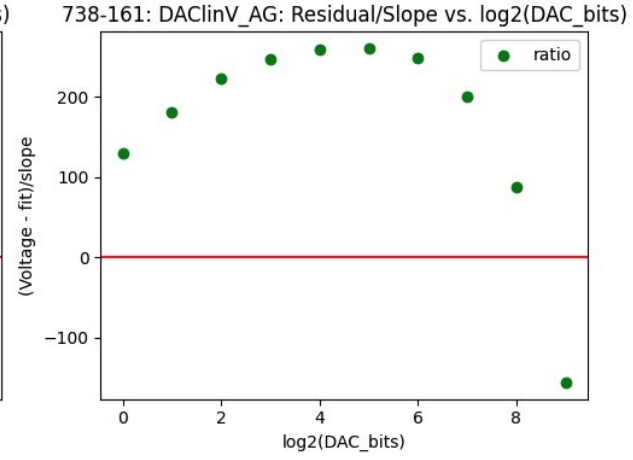
Parameter scan: Problem shoot (738-161: DAClinV_AG)

```
DAC linearity   V_AG
0   1   2   4   8   16  32  64  128 256 512
2,0640459   2,0663909   2,0673200   2,0680968   2,0685892   2,0689519   2,0692666   2,0696222   2,0699148   2,0701681   2,0704014
```

e

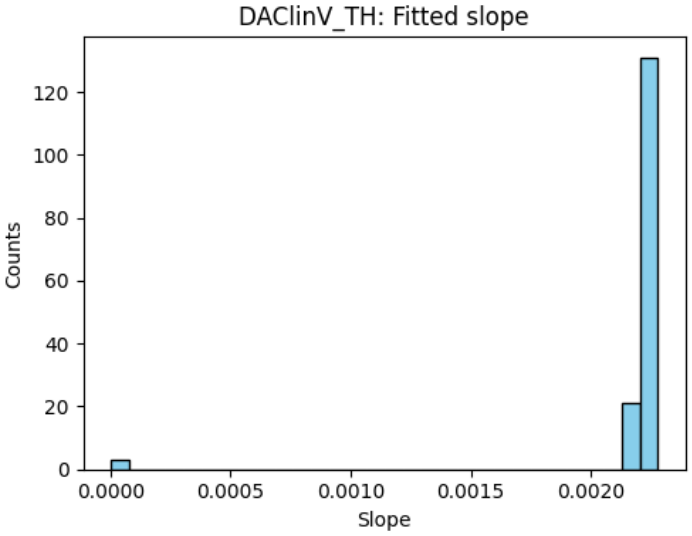


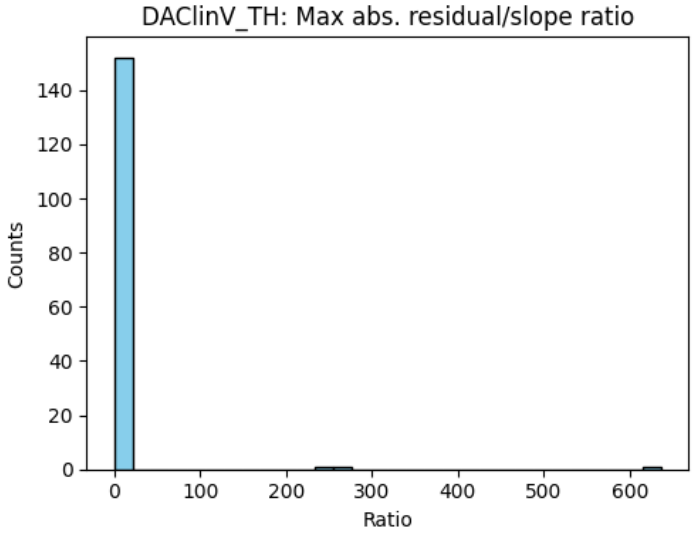


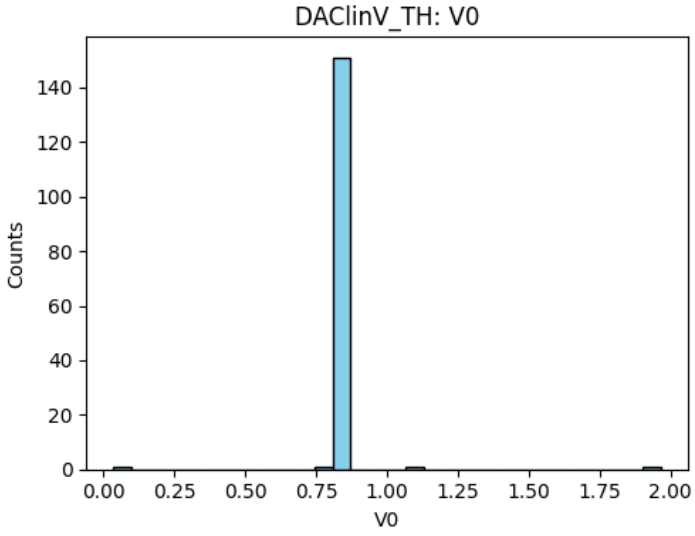



```
738-161: DAClinV_AG
Equation of the linear fit:
Voltage = 1.7842507510690275e-05 * DAC + 2.0640459
```

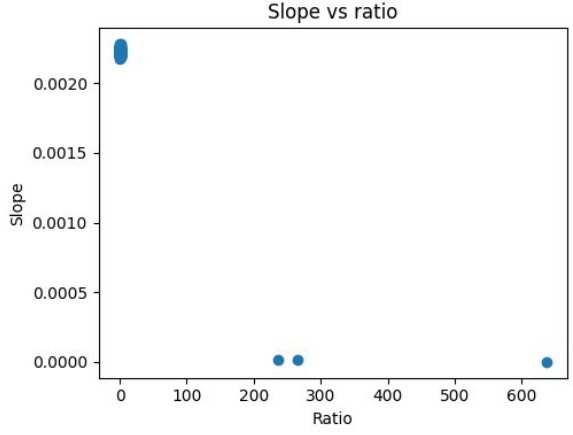
Parameter scan: Summary analysis of DAClinV_TH

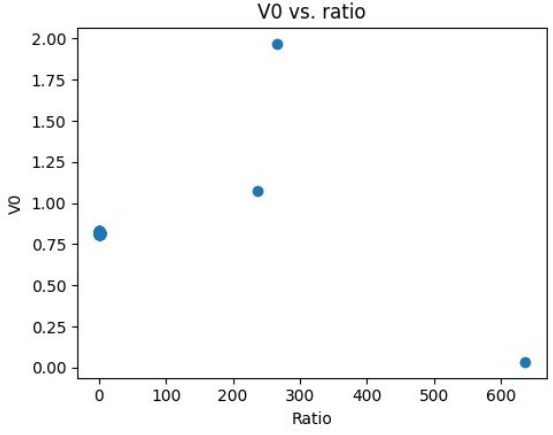




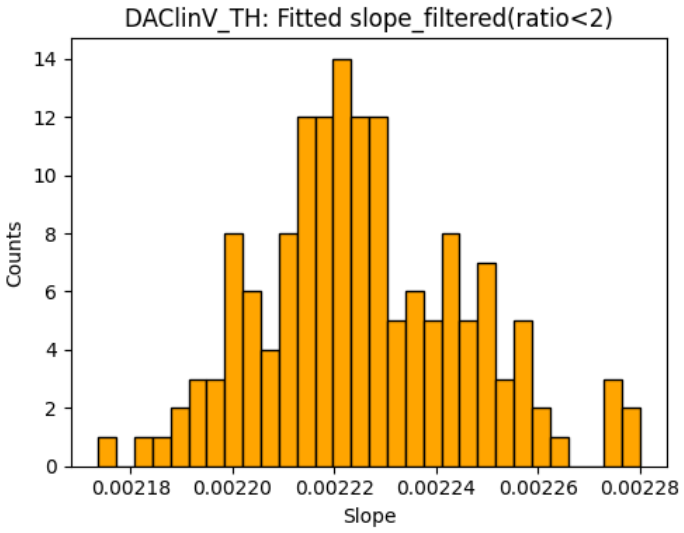


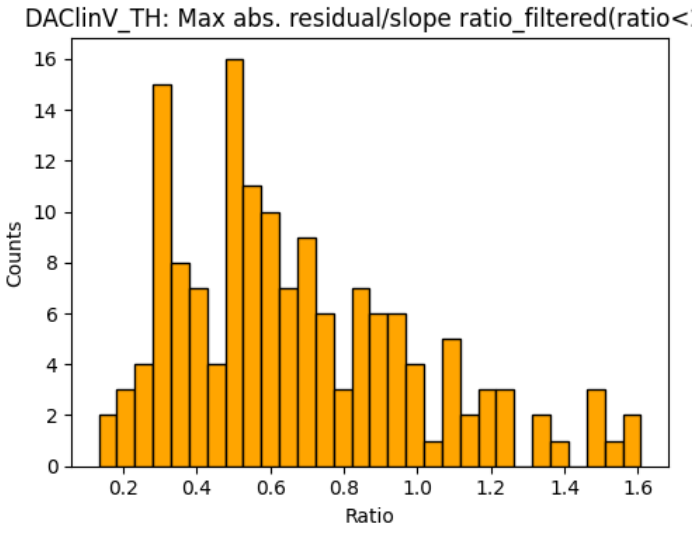
Scatter plot showing correlation of slope and V0 with ratio:

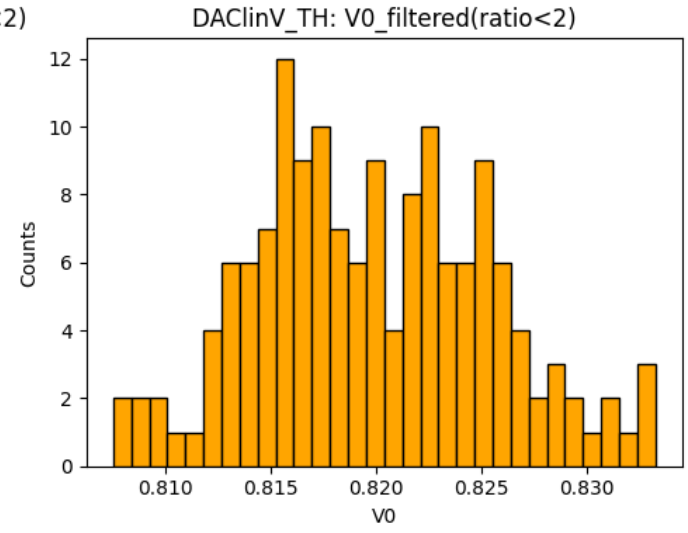




Parameter scan: Summary analysis of DAClinV_TH





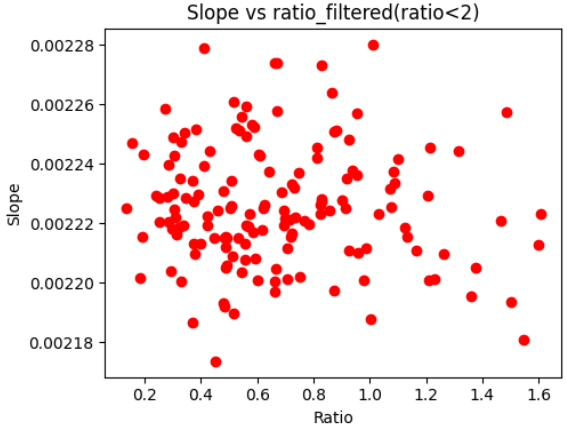


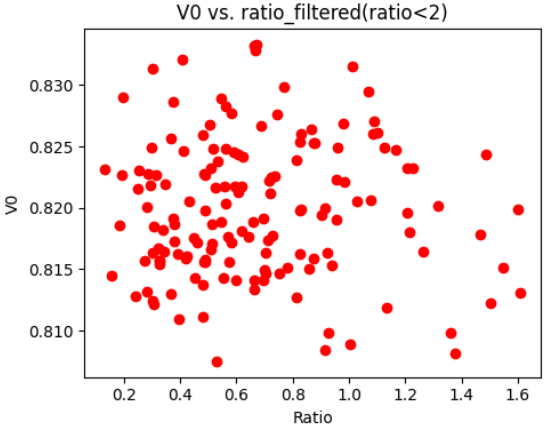
Filt

excluded ASICs: (ratio >=2):

	ASIC	Max abs. residual/slope ratio
3	738-251	636.565522
23	2127-407	265.956669
74	2127-403	2.365320
131	2127-274	236.147975

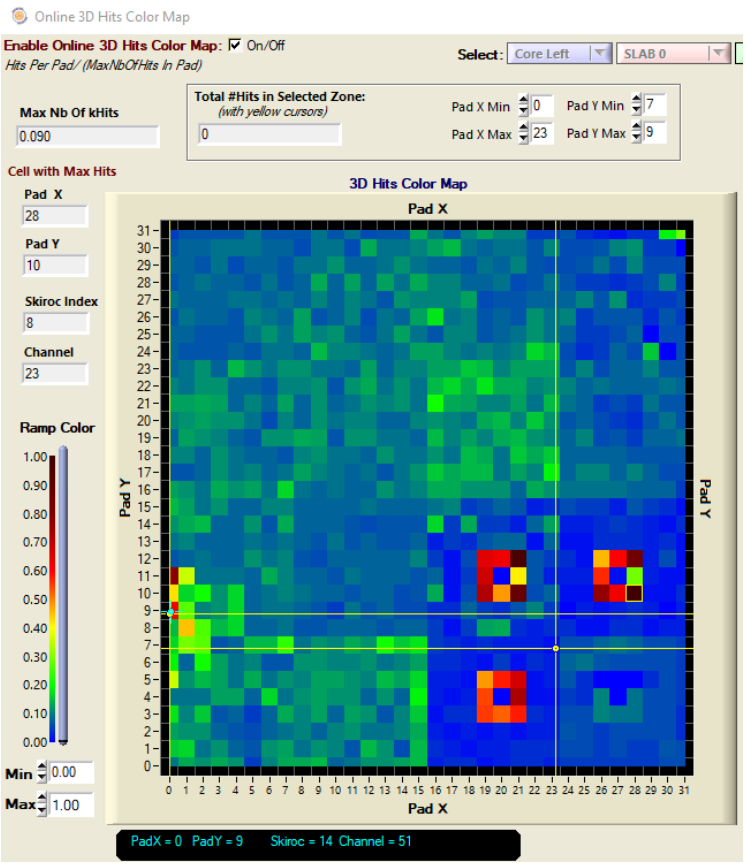
total number of ASICs: 154
number of excluded ASICs: 4
number of valid ASICs: 150

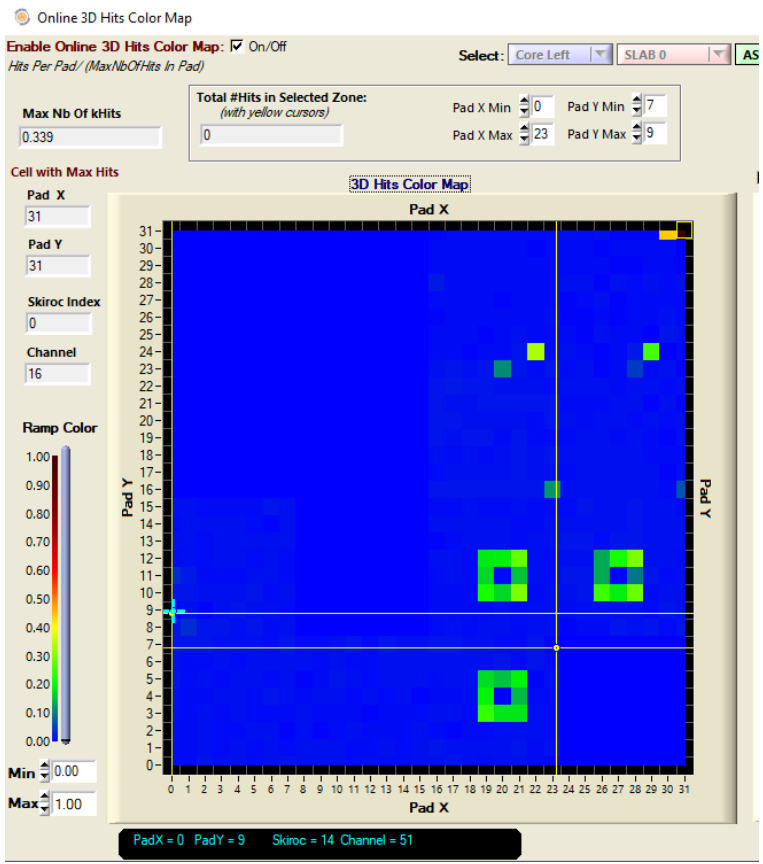


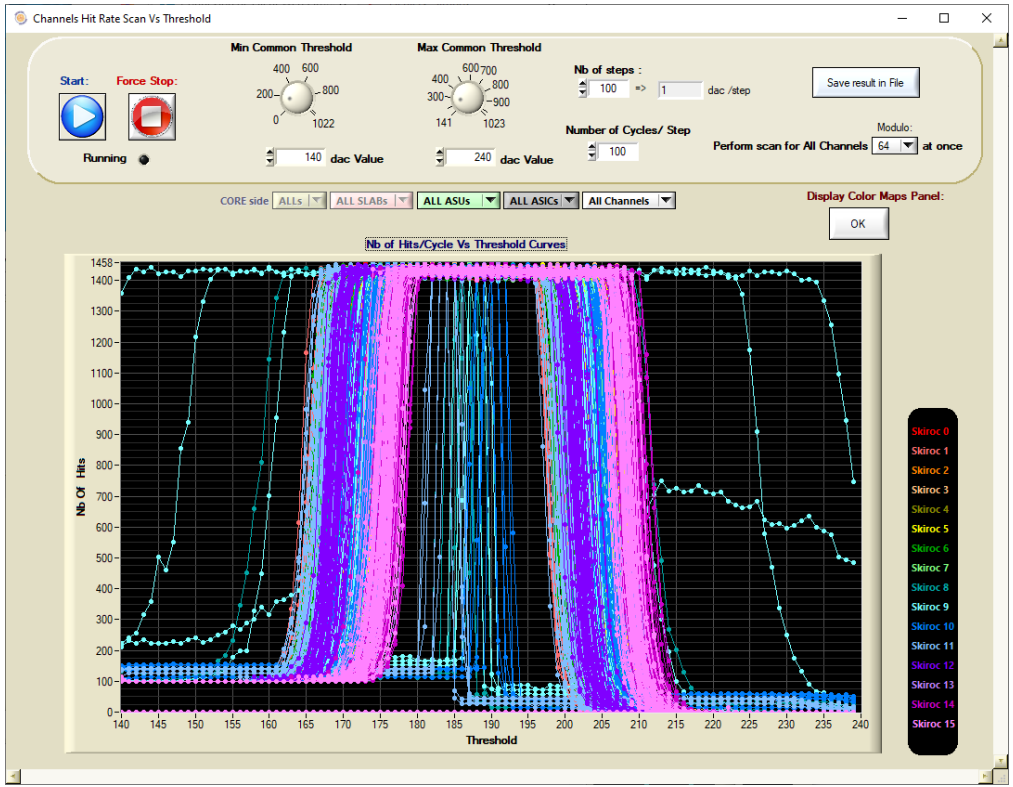


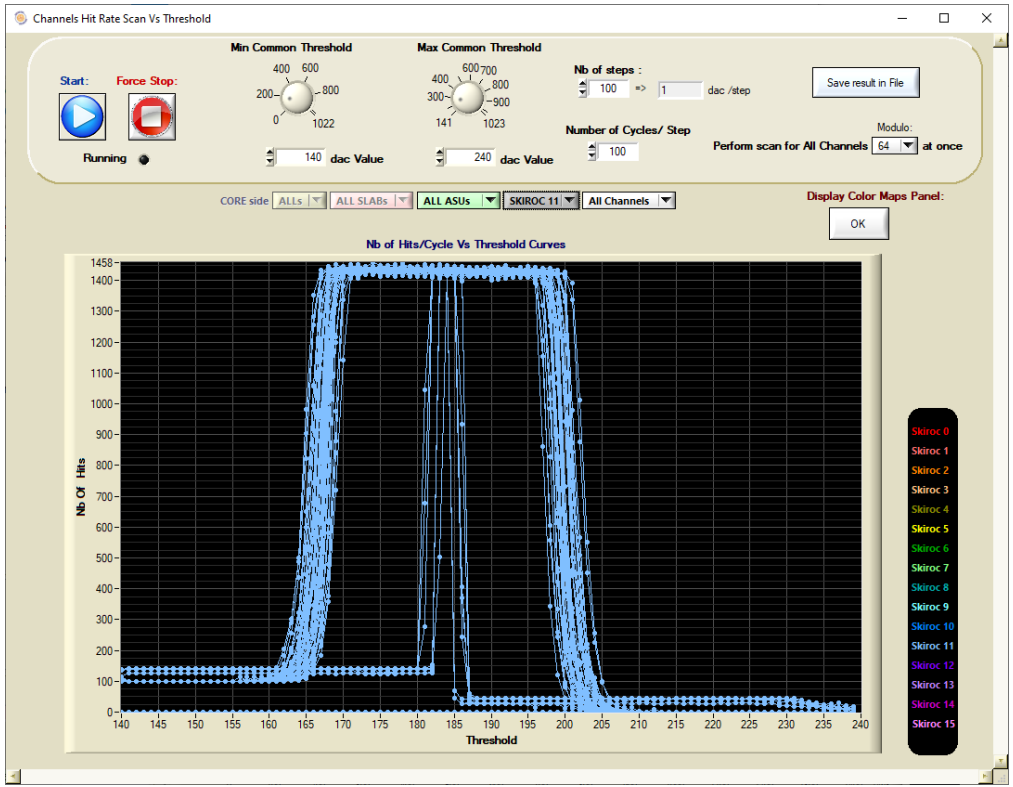
8 Measurements methods

Test of FEV board with HV + babywafer






Channels Hit Rate Scan Vs Threshold
Start:
Force Stop:
Running
Min Common Threshold
140 dac Value
Max Common Threshold
240 dac Value
Nb of steps :
100 => 1 dac /step
Number of Cycles/ Step
100
Save result in File
Perform scan for All Channels
Modulo:
64
at once
CORE side
ALLs
ALL SLABs
ALL ASUs
ALL ASICs
All Channels
Display Color Maps Panel:
OK
Nb of Hits/Cycle Vs Threshold Curves
Nb Of Hits
Threshold
Skiroc 0
Skiroc 1
Skiroc 2
Skiroc 3
Skiroc 4
Skiroc 5
Skiroc 6
Skiroc 7
Skiroc 8
Skiroc 9
Skiroc 10
Skiroc 11
Skiroc 12
Skiroc 13
Skiroc 14
Skiroc 15


Channels Hit Rate Scan Vs Threshold
Start:
Force Stop:
Running
Min Common Threshold
140 dac Value
Max Common Threshold
240 dac Value
Nb of steps :
100 => 1 dac /step
Number of Cycles/ Step
100
Save result in File
Perform scan for All Channels
Modulo:
64
at once
CORE side
ALLs
ALL SLABs
ALL ASUs
SKIROC 11
All Channels
Display Color Maps Panel:
OK
Nb of Hits/Cycle Vs Threshold Curves
Nb Of Hits
Threshold
Skiroc 0
Skiroc 1
Skiroc 2
Skiroc 3
Skiroc 4
Skiroc 5
Skiroc 6
Skiroc 7
Skiroc 8
Skiroc 9
Skiroc 10
Skiroc 11
Skiroc 12
Skiroc 13
Skiroc 14
Skiroc 15

Conclusion:

- Data analysized from 158 chips
- Channel Scans (single measurement by external device from 64 channels)
  - Non Gaussian distribution of std in VDC_FS,
    - Fast shaper ------> packaging 738 twice the std of 2127
- Full analysis of all measurement done → stored in CSV files
  - Look for correlations
  - List of outliers ready
-